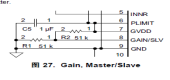


**TABLE 1. Gain and Master/Slave**

MASTER/SLAVE	GAIN	R1 (Ω)	R2 (Ω)	R3 (kΩ)	INPUT IMPEDANCE
Master	20 dB	5.0 kΩ	0.1 kΩ	100 kΩ	60 kΩ
Master	26 dB	20 kΩ	0.1 kΩ	100 kΩ	30 kΩ
Master	32 dB	30 kΩ	0.1 kΩ	100 kΩ	15 kΩ
Slave	20 dB	40 kΩ	75 kΩ	0.1 kΩ	60 kΩ
Slave	26 dB	51 kΩ	51 kΩ	0.1 kΩ	30 kΩ
Slave	32 dB	75 kΩ	30 kΩ	0.1 kΩ	15 kΩ

(1) Resistor tolerance should be 5% or better.



**FIG 27. Gain, Master/Slave**

DATAOUT1 ↔ DATAOUT1  
 MCLK ↔ MCLK  
 LCLK ↔ LCLK  
 RCLK ↔ RCLK  
 LOUT1 ↔ LOUT1  
 LOUT2 ↔ LOUT2  
 ROUT1 ↔ ROUT1  
 ROUT2 ↔ ROUT2  
 AMP\_SD ↔ AMP\_SD  
 AMP\_MUTE ↔ AMP\_MUTE  
 OUT1 ↔ OUT1  
 OUT2 ↔ OUT2  
 OUT3 ↔ OUT3  
 OUT4 ↔ OUT4  
 AUD\_L ↔ AUD\_L  
 AUD\_R ↔ AUD\_R

$$P_{OUT} = \frac{\left( \frac{R_L}{R_L + 2 \times R_S} \times V_p \right)^2}{2 \times R_L} \text{ for unclipped power}$$

where

- $P_{OUT}$  (10% THD) =  $1.25 \times P_{OUT}$  (unclipped)
- $R_L$  is the load resistance.
- $R_S$  is the total series resistance including  $R_{DS(on)}$  and output filter resistance.
- $V_p$  is the peak amplitude
- $V_p = 4 \times \text{PLIMIT}$  voltage if  $\text{PLIMIT} < 4 \times V_p$