TAS2563 6.1-W Boosted Class-D Audio Amplifier With Integrated DSP And IV Sense

1 Features

- High performance Class-D amplifier
  - 6.1-W 1% THD+N (4 Ω at 3.6 V)
  - 5-W 1% THD+N (8 Ω at 3.6 V)
  - Boost bypass mode: 10 W(12 W) at 1% (10%) THD+ N (4 Ω,12 V)
- 15-µVrms A-weighted idle channel noise
- 112.5dB SNR at 1% THD+N (8 Ω)
- 100dB PSRR with 200-mV_{PP} ripple at 20Hz to 20 kHz
- 83.5% Efficiency at 1 W (8 Ω, VBAT = 4.2 V)
- < 1-µA HW Shutdown VBAT current
- Speaker voltage and current sense
- VBAT Tracking peak voltage limiter with brown-out prevention
- Dedicated real-time DSP for speaker protection
  - Thermal and excursion protection
  - Detects leak and damaged speaker
- 14.47-kHz to 96-kHz Sample rates
- 2 PDM MIC Inputs
- Flexible user interfaces
  - I^2S/TDM: 8 Channels (32 bit / 96 kHz)
  - I^2C: Selectable addresses
- MCLK Free operation
- Two 2.54 to 6.76 MHz PDM inputs
- Advanced brown-out prevention
- Power supplies
  - VBAT: 2.7 V to 5.5 V
  - VDD: 1.65 V to 1.95 V
  - IOVDD: 1.65 V to 3.6 V
- Spread-spectrum low EMI mode
- Thermal and overcurrent protection
- 42-Ball, 0.4 mm pitch, DSBGA package

2 Applications

- Smart Phone
- Tablets
- Laptop
- Wireless Speaker

3 Description

The TAS2563 is a digital input Class-D audio amplifier optimized for efficiently driving high peak power into small loudspeaker applications. The Class-D amplifier is capable of delivering 6.1 W of peak power into a 4 Ω load at a battery voltage of 3.6 V. TAS2563 supports boost bypass mode (External PVDD mode) where it can achieve 12W at 10% THD+N (4 Ω at 12 V).

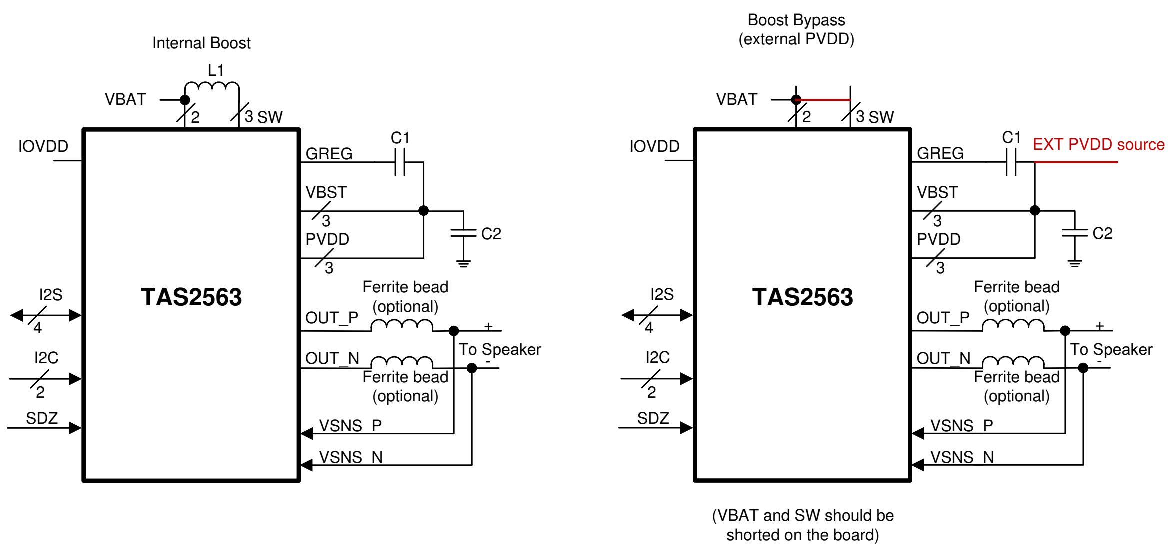
An on-chip, low-latency DSP supports Texas Instruments SmartAmp speaker protection algorithms to maximizes loudness while maintaining safe speaker conditions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TAS2563	DSBGA	2.5 mm × 3 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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5 Description (continued)

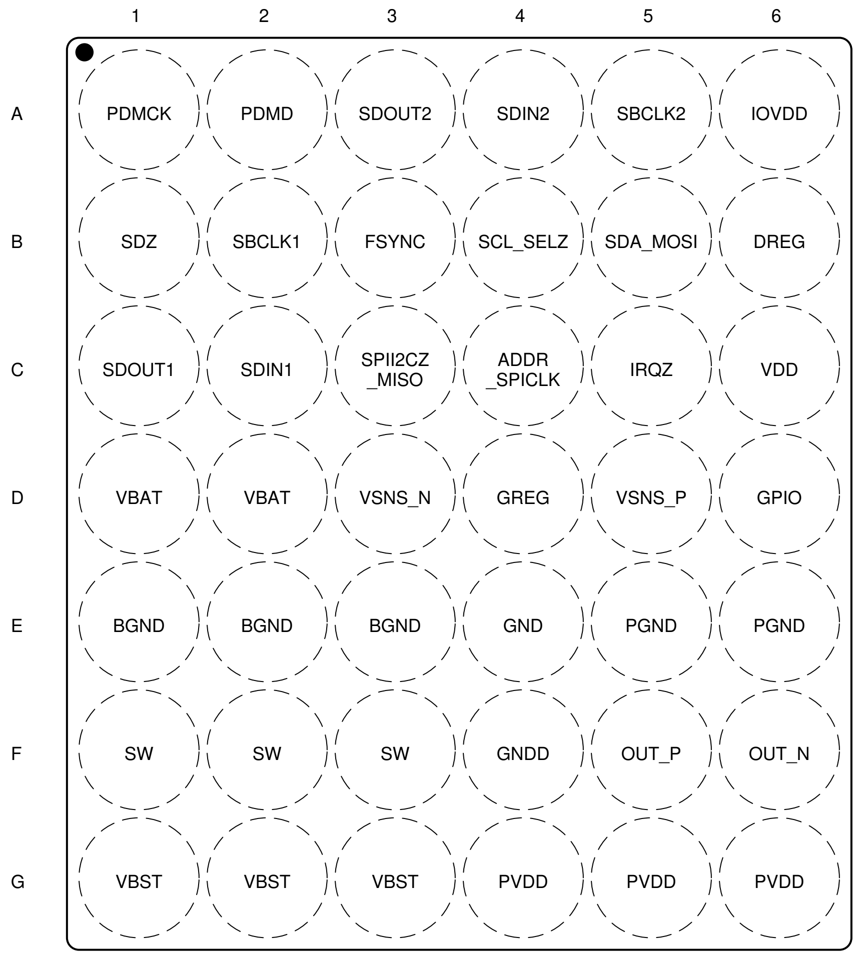
Integrated speaker voltage and current sense with internal protection algorithms provides for real time monitoring of the loudspeakers. This permits pushing peak SPL while keeping speakers in the safe operation area. A battery tracking peak voltage limiter with brown-out prevention optimizes amplifier headroom over the entire charge cycle preventing system shutdowns.

Up to eight devices can share a common bus via I^2S/TDM + I^2C interfaces.

The TAS2563 device is available in a 42-ball, 0.4 mm pitch DSBGA (YBG) for a compact PCB footprint.

6 Pin Configuration and Functions

YBG Package
42-Ball DSBGA
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ADDR_SPICLK	C4	I	I2C Mode - Address selection pin See General I2C operation. SPI Mode - SPI clock
DREG	B6	P	Digital core voltage regulator output. Bypass to GND with a cap. Do not connect to external load.
FSYNC	B3	I	I2S word clock or TDM frame sync for ASI1 and ASI2 channels.
GNDB	E1, E2, E3	P	Boost ground. Connect to PCB GND plane.
GNDD	E4,F4	P	Digital ground. Connect to PCB GND plane.
GNDP	E5,E6	P	Power stage ground. Connect to PCB GND plane.
GPIO	D6	IO	General purpose input-ouput or MCLK base on register configuration.
GREG	D4	P	High-side gate CP regulator output. Do not connect to external load.
IOVDD	A6	P	3.3-V/1.8-V IOVDD Supply
IRQZ	C5	O	Open drain, active low interrupt pin. Pull up to VDDD with resistor if optional internal pull up is not used.
OUT_N	F6	O	Class-D negative output for receiver channel.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
OUT_P	F5	O	Class-D positive output for receiver channel.
PDMCLK	A1	IO	PDM clock.
PDMD	A2	IO	PDM data.
PVDD	G4, G5, G6	P	Power stage supply.
SBCLK1	B2	I	ASI1 channel I2S/TDM serial bit clock.
SBCLK2	A5	I	ASI2 channel I2S/TDM serial bit clock.
SDA_MOSI	B5	IO	I2C Mode: I^2C Data Pin. Pull up to VDD with a resistor. SPI Mode: Serial data input pin.
SDIN1	C2	I	ASI1 channel I2S/TDM serial data input.
SDIN2	A4	I	ASI2 channel I2S/TDM serial data input.
SDOUT1	C1	IO	ASI1 channel I2S/TDM serial data output.
SDOUT2	A3	IO	ASI2 channel I2S/TDM serial data output.
SDZ	B1	I	Active low hardware shutdown.
SCL_SELZ	B4	IO	I2C Mode: I2C clock pin. Pull up to IOVDD with a resistor. SPI Mode: active low chip select.
SPII2CZ_MISO	C3	IO	Pin is queried on power-up. Short to GND for I2C Mode. Pull to IOVDD with resistor for SPI mode. SPI serial data output pin.
SW	F1, F2, F3	P	Boost converter switch input.
VBAT	D1, D2	P	Battery power supply input. Connect to 2.7 V to 5.5 V supply and decouple with a cap.
VBST	G1, G2, G3	P	Boost converter output. Do not connect to external load.
VDD	C6	P	Analog, digital, and IO power supply. Connect to 1.8 V supply and decouple to GND with cap.
VSNS_N	D3	I	Voltage sense negative input. Connect to Class-D OUT_N output after Ferrite bead filter.
VSNS_P	D5	I	Voltage sense positive input. Connect to Class-D OUT_P output after Ferrite bead filter.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
IO Supply IOVDD	IOVDD	-0.3	3.9	V
Analog Voltage	VDD	–0.3	2	V
Battery Supply Voltage	VBAT	–0.3	6	V
Class-D Output Pins	OUT_P/OUT_N	-1	18.5	V
V-Sense Pins	VSNS_P/VSNS_N (2)	-1	18.5	V
Boost Pin	VBST	-0.3	18.5	V
Power Supply Voltage	PVDD (3)	-0.3	18.5	V
Switching Pin	SW	-0.7	16	V
High Side Regulator Pin	GREG	-0.3	PVDD+6	V
Digital Regular Pin	DREG	-0.3	1.65	V
Input voltage (4)	Digital IOs referenced to VDD supply	–0.3	VDD+0.3	V
Operating free-air temperature, T_A		–40	85	°C
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Procedures*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) VSNS_P/VSNS_N can handle 25V transients for less than 10ns
(3) PVDD can handle 19V transients for less than 10ns
(4) All digital inputs and IOs are failsafe.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 OUT_N / OUT_P / VSNS_N / VSNS_P Pins[1]	±3000	V
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IOVDD	IO Supplly Voltage 1.8V	1.62	1.8	1.98	V
IOVDD	IO Supply Voltage 3.3V	3	3.3	3.6	V
VBAT	Supply voltage	2.5	3.6	5.5	V
VDD	Supply voltage	1.62	1.8	1.95	V
PVDD (VBST)	Supply voltage - external boost mode	VBAT		16	V
V_{IH}	High-level digital input voltage	0.7 x IOVDD			V
V_{IL}	Low-level digital input voltage		0		V
R_{SPK}	Minimum speaker impedance	3.2			Ω
L_{SPK}	Minimum speaker inductance	10			µH

7.4 Thermal Information

THERMAL METRIC		TAS2563 YBG (WCSP) 42 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

7.5 Electrical Characteristics

T_A = 25 °C, VBAT = 3.6 V, (External PVDD = 12 V), VDD = 1.8 V, R_L = 8Ω + 33 µH, f_{in} = 1 kHz, SSM, f_s = 48 kHz, Gain = 16 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT and OUTPUT						
V_{IH}	High-level digital input logic voltage threshold (max current limit = 30 mA)	All digital pins except SDA_MOSI and SCL_SELZ	0.65 × IOVDD			V
V_{IL}	Low-level digital input logic voltage threshold (max current limit = 30 mA)	All digital pins except SDA_MOSI and SCL_SELZ			0.35 × IOVDD	V
$V_{IH(I2C)}$	High-level digital input logic voltage threshold (max current limit = 30 mA)	SDA_MOSI and SCL_SELZ	0.7 × IOVDD			V
$V_{IL(I2C)}$	Low-level digital input logic voltage threshold (max current limit = 30 mA)	SDA_MOSI and SCL_SELZ			0.3 × IOVDD	V
V_{OH}	High-level digital output voltage (max current limit = 30 mA)	All digital pins except SDA_MOSI ,SCL_SELZ and IRQZ; I_{OH} = 2 mA.	IOVDD – 0.45 V			V
V_{OL}	Low-level digital output voltage (max current limit = 30 mA)	All digital pins except SDA_MOSI ,SCL_SELZ and IRQZ; I_{OL} = –2 mA.			0.45	V
$V_{OL(I2C)}$	Low-level digital output voltage (max current limit = 30 mA)	SDA and SCL; $I_{OL(I2C)}$ = –2 mA.			0.2 × IOVDD	V
$V_{OL(IRQZ)}$	Low-level digital output voltage for IRQZ open drain Output (max current limit = 30 mA)	IRQZ; $I_{OL(IRQZ)}$ = –2 mA.			0.45	V

Electrical Characteristics (continued)

T_A = 25 °C, VBAT = 3.6 V, (External PVDD = 12 V), VDD = 1.8 V, R_L = 8Ω + 33 µH, f_{in} = 1 kHz, SSM, f_s = 48 kHz, Gain = 16 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	Input logic-high leakage for digital inputs	All digital pins; Input = VDD.	–5	0.1	5	µA
I_{IL}	Input logic-low leakage for digital inputs	All digital pins; Input = GND.	–5	0.1	5	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pull down resistance for digital input/IO pins when asserted on	SDOUT, SDIN, FSYNC, SBCLK, PDMD, PDMCLK		50		kΩ
AMPLIFIER PERFORMANCE - Internal Boost						
	Output Voltage for Full-scale digital Input	Measured at -6 dB FS input		6.32		Vrms
P_{OUT}	Maximum Continuous Output Power	R_L = 32Ω + 33 µH, THD+N = 0.03 %, f_{in} = 1 kHz		1.25		W
		R_L = 8 Ω + 33 µH, THD+N = 0.03 %, f_{in} = 1 kHz		5		W
		R_L = 4 Ω + 33 µH, THD+N = 1 %, f_{in} = 1 kHz		6.1		W
	System efficiency at P_{OUT} = 1 W	R_L = 8 Ω + 33 µH, f_{in} = 1 kHz		82		%
		R_L = 4 Ω + 33 µH, f_{in} = 1 kHz		78.5		%
		R_L = 8 Ω + 33 µH, f_{in} = 1 kHz, VBAT = 4.2 V		82.5		%
		R_L = 4 Ω + 33 µH, f_{in} = 1 kHz, VBAT = 4.2 V		84.2		%
	System efficiency at P_{OUT} =0.5 W	R_L = 8 Ω + 33 µH, f_{in} = 1 kHz		76.6		%
		R_L = 4 Ω + 33 µH, f_{in} = 1 kHz		81.1		%
		R_L = 8 Ω + 33 µH, f_{in} = 1 kHz, VBAT = 4.2 V		84.2		%
		R_L = 4 Ω + 33 µH, f_{in} = 1 kHz, VBAT = 4.2 V		81.6		%
	System efficiency at 0.1% THD+N power level	R_L = 32 Ω + 33 µH, f_{in} = 1 kHz,		78.8		%
		R_L = 8 Ω + 33 µH, f_{in} = 1 kHz,		80		%
		R_L = 4 Ω + 33 µH, f_{in} = 1 kHz		76.2		%
THD+N	Total harmonic distortion + noise	P_{OUT} = 0.25 W, R_L = 32Ω + 33 µH, f_{in} = 1 kHz		0.01		%
		P_{OUT} = 1 W, R_L = 8 Ω + 33 µH, f_{in} = 1 kHz		0.01		%
		P_{OUT} = 1 W, R_L = 4 Ω + 33 µH, f_{in} = 1 kHz		0.01		%
V_N	Idle channel noise	A-Weighted, 20 Hz - 20 kHz, DAC Modulator Running		14.8		µV
F_{PWM}	Class-D PWM switching frequency	Average frequency in Spread Spectrum Mode, CLASSD_SYNC=0		384		kHz
		Fixed Frequency Mode, CLASSD_SYNC=0		384		kHz
		Fixed Frequency Mode, CLASSD_SYNC=1, f_s = 44.1, 88.2, 174.6 kHz		352.8		kHz
		Fixed Frequency Mode, CLASSD_SYNC=1, f_s = 48, 96, 192 kHz		384		kHz
V_{OS}	Output offset voltage		-1		1	mV
DNR	Dynamic range	A-Weighted, -60 dBFS Method		109		dB
SNR	Signal to noise ratio	A-Weighted, Referenced to 1 % THD+N Output Level		112.5		dB
K_{CP}	Click and pop performance	Into and out of Mute, Shutdown, Power Up, Power Down and audio clocks starting and stopping. Measured with APx Plugin.		3.4		mV
	Programmable output level range		8		18	dBV
	Programmable output level step size			0.5		dB
AV_{ERROR}	Amplifier gain error	P_{OUT} = 1 W		±0.1		dB

Electrical Characteristics (continued)

T_A = 25 °C, VBAT = 3.6 V, (External PVDD = 12 V), VDD = 1.8 V, R_L = 8Ω + 33 µH, f_{in} = 1 kHz, SSM, f_s = 48 kHz, Gain = 16 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Mute attenuation	Device in Shutdown or Muted in Normal Operation		110		dB
	VBAT power-supply rejection ratio	VBAT = 3.6 V + 200 mV_{pp}, f_{ripple} = 217 Hz		108		dB
		VBAT = 3.6 V + 200 mV_{pp}, f_{ripple} = 20 kHz		90		dB
	AVDD power-supply rejection ratio	VDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 217 Hz		98		dB
		VDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 20 kHz		93		dB
	Turn on time from release of SW shutdown	No Volume Ramping		1.8		ms
		Volume Ramping		4.5		ms
	Turn off time from assertion of SW shutdown to amp Hi-Z	No Volume Ramping		1.5		ms
		Volume Ramping		12.5		ms
AMPLIFIER PERFORMANCE - External PVDD						
	Output Voltage for Full-scale digital Input	Measured at -6 dB FS input		7.94		Vrms
P_{OUT}	Maximum Continuous Output Power	R_L = 32Ω + 33 µH, THD+N = 1 %, f_{in} = 1 kHz		1.3		W
		R_L = 8 Ω + 33 µH, THD+N = 1 %, f_{in} = 1 kHz		5.2		W
		R_L = 4 Ω + 33 µH, THD+N = 1 %, f_{in} = 1 kHz		10.4		W
		R_L = 32Ω + 33 µH, THD+N = 10 %, f_{in} = 1 kHz		1.6		W
		R_L = 8 Ω + 33 µH, THD+N = 10 %, f_{in} = 1 kHz		6.3		W
		R_L = 4 Ω + 33 µH, THD+N = 10%, f_{in} = 1 kHz		12.6		W
	System efficiency at P_{OUT} = 1 W	R_L = 8 Ω + 33 µH, f_{in} = 1 kHz		83.8		%
		R_L = 4 Ω + 33 µH, f_{in} = 1 kHz		80		%
		R_L = 8 Ω + 33 µH, f_{in} = 1 kHz, External PVDD = 8.4 V		85.9		%
		R_L = 4 Ω + 33 µH, f_{in} = 1 kHz, External PVDD = 8.4 V		81.8		%
	System efficiency at 0.1% THD+N power level	R_L = 32 Ω + 33 µH, f_{in} = 1 kHz,		87.4		%
		R_L = 8 Ω + 33 µH, f_{in} = 1 kHz,		90		%
		R_L = 4 Ω + 33 µH, f_{in} = 1 kHz		85.2		%
		R_L = 32 Ω + 33 µH, f_{in} = 1 kHz, External PVDD = 8.4 V		81.9		%
		R_L = 8 Ω + 33 µH, f_{in} = 1 kHz, External PVDD = 8.4 V		90		%
		R_L = 4 Ω + 33 µH, f_{in} = 1 kHz, External PVDD = 8.4 V		86		%
THD+N	Total harmonic distortion + noise	P_{OUT} = 0.25 W, R_L = 32Ω + 33 µH, f_{in} = 1 kHz		0.01		%
		P_{OUT} = 1 W, R_L = 8 Ω + 33 µH, f_{in} = 1 kHz		0.01		%
		P_{OUT} = 1 W, R_L = 4 Ω + 33 µH, f_{in} = 1 kHz		0.02		%
V_N	Idle channel noise	A-Weighted, 20 Hz - 20 kHz, DAC Modulator Running		21.3		µV
F_{PWM}	Class-D PWM switching frequency	Average frequency in Spread Spectrum Mode, CLASSD_SYNC=0		384		kHz
		Fixed Frequency Mode, CLASSD_SYNC=0		384		kHz
		Fixed Frequency Mode, CLASSD_SYNC=1, f_s = 44.1, 88.2, 174.6 kHz		352.8		kHz
		Fixed Frequency Mode, CLASSD_SYNC=1, f_s = 48, 96, 192 kHz		384		kHz
V_{OS}	Output offset voltage		-1		1	mV

Electrical Characteristics (continued)

T_A = 25 °C, VBAT = 3.6 V, (External PVDD = 12 V), VDD = 1.8 V, R_L = 8Ω + 33 µH, f_{in} = 1 kHz, SSM, f_s = 48 kHz, Gain = 16 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DNR	Dynamic range	A-Weighted, -60 dBFS Method		109		dB
SNR	Signal to noise ratio	A-Weighted, Referenced to 1 % THD+N Output Level		109.5		dB
K_{CP}	Click and pop performance	Into and out of Mute, Shutdown, Power Up, Power Down and audio clocks starting and stopping. Measured with APx Plugin.		3		mV
	Programmable output level range		8		18	dBV
	Programmable output level step size			0.5		dB
AV_{ERROR}	Amplifier gain error	P_{OUT} = 1 W		±0.1		dB
	Mute attenuation	Device in Shutdown or Muted in Normal Operation		110		dB
	VBAT power-supply rejection ratio	VBAT = 3.6 V + 200 mV_{pp}, f_{ripple} = 217 Hz		110		dB
		VBAT = 3.6 V + 200 mV_{pp}, f_{ripple} = 20 kHz		90		dB
	PVDD power-supply rejection ratio	PVDD = 12 V + 200 mV_{pp}, f_{ripple} = 217 Hz		105		dB
		PVDD = 12 V + 200 mV_{pp}, f_{ripple} = 20 kHz		90		dB
	AVDD power-supply rejection ratio	VDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 217 Hz		86		dB
		VDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 20 kHz		73		dB
	Turn on time from release of SW shutdown	No Volume Ramping		1.8		ms
		Volume Ramping		4.5		ms
	Turn off time from assertion of SW shutdown to amp Hi-Z	No Volume Ramping		0.75		ms
		Volume Ramping		12.5		ms
BOOST CONVERTER						
	Startup inrush current limit	default setting		1.5		A
	Startup inrush limit time	default setting		0.45		ms
	Switching Frequency	PFM mode		50		kHz
		Current Control Mode		4		MHz
	Inductor Peak Current Limit	default setting		4		A
DIE TEMPERATURE SENSOR						
	Resolution			8		bits
	Die temperature measurement range		-40		150	°C
	Die temperature resolution			0.75		°C
	Die temperature accuracy			±5		°C
VOLTAGE MONITOR						
	Resolution			10		bits
	VBAT measurement range		2		6	V
	VBAT resolution			6		mV
	VBAT accuracy			±25		mV
TDM SERIAL AUDIO PORT						
	PCM Sample Rates & FSYNC Input Frequency		16		96	kHz
	SBCLK Input Frequency	I^2S/TDM Operation	0.512		24.57	MHz
	SBCLK Maximum Input Jitter	RMS Jitter below 40 kHz that can be tolerated without performance degradation			1	ns
		RMS Jitter above 40 kHz that can be tolerated without performance degradation			10	ns

Electrical Characteristics (continued)

T_A = 25 °C, VBAT = 3.6 V, (External PVDD = 12 V), VDD = 1.8 V, R_L = 8Ω + 33 µH, f_{in} = 1 kHz, SSM, f_s = 48 kHz, Gain = 16 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	SBCLK Cycles per FSYNC in I²S and TDM Modes	Values: 64, 96, 128, 192, 256, 384 and 512	64		512	Cycles
PCM PLAYBACK CHARACTERISTICS to fs ≤ 48 kHz						
fs	Sample Rates		16		48	kHz
	Passband LPF Corner			0.454		fs
	Passband Ripple	20 Hz to LPF cutoff	-0.3		0.3	dB
	Stop Band Attenuation	≥ 0.55 fs		60		dB
		≥ 1 fs		65		dB
	Group Delay (ROM MODE)	DC to 0.454 fs			17.2	1/fs
PCM PLAYBACK CHARACTERISTICS fs > 48 kHz						
fs	Sample Rates		88.2		96	kHz
	Passband LPF Corner	fs = 96 kHz		0.42		fs
	Passband Ripple	DC to LPF cutoff	-0.5		0.5	dB
	Stop Band Attenuation	≥ 0.55 fs		60		dB
		≥ 1 fs		65		dB
CURRENT SENSE						
DNR	Dynamic range	Un-Weighted, Relative to 0 dBFS		69		dB
THD+N	Total harmonic distortion + noise	R_L = 8 Ω + 33 µH, f_{in} = 1 kHz, P_{OUT} = 1 W		-56		dB
		R_L = 4 Ω + 33 µH, f_{in} = 1 kHz, P_{OUT} = 1 W		-57		dB
	Full-scale input current			2.0		A
	Current-sense accuracy	R_L = 8 Ω + 33 µH, I_{OUT} = 354 mA_{RMS} (P_{OUT} = 1 W @ 1kHz)		±1		%
	Current-sense gain error over temperature	0°C to 70°C, 8 Ω, using a 60Hz -40dB pilot tone		±1		%
	Current-sense gain error over output power	50mW to 0.1 % THD+N level, f_{in} = 1 kHz, 8 Ω, using a 60Hz -40dB pilot tone		±1.5		%
	LPF passband corner	fs = 8 kHz to 48 kHz		0.417		fs
		fs = 88.2 kHz		0.208		fs
		fs = 96 kHz		0.208		fs
	LPF passband ripple		-0.05		0.05	dB
	LPF stopband attenuation	0.55 fs		60		dB
VOLTAGE SENSE						
DNR	Dynamic range	Un-Weighted, Relative 0 dBFS		69		dB
THD+N	Total harmonic distortion + noise	R_L = 8 Ω + 33 µH, f_{in} = 1 kHz, P_{OUT} = 1W		-60		dB
		R_L = 4 Ω + 33 µH, f_{in} = 1 kHz, P_{OUT} = 1W		-60		dB
	Full-scale input voltage			14		V_{PK}
	Voltage-sense accuracy	R_L = 8 Ω + 33 µH, I_{OUT} = 354 mA_{RMS} (P_{OUT} = 1 W)		±0.5%		
	Voltage-sense gain error over temperature	0°C to 70°C, 8 Ω, using a 60Hz -40dB pilot tone		±0.5%		
	Voltage-sense gain error over output power	50mV to 0.1 % THD+N level, 8 Ω, using a 60Hz -40dB pilot tone		±0.5%		
	LPF passband corner	fs = 14.7 kHz to 48 kHz		0.417		fs
		fs = 88.2 kHz		0.208		fs
		fs = 96 kHz		0.208		fs
	LPF passband ripple		-0.05		0.05	dB
	LPF stopband attenuation	0.55 fs		60		dB

Electrical Characteristics (continued)

T_A = 25 °C, VBAT = 3.6 V, (External PVDD = 12 V), VDD = 1.8 V, R_L = 8Ω + 33 µH, f_{in} = 1 kHz, SSM, f_s = 48 kHz, Gain = 16 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE/CURRENT SENSE RATIO						
	Gain ratio error over output power	50mW to 0.1 % THD+N level, fin = 1 kHz, 8Ω, using a 60Hz -40dB pilot tone		±1%		
	Gain ratio drift over temperature	0°C to 70°C		±1%		
	V/I phase error			300		ns
TYPICAL CURRENT CONSUMPTION						
	Current consumption in hardware shutdown	SDZ = 0, VBAT		1		µA
		SDZ = 0, VDD		1		µA
	Current consumption in software shutdown	All Clocks Stopped, VBAT		1		µA
		All Clocks Stopped, VDD		10		µA
	Current consumption in idle channel	Clocking 0s PCM mode, VBAT		2.7		mA
		Clocking 0s PCM mode, VDD		10.9		mA
	Current consumption during active operation with IV sense disabled	f_s = 48 kHz, VBAT		4.6		mA
		f_s = 48 kHz, VDD		10.9		mA
	Current consumption during active operation with IV sense enabled	f_s = 48 kHz, VBAT		4.6		mA
		f_s = 48 kHz, VDD		12.5		mA
PROTECTION CIRCUITRY						
	Thermal shutdown temperature			140		°C
	Thermal shutdown retry			1.5		s
	VBAT undervoltage lockout threshold (UVLO)	UVLO is asserted	2			V
		UVLO is released			2.55	V
	Output short circuit limit	Output to Output, Output to GND, Output to VBST or Output to VBAT Short		3.75		A

7.6 I²C Timing Requirements

T_A = 25 °C, VDD = 1.8 V (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Standard-Mode					
f_{SCL}	SCL clock frequency	0		100	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4			µs
t_{LOW}	LOW period of the SCL clock	4.7			µs
t_{HIGH}	HIGH period of the SCL clock	4			µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7			µs
$t_{HD;DAT}$	Data hold time: For I²C bus devices	0		3.45	µs
$t_{SU;DAT}$	Data set-up time	250			ns
t_r	SDA and SCL rise time			1000	ns
t_f	SDA and SCL fall time			300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
C_b	Capacitive load for each bus line			400	pF
Fast-Mode					
f_{SCL}	SCL clock frequency	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6			µs
t_{LOW}	LOW period of the SCL clock	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition	40.6			µs
$t_{HD;DAT}$	Data hold time: For I²C bus devices	0		0.9	µs
$t_{SU;DAT}$	Data set-up time	100			ns
t_r	SDA and SCL rise time	20 + 0.1 × Cb		300	ns
t_f	SDA and SCL fall time	20 + 0.1 × Cb		300	ns
$t_{SU;STO}$	Set-up time for STOP condition	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
C_b	Capacitive load for each bus line			400	pF
Fast-Mode Plus					
f_{SCL}	SCL clock frequency	0		1000	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26			µs
t_{LOW}	LOW period of the SCL clock	0.5			µs
t_{HIGH}	HIGH period of the SCL clock	0.26			µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.26			µs
$t_{HD;DAT}$	Data hold time: For I²C bus devices	0			µs
$t_{SU;DAT}$	Data set-up time	50			ns
t_r	SDA and SCL Rise Time			120	ns
t_f	SDA and SCL Fall Time			120	ns
$t_{SU;STO}$	Set-up time for STOP condition				µs
t_{BUF}	Bus free time between a STOP and START condition	0.5			µs
C_b	Capacitive load for each bus line			550	pF

7.7 SPI Timing Requirements

For SPI interface signals over recommended operating conditions (unless otherwise noted). **Note:** All timing specifications are specified by design but not tested at final test. See

SYMBOL	PARAMETER	CONDITIONS	IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{sck}	SCLK Period		60		50		ns
t_{sckh}	SCLK Pulse width High		30		25		ns
t_{sckl}	SCLK Pulse width Low		30		25		ns
t_{lead}	Enable Lead Time		60		50		ns
t_{trail}	Enable Trail Time		60		50		ns
$t_{d;seqxfr}$	Sequential Transfer Delay		60		50		ns
t_a	Slave DOUT access time			20		20	ns
t_{dis}	Slave DOUT disable time			20		20	ns
t_{su}	DIN data setup time		8		8		ns
$t_{h;DIN}$	DIN data hold time		8		8		ns
$t_{v;DOUT}$	DOUT data valid time			20		20	ns
t_r	SCLK Rise Time			4		4	ns
t_f	SCLK Fall Time			4		4	ns
Pd-spi	External Pullup on SPII2CSELZ_MISO_PAD		18		18		kΩ

7.8 PDM Port Timing Requirements

T_A = 25 °C, AVDD = IOVDD = 1.8 V, 20 pF load on all outputs (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{SU}(PDM)	PDM IN setup time		20			ns
t_{HLD}(PDM)	PDM IN hold time		3			ns
t_r(PDM)	PDM IN rise time	10 % - 90 % Rise Time			4	ns
t_f(PDM)	PDM IN fall time	90 % - 10 % Fall Time			4	ns

7.9 TDM Port Timing Requirements

T_A = 25 °C, VDD = 1.8 V, 20 pF load on all outputs (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_H(SBCLK)	SBCLK high period		20			ns
t_L(SBCLK)	SBCLK low period		20			ns
t_{SU}(FSYNC)	FSYNC setup time		6.5			ns
t_{HLD}(FSYNC)	FSYNC hold time		6.5			ns
t_{SU}(FSYNC)	SDIN setup time		6.5			ns
t_{HLD}(SDIN)	SDIN hold time		6.5			ns
t_d(DO-SBCLK)	SBCLK to SDOUT delay	50% of SBCLK to 50% of SDOUT			29	ns
t_r(SBCLK)	SBCLK rise time	10% - 90 % Rise Time			8	ns
t_f(SBCLK)	SBCLK fall time	90% - 10 % Fall Time			8	ns

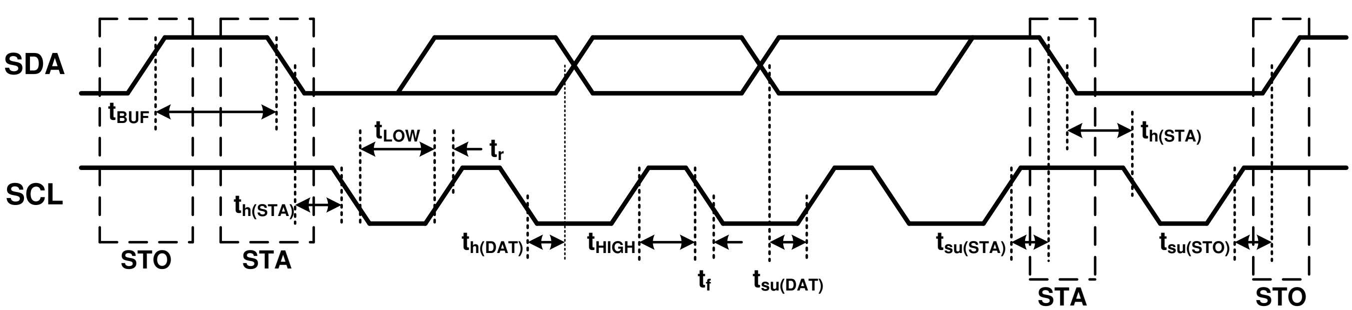


Figure 1. I2C Timing Diagram

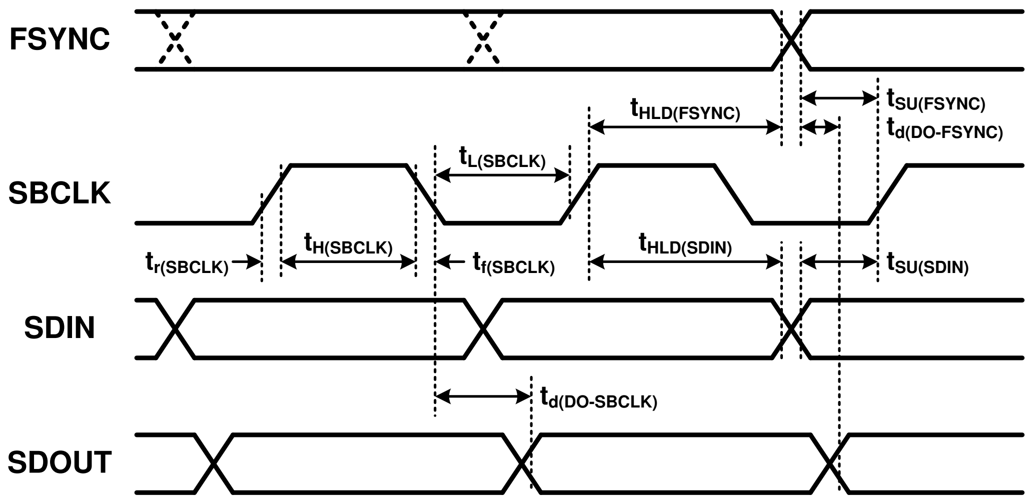


Figure 2. TDM Timing Diagram

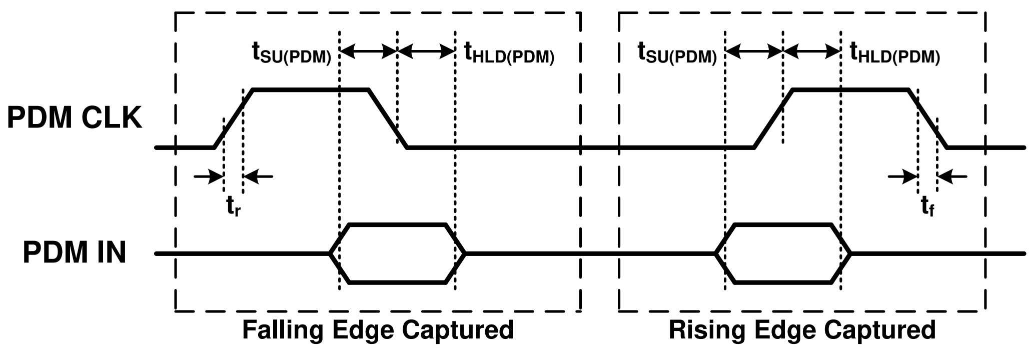


Figure 3. PDM Timing Diagram

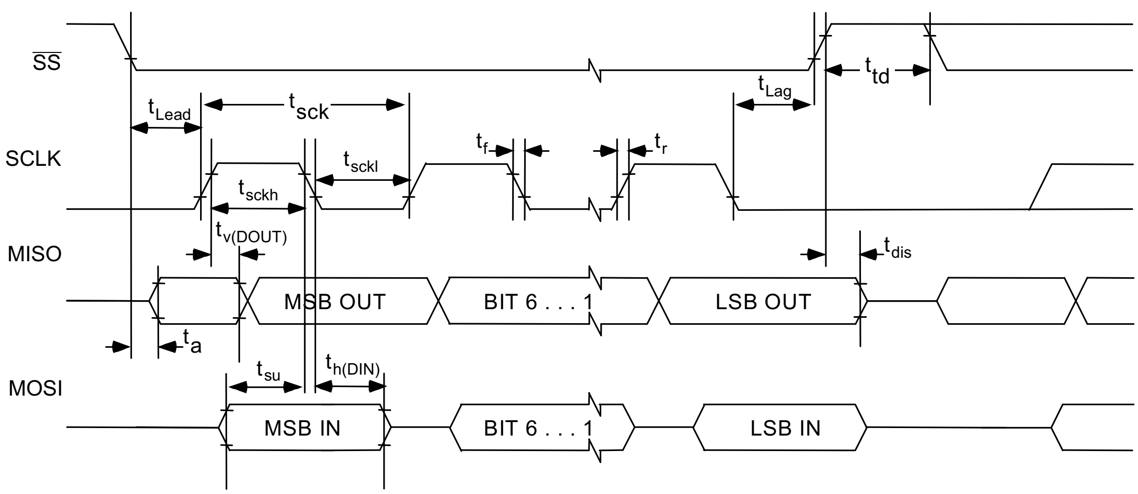
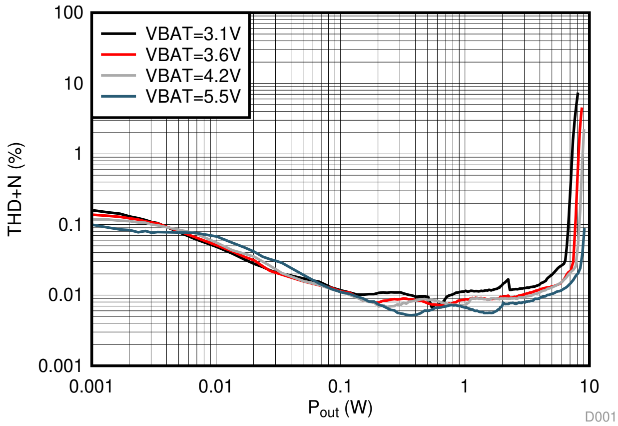


Figure 4. SPI Interface Timing Diagram

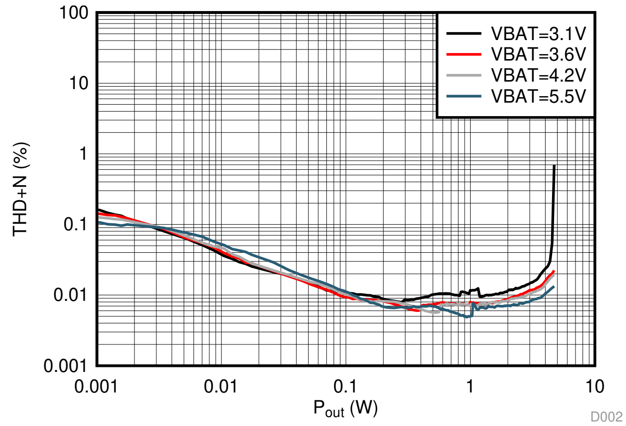
7.10 Typical Characteristics

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 µH, unless otherwise noted.



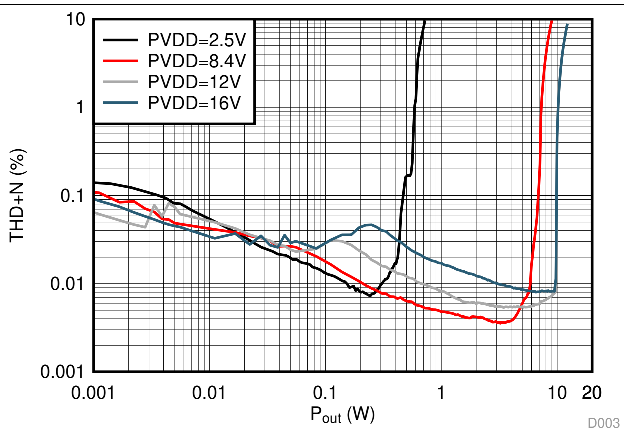
RL = 4 Ω + 30 µH F_{IN} = 1 kHz

Figure 5. THD+N vs Output Power



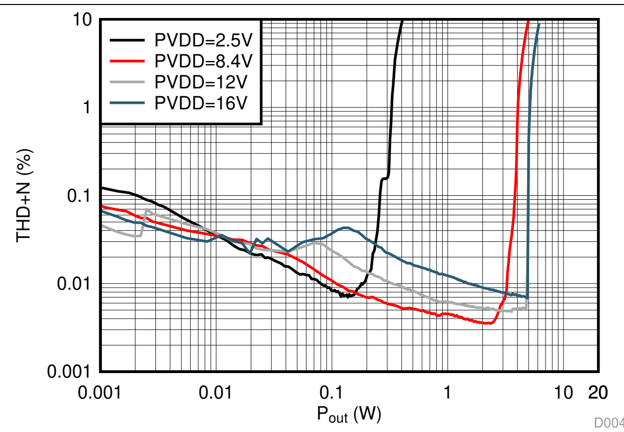
RL = 8 Ω + 30 µH F_{IN} = 1 kHz

Figure 6. THD+N vs Output Power



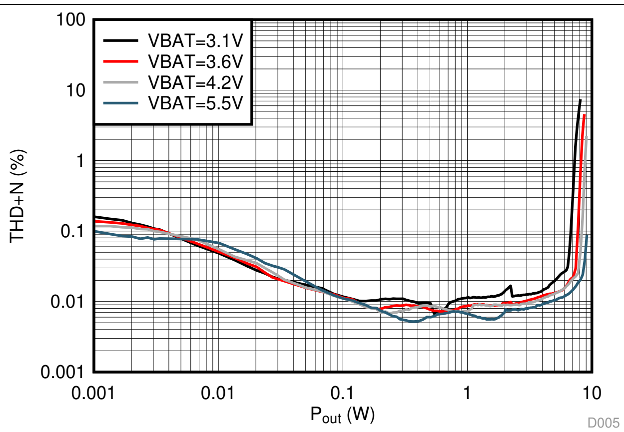
RL = 4 Ω + 30 µH F_{IN} = 1 kHz

Figure 7. THD+N vs Output Power



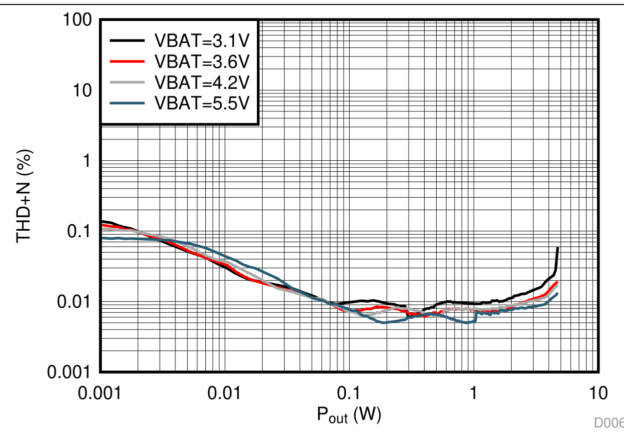
RL = 8 Ω + 30 µH F_{IN} = 1 kHz

Figure 8. THD+N vs Output Power



RL = 4 Ω + 30 µH F_{IN} = 6.667 kHz

Figure 9. THD+N vs Output Power

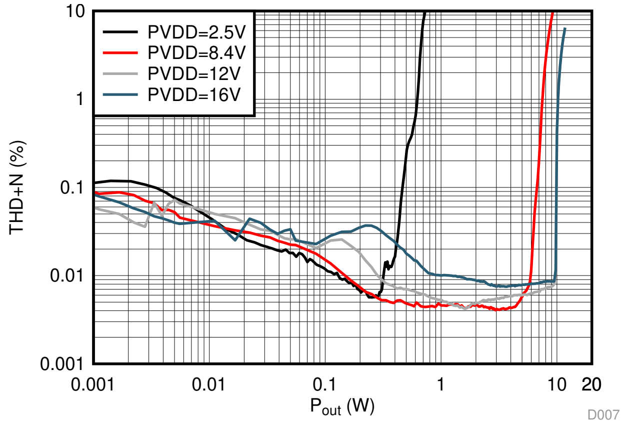


RL = 8 Ω + 30 µH F_{IN} = 6.667 kHz

Figure 10. THD+N vs Output Power

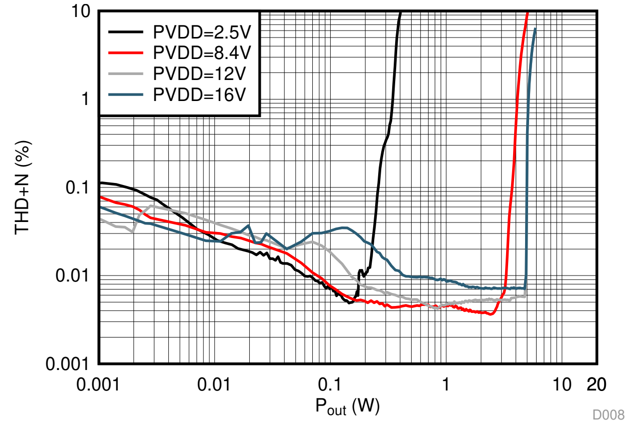
Typical Characteristics (continued)

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 µH, unless otherwise noted.



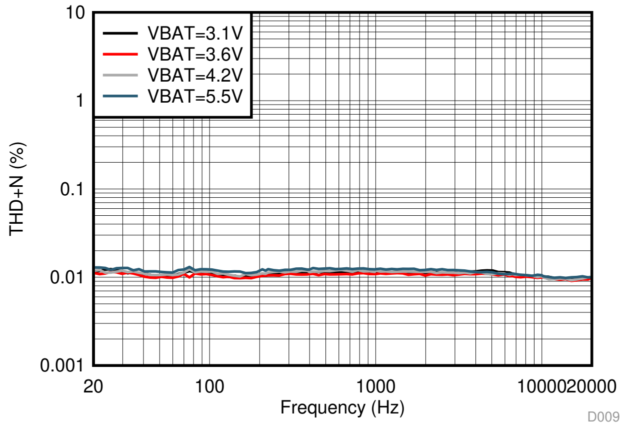
RL = 4 Ω + 30 µH F_{IN} = 1 kHz

Figure 11. THD+N vs Output Power



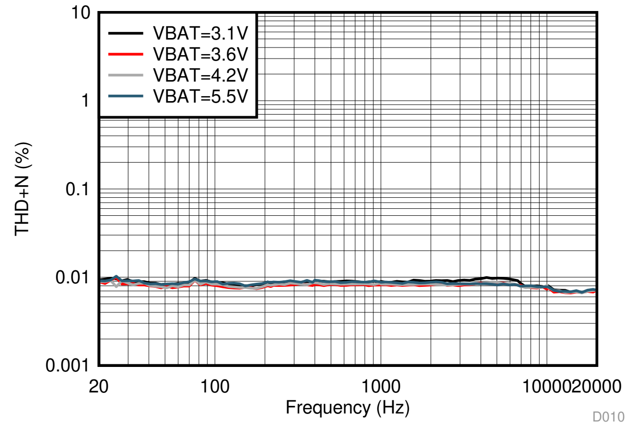
RL = 8 Ω + 30 µH F_{IN} = 1 kHz

Figure 12. THD+N vs Output Power



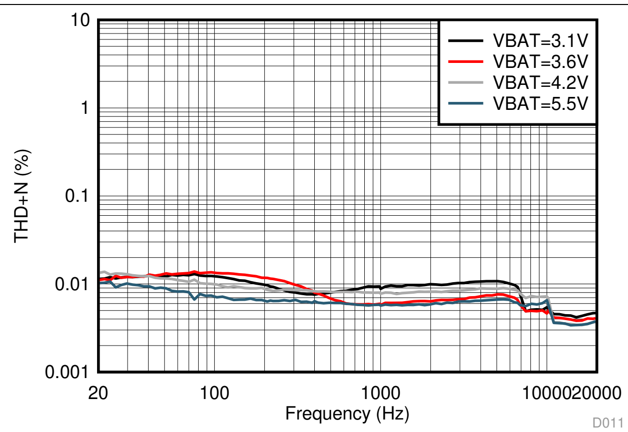
RL = 4 Ω + 30 µH   P = 0.1 W

Figure 13. THD+N vs Frequency



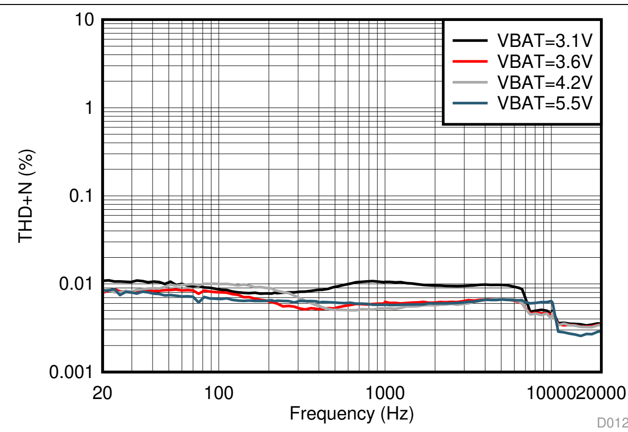
RL = 8 Ω + 30 µH   P = 0.1 W

Figure 14. THD+N vs Frequency



RL = 4 Ω + 30 µH   P = 1 W

Figure 15. THD+N vs Frequency



RL = 8 Ω + 30 µH   P = 1 W

Figure 16. THD+N vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 µH, unless otherwise noted.

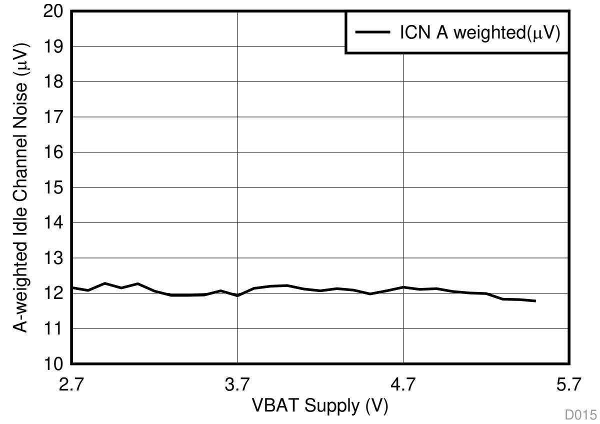


Figure 17. Idle Channel Noise (A-Weighted) vs VBAT

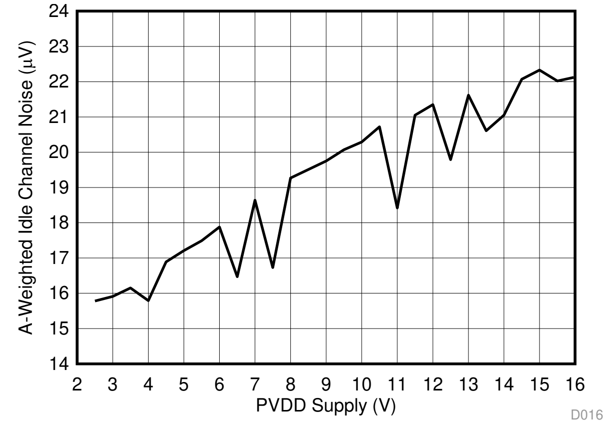
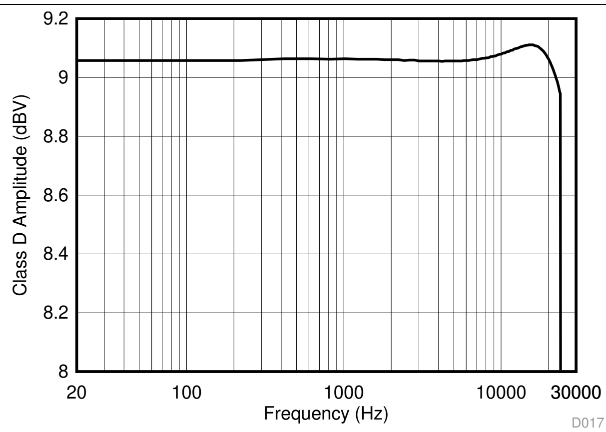
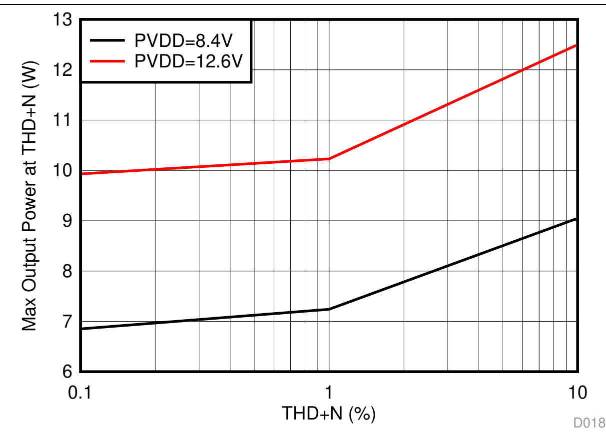


Figure 18. Idle Channel Noise (A-Weighted) vs PVDD



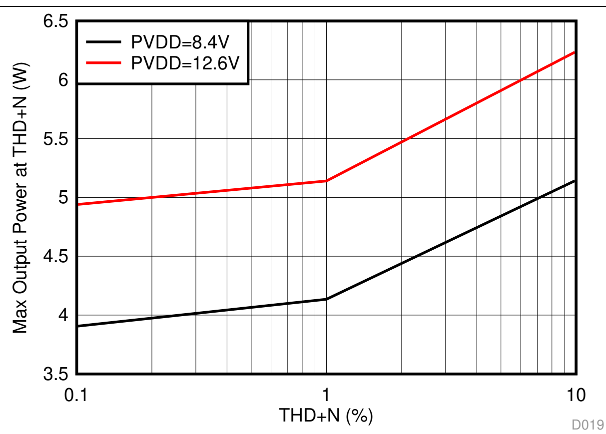
RL = 8 Ω + 30 µH F_S = 48 kHz

Figure 19. Amplitude vs Frequency



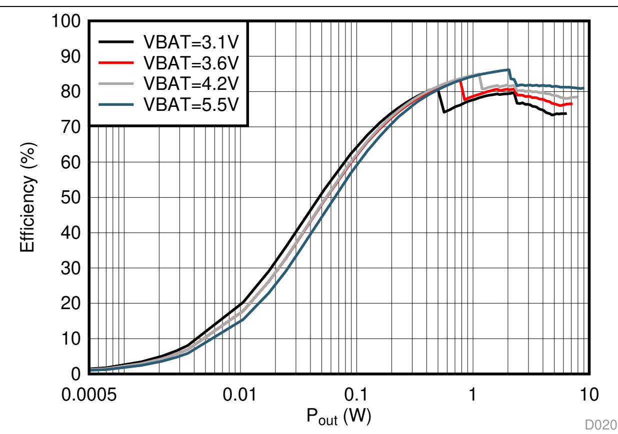
RL = 4 Ω + 30 µH

Figure 20. Max Output Power vs THD+N



RL = 8 Ω + 30 µH

Figure 21. Max Output Power vs THD+N

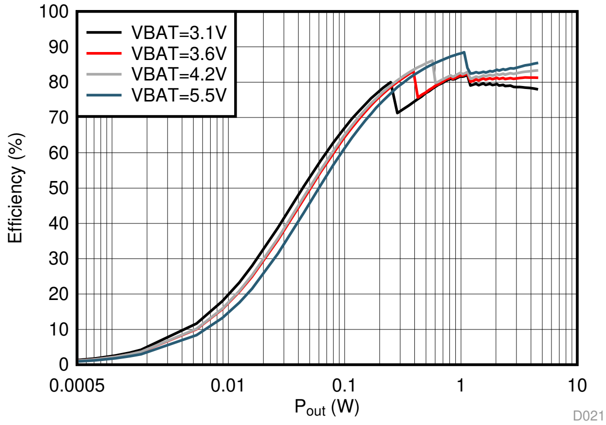


RL = 4 Ω + 30 µH F_{IN} = 1 kHz

Figure 22. Efficiency vs Output Power

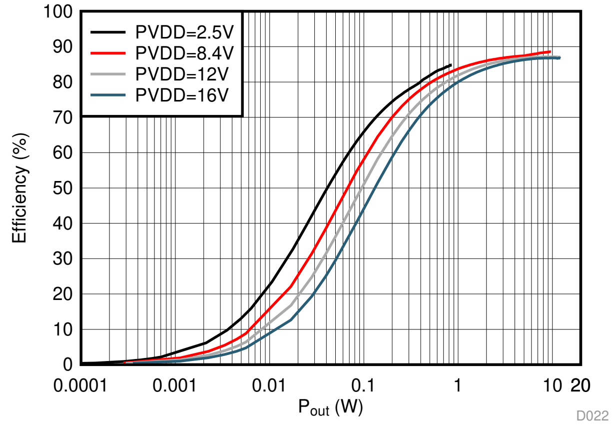
Typical Characteristics (continued)

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 µH, unless otherwise noted.



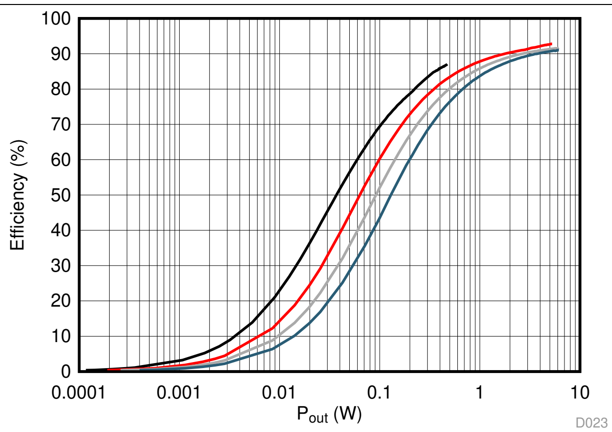
RL = 8 Ω + 30 µH F_{IN} = 1 kHz

Figure 23. Efficiency vs Output Power



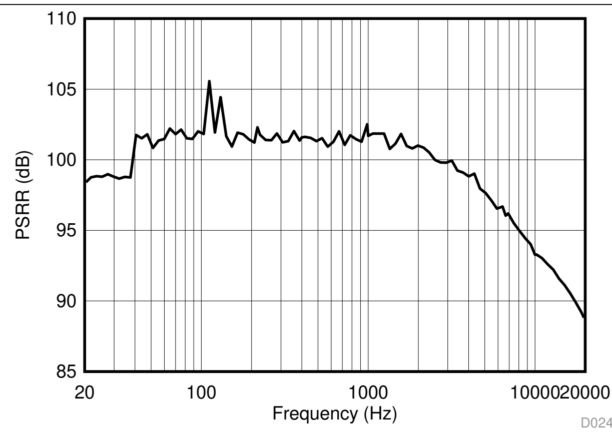
RL = 4 Ω + 30 µH F_{IN} = 1 kHz   Bypass Mode

Figure 24. Efficiency vs Output Power



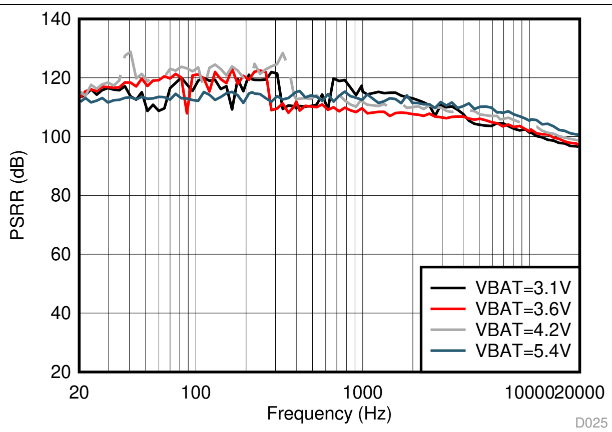
RL = 8 Ω + 30 µH F_{IN} = 1 kHz   Bypass Mode

Figure 25. Efficiency vs Output Power



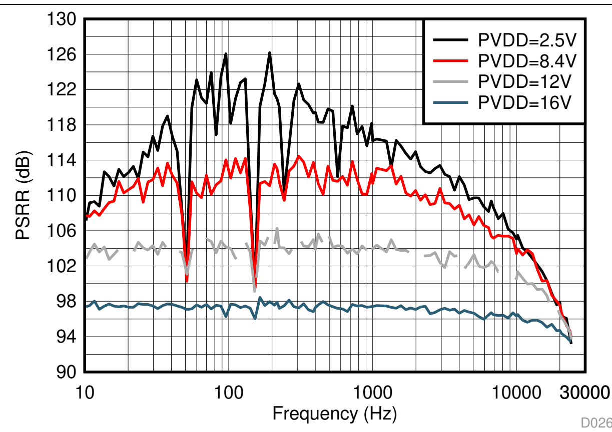
RL = 8 Ω + 30 µH   Idle Channel

Figure 26. AVDD PSRR vs Frequency



RL = 8 Ω + 30 µH   Idle Channel

Figure 27. VBAT PSRR vs Frequency



RL = 8 Ω + 30 µH   Idle Channel

Figure 28. PVDD PSRR vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 µH, unless otherwise noted.

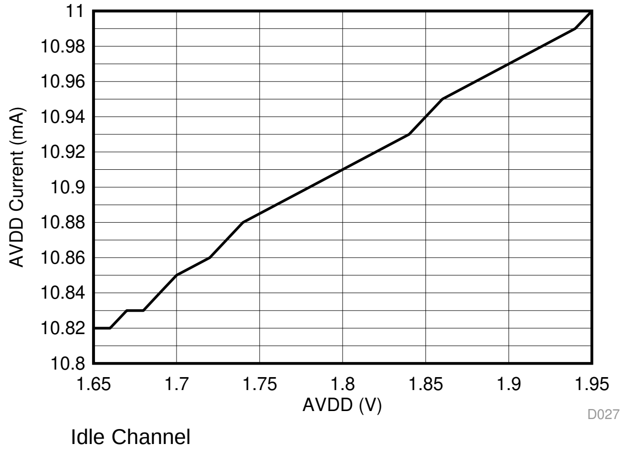


Figure 29. AVDD Idle Current vs AVDD

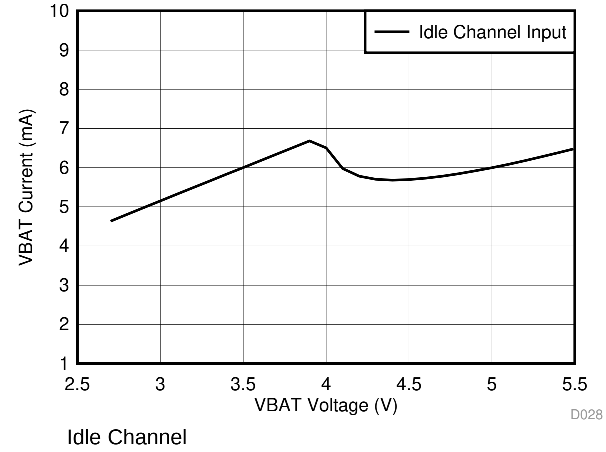


Figure 30. VBAT Idle Current vs VBAT

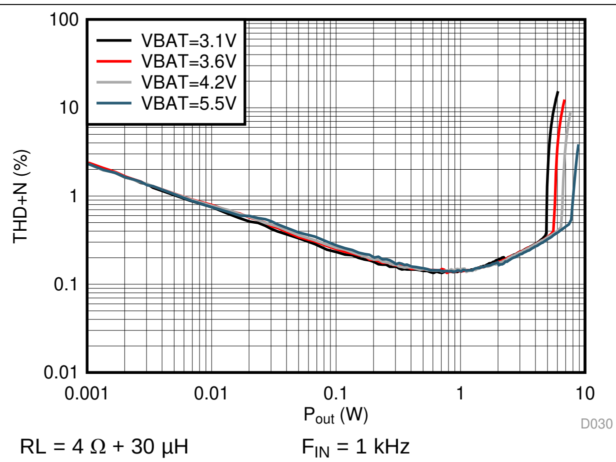


Figure 31. I-sense THD+N vs Output Power

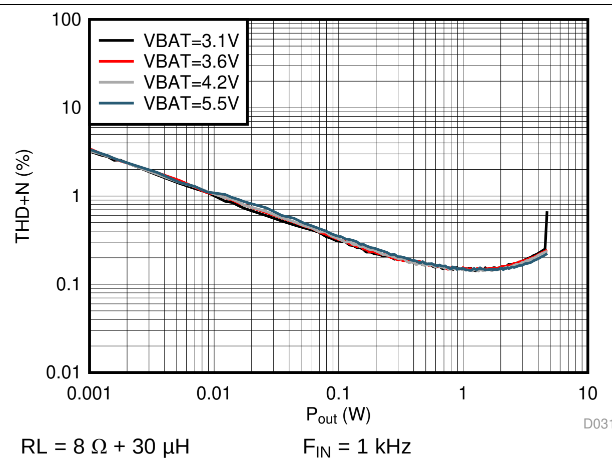


Figure 32. I-sense THD+N vs Output Power

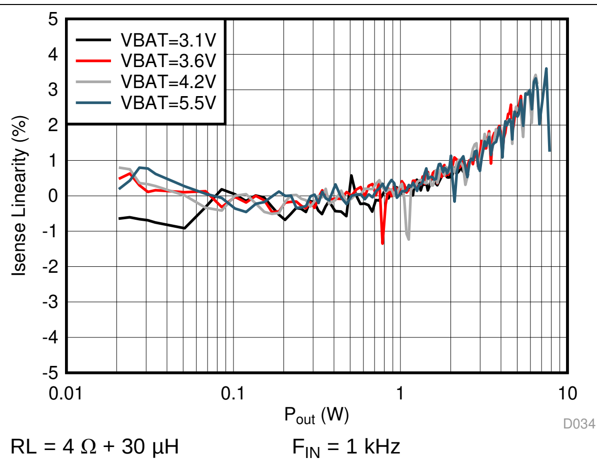


Figure 33. I-sense Linearity vs Output Power

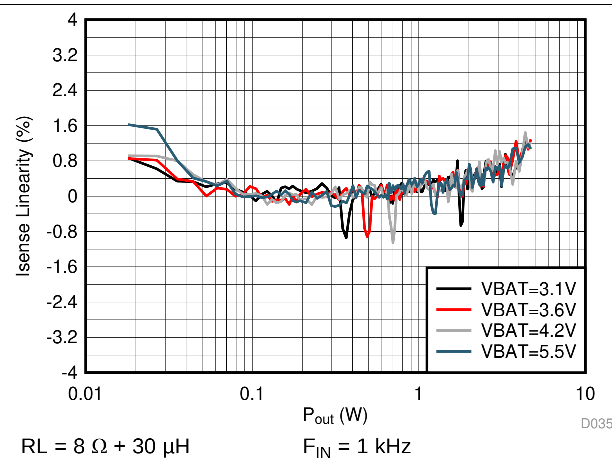
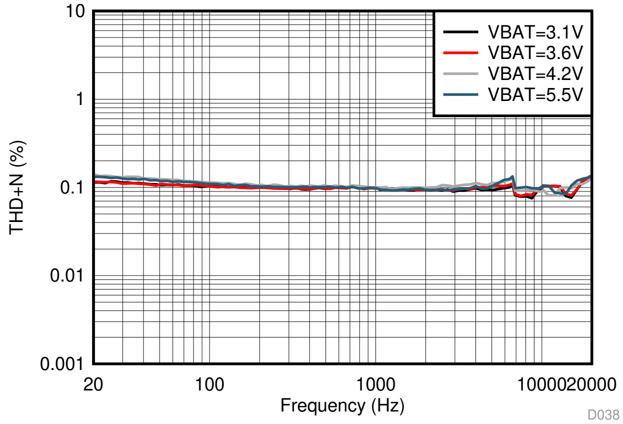


Figure 34. I-sense Linearity vs Output Power

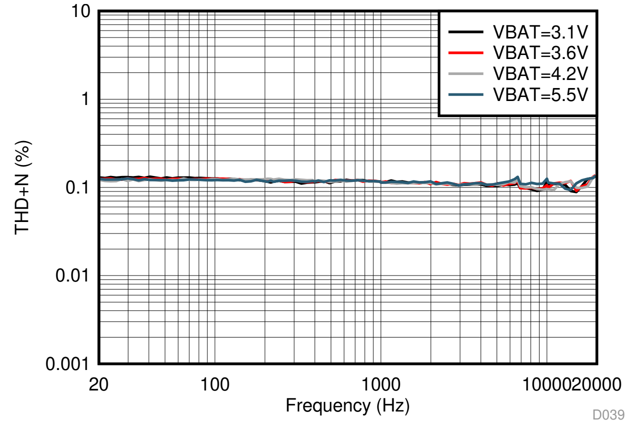
Typical Characteristics (continued)

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 µH, unless otherwise noted.



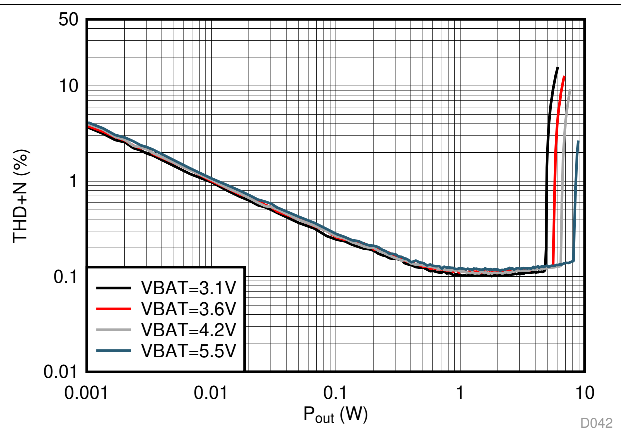
RL = 4 Ω + 30 µH P = 1 W

Figure 35. I-sense THD+N vs Frequency



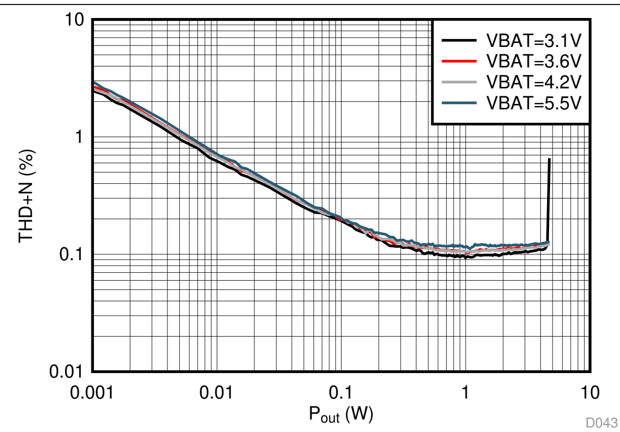
RL = 8 Ω + 30 µH P = 1 W

Figure 36. I-sense THD+N vs Frequency



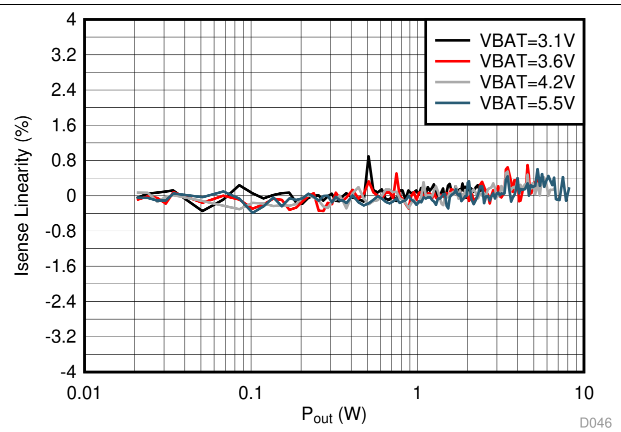
RL = 4 Ω + 30 µH F_{IN} = 1 kHz

Figure 37. V-sense THD+N vs Output Power



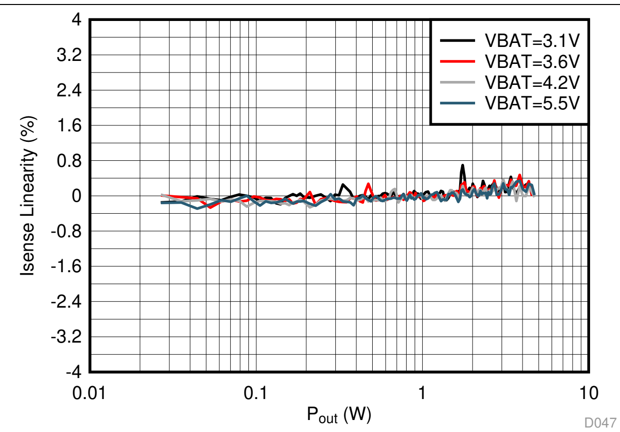
RL = 8 Ω + 30 µH F_{IN} = 1 kHz

Figure 38. V-sense THD+N vs Output Power



RL = 4 Ω + 30 µH F_{IN} = 1 kHz

Figure 39. V-sense Linearity vs Output Power

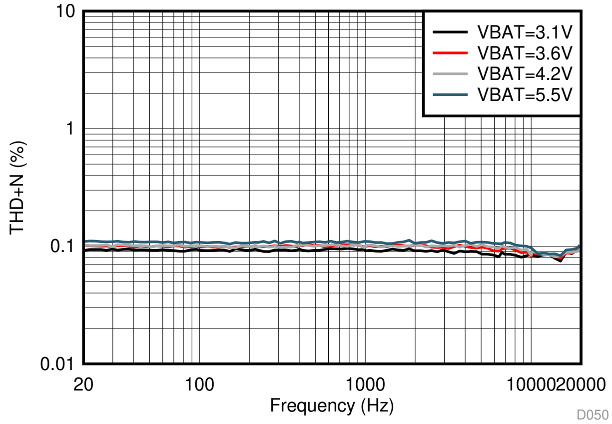


RL = 8 Ω + 30 µH F_{IN} = 1 kHz

Figure 40. V-sense Linearity vs Output Power

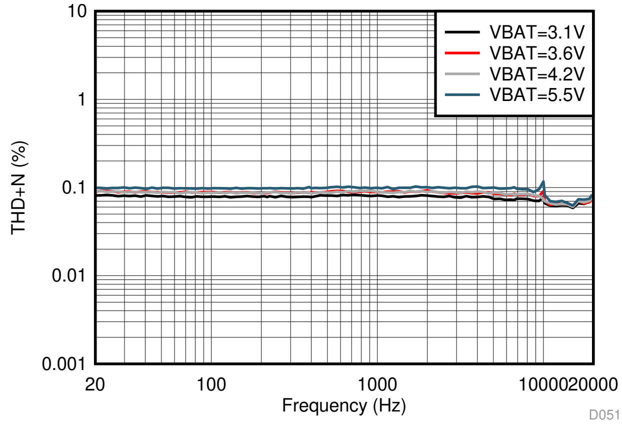
Typical Characteristics (continued)

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 µH, unless otherwise noted.



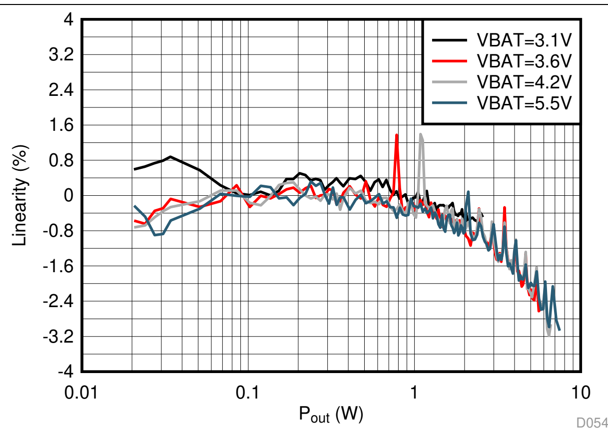
RL = 4 Ω + 30 µH P = 1 W

Figure 41. V-sense THD+N vs Frequency



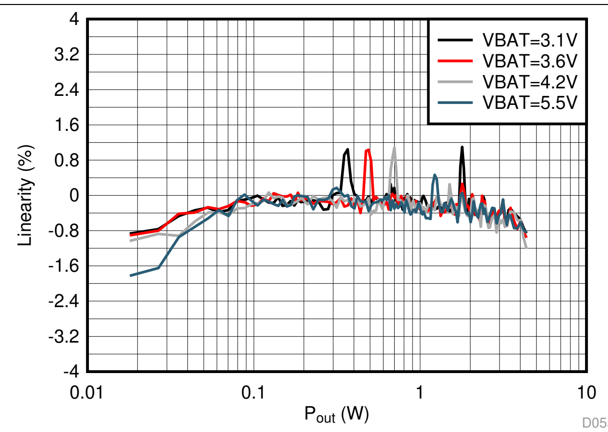
RL = 8 Ω + 30 µH P = 1 W

Figure 42. V-sense THD+N vs Frequency



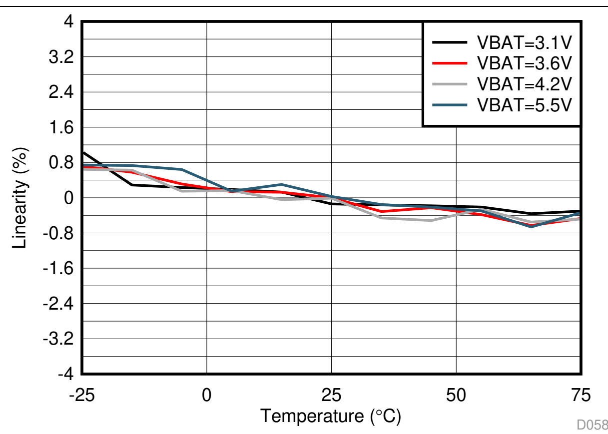
RL = 4 Ω + 30 µH F_{IN} = 1 kHz

Figure 43. V/I-sense Linearity vs Output Power



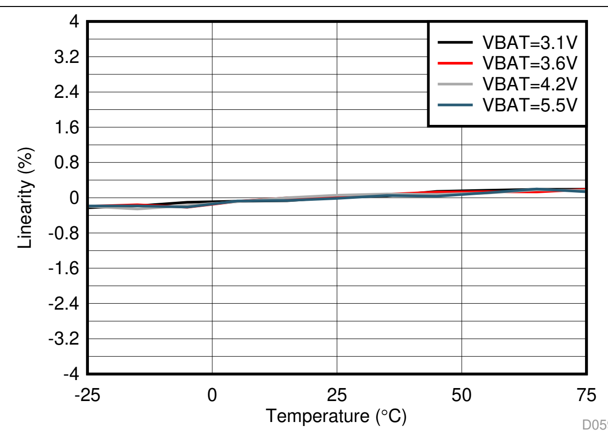
RL = 8 Ω + 30 µH F_{IN} = 1 kHz

Figure 44. V/I-sense Linearity vs Output Power



RL = 8 Ω + 30 µH P = 1 W

Figure 45. I-sense Linearity vs Temperature

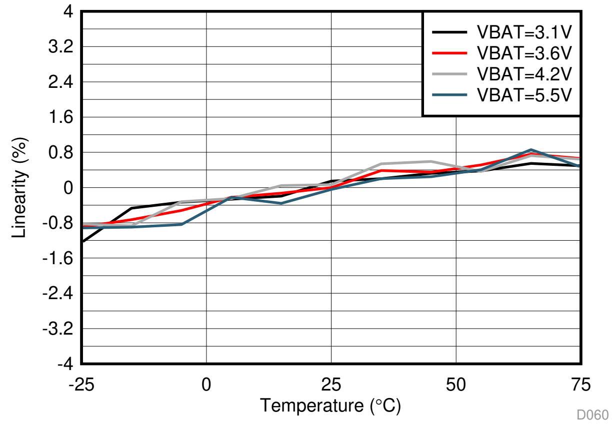


RL = 8 Ω + 30 µH P = 1 W

Figure 46. V-sense Linearity vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 µH, unless otherwise noted.



RL = 8 Ω + 30 µH P = 1 W

Figure 47. V/I-sense Linearity vs Temperature

8 Parameter Measurement Information

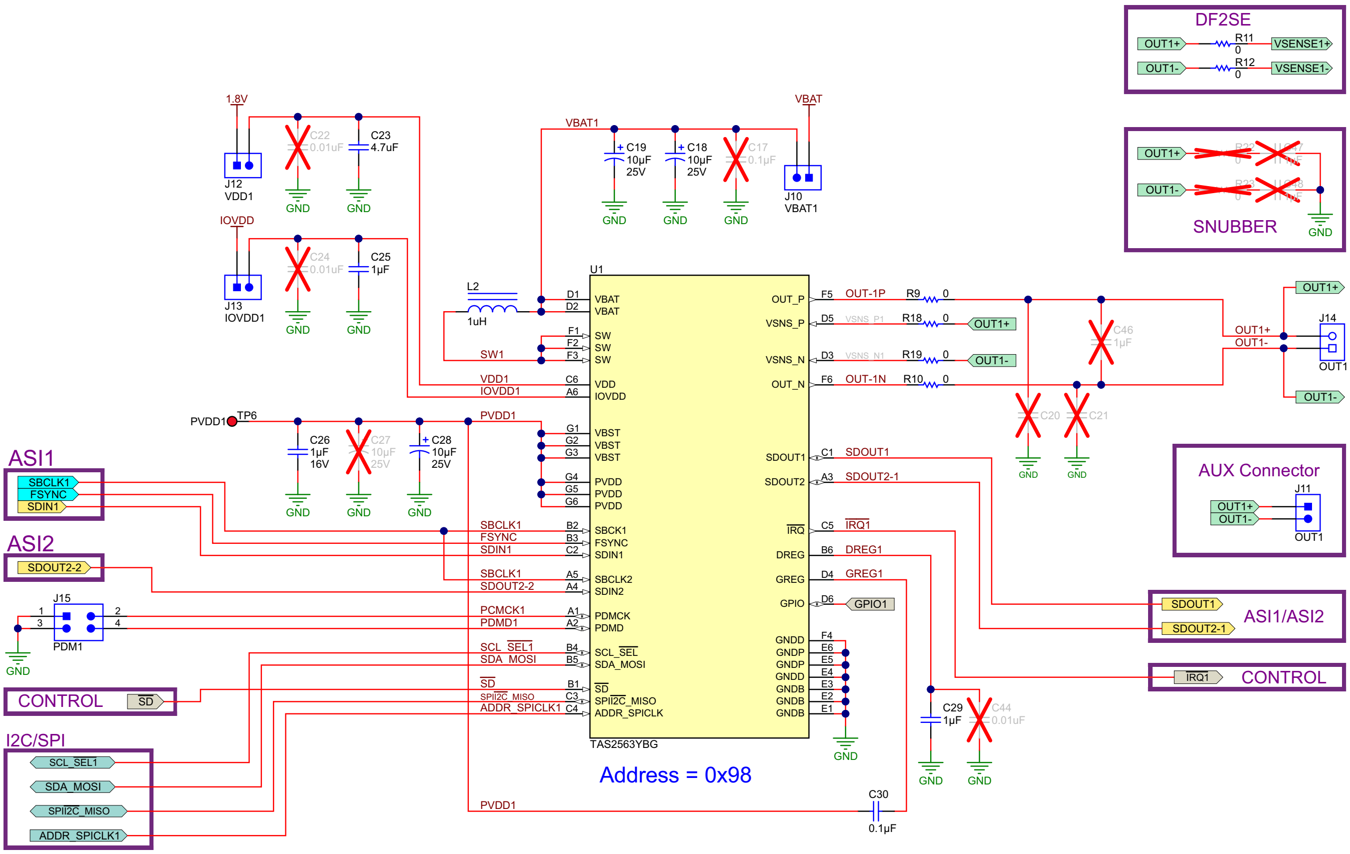


Figure 48. TAS2563 Circuit

Parameter Measurement Information (continued)

All typical characteristics for the devices are measured using the Bench EVM and an Audio Precision SYS-2722 Audio Analyzer. A PSIA interface is used to allow the I^2S interface to be driven directly into the SYS-2722. Speaker output terminals are connected to the Audio-Precision analyzer analog inputs through a differential-to-single ended(D2S) filter as shown below. The D2S filter contains a 1st order Passive pole at 120 kHz. The D2S filter ensures the TAS2563 high performance class-D amplifier sees a fully differential matched loading at its outputs. This prevents measurement errors due to loading effects of AUX-0025 filter on the class-D outputs.

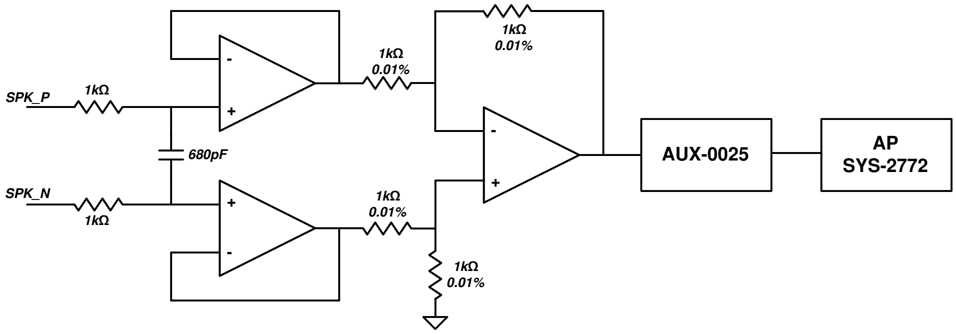


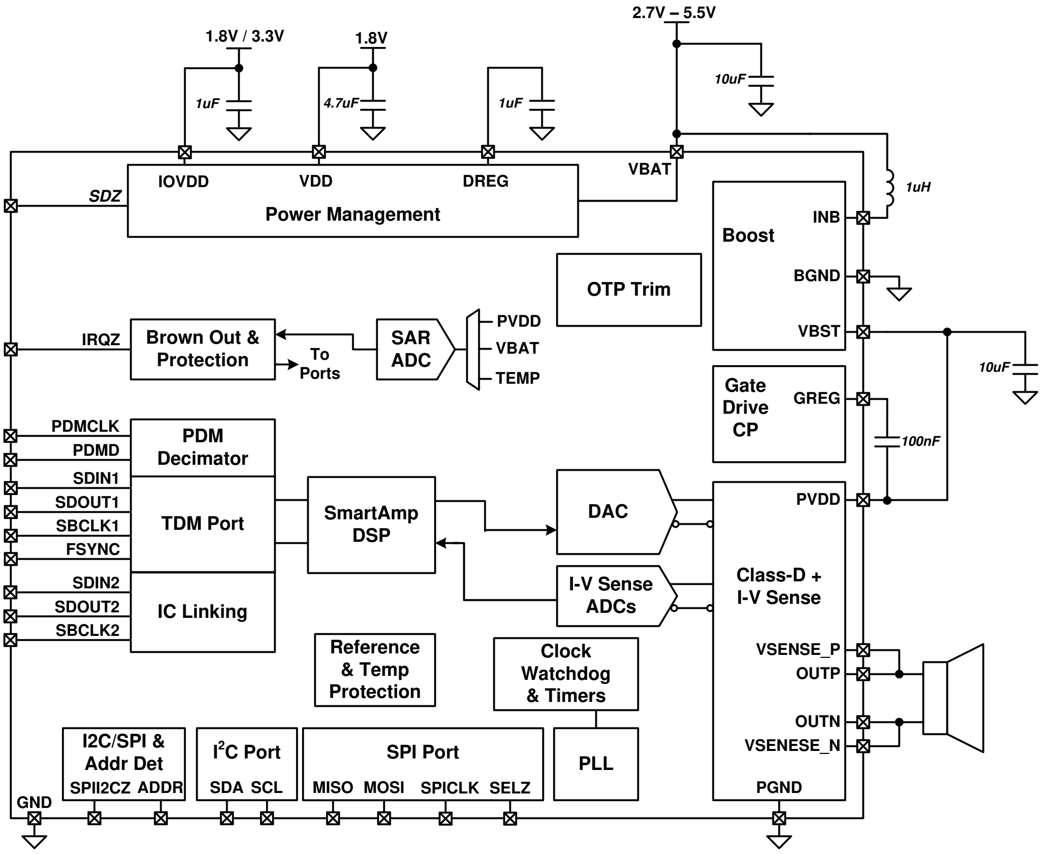
Figure 49. Differential To Single Ended (D2S) Filter

9 Detailed Description

9.1 Overview

The TAS2563 is a mono digital input Class-D amplifier optimized for mobile applications where efficient battery operation and small solution size are crucial. It integrates speaker voltage and current sensing and battery tracking limiting with brown out prevention.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 PurePath™ Console 3 Software

The TAS2563 advanced features and device configuration should be performed using PurePath Console 3 (PPC3) software. The base software PPC3 is downloaded and installed from the TI website. Once installed the TAS2563 application can be download from with-in PPC3. The PCC3 tool will calculate necessary register coefficients that are described in the following sections. It is the recommended method to configure the device. Once the TAS2563 application calculates and updates the device, the registers values can be read back using the PPC3 tool for final system integration.

Feature Description (continued)

9.3.2 Device Mode and Address Selection

The TAS2563 has a global 7-bit I^{2}C address 0x48. When enabled the device will additionally respond to I^{2}C commands at this address once it is put in I2C Mode. This is used to speed up device configuration when using multiple TAS2563 devices and programming similar settings across all devices. The I^{2}C ACK / NACK cannot be used during the multi-device writes since multiple devices are responding to the I^{2}C command. The I^{2}C CRC function should be used to ensure each device properly received the I^{2}C commands. At the completion of writing multiple devices using the global address, the CRC at *I2C_CKSUM* register should be checked on each device using the local address for a proper value. The global I^{2}C address can be disabled using *I2C_GBL_EN* register. The I^{2}C address is detected by sampling the address pins when SDZ pin is released. Additionally, the address may be re-detected by setting *I2C_AD_DET* high after power up and the pins will be resampled.

Table 1. I^{2}C Global Address Enable

I2C_GBL_EN	SETTING
0	Disabled
1	Enabled (default)

Table 2. I^{2}C Global Address Enable

I2C_AD_DET	SETTING
0	normal (default)
1	Re-detect

9.3.3 General I^{2}C Operation

The I^{2}C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. shows a typical sequence.

To configure the TAS2563 for I2C operation set the SPII2CZ_MISO pin to ground. The I2C address can then be set using pins ADDR_SPICLK according to Table 3. The pin configures the two LSB bits of the following 7-bit binary address A6-A0 of 10011xx. This permits the I2C address of TAS2563 to be 0x4C(7-bit) through 0x4F(7-bit). For example, if both ADDR_SPICLK is connected to ground the I2C address for the TAS2563 would be 0x4C(7-bit). This is equivalent to 0x98 (8-bit) for writing and 0x99 (8-bit) for reading. The ADDR_SPICLK should be only pulled high to the AVDD pin voltage.

Table 3. I^{2}C Mode Address Selection

I2C SLAVE ADDRESS	ADDR_SPICLK PIN
0x48 (global address)	NA
0x4C	GND
0x4D	10k to GND
0x4E	10k to VDD
0x4F	VDD

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus. Pull Up Resistor can be calculated as per the table below. For Capacitive Loads different from mentioned below in table, use interpolated values.

Do not allow the SDA and SCL voltages to exceed the device supply voltage, IOVDD. The I²C pins are fault tolerant and will not load the I2C bus when the device is powered down.

Table 4. I²C Pull Up Resistor Selection

I2C Mode of Operation	Capacitive Load	Recommended Pull Up Resistor
Standard/Fast	10pF	500Ω to 4.7KΩ
	400pF	500Ω to 1KΩ
Fast Mode Plus	10pF	500Ω to 4KΩ
	550pF	350Ω to 400Ω

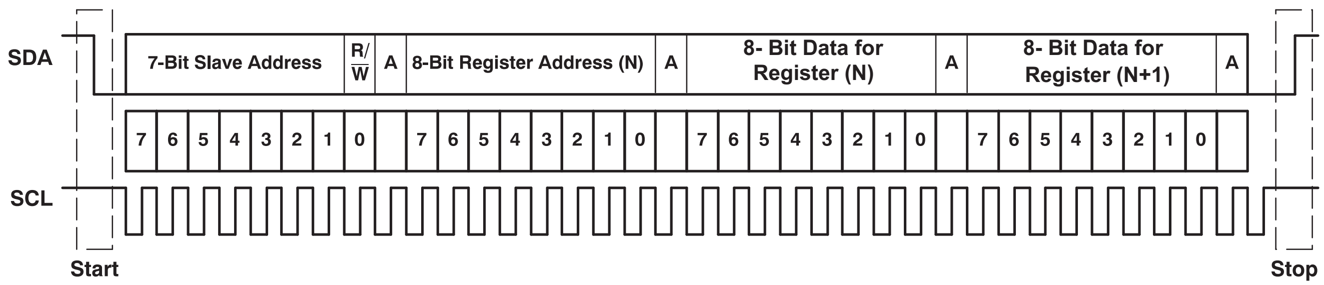


Figure 50. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. Figure 50 shows a generic data transfer sequence.

9.3.4 General SPI Operation

The TAS2563 operates as an SPI slave over the AVDD voltage range. To enable SPI mode the SPII2CZ_MISO pin is pulled to AVDD using a resistor. During the device power up the pin state is queried and if high will enter SPI mode.

In the SPI control mode, the TAS2563 uses the terminals SCL_SELZ as SS, ADDR_SPICLK as SCLK, SPII2CZ_MISO as MISO, SDA_MOSI as MOSI; The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave device depends on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI terminal under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI terminal, a byte shifts out on the MISO terminal to the master shift register.

The TAS2563 interface is designed so that with a clock-phase bit setting of 1 (typical microprocessor SPI control bit CPHA = 1), the master begins driving its MOSI terminal and the slave begins driving its MISO terminal on the first serial clock edge. The SSZ terminal can remain low between transmissions; however, the TAS2563 only interprets the first 8 bits transmitted after the falling edge of SSZ as a command byte, and the next 8 bits as a data byte only if writing to a register. Reserved register bits should be written to their default values. The TAS2563 is entirely controlled by registers. Reading and writing these registers is accomplished by an 8-bit command sent to the MOSI terminal of the part prior to the data for that register. The command is structured as shown in Table 5 below. The first 7 bits specify the address of the register which is being written or read, from 0 to 127 (decimal). The command word ends with an R/W bit, which specifies the direction of data flow on the serial bus. In the case of a register write, the R/W bit should be set to 0. A second byte of data is sent to the MOSI terminal and contains the data to be written to the register. Reading of registers is accomplished in a similar fashion. The 8-bit command word sends the 7-bit register address, followed by the R/W bit = 1 to signify a register read is occurring. The 8-bit register data is then clocked out of the part on the MISO terminal during the second 8 SCLK clocks in the frame.

Table 5. Command Word

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR(6)	ADDR(5)	ADDR(4)	ADDR(3)	ADDR(2)	ADDR(1)	ADDR(0)	R/WZ

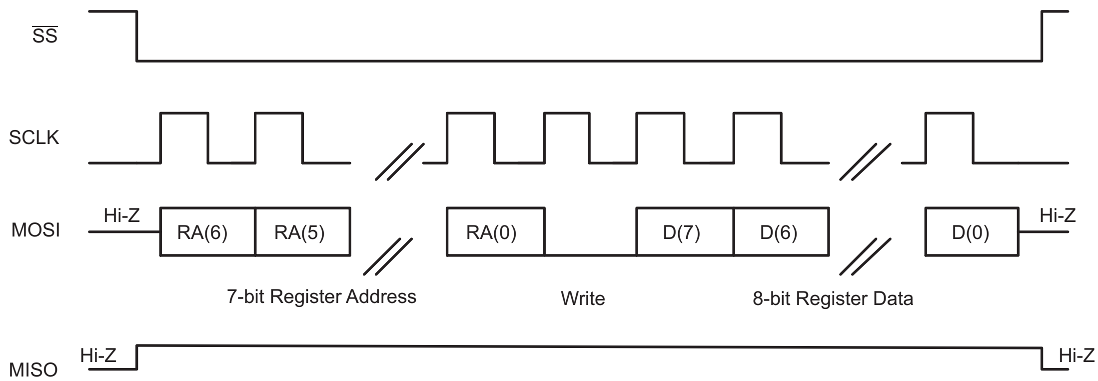


Figure 51. SPI Timing Diagram for Register Write

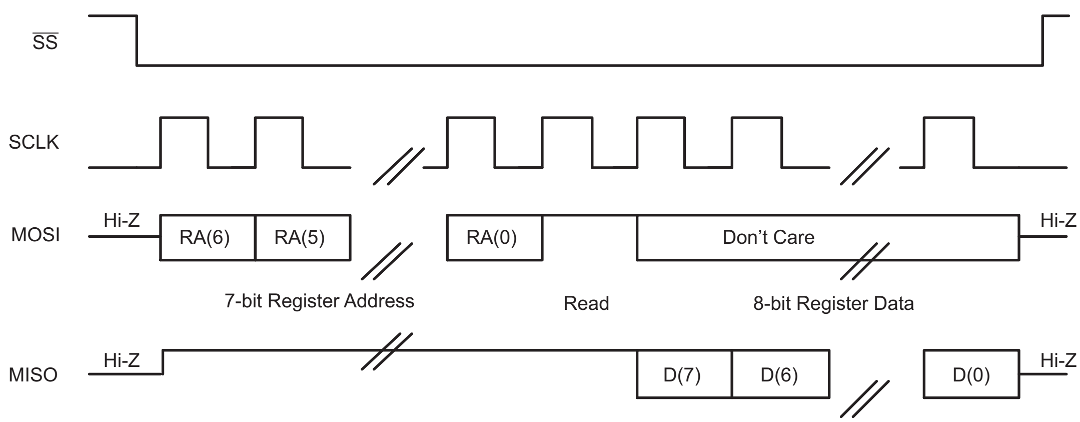


Figure 52. SPI Timing Diagram for Register Read

9.3.5 Single-Byte and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the TAS2563 responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The TAS2563 supports sequential I^{2}C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I^{2}C write transaction has taken place. For I^{2}C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines to how many registers are written.

9.3.6 Single-Byte Write

As shown in Figure 53, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I^{2}C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I^{2}C device address and the read/write bit, the TAS2563 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the device internal memory address being accessed. After receiving the register byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

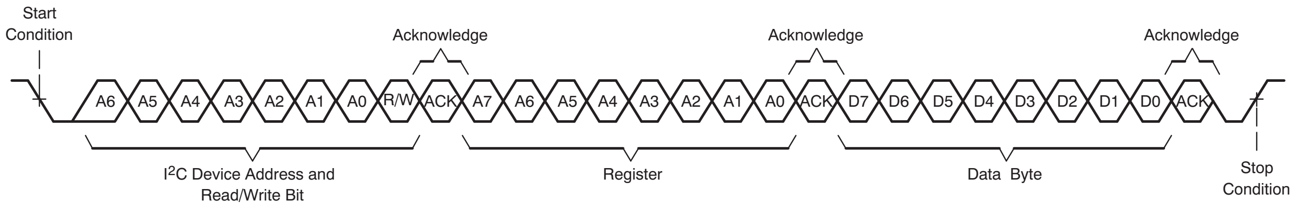


Figure 53. Single-Byte Write Transfer

9.3.7 Multiple-Byte Write and Incremental Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the TAS2563 as shown in Figure 54. After receiving each data byte, the device responds with an acknowledge bit.

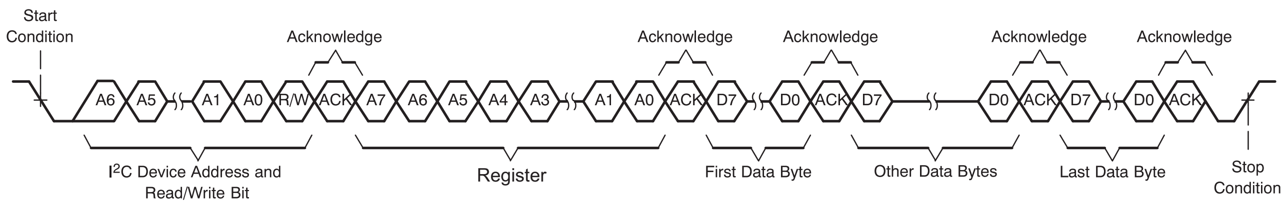


Figure 54. Multi-Byte Write Transfer

9.3.8 Single-Byte Read

As shown in Figure 55, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I^{2}C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the TAS2563 address and the read/write bit, the device responds with an acknowledge bit. The master then sends the internal memory address byte, after which the device issues an acknowledge bit. The master device transmits another start condition followed by the TAS2563 address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the TAS2563 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.

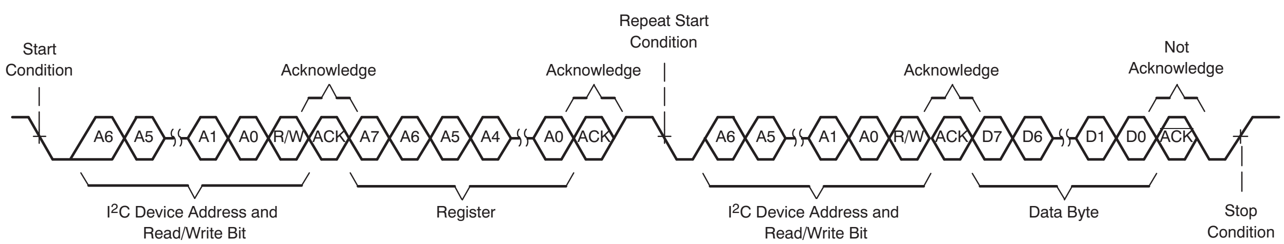


Figure 55. Single-Byte Read Transfer

9.3.9 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the TAS2563 to the master device as shown in Figure 56. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

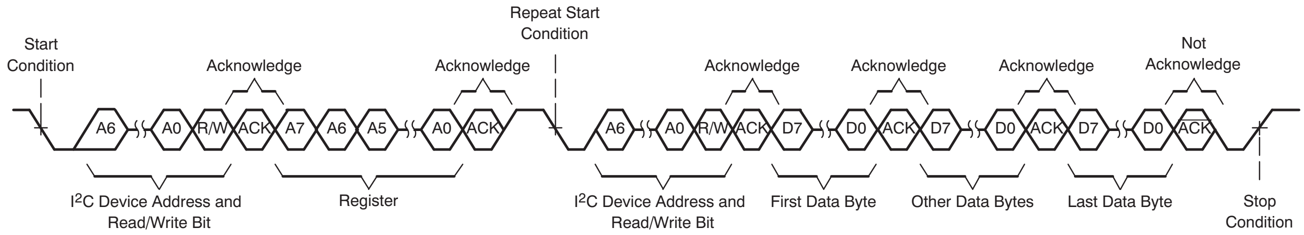


Figure 56. Multi-Byte Read Transfer

9.3.10 Register Organization

Device configuration and coefficients are stored using a page and book scheme. Each page contains 128 bytes and each book contains 256 pages. All device configuration registers are stored in book 0, page 0, which is the default setting at power up (and after a software reset). The book and page can be set by the *BOOK[7:0]* and *PAGE[7:0]* registers respectively.

9.3.11 Operational Modes

9.3.11.1 Hardware Shutdown

The device enters Hardware Shutdown mode if the SDZ pin is asserted low. In Hardware Shutdown mode, the device consumes the minimum quiescent current from VDD and VBAT supplies. All registers loose state in this mode and I^2C communication is disabled.

In normal shutdown mode if SDZ is asserted low while audio is playing, the device will ramp down volume on the audio, stop the Class-D switching, power down analog and digital blocks and finally put the device into Hardware Shutdown mode. If configured in normal with timeout shutdown mode the device will force a hard shutdown after a timeout of the configurable shutdown timer. Finally the device can be configured for hard shutdown and will not attempt to gracefully stop the audio channel.

Table 6. Shutdown Control

SDZ_MODE[1:0]	SETTING
00	Normal Shutdown with Timer (default)
01	Immediate Shutdown
10	Normal Shutdown
11	Reserved

Table 7. Shutdown Control

SDZ_TIMEOUT[1:0]	SETTING
00	2 ms
01	4 ms
10	6 ms (default)
11	23.8 ms

When SDZ is released, the device will sample the AD0 and AD1 pins and enter the software shutdown mode.

9.3.11.2 Software Shutdown

Software Shutdown mode powers down all analog blocks required to playback audio, but does not cause the device to loose register state. Software Shutdown is enabled by asserting the *MODE[1:0]* register bits to 2'b10. If audio is playing when Software Shutdown is asserted, the Class-D will volume ramp down before shutting down. When deasserted, the Class-D will begin switching and volume ramp back to the programmed digital volume setting.

9.3.11.3 Mute

The TAS2563 will volume ramp down the Class-D amplifier to a mute state by setting the *MODE[1:0]* register bits to 2'b01. During mute the Class-D still switches, but transmits no audio content. If mute is deasserted, the device will volume ramp back to the programmed digital volume setting.

9.3.11.4 Active

In Active Mode the Class-D switches and plays back audio. Speaker voltage and current sensing are operational if enabled. Set the *MODE[1:0]* register bits to 2'b00 to enter active mode.

9.3.11.5 Perform Load Diagnostics

In Load Diagnostics Mode, TAS2563 checks the speaker terminal for an open or short. This can be used to determine if a problem exists with the speaker or trace to the speaker. The entire operation is performed by the TAS2563 and results reported using the IRQZ pin or read over I2C bus on completion. Set the *MODE[1:0]* register bits to 2'b11 to enter load diagnostics mode.

9.3.11.6 Mode Control and Software Reset

The TAS2563 mode can be configured by writing the *MODE[1:0]* bits.

Table 8. Mode Control

MODE[1:0]	SETTING
00	Active
01	Mute
10	Software Shutdown (default)
11	Perform Load Diagnostics

A software reset can be accomplished by asserting the *SW_RESET* bit, which is self clearing. This will restore all registers to their default values.

Table 9. Software Reset

SW_RESET	SETTING
0	Don't reset (default)
1	Reset

9.3.12 Faults and Status

During the power-up sequence, the power-on-reset circuit (POR) monitoring the VDD and VBAT pins will hold the device in reset (including all configuration registers) until the supply is valid. The device will not exit hardware shutdown until VDD and VBAT are valid and the SDZ pin is released. Once SDZ is released, the digital core voltage regulator will power up, enabling detection of the operational mode. If VDD dips below the POR threshold, the device will immediately be forced into a reset state.

The device also monitors the VBAT supply and holds the analog core in power down if the supply is below the UVLO threshold. If the TAS2563 is in active operation and a UVLO fault occurs, the analog supplies will immediately power down to protect the device. These faults are latching and require a transition through HW/SW shutdown to clear the fault. The live and latched registers will report UVLO faults.

The device transitions into software shutdown mode if it detects any faults with the TDM clocks such as:

- Invalid SBCLK to FSYNC ratio
- Invalid FSYNC frequency
- Halting of SBCLK or FSYNC clocks

Upon detection of a TDM clock error, the device transitions into software shutdown mode as quickly as possible to limit the possibility of audio artifacts. Once all TDM clock errors are resolved, the device volume ramps back to its previous playback state. During a TDM clock error, the IRQZ pin will assert low if the clock error interrupt mask register bit is set low (*INT_MASK[2]*). The clock fault is also available for readback in the live or latched fault status registers (*INT_LIVE[2]* and *INT_LTCH[2]*). Reading the latched fault status register (*INT_LTCH[7:0]*) clears the register.

The TAS2563 also monitors die temperature and Class-D load current and will enter software shutdown mode if either of these exceed safe values. As with the TDM clock error, the IRQZ pin will assert low for these faults if the appropriate fault interrupt mask register bit is set low (*INT_MASK[0]* for over temp and *INT_MASK[1]* for over current). The fault status can also be monitored in the live and latched fault registers as with the TDM clock error.

Die over temp and Class-D over current errors can either be latching (i.e. the device will enter software shutdown until a HW/SW shutdown sequence is applied) or they can be configured to automatically retry after a prescribed time. This behavior can be configured in the *OTE_RETRY* and OCE_RETRY register bits (for over temp and over current respectively). Even in latched mode, the Class-D will not attempt to retry after an over temp or over current error until the retry time period (1.5s) has elapsed. This prevents applying repeated stress to the device in a rapid fashion that could lead to device damage. If the device has been cycled through SW/HW shutdown, the device will only begin to operate after the retry time period.

The status registers (and IRQZ pin if enabled via the status mask register) also indicates limiter behavior including when the limiter is activity, when VBAT is below the inflection point, when maximum attenuation has been applied, when the limiter is in infinite hold and when the limiter has muted the audio.

Interrupts can be queried using the *INT_LIVE[9:0]* and *INT_LTCH[13:0]* registers and correspond to the *INT_MASK[10:0]* Interrupts. The latched registers are cleared by writing the self clearing register *INT_CLR_LTCH* high.

The IRQZ pin is an open drain output that asserts low during unmasked fault conditions and therefore must be pulled up with a resistor to . An internal pull up resistor is provided in the TAS2563 and can be accessed by setting the *IRQZ_PU* register bit high. Figure 57 below highlights the IRQZ pin circuit.

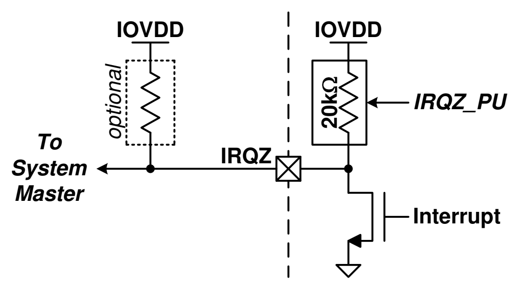


Figure 57. IRQZ Pin

Table 10. Fault Interrupt Mask

INT_MASK[10:0] BIT	INTERRUPT	DEFAULT (1 = Mask)
0	Over Temp Error	0
1	Over Current Error	0
2	TDM Clock Error	1
3	Limiter Active	1
4	Limter Voltage < Inf Point	1
5	Limiter Max Atten	1
6	Limiter Inf Hold	1
7	Limiter Mute	1
8	Brown Out on VBAT Supply	0
9	Brown Out Protection Active	1

Table 10. Fault Interrupt Mask (continued)

INT_MASK[10:0] BIT	INTERRUPT	DEFAULT (1 = Mask)
10	Brown Out Power Down (Latched Only)	1
11:12	Speaker Open Load (Latched Only)	00
13	Load Diagnostic Complete (Latched Only)	1

Table 11. IRQ Clear Latched

INT_CLR_LTCH	STATE
0	Don't Clear
1	Clear (self clearing)

Table 12. IRQZ Internal Pull Up Enable

IRQZ_PU	STATE
0	Disabled (default)
1	Enabled

Table 13. IRQZ Polarity

IRQZ_POL	STATE
0	Active High
1	Active Low (default)

Table 14. IRQZ Assert Interrupt Configuration

IRQZ_PIN_CFG[1:0]	VALUE
00	On any unmasked live interrupts
01	On any unmasked latched interrupts (default)
10	For 2-4ms one time on any unmasked live interrupt event
11	For 2-4ms every 4ms on any unmasked latched interrupts

Table 15. Retry after Over Current Event

OCE_RETRY	STATE
0	Disabled (default)
1	Enabled

Table 16. Retry after Over Temperature Event

OTE_RETRY	VALUE
0	Do not retry (default)
1	Retry after 1.5s

9.3.13 Power Sequencing Requirements

There are no other power sequencing requirements for order of rate of ramping up or down.

9.3.14 Digital Input Pull Downs

Each digital input and IO has an optional weak pull down to prevent the pin from floating. Pull downs are not enabled during HW shutdown.

Table 17. Digital Input Pull Down Enables

REGISTER BIT	DESCRIPTION	BIT VALUE	STATE
DIN_PD[0]	Weak pull down for SBCLK.	0	Disabled (default)
		1	Enabled
DIN_PD[1]	Weak pull down for FSYNC.	0	Disabled (default)
		1	Enabled
DIN_PD[2]	Weak pull down for SDIN.	0	Disabled (default)
		1	Enabled
DIN_PD[3]	Weak pull down for SDOUT.	0	Disabled (default)
		1	Enabled
DIN_PD[4]	Weak pull down forAD0.	0	Disabled (default)
		1	Enabled
DIN_PD[5]	Weak pull down for AD1.	0	Disabled(default)
		1	Enabled
DIN_PD[7]	Weak pull down for GPIO.	0	Disabled
		1	Enabled (default)

9.4 Device Functional Modes

9.4.1 PDM Input

The TAS2563 provides one PDM input. Figure 58 below illustrates the double data rate nature of the PDM input. It has two interleaved PDM channels, one sampled by the rising edge and the other by the falling edge of the clock.

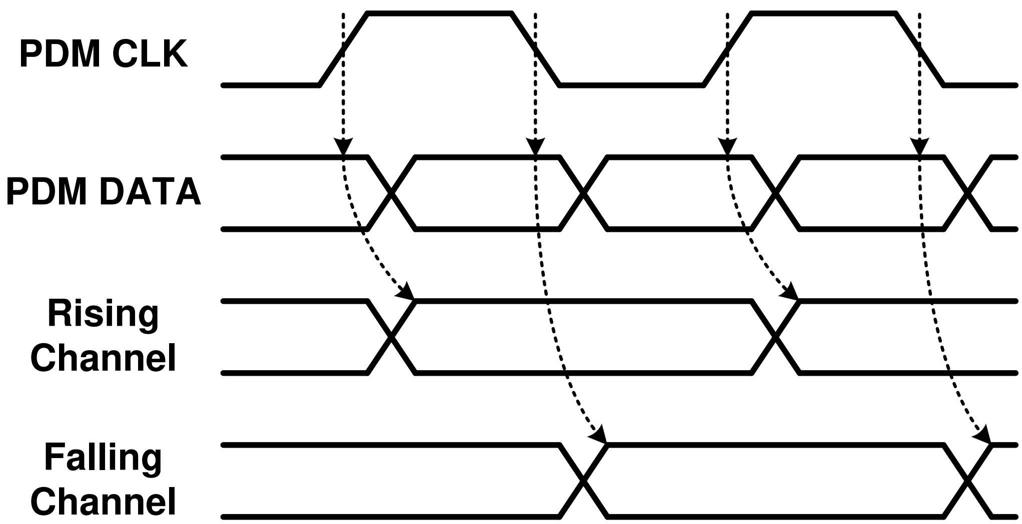


Figure 58. PDM Waveform

The PDM inputs are sampled by the PDMCK pin, which can be configured as either a PDM clock slave input or a PDM clock master output. The *PDM_MIC_EDGE* and *PDM_MIC_SLV* register bits select the sample clock edge and master/slave mode PDM inputs. In master mode the PDMCK pin can disable the clocks (and drive a logic 0) by setting the *PDM_GATE_PAD0* register bits low.

When configured as a clock slave, the PDM clock input does not require a specific phase relationship to the system clock (SBCLK in TDM/I^{2}S Mode), but must be from the same source as audio sample rate. This is equivalent to 64/32/16 (~3 MHz) or 128/64/32 (~6 MHz) times a single/double/quadruple speed sample rate. The PDM rate is set by the *PDM_RATE_PAD0* .

Device Functional Modes (continued)

When PDMCK pin is configured as a clock master, the TAS2563 will output a 50% duty cycle clock of frequency that is set by the *PDM_RATE_PAD0* and register bit (64/32/16 or 128/64/32 times a single/double/quadruple speed sample rate).

Table 18. PDM Clock Slave

PDM INPUT PIN	REGISTER BIT	VALUE	MASTER/SLAVE
PDMD	*PDM_MIC_SLV*	0	Master
		1	Slave (default)

Table 19. PDM Master Mode Clock Gate

PDM CLOCK PIN	REGISTER BIT	VALUE	GATING
PDMCK	*PDM_GATE_PAD0*	1	Gated Off (default)
		0	Active

Table 20. PDM Input Sample Rate

PDM INPUT PIN	REGISTER BITS	VALUE	SAMPLE RATE
PDMD	*PDM_RATE_PAD0*	0	3.072 MHz (default)
		1	6.144 MHz

Table 21. PDM MIC Enable

PDM_MIC_EN	MAPPING
`PDM_MIC2_EN= 0`	Disable MIC2
`PDM_MIC2_EN= 1`	Enable MIC2
`PDM_MIC1_EN= 0`	Disable MIC1
`PDM_MIC1_EN= 1`	Enable MIC1

9.4.2 TDM Port

The TAS2563 provides a flexible TDM serial audio port. The port can be configured to support a variety of formats including stereo I^2S, Left Justified and TDM. Mono audio playback is available via the SDIN pin. The SDOUT pin is used to transmit sample streams including speaker voltage and current sense, VBAT voltage, die temperature and channel gain.

The TDM serial audio port supports up to 16 32-bit time slots at 44.1/48 kHz, 8 32-bit time slots at a 88.2/96 kHz sample rate and 4 32-bit time slots at a 176.4/192 kHz sample rate. The device supports 2 time slots at 32 bits in width and 4 or 8 time slots at 16, 24 or 32 bits in width. Valid SBCLK to FSYNC ratios are 64, 96, 128, 192, 256, 384 and 512. The device will automatically detect the number of time slots and this does not need to be programmed.

By default, the TAS2563 will automatically detect the PCM playback sample rate. This can be disabled by setting the *AUTO_RATE* register bit high and manually configuring the device.

The *SAMP_RATE[2:0]* register bits set the PCM audio sample rate when *AUTO_RATE* is enabled. The TAS2563 employs a robust clock fault detection engine that will automatically volume ramp down the playback path if FSYNC does not match the configured sample rate (*AUTO_RATE* enabled) or the ratio of SBCLK to FSYNC is not supported (minimizing any audible artifacts). Once the clocks are detected to be valid in both frequency and ratio, the device will automatically volume ramp the playback path back to the configured volume and resume playback.

When using the auto rate detection the sampling rate and SBCLK to FSYNC ration detected on the TDM bus is reported back on the read-only register *FS_RATE* and *FS_RATIO* respectively.

While the sampling rate of 192kHz is supported, it is internally down-sampled to 96kHz. Therefore audio content greater than 40kHz should not be applied to prevent aliasing. This additionally effects all processing blocks like BOP and limiter which should use 96kHz fs when accepting 192 kHz audio. It is recommend to use PurePath™ Console 3 Software to configure the device.

Table 22. PCM Auto Sample Rate Detection

AUTO_RATE	SETTING
0	Enabled (default)
1	Disabled

Table 23. PCM Audio Sample Rates

SAMP_RATE[2:0]	*FS_RATE*(read only)	SAMPLE RATE
000	000	Reserved
001	001	14.7kHz / 16kHz
010	010	Reserved
011	011	29.4 kHz / 32 kHz
100	100	44.1 kHz / 48 kHz (default)
101	101	88.2 kHz / 96 kHz
110	110	Reserved
111	111	Reserved

Table 24. PCM SBCLK to FSYNC Ratio Rates

FS_RATIO[3:0]	SAMPLE RATE
0x0-0x3	Reserved
0x4	64
0x5	96
0x6	128
0x7	192
0x8	256
0x9	384
0xA	512
0xB-0xE	Reserved
0xF	Error Condition

Figure 59 and Figure 60 below illustrates the receiver frame parameters required to configure the port for playback. A frame begins with the transition of FSYNC from either high to low or low to high (set by the *FRAME_START* register bit). FSYNC and SDIN are sampled by SBCLK using either the rising or falling edge (set by the *RX_EDGE* register bit). The *RX_OFFSET[4:0]* register bits define the number of SBCLK cycles from the transition of FSYNC until the beginning of time slot 0. This is typically set to a value of 0 for Left Justified format and 1 for an I^{2}S format.

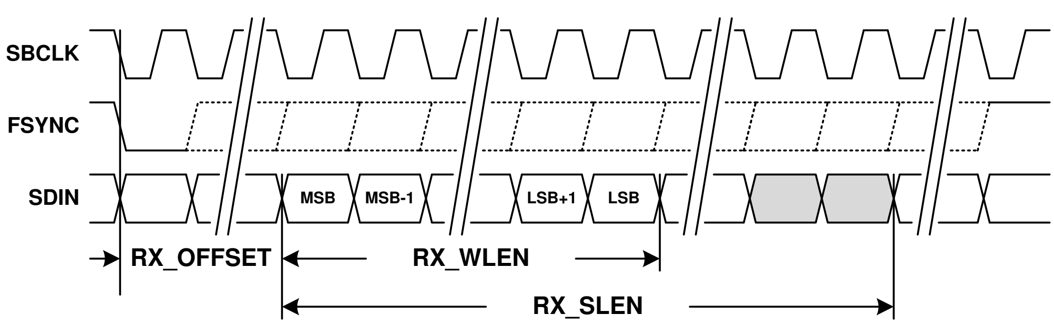


Figure 59. TDM RX Time Slot with Left Justification

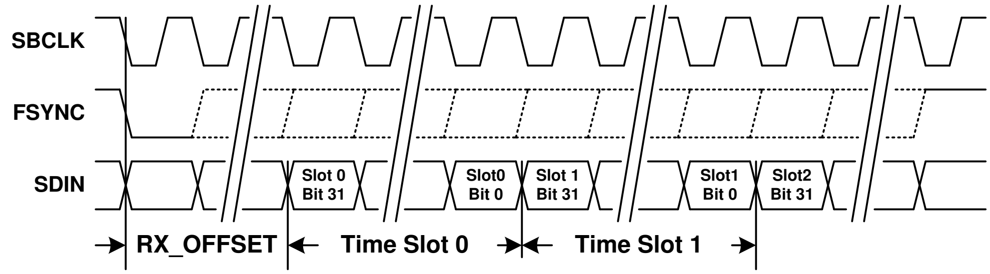


Figure 60. TDM RX Time Slots

Table 25. TDM Start of Frame Polarity

FRAME_START	POLARITY
0	Low to High on FSYNC (1)
1	High to Low on FSYNC (default) (2)

(1) When Low to High is used RX_EDGE and TX_EDGE cannot both simultaneously be set to rising edge.
(2) When High to Low is used RX_EDGE and TX_EDGE cannot both simultaneously be set to falling edge.

Table 26. TDM RX Capture Polarity

RX_EDGE	FSYNC AND SDIN CAPTURE EDGE
0	Rising edge of SBCLK (default)
1	Falling edge of SBCLK

Table 27. TDM RX Start of Frame to Time Slot 0 Offset

RX_OFFSET[4:0]	SBCLK CYCLES
0x00	0
0x01	1 (default)
0x02	2
...	...
0x1E	30
0x1F	31

The *RX_SLEN[1:0]* register bits set the length of the RX time slot. The length of the audio sample word within the time slot is configured by the *RX_WLEN[1:0]* register bits. The RX port will left justify the audio sample within the time slot by default, but this can be changed to right justification via the *RX_JUSTIFY* register bit. The TAS2563 supports mono and stereo down mix playback ([L+R]/2) via the left time slot, right time slot and time slot configuration register bits (*RX_SLOT_L[3:0]*, *RX_SLOT_R[3:0]* and *RX_SCFG[1:0]* respectively). By default the device will playback mono from the time slot equal to the I^2C base address offset for playback. The *RX_SCFG[1:0]* register bits can be used to override the playback source to the left time slot, right time slot or stereo down mix set by the *RX_SLOT_L[3:0]* and *RX_SLOT_R[3:0]* register bits.

If time slot selections places reception either partially or fully beyond the frame boundary, the receiver will return a null sample equivalent to a digitally muted sample.

Table 28. TDM RX Time Slot Length

RX_SLEN[1:0]	TIME SLOT LENGTH
00	16-bits
01	24-bits
10	32-bits (default)
11	reserved

Table 29. TDM RX Sample Word Length

RX_WLEN[1:0]	LENGTH
00	16-bits
01	20-bits
10	24-bits (default)
11	32-bits

Table 30. TDM RX Sample Justification

RX_JUSTIFY	JUSTIFICATION
0	Left (default)
1	Right

Table 31. TDM RX Time Slot Select Configuration

RX_SCFG[1:0]	CONFIG ORIGIN
00	Mono with Time Slot equal to I^2C Address Offset (default)
01	Mono Left Channel
10	Mono Right Channel
10	Stereo Down Mix [L+R]/2
11	TAS2563 + TAS2562 Mode

Table 32. TDM RX Left Channel Time Slot

RX_SLOT_L[3:0]	TIME SLOT
0x0	0 (default)
0x1	1
...	...
0xE	14
0xF	15

Table 33. TDM RX Right Channel Time Slot

RX_SLOT_R[3:0]	TIME SLOT
0x0	0
0x1	1 (default)
...	...
0xE	14
0xF	15

The TDM port can transmit a number sample streams on the SDOUT pin including speaker voltage sense, speaker current sense, VBAT voltage, die temperature and channel gain. Figure 61 below illustrates the alignment of time slots to the beginning of a frame and how a given sample stream is mapped to time slots. Either the rising or falling edge of SBCLK can be used to transmit data on the SDOUT pin, which can be configured by setting the *TX_EDGE* register bit. The *TX_OFFSET* register defines the number SBCLK cycles between the start of a frame and the beginning of time slot 0. This would typically be programmed to 0 for Left Justified format and 1 for I^2S format. The TDM TX can either transmit logic 0 or Hi-Z depending on the setting of the *TX_FILL* register bit setting. An optional bus keeper will weakly hold the state of SDOUT when all devices driving are Hi-Z. Since only one bus keeper is required on SDOUT, this feature can be disabled via the *TX_KEEPEN* register bit. The bus-keeper can additionally be configured to be enabled for only 1LSB cycle or always using *TX_KEEPLN* and to drive the full or half cycle of the LSB using *TX_KEEPCY*.

Each sample stream is composed of either one or two 8-bit time slots. , so they will always utilize two TX time slots. The VBAT voltage stream is 10-bit precision, and can either be transmitted left justified in a 16-bit word (using two time slots) or can be truncated to 8-bits (the top 8 MSBs) and be transmitted in a single time slot. This is configured by setting *VBAT_SLEN* register bit. The Die temperature and gain are both 8-bit precision and are transmitted in a single time slot.

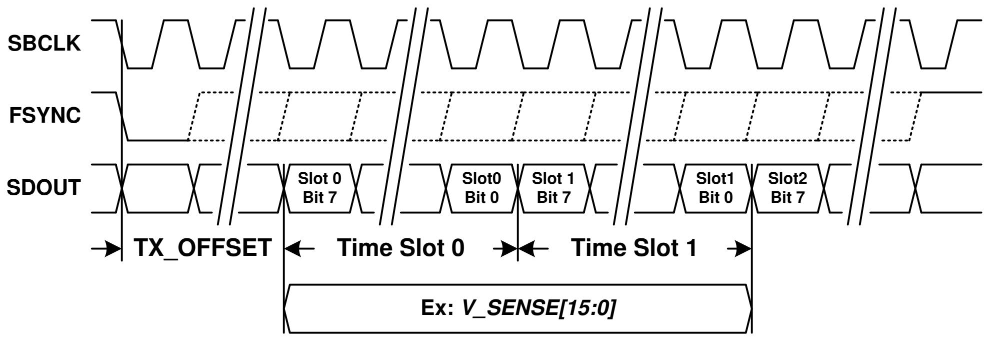


Figure 61. TDM Port TX Diagram

Table 34. TDM TX Transmit Polarity

TX_EDGE	SDOUT TRANSMIT EDGE
0	Rising edge of SBCLK
1	Falling edge of SBCLK (default)

Table 35. TDM TX Start of Frame to Time Slot 0 Offset

TX_OFFSET[2:0]	SBCLK CYCLES
0x0	0
0x1	1 (default)
0x2	2
...	...
0x6	6
0x7	7

Table 36. TDM TX Unused Bit Field Fill

TX_FILL	SDOUT UNUSED BIT FIELDS
0	Transmit 0
1	Transmit Hi-Z (default)

Table 37. TDM TX SDOUT Bus Keeper Enable

TX_KEEPEN	SDOUT BUS KEEPER
0	Disable bus keeper
1	Enable bus keeper (default)

Table 38. TDM TX SDOUT Bus Keeper Length

TX_KEEPLN	SDOUT BUS KEEPER ENABLED FOR
0	1 LSB cycle (default)
1	Always

Table 39. TDM TX SDOUT Bus Keeper LSB Cycle

TX_KEEPCY	SDOUT BUS KEEPER DRIVEN
0	full-cycle (default)
1	half-cycle

The time slot register for each sample stream defines where the MSB transmission begins. For instance, if *VSNS_SLOT* is set to 2, the upper 8 MSBs will be transmitted in time slot 2 and the lower 8 LSBs will be transmitted in time slot 3. Each sample stream can be individually enabled or disabled. This is useful to manage limited TDM bandwidth since it may not be necessary to transmit all streams for all devices on the bus.

It is important to ensure that time slot assignments for actively transmitted sample streams do not conflict. For instance, if *VSNS_SLOT* is set to 2 and *ISNS_SLOT* is set to 3, the lower 8 LSBs of voltage sense will conflict with the upper 8 MSBs of current sense. This will produce unpredictable transmission results in the conflicting bit slots (i.e. the priority is not defined).

The current and voltage values are transmitted at the full 16-bit measured values by default. The *IVMON_LEN* register can be used to transmit only the 8 MSB bits in one slot or 12 MSB bits values across multiple slots. The special 12-bit mode is used when only 24-bit I2S/TDM data can be processed by the host processor. The device should be configured with the voltage-sense slot and current-sense slot off by 1 slot and will consume 3 consecutive 8-bit slots. In this mode the device will transmit the first 12 MSB bits followed by the second 12 MSB bits specified by the preceding slot.

If time slot selections place transmission beyond the frame boundary, the transmitter will truncate transmission at the frame boundary.

It is recommended to keep the following slot ordering:

ISNS_SLOT<VSNS_SLOT<VBAT_SLOT<TEMP_SLOT<GAIN_SLOT<BIL_ILIM_SLOT.

Table 40. TDM Voltage/Current Length

IVMON_LEN[1:0]	LENGTH BITS
00	16 bits (default)
01	12 bits
10	8 bits
11	Reserved

Table 41. TDM Voltage Sense Time Slot

VSNS_SLOT[5:0]	SLOT
0x00	0
0x01	1
0x02	2 (default)
...	...
0x3E	62
0x3F	63

Table 42. TDM Voltage Sense Transmit Enable

VSNS_TX	STATE
0	Disabled (default)
1	Enabled

Table 43. TDM Current Sense Time Slot

ISNS_SLOT[5:0]	SLOT
0x00	0 (default)
0x01	1
0x02	2

Table 43. TDM Current Sense Time Slot (continued)

ISNS_SLOT[5:0]	SLOT
...	...
0x3E	62
0x3F	63

Table 44. TDM Current Sense Transmit Enable

ISNS_TX	STATE
0	Disabled (default)
1	Enabled

Table 45. TDM VBAT Time Slot

VBAT_SLOT[5:0]	SLOT
0x00	0
0x01	1
...	...
0x04	4 (default)
...	...
0x3E	62
0x3F	63

Table 46. TDM VBAT Time Slot Length

VBAT_SLEN	SLOT LENGTH
0	Truncate to 8-bits (default)
1	Left justify to 16-bits

Table 47. TDM VBAT Transmit Enable

VBAT_TX	STATE
0	Disabled (default)
1	Enabled

Table 48. TDM Temp Sensor Time Slot

TEMP_SLOT[5:0]	SLOT
0x00	0
0x01	1
...	...
0x05	5 (default)
...	...
0x3E	62
0x3F	63

Table 49. TDM Temp Sensor Transmit Enable

TEMP_TX	STATE
0	Disabled (default)
1	Enabled

The following sample streams are part of the system. These data streams can be routed over the audio TDM bus.

Table 50. TDM Limiter Gain Reduction Time Slot

GAIN_SLOT[5:0]	SLOT
0x00	0
0x01	1
...	...
0x06	6 (default)
...	...
0x3E	62
0x3F	63

Table 51. TDM Limiter Gain Reduction Transmit Enable

GAIN_TX	STATE
0	Disabled (default)
1	Enabled

Table 52. TDM Boost Sync Time Slot

BST_SLOT[5:0]	SLOT
0x00	0
0x01	1
...	...
0x07	7 (default)
...	...
0x3E	62
0x3F	63

Table 53. TDM Boost Sync Enable

BST_TX	STATE
0	Disabled (default)
1	Enabled

9.4.3 Playback Signal Path

9.4.3.1 Digital Signal Processor

An on-chip, low-latency DSP supports Texas Instruments' Smart Amp speaker protection algorithms to maximize loudness while maintaining safe speaker conditions.

9.4.3.2 High Pass Filter

Excessive DC and low frequency content in audio playback signal can damage loudspeakers. The TAS2563 employs a high-pass filter (HPF) to prevent this from occurring for the PCM playback path. The HPF can be disabled using register HPF_EN. The HPF Bi-Quad filter coefficients can be changed from the default 2 Hz using the *HPFC_N0*, *HPFC_N1*, *HPFC_D1* registers using the equation [N, D] = butter(1, fc/(fs/2), 'high'); round(N(0)*2^31);. These coefficients should be calculated and set using PurePath™ Console 3 Software.

Table 54. HPF Enable

HPF_EN	STATE
0	Enabled (default)
1	Disabled

9.4.3.3 Digital Volume Control and Amplifier Output Level

The gain from audio input to speaker terminals is controlled by setting the amplifier's output level and digital volume control (DVC).

Amplifier output level settings are presented in dBV (dB relative to 1 V_{rms}) with a full scale digital audio input (0 dBFS) and the digital volume control set to 0 dB. It should be noted that these levels may not be achievable because of analog clipping in the amplifier, so they should be used to convey gain only. Table 55 below shows gain settings that can be programmed via the *AMP_LEVEL* register.

Table 55. Amplifier Output Level Settings

AMP_LEVEL[4:0]	FULL SCALE OUTPUT	
	dBV	V_{PEAK} (V)
0x00	8	3.55
0x01	8.5	3.76
0x02	9	3.99
...	...	...
0x10	16	8.92
...	...	...
0x13	17.5	10.60
0x14	18	11.23
0x15-0x1F	Reserved	Reserved

Equation 1 calculates the amplifiers output voltage.

$$V_{AMP} = Input + A_{dvc} + A_{AMP} \ \ dBV$$

where

- V_{AMP} is the amplifier output voltage in dBV
- Input is the digital input amplitude in dB with respect to 0 dBFS
- A_{dvc} is the digital volume control setting, 0 dB to -100 dB in 0.5 dB steps
- A_{AMP} is the amplifier output level setting in dBV (1)

Settings greater than 0xC8 are interpreted as mute. When a change in digital volume control occurs, the device ramps the volume to the new setting based on the *DVC_RAMP* register bits. If *DVC_RAMP* is set to 0x0000 0000, volume ramping is disabled. This can be used to speed up startup, shutdown and digital volume changes when volume ramping is handled by the system master.

The digital voltage control registers *DVC_PCM* represent the volume in a 2.X format. To calculate the value to write to these 4 registers apply the following formula to the desired dB DVC_PCM = round(10^(dB/20)*2^30).

A volume ramp rate can be set using *DVC_RAMP* and represents a rate in 1.X format. To calculate the value to write to these 4 registers apply the following formula DVC_RAMP = round((1-exp(-1/(0.2*fs*time in seconds))*2^31).

Table 56. PCM Digital Volume Control

DVC_PCM[31:0]	VOLUME (dB)
0x0000 0D43 (MIN)	-110
...	...
0x4000 0000	0 (default)
...	...
0x5092 BEE4 (MAX)	2

Table 57. Digital Volume Ramp Rate

DVC_RAMP[31:0]	RAMP RATE @ 48kHz (s)
0x0000 0D43	0
...	

Table 57. Digital Volume Ramp Rate (continued)

DVC_RAMP[31:0]	RAMP RATE @ 48kHz (s)
0x7FFC 963B	1 s

9.4.3.4 Auto-mute During Idle Channel Mode

Device will stop playing audio if the input audio level drops below the programmable threshold for a programmable timer window. If this behavior is not preferred, threshold level can be kept at very low levels.

9.4.3.5 Auto-start/stop on Audio Clocks

The TAS2563 can enter low power software shutdown when the TDM clocks are stopped instead of going into clock error. The device will resume operation when the clocks resume.

9.4.3.6 Supply Tracking Limiters with Brown Out Prevention

The TAS2563 monitors battery voltage (VBAT) and the class-D voltage (PVDD) along with the audio signal to automatically decrease gain when the audio signal peaks exceed a programmable threshold. This helps prevent clipping and extends playback time through end of charge battery conditions. The limiters threshold can be configured to track the monitored voltage below a programmable inflection point with a programmable slope. A minimum threshold sets the limit of threshold reduction from the voltage tracking. Configurable attack rate, hold time and release rate are provided to shape the dynamic response of each limiter. The total attenuation is the sum of both the VBAT and PVDD limiter. If the ICLA is enabled the actual attenuation is based on the ICLA configuration using the calculated attenuation value of all devices on the selected ICLA bus.

A Brown Out Prevention (BOP) feature provides a priority input to provide a very fast response to transient dips in the battery supply (VBAT) which at end of charge conditions that can cause system level brown out. When the selected supply dips below the brown-out threshold the BOP will begin reducing gain with an first attack latency of less than 10 µs and a configurable attack rate. When the VBAT supply rises above the brownout threshold, the BOP will begin to release after the programmed hold time. During a BOP event the limiter updates will be paused. This is to prevent a limiter from releasing during a BOP event. The VBAT and PVDD limiters are enabled by setting the respective *LIMB_EN and LIMP_EN* bits high.

Table 58. VBAT Tracking Limiter Enable

LIMB_EN	VALUE
0	Disabled (default)
1	Enabled

Table 59. PVDD Tracking Limiter Enable

LIMP_EN	VALUE
0	Disabled (default)
1	Enabled

The limiters have configurable attack rates, hold times and release rates, which are available via the *LIMB_ATK_RT[2:0]*, *LIMB_HLD_TM[2:0]*, *LIMB_RLS_RT[2:0]* register bits respectively for VBAT and *LIMP_ATK_RT[2:0]*, *LIMP_HLD_TM[2:0]*, *LIMP_RLS_RT[2:0]* register bits respectively for PVDD . The limiters attack and release step sizes can be set by configuring the *LIMB_ATK_ST[1:0]* and *LIMB_RLS_ST[1:0]* register bits respectively for VBAT and *LIMP_ATK_ST[1:0]* and *LIMP_RLS_ST[1:0]* register bits respectively for PVDD. For sampling rates less that 44.1kHz and greater than 8 kHz the minimum attack rate is 20µs and for sampling rates of 8kHz or less the minimum attack rate is 40µs.

A maximum level of attenuation applied by the limiters and brown out prevention feature is configurable via the *LIM_MAX_ATN* register. This attenuation limit is shared between the features. For instance, if the maximum attenuation is set to 6 dB and the limiters have reduced gain by 4 dB, the brown out prevention feature will only be able to reduce the gain further by another 2 dB. If the limiter or brown out prevention feature is attacking and it reaches the maximum attenuation, gain will not be reduced any further.

The limiter max attenuation *LIM_MAX_ATN* represent the limit in a 1.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired dB using equation *LIMB_MAX_ATN* = round(10^(-dB/20)*2^31).

Table 60. Limiter Max Attenuation

LIM_MAX_ATN[31:0]	ATTENUATION (dB)
0x7214 82C0	-1
...	...
0x2D6A 866F	-9 (default)
...	...
0x1326 DD71	-16.5

The limiter begins reducing gain when the output signal level is greater than the limiter threshold. The limiter can be configured to track selected supply below a programmable inflection point with a minimum threshold value. Figure 62 below shows the limiter configured to limit to a constant level regardless of the selected supply level. To achieve this behavior, set the limiter maximum threshold to the desired level using *LIM_TH_MAX*. Set the limiter inflection point using *LIM_INF_PT* below the minimum allowable supply setting. The limiter minimum threshold register *LIM_TH_MIN* does not impact limiter behavior in this use case.

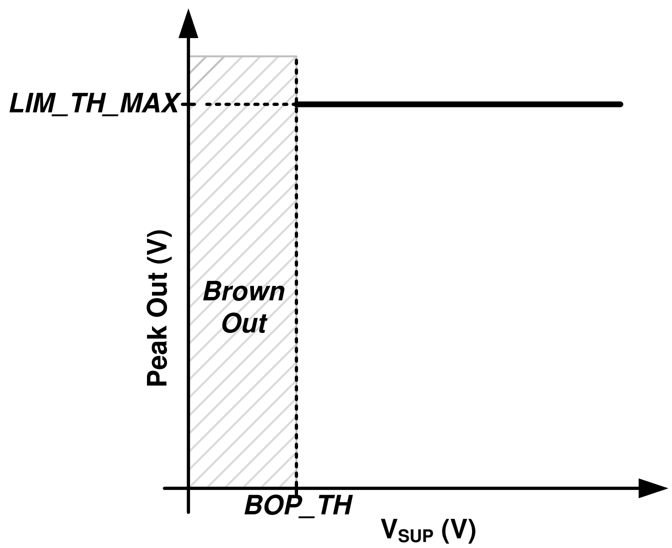


Figure 62. Limiter with Fixed Threshold

The VBAT limiter threshold max *LIMB_TH_MAX* and min *LIMB_TH_MIN* registers represent the limit in a 5.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired threshold voltage using the equation *LIMB_TH_MAX* or *LIMB_TH_MIN* = round(Volts*2^27).

Table 61. VBAT Limiter Maximum Threshold

LIMB_TH_MAX[31:0]	THRESHOLD (V)
0x1400 0000	2.5
...	...
0x4800 0000	9 (default)
...	...
0x7C00 0000	15.5

Table 62. VBAT Limiter Minimum Threshold

LIMB_TH_MIN[31:0]	THRESHOLD (V)
0x1400 0000	2.5
...	...
0x2000 0000	4 (default)
...	...
0x7C00 0000	15.5

The VBAT limiter inflection point *LIMB_INF_PT* represent the limit in a 5.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired infection voltage using the equation *LIMB_INF_PT* = round(Volts*2^27).

Table 63. VBAT Limiter Inflection Point

LIMB_INF_PT[31:0]	THRESHOLD (V)
`0x2000 0000`	2
`...`	...
`0x34CC CCCD`	3.3 (default)
`...`	...
`0x3000 0000`	6

Figure 63 shows how to configure the limiter to track selected supply below a threshold without a minimum threshold. Set the *LIM_TH_MAX* register to the desired threshold and *LIM_INF_PT* register to the desired inflection point where the limiter will begin reducing the threshold with the selected supply. The default value of 1 V/V will reduce the threshold 1 V for every 1 V of drop in the supply voltage. More aggressive tracking slopes can be programmed if desired. Program the *LIM_TH_MIN* below the minimum the selected supply to prevent the limiter from having a minimum threshold reduction when tracking the selected supply.

The VBAT limiter tracking slope *LIMB_SLOPE[31:0]* represent the limit in a 5.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired infection voltage using equation *LIMB_SLOPE* = round(slope(V/V)*2^27)

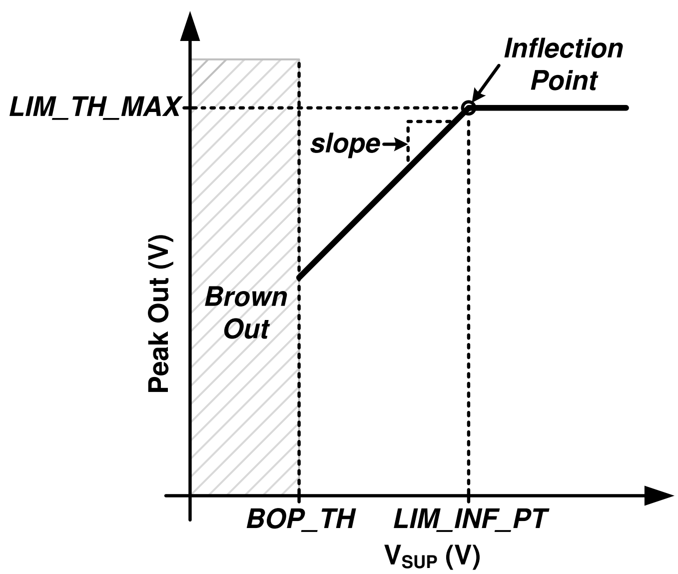


Figure 63. Limiter with Inflection Point

To achieve a limiter that tracks the selected supply below a threshold, configure the limiter as explained in the previous example, except program the *LIM_TH_MIN* register to the desired minimum threshold. This is shown in Figure 64 below.

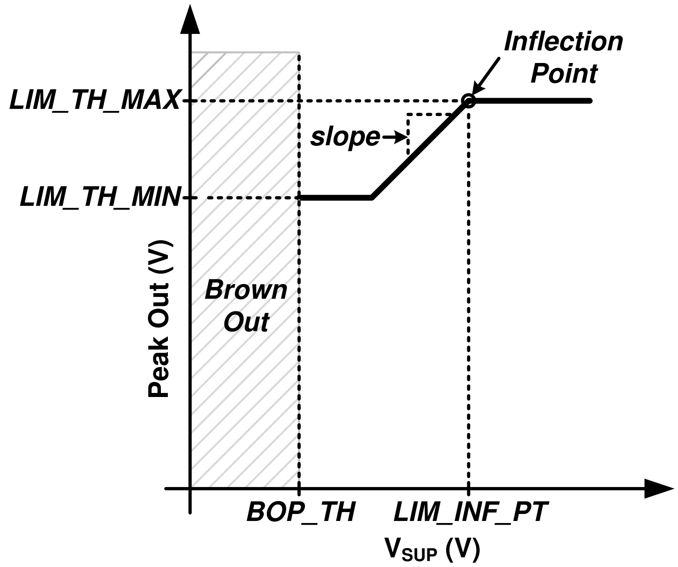


Figure 64. Limiter with Inflection Point and Minimum Threshold

The TAS2563 also employs a Brown Out Prevention (BOP) feature that serves as a low latency priority input to the limiter engine that begins attacking the VBAT supply dipping below the programmed BOP threshold. This feature can be enabled by setting the *BOP_EN* register bit high. It should be noted that the BOP feature is independent of the limiter and will function if enabled, even if the limiter is disabled. The BOP threshold is configured by setting the threshold with register bits *BOP_TH*.

Table 64. Brown Out Prevention Enable

BOP_EN	VALUE
0	Disabled
1	Enabled (default)

The Brownout prevention threshold *BOP_TH* represent a threshold in a 5.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired brownout threshold using equation *BOP_TH* = round(Volts*2^27).

Table 65. Brown Out Prevention Threshold

BOP_TH[31:0]	VBAT THRESHOLD (V)
0x0000 000 - 0x1FFF FFFF	Reserved
0x2000 0000	2.5
...	...
0x2E66 6666	2.9 (default)
...	...
0x2000 0000	4
0x2000 0001 - 0xFFFF FFFF	Reserved

The BOP feature has a separate attack rate *BOP_ATK_RT*, attack step size *BOP_ATK_ST* and hold time *BOP_HLD_TM* from the battery tracking limiter. The BOP feature uses the *LIMB_RLS_RT* register setting to release after a brown out event. The rates are based on the number of audio samples and actual time values can be calculated by multiplying by 1/fs. For example the attack rate of 4 samples at 48 ksps would be approximately 83 µs.

Table 66. Brown Out Prevention Attack Rate

BOP_ATK_RT[2:0]	ATTACK RATE (samples/step)	ATTACK RATE @ 48 ksps (~µs)
0x0	1	20
0x1	2	42
0x2	4	83
0x3	8	167
0x4	16	333
0x5	32	666
0x6	64	1300
0x7	128	2700

Table 67. Brown Out Prevention Attack Step Size

BOP_ATK_ST[1:0]	STEP SIZE (dB)
00	0.5
01	1 (default)
10	1.5
11	2

Table 68. Brown Out Prevention Hold Time

BOP_HLD_TM[2:0]	HOLD TIME (ms)
0x0	0
0x1	10
0x2	25
0x3	50
0x4	100
0x5	250
0x6	500 (default)
0x7	1000

The TAS2563 can also shutdown the device when a brown out event occurs if the *BOP_MUTE* register bit is set high. For the device to continue playing audio again, the device must transition through a SW/HW shutdown state. Setting the *BOP_INF_HLD* high will cause the limiter to stay in the hold state (i.e. never release) after a cleared brown out event until either the device transitions through a mute or SW/HW shutdown state or the register bit *BOP_HLD_CLR* is written to a high value (which will cause the device to exit the hold state and begin releasing). This bit is self clearing and will always readback low. Figure 65 below illustrates the entering and exiting from a brown out event.

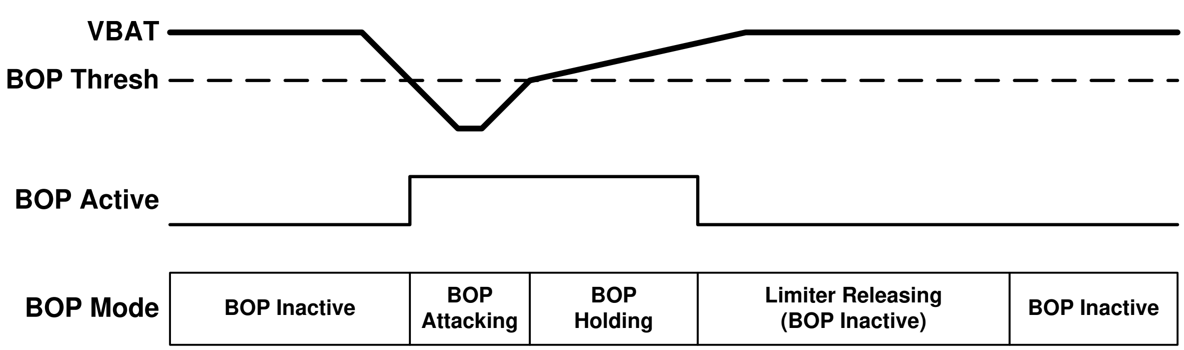


Figure 65. Brown Out Prevention Event

Table 69. Shutdown on Brown Out Event

BOP_MUTE	VALUE
0	Don't Shutdown (default)
1	Mute then shutdown

Table 70. Infinite Hold on Brown Out Event

BOP_INF_HLD	VALUE
0	Use *BOP_HLD_TM* after Brown Out event (default)
1	Do not release until *BOP_HLD_CLR* is asserted high

Table 71. BOP Infinite Hold Clear

BOP_HLD_CLR	VALUE
0	Don't clear (default)
1	Clear event (self clearing)

A hard brownout level can be set to shutdown the TAS2563 if the BOP cannot mitigate the drop in battery voltage VBAT. This will shutdown the device and should not be used if the *BOP_MUTE* is enable. The brownout shutdown will only function if brownout engine is enabled using *BOP_EN*.

Table 72. Brown Out Shutdown Enable

BOSD_EN	VALUE
0	Disabled (default)
1	Enabled

The Brownout prevention shutdown threshold *BOSD_TH* represent a threshold in a 5.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired brownout threshold using equation *BOSD_TH* = round(Volts*2^27).

Table 73. Brown Out Shutdown Threshold

BOSD_TH[31:0]	VBAT THRESHOLD (V)
0x2000 0000	2.5
...	...
0x2B33 3333	2.7 (default)
...	...
0x3FFF FFFF	3.99

9.4.3.7 Class-D Settings

The TAS2563 Class-D amplifier supports spread spectrum PWM modulation, which can be enabled by setting the *AMP_SS* register bit high. This can help reduce EMI in some systems.

Table 74. Low EMI Spread Spectrum Mode

AMP_SS	SPREAD SPECTRUM
0	Disabled
1	Enabled (default)

By default the Class-D amplifier's switching frequency is based on the device's trimmed internal oscillator. To synchronize switching to the audio sample rate, set the *CLASSD_SYNC* register bit high. When the Class-D is synchronized to the audio sample rate, the *RATE_RAMP* register bit must be set based whether the audio sample rate is based on a 44.1 kHz or 48 kHz frequency. For 44.1, 88.2 and 176.4 kHz, set this bit high. for 48, 96 and 192 kHz, set this bit low. This ensures that the internal ramp generator has the appropriate slope.

Table 75. Class-D Synchronization Mode

CLASSD_SYNC	SYNCHRONIZATION MODE
0	Not synchronized to audio clocks (default)
1	Synchronized to audio clocks

Table 76. Sample Rate for Class-D Synchronized Mode

RAMP_RATE	PLAYBACK SAMPLE RATE
0	multiples of 48 kHz(default)
1	multiples of 44.1 kHz

9.4.4 SAR ADC

A 10-bit SAR ADC monitors VBAT voltage *VBAT_CNV* , PVDD voltage *PVDD_CNV* and die temperature *TMP_CNV*. VBAT voltage conversions are also used by the limiter and brown out prevention features.

Actual VBAT voltage is calculated by dividing the *VBAT_CNV* register by 64. Actual die temperature is calculated by subtracting 93 from *TMP_CNV* register. The battery voltage VBAT can be filtered using *VBAT_FLT* register but will increase the latency. The *VBAT_CNV* registers should be read *VBAT_MSB* followed by *VBAT_LSB*.

Table 77. ADC VBAT Voltage Conversion

VBAT_CNV[9:0]	VBAT VOLTAGE (V)
0x000	0 V
0x001	0.0156 V
...	...
0x100	4.0 V
...	...
0x17F	5.9844 V
0x180	6.0 V

Table 78. ADC Die Temperature Conversion

TMP_CNV[7:0]	DIE TEMPERATURE (°C)
0x00	-93 °C
0x01	-92 °C
...	...
0x76	25 °C
...	...
0xFE	161 °C
0xFF	162 °C

9.4.5 IV Sense

The TAS2563 provides speaker voltage and current sense for real time monitoring of loudspeaker behavior. The VSNS_P and VSNS_N pins should be connected after any ferrite bead filter (or directly to the OUT_P and OUT_N connections if no EMI filter is used). The V-Sense connections eliminate IR drop error due to packaging, PCB interconnect or ferrite bead filter resistance. It should be noted that any interconnect resistance after the V-Sense terminals will not be corrected for, so it is advised to connect the sense connections as close to the load as possible.

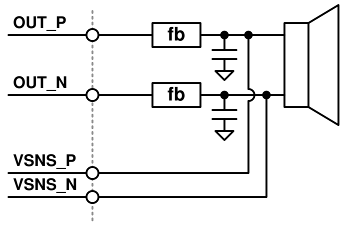


Figure 66. V-Sense Connections

I-Sense and V-Sense can be powered down by asserting the *ISNS_PD* and *VSNS_PD* register bits respectively. When powered down, the device will return null samples for the powered down block. The IV-sense is High Passed Filtered and the Bi-Quad filter coefficients can be changed from the default 2 Hz using the *IVHPFC_N0*, *IVHPFC_N1*, *IVHPFC_D1* registers using the equations [N, D] = butter(1, fc/(fs/2), 'high'); round(N(0)*2^31);. These coefficients can be calculated and set using PurePath™ Console 3 Software.

Table 79. I-Sense Power Down

ISNS_PD	SETTING
0	I-Sense is active
1	I-Sense is powered down (default)

Table 80. V-Sense Power Down

VSNS_PD	SETTING
0	V-Sense is active
1	V-Sense is powered down (default)

9.4.6 Load Diagnostics

The TAS2563 can check the speaker terminal for an open or short. This can be used to determine if a problem exists with the speaker or trace to the speaker. The entire operation is performed by the TAS2563 and results reported using the IRQZ pin or read over I2C bus on completion. The load diagnostics can be performed using external audio clock or the internal oscillator.

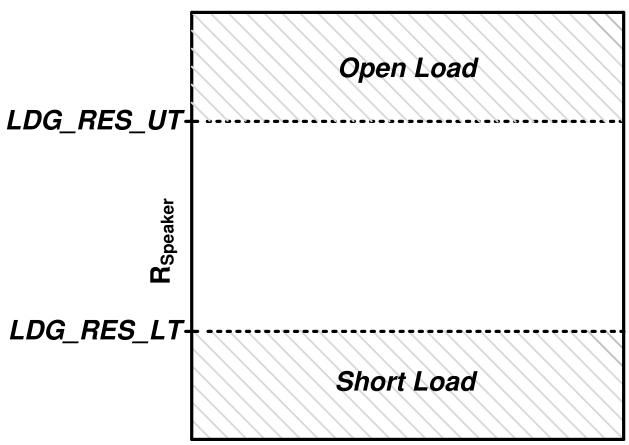


Figure 67. Load Diagnostics

The speaker open and short thresholds are configured using the respective *LDG_RES_UT* and *LDG_RES_LT* registers using equation round(Ω/7*2^22). The load diagnostic mode can be run in two ways. First if the device is in Software Shutdown the load diagnostic mode can be run but setting LDG_MODE high. The diagnostic will be run and the device will return to Software Shutdown. The load diagnostics can also be run before transitioning to Active. This is done by setting the MODE register to Perform Load Diagnostics. If the load is within the specified range the device will transition to Active otherwise it will transition to Software Shutdown. When the load diagnostics is run it will play a 22 kHz at -35dBFS for 100ms and measure the resistance of the speaker trace. The result is averaged over the time specified by the IVSNS_AVG register. The measured speaker impedance can be read from *LDS_RES_VAL1* using the equations Impedance = 7*(LD_RES_VAL1)/2^22) Ω.

Table 81. IV-sense Averaging

IVSNS_AVG[1:0]	SETTING
00	5 ms (default)
01	10 ms
10	50 ms
11	100 ms

Table 82. Load Diagnostic Mode

LDG_MODE	SETTING
0	Load Diagnostic Not Running (default)
1	Run Load Diagnostic

Table 83. Load Diagnostic Clock Source

LDG_CLK	SETTING
0	External TDM
1	Internal Oscillator (default)

9.4.7 Clocks and PLL

In TMD/I^{2}C Mode, the device operates from SBCLK. Table 84 and Table 85 below shows the valid SBCLK frequencies for each sample rate and SBCLK to FSYNC ratio (for 44.1 kHz and 48 kHz family frequencies respectively.

If the sample rate is properly configured via the *SAMP_RATE[1:0]* bits, no additional configuration is required as long as the SBCLK to FSYNC ratio is valid. The device will detect improper SBCLK frequencies and SBCLK to FSYNC ratios and volume ramp down the playback path to minimize audible artifacts. After the clock error is detected the device will enter a low power halt mode after *CLK_HALT_TIMER* if *CLK_HALT_EN* is enabled. Additionally the device can automatically power up and down on valid clock signals if *CLK_ERR_PWR_EN* is set. The device sampling rate should not be changed while this feature is enabled. Additionally, the *CLK_HALT_EN* should be set when *CLK_ERR_PWR_EN* is set for this feature to work properly.

Table 84. Supported SBCLK Frequencies (48 kHz based sample rates)

Sample Rate (kHz)	SBCLK to FSYNC Ratio						
	64	96	128	192	256	384	512
16 kHz	1.024 MHz	1.536 MHz	2.048 MHz	3.072 MHz	4.096 MHz	6.144 MHz	8.192 MHz
32 kHz	2.048 MHz	3.072 MHz	4.0960 MHz	6.144 MHz	8.192 MHz	12.288 MHz	16.384 MHz
48 kHz	3.072 MHz	4.608 MHz	6.144 MHz	9.216 MHz	12.288 MHz	18.432 MHz	24.576 MHz
96 kHz	6.144 MHz	9.216 MHz	12.288 MHz	18.432 MHz	24.576 MHz	-	-

Table 85. Supported SBCLK Frequencies (44.1 kHz based sample rates)

Sample Rate (kHz)	SBCLK to FSYNC Ratio						
	64	96	128	192	256	384	512
14.7 kHz	940.8 kHz	1.4112 MHz	1.8816 MHz	2.8224 MHz	3.7632 MHz	5.6448 MHz	7.5264 MHz

Table 85. Supported SBCLK Frequencies (44.1 kHz based sample rates) (continued)

Sample Rate (kHz)	SBCLK to FSYNC Ratio						
	64	96	128	192	256	384	512
29.4 kHz	1.8816 MHz	2.8224 MHz	3.7632 MHz	5.6448 MHz	7.5264 MHz	11.2896 MHz	15.0528 MHz
44.1 kHz	2.8224 MHz	4.2336 MHz	5.6448 MHz	8.4672 MHz	11.2896 MHz	16.9344 MHz	22.5792 MHz
88.2 kHz	5.6448 MHz	8.4672 MHz	11.2896 MHz	16.9344 MHz	22.5792 MHz	-	-

Table 86. Clock Power Up/Down on Valid ASI Clocks

CLK_ERR_PWR_EN	Setting
0	Disabled (default)
1	Enabled

Table 87. Clock Halt(Sleep) After Errors Longer Than Halt Timer

CLK_HALT_EN	Setting
0	Enabled (default)
1	Disabled

Table 88. Clock Halt Timer

CLK_HALT_TIMER[2:0]	Setting
000	1 ms
001	3.27 ms
010	26.21 ms
011	52.42 ms (default)
100	104.85 ms
101	209.71 ms
110	419.43 ms
111	838.86 ms

9.4.8 Thermal Foldback

The TAS2563 monitors the die temperature and can automatically limit the audio signal when the die temperature reaches a set threshold. It is recommended to use PurePath™ Console 3 Software to configure the thermal foldback as the software will perform the necessary math for each register.

Thermal foldback can be disabled using *TF_EN*. If the die temperature reaches *TF_TEMP_TH* this feature will begin to attenuate the audio signal to prevent the device from shutting down due to over-temperature. It will attenuate the audio signal by TF_LIMS db per degree of temperature over TF_TEMP_TH. The thermal foldback with attack at a fixed rate of 0.25dB per sample. A maximum attenuation of TF_MAX_ATTN can be specified. However if the device continue to heat up eventually the device over-temperature will be triggered. The attenuation will be held for *TF_HOLD_CNT* samples before the attenuation will begin releasing.

Table 89. Thermal Foldback Enable

TF_EN	SETTING
0	Disabled
1	Enabled (default)

Table 90. Thermal Foldback Registers

REGISTER	DESCRIPTION	CALCULATION
TF_LIMS	Thermal foldback limiter slope (in db/°C)	round(10^(-slope / 20)*2^31)
TF_HOLD_CNT	Thermal foldback hold count (samples)	round(seconds * 1000)

Table 90. Thermal Foldback Registers (continued)

REGISTER	DESCRIPTION	CALCULATION
TF_REL_RATE	Thermal foldback limiter release rate (db/samples)	round(10^(dB per sample / 20)*2^30)
TF_TEMP_TH	Thermal foldback limiter temperature threshold (°C)	round(°C * 2^23)
TF_MAX_ATTN	Thermal foldback max gain reduction (dB)	round(10^(max attn dB/20)*2^31)

9.5 Register Maps

9.5.1 Register Summary Table Page=0x00

Addr	Register	Description	Section
0x00	PAGE	Device Page	PAGE (page=0x00 address=0x00) [reset=0h]
0x01	SW_RESET	Software Reset	SW_RESET (page=0x00 address=0x01) [reset=0h]
0x02	PWR_CTL	Power Control	PWR_CTL (page=0x00 address=0x02) [reset=Eh]
0x03	PB_CFG1	Playback Configuration 1	PB_CFG1 (page=0x00 address=0x03) [reset=20h]
0x04	MISC_CFG1	Misc Configuration 1	MISC_CFG1 (page=0x00 address=0x04) [reset=C6h]
0x05	MISC_CFG2	Misc Configuration 2	MISC_CFG2 (page=0x00 address=0x05) [reset=22h]
0x06	TDM_CFG0	TDM Configuration 0	TDM_CFG0 (page=0x00 address=0x06) [reset=9h]
0x07	TDM_CFG1	TDM Configuration 1	TDM_CFG1 (page=0x00 address=0x07) [reset=2h]
0x08	TDM_CFG2	TDM Configuration 2	TDM_CFG2 (page=0x00 address=0x08) [reset=4Ah]
0x09	TDM_CFG3	TDM Configuration 3	TDM_CFG3 (page=0x00 address=0x09) [reset=10h]
0x0A	TDM_CFG4	TDM Configuration 4	TDM_CFG4 (page=0x00 address=0x0A) [reset=13h]
0x0B	TDM_CFG5	TDM Configuration 5	TDM_CFG5 (page=0x00 address=0x0B) [reset=2h]
0x0C	TDM_CFG6	TDM Configuration 6	TDM_CFG6 (page=0x00 address=0x0C) [reset=0h]
0x0D	TDM_CFG7	TDM Configuration 7	TDM_CFG7 (page=0x00 address=0x0D) [reset=4h]
0x0E	TDM_CFG8	TDM Configuration 8	TDM_CFG8 (page=0x00 address=0x0E) [reset=5h]
0x0F	TDM_CFG9	TDM Configuration 9	TDM_CFG9 (page=0x00 address=0x0F) [reset=6h]
0x10	TDM_CFG10	TDM Configuration 10	TDM_CFG10 (page=0x00 address=0x10) [reset=7h]
0x11	DSP Mode & TDM_DET	TDM Clock detection monitor	DSP Mode & TDM_DET (page=0x00 address=0x11) [reset=7Fh]
0x12	LIM_CFG0	Limiter Configuration 0	LIM_CFG0 (page=0x00 address=0x12) [reset=12h]
0x13	LIM_CFG1	Limiter Configuration 1	LIM_CFG1 (page=0x00 address=0x13) [reset=76h]
0x14	DSP FREQUENCY & BOP_CFG0	Brown Out Prevention 0	DSP FREQUENCY & BOP_CFG0 (page=0x00 address=0x14) [reset=1h]
0x15	BOP_CFG0	Brown Out Prevention 2	BOP_CFG0 (page=0x00 address=0x15) [reset=2Eh]
0x16	BIL_and_ICLA_CFG0	Boost Current limiter and ICLA	BIL_and_ICLA_CFG0 (page=0x00 address=0x16) [reset=60h]
0x17	BIL_ICLA_CFG1	Inter Chip Limiter Alignment 0	BIL_ICLA_CFG1 (page=0x00 address=0x17) [reset=0h]
0x18	GAIN_ICLA_CFG0	Inter Chip Limiter Alignment 0	GAIN_ICLA_CFG0 (page=0x00 address=0x18) [reset=0h]
0x19	ICLA_CFG1	Inter Chip Limiter Alignment 1	ICLA_CFG1 (page=0x00 address=0x19) [reset=0h]
0x1A	INT_MASK0	Interrupt Mask 0	INT_MASK0 (page=0x00 address=0x1A) [reset=FCh]
0x1B	INT_MASK1	Interrupt Mask 1	INT_MASK1 (page=0x00 address=0x1B) [reset=A6h]
0x1C	INT_MASK2	Interrupt Mask 2	INT_MASK2 (page=0x00 address=0x1C) [reset=DFh]
0x1D	INT_MASK3	Interrupt Mask 3	INT_MASK3 (page=0x00 address=0x1D) [reset=FFh]
0x1F	INT_LIVE0	Live Interrupt Readback 0	INT_LIVE0 (page=0x00 address=0x1F) [reset=0h]
0x20	INT_LIVE1	Live Interrupt Readback 1	INT_LIVE1 (page=0x00 address=0x20) [reset=0h]
0x21	INT_LIVE3	Live Interrupt Readback 2	INT_LIVE3 (page=0x00 address=0x21) [reset=0h]
0x22	INT_LIVE4	Live Interrupt Readback 3	INT_LIVE4 (page=0x00 address=0x22) [reset=0h]
0x24	INT_LTCH0	Latched Interrupt Readback 0	INT_LTCH0 (page=0x00 address=0x24) [reset=0h]
0x25	INT_LTCH1	Latched Interrupt Readback 1	INT_LTCH1 (page=0x00 address=0x25) [reset=0h]
0x26	INT_LTCH3	Latched Interrupt Readback 2	INT_LTCH3 (page=0x00 address=0x26) [reset=0h]

Register Maps (continued)

0x27	INT_LTCH4	Latched Interrupt Readback 3	INT_LTCH4 (page=0x00 address=0x27) [reset=0h]
0x2A	VBAT_MSB	SAR ADC Conversion 0	VBAT_MSB (page=0x00 address=0x2A) [reset=0h]
0x2B	VBAT_LSB	SAR ADC Conversion 1	VBAT_LSB (page=0x00 address=0x2B) [reset=0h]
0x2C	TEMP	SAR ADC Conversion 2	TEMP (page=0x00 address=0x2C) [reset=0h]
0x30	INT & CLK CFG		INT & CLK CFG (page=0x00 address=0x30) [reset=19h]
0x31	DIN_PD	Digital Input Pin Pull Down	DIN_PD (page=0x00 address=0x31) [reset=40h]
0x32	MISC	Misc Configuration	MISC (page=0x00 address=0x32) [reset=80h]
0x33	BOOST_CFG1	Boost Configure 1	BOOST_CFG1 (page=0x00 address=0x33) [reset=34h]
0x34	BOOST_CFG2	Boost Configure 2	BOOST_CFG2 (page=0x00 address=0x34) [reset=4Bh]
0x35	BOOST_CFG3	Boost Configure 3	BOOST_CFG3 (page=0x00 address=0x35) [reset=74h]
0x3B	MISC		MISC (page=0x00 address=0x3B) [reset=58h]
0x3F	TG_CFG0	Tone Generator	TG_CFG0 (page=0x00 address=0x3F) [reset=0h]
0x40	BST_ILIM_CFG0	Boost ILIM configuration-0	BST_ILIM_CFG0 (page=0x00 address=0x40) [reset=36h]
0x41	PDM_CONFIG0		PDM_CONFIG0 (page=0x00 address=0x41) [reset=1h]
0x42	DIN_PD & PDM_CONFIG3		DIN_PD & PDM_CONFIG3 (page=0x00 address=0x42) [reset=F8h]
0x43	ASI2_CONFIG0		ASI2_CONFIG0 (page=0x00 address=0x43) [reset=8h]
0x44	ASI2_CONFIG1		ASI2_CONFIG1 (page=0x00 address=0x44) [reset=0h]
0x45	ASI2_CONFIG2		ASI2_CONFIG2 (page=0x00 address=0x45) [reset=1h]
0x46	ASI2_CONFIG3		ASI2_CONFIG3 (page=0x00 address=0x46) [reset=FCh]
0x49	PVDD_MSB_DSP	SAR ADC Conversion 0	PVDD_MSB_DSP (page=0x00 address=0x49) [reset=0h]
0x4A	PVDD_LSB_DSP	SAR ADC Conversion 1	PVDD_LSB_DSP (page=0x00 address=0x4A) [reset=0h]
0x7D	REV_ID	Revision and PG ID	REV_ID (page=0x00 address=0x7D) [reset=0h]
0x7E	I2C_CKSUM	I2C Checksum	I2C_CKSUM (page=0x00 address=0x7E) [reset=0h]
0x7F	BOOK	Device Book	BOOK (page=0x00 address=0x7F) [reset=0h]

9.5.2 PAGE (page=0x00 address=0x00) [reset=0h]

The device's memory map is divided into pages and books. This register sets the page.

Figure 68. PAGE Register Address: 0x00

7	6	5	4	3	2	1	0
PAGE[7:0]							
RW-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 91. Device Page Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	RW	0h	Sets the device page. 00h = Page 0 01h = Page 1 ... FFh = Page 255

9.5.3 SW_RESET (page=0x00 address=0x01) [reset=0h]

Asserting Software Reset will place all register values in their default POR (Power on Reset) state.

Figure 69. SW_RESET Register Address: 0x01

7	6	5	4	3	2	1	0
Reserved							SW_RESET
R-0h							RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 92. Software Reset Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0h	Reserved
0	SW_RESET	RW	0h	Software reset. Bit is self clearing. 0b = Don't reset 1b = Reset

9.5.4 PWR_CTL (page=0x00 address=0x02) [reset=Eh]

Sets device's mode of operation and power down of IV sense blocks.

Figure 70. PWR_CTL Register Address: 0x02

7	6	5	4	3	2	1	0
PDM_I2S_MODE	LDG_MODE_ONLY	Reserved	Reserved	ISNS_PD	VSNS_PD	MODE[1:0]	
RW-0h	RW-0h	RW-0h	RW-0h	RW-1h	RW-1h	RW-2h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 93. Power Control Field Descriptions

Bit	Field	Type	Reset	Description
7	PDM_I2S_MODE	RW	0h	PDM I2S mode 0b = PDM_I2S mode disabled 1b = PDM_I2S mode enabled
6	LDG_MODE_ONLY	RW	0h	Only Load Diagnsotics mode, self clearing bit 0b = Only Load diagnostics mode disabled 1b = Only Load diagnostics mode enabled
5	Reserved	RW	0h	Reserved
4	Reserved	RW	0h	Reserved
3	ISNS_PD	RW	1h	Current sense power down. 0b = Current sense active 1b = Current sense is powered down
2	VSNS_PD	RW	1h	Voltage sense power down. 0b = voltage sense is active 1b = Voltage sense is powered down
1-0	MODE[1:0]	RW	2h	Device operational mode. 00b = Active 01b = Mute 10b = Software Shutdown 11b = Load Diagnostics followed by device ACTIVE

9.5.5 PB_CFG1 (page=0x00 address=0x03) [reset=20h]

Sets playback high pass filter corner (PCM playback only).

Figure 71. PB_CFG1 Register Address: 0x03

7	6	5	4	3	2	1	0
Reserved	DIS_DC_BLOCKER	AMP_LEVEL[4:0]					Reserved
R-0h	RW-0h	RW-10h					RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 94. Playback Configuration 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	DIS_DC_BLOCKER	RW	0h	Disable DC Blocker 0b = DC Blocker Enabled 1b = DC Blocker Disabled

Table 94. Playback Configuration 1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-1	AMP_LEVEL[4:0]	RW	10h	1Dh-1Fh - Reserved 01h = 8.5 dBV(3.76Vpk) 02h = 9.0 dBV(3.99Vpk) 03h = 9.5 dBV(4.22Vpk) 04h = 10.0 dBV(4.47Vpk) 05h = 10.5 dBV(4.74Vpk) 06h = 11.0 dBV (5.02 Vpk) 07h = 11.5 dBV (5.32 Vpk) 08h = 12.0 dBV (5.63 Vpk) 09h = 12.5 dBV (5.96 Vpk) 0Ah = 13.0 dBV (6.32 Vpk) 0Bh = 13.5 dBV (6.69 Vpk) 0Ch = 14.0 dBV (7.09 Vpk) 0Dh = 14.5 dBV (7.51 Vpk) 0Eh = 15.0 dBV (7.95 Vpk) 0Fh = 15.5 dBV (8.42 Vpk) 10h = 16.0 dBV (8.92 Vpk) 11h = 16.5 dBV (9.45 Vpk) 12h = 17.0 dBV (10.01 Vpk) 13h = 17.5 dBV (10.61 Vpk) 14h = 18.0 dBV (11.23 Vpk) 15h = 18.5dBV(11.90 Vpk) 16h = 19dBV(12.60Vpk) 17h = 19.5dBV(13.35Vpk) 18h = 20.0dBV(14.14Vpk) 19h = 20.5dBV(14.98Vpk) 1Ah = 21dBV(15.87Vpk) 1Bh = 21.5dBV(16.81Vpk) 1Ch = 22dBV(17.8Vpk) 1Dh-1Fh - Reserved
0	Reserved	RW	0h	Reserved

9.5.6 MISC_CFG1 (page=0x00 address=0x04) [reset=C6h]

Sets DVC Ramp Rate, OTE/OCE retry, IRQZ pull up, amp spread spectrum and I-Sense current range.

Figure 72. MISC_CFG1 Register Address: 0x04

7	6	5	4	3	2	1	0
CP_PG_RETRY	VBAT_POR_RETRY	OCE_RETRY	OTE_RETRY	IRQZ_PU	AMP_SS	Reserved	
RW-1h	RW-1h	RW-0h	RW-0h	RW-0h	RW-1h	RW-2h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 95. Misc Configuration 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	CP_PG_RETRY	RW	1h	Retry after vbat por event. 0b = Do not retry 1b = Retry after 1.5 s
6	VBAT_POR_RETRY	RW	1h	Retry after vbat por event. 0b = Do not retry 1b = Retry after 1.5 s
5	OCE_RETRY	RW	0h	Retry after over current event. 0b = Do not retry 1b = Retry after 1.5 s
4	OTE_RETRY	RW	0h	Retry after over temperature event. 0b = Do not retry 1b = Retry after 1.5 s
3	IRQZ_PU	RW	0h	IRQZ internal pull up enable. 0b = Disabled 1b = Enabled

Table 95. Misc Configuration 1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	AMP_SS	RW	1h	Low EMI spread spectrum enable. 0b = Disabled 1b = Enabled
1-0	Reserved	RW	2h	Reserved

9.5.7 MISC_CFG2 (page=0x00 address=0x05) [reset=22h]

Figure 73. MISC_CFG2 Register Address: 0x05

7	6	5	4	3	2	1	0
SDZ_MODE[1:0]		SDZ_TIMEOUT[1:0]		Reserved	DIS_VBAT_FLT	I2C_GBL_EN	DIS_PVDD_FLT
RW-0h		RW-2h		RW-0h	RW-0h	RW-1h	RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 96. Misc Configuration 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SDZ_MODE[1:0]	RW	0h	SDZ Mode configuration. 00b = initiates normal shutdown; force shutdown after timeout 01b = immediate force shutdown 10b = normal shutdown only 11b = reserved
5-4	SDZ_TIMEOUT[1:0]	RW	2h	SDZ Timeout value 00b = 2 ms 01b = 4 ms 10b = 6 ms 11b = 23.8 ms
3	Reserved	RW	0h	Reserved
2	DIS_VBAT_FLT	RW	0h	VBAT filter into SAR ADC 0b = VBAT filter with 100kHz cut off 1b = Bypass VBAT FLT
1	I2C_GBL_EN	RW	1h	I2C global address is 0b = disabled 1b = enabled
0	DIS_PVDD_FLT	RW	0h	PVDD filter into SAR ADC 0b = PVDD filter with 100kHz cut off 1b = Bypass PVDD FLT

9.5.8 TDM_CFG0 (page=0x00 address=0x06) [reset=9h]

Sets the TDM frame start, TDM sample rate, TDM auto rate detection and whether rate is based on 44.1 kHz or 48 kHz frequency.

Figure 74. TDM_CFG0 Register Address: 0x06

7	6	5	4	3	2	1	0
Reserved	CLASSD_SYNC	RAMP_RATE	AUTO_RATE	SAMP_RATE[2:0]			FRAME_START
R-0h	RW-0h	RW-0h	RW-0h	RW-4h			RW-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 97. TDM Configuration 0 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	CLASSD_SYNC	RW	0h	Class-D synchronization mode. 0b = Not synchronized to audio clocks 1b = Synchronized to audio clocks

Table 97. TDM Configuration 0 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RAMP_RATE	RW	0h	Sample rate based on 44.1kHz or 48kHz when CLASSD_SYNC=1. 0b = 48kHz 1b = 44.1kHz
4	AUTO_RATE	RW	0h	Auto detection of TDM sample rate. 0b = Enabled 1b = Disabled
3-1	SAMP_RATE[2:0]	RW	4h	Sample rate of the TDM bus. 000b = 7.35/8 kHz 001b = 14.7/16 kHz 010b = 22.05/24 kHz 011b = 29.4/32 kHz 100b = 44.1/48 kHz 101b = 88.2/96 kHz 110b = 176.4/192 kHz 111b = Reserved
0	FRAME_START	RW	1h	TDM frame start polarity. 0b = Low to High on FSYNC 1b = High to Low on FSYNC

9.5.9 TDM_CFG1 (page=0x00 address=0x07) [reset=2h]

Sets TDM RX justification, offset and capture edge.

Figure 75. TDM_CFG1 Register Address: 0x07

7	6	5	4	3	2	1	0
Reserved	RX_JUSTIFY	RX_OFFSET[4:0]					RX_EDGE
R-0h	RW-0h	RW-1h					RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 98. TDM Configuration 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	RX_JUSTIFY	RW	0h	TDM RX sample justification within the time slot. 0b = Left 1b = Right
5-1	RX_OFFSET[4:0]	RW	1h	TDM RX start of frame to time slot 0 offset (SBCLK cycles).
0	RX_EDGE	RW	0h	TDM RX capture clock polarity. 0b = Rising edge of SBCLK 1b = Falling edge of SBCLK

9.5.10 TDM_CFG2 (page=0x00 address=0x08) [reset=4Ah]

Sets TDM RX time slot select, word length and time slot length.

Figure 76. TDM_CFG2 Register Address: 0x08

7	6	5	4	3	2	1	0
IVMON_LEN[1:0]		RX_SCFG[1:0]		RX_WLEN[1:0]		RX_SLEN[1:0]	
RW-1h		RW-0h		RW-2h		RW-2h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 99. TDM Configuration 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	IVMON_LEN[1:0]	RW	1h	Sets the current and voltage data to length of 00b = 8 bits 01b = 16 bits 10b = 24 bits 11b = 32 bits
5-4	RX_SCFG[1:0]	RW	0h	TDM RX time slot select config. 00b = Mono with time slot equal to I2C address offset 01b = Mono left channel 10b = Mono right channel 11b = Stereo downmix (L+R)/2
3-2	RX_WLEN[1:0]	RW	2h	TDM RX word length. 00b = 16-bits 01b = 20-bits 10b = 24-bits 11b = 32-bits
1-0	RX_SLEN[1:0]	RW	2h	TDM RX time slot length. 00b = 16-bits 01b = 24-bits 10b = 32-bits 11b = Reserved

9.5.11 TDM_CFG3 (page=0x00 address=0x09) [reset=10h]

Sets TDM RX left and right time slots.

Figure 77. TDM_CFG3 Register Address: 0x09

7	6	5	4	3	2	1	0
RX_SLOT_R[3:0]				RX_SLOT_L[3:0]			
RW-1h				RW-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 100. TDM Configuration 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RX_SLOT_R[3:0]	RW	1h	TDM RX Right Channel Time Slot.
3-0	RX_SLOT_L[3:0]	RW	0h	TDM RX Left Channel Time Slot.

9.5.12 TDM_CFG4 (page=0x00 address=0x0A) [reset=13h]

Sets TDM TX bus keeper, fill, offset and transmit edge.

Figure 78. TDM_CFG4 Register Address: 0x0A

7	6	5	4	3	2	1	0
TX_KEEPCY	TX_KEEPLN	TX_KEEPEN	TX_FILL	TX_OFFSET[2:0]			TX_EDGE
RW-0h	RW-0h	RW-0h	RW-1h	RW-1h			RW-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 101. TDM Configuration 4 Field Descriptions

Bit	Field	Type	Reset	Description
7	TX_KEEPCY	RW	0h	TDM TX SDOUT LSB data will be driven for 0b = full-cycle 1b = half-cycle
6	TX_KEEPLN	RW	0h	TDM TX SDOUT will hold the bus for the following when TX_KEEPEN is enabled 0b = 1 LSB cycle 1b = always

Table 101. TDM Configuration 4 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TX_KEEPEN	RW	0h	TDM TX SDOUT bus keeper enable. 0b = Disable bus keeper 1b = Enable bus keeper
4	TX_FILL	RW	1h	TDM TX SDOUT unused bitfield fill. 0b = Transmit 0 1b = Transmit Hi-Z
3-1	TX_OFFSET[2:0]	RW	1h	TDM TX start of frame to time slot 0 offset.
0	TX_EDGE	RW	1h	TDM TX launch clock polarity. 0b = Rising edge of SBCLK 1b = Falling edge of SBCLK

9.5.13 TDM_CFG5 (page=0x00 address=0x0B) [reset=2h]

Sets TDM TX V-Sense time slot and enable.

Figure 79. TDM_CFG5 Register Address: 0x0B

7	6	5	4	3	2	1	0
Reserved	VSNS_TX	VSNS_SLOT[5:0]					
R-0h	RW-0h	RW-2h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 102. TDM Configuration 5 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	VSNS_TX	RW	0h	TDM TX voltage sense transmit enable. 0b = Disabled 1b = Enabled
5-0	VSNS_SLOT[5:0]	RW	2h	TDM TX voltage sense time slot.

9.5.14 TDM_CFG6 (page=0x00 address=0x0C) [reset=0h]

Sets TDM TX I-Sense time slot and enable.

Figure 80. TDM_CFG6 Register Address: 0x0C

7	6	5	4	3	2	1	0
Reserved	ISNS_TX	ISNS_SLOT[5:0]					
R-0h	RW-0h	RW-0h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 103. TDM Configuration 6 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	ISNS_TX	RW	0h	TDM TX current sense transmit enable. 0b = Disabled 1b = Enabled
5-0	ISNS_SLOT[5:0]	RW	0h	TDM TX current sense time slot.

9.5.15 TDM_CFG7 (page=0x00 address=0x0D) [reset=4h]

Sets TDM TX VBAT time slot and enable.

Figure 81. TDM_CFG7 Register Address: 0x0D

7	6	5	4	3	2	1	0
VBAT_SLEN	VBAT_TX	VBAT_SLOT[5:0]					
RW-0h	RW-0h	RW-4h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 104. TDM Configuration 7 Field Descriptions

Bit	Field	Type	Reset	Description
7	VBAT_SLEN	RW	0h	TDM TX VBAT time slot length. 0b = Truncate to 8-bits 1b = Left justify to 16-bits
6	VBAT_TX	RW	0h	TDM TX VBAT transmit enable. 0b = Disabled 1b = Enabled
5-0	VBAT_SLOT[5:0]	RW	4h	TDM TX VBAT time slot.

9.5.16 TDM_CFG8 (page=0x00 address=0x0E) [reset=5h]

Sets TDM TX temp time slot and enable.

Figure 82. TDM_CFG8 Register Address: 0x0E

7	6	5	4	3	2	1	0
Reserved	TEMP_TX	TEMP_SLOT[5:0]					
R-0h	RW-0h	RW-5h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 105. TDM Configuration 8 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	TEMP_TX	RW	0h	TDM TX temp sensor transmit enable. 0b = Disabled 1b = Enabled
5-0	TEMP_SLOT[5:0]	RW	5h	TDM TX temp sensor time slot.

9.5.17 TDM_CFG9 (page=0x00 address=0x0F) [reset=6h]

Sets ICLA bus, TDM TX limiter gain reduction time slot and enable.

Figure 83. TDM_CFG9 Register Address: 0x0F

7	6	5	4	3	2	1	0
Reserved	GAIN_TX	GAIN_SLOT[5:0]					
R-0h	RW-0h	RW-6h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 106. TDM Configuration 9 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	GAIN_TX	RW	0h	TDM TX limiter gain reduction transmit enable. 0b = Disabled 1b = Enabled
5-0	GAIN_SLOT[5:0]	RW	6h	TDM TX limiter gain reduction time slot.

9.5.18 TDM_CFG10 (page=0x00 address=0x10) [reset=7h]

Sets boost current limiter slot and enable

Figure 84. TDM_CFG10 Register Address: 0x10

7	6	5	4	3	2	1	0
BST_TX	BST_SYNC_TX	BST_SLOT[5:0]					
RW-0h	RW-0h	RW-7h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 107. TDM Configuration 10 Field Descriptions

Bit	Field	Type	Reset	Description
7	BST_TX	RW	0h	TDM TX boost current limiter enable. 0b = Disabled 1b = Enabled
6	BST_SYNC_TX	RW	0h	TDM TX boost clock sync enable. 0b = Disabled 1b = Enabled
5-0	BST_SLOT[5:0]	RW	7h	TDM TX boost sync and current limit time slot.

9.5.19 DSP Mode & TDM_DET (page=0x00 address=0x11) [reset=7Fh]

Readback of internal auto-rate detection.

Figure 85. DSP Mode & TDM_DET Register Address: 0x11

7	6	5	4	3	2	1	0
Reserved	FS_RATIO[3:0]				FS_RATE[2:0]		
R-0h	R-Fh				R-7h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 108. TDM Clock detection monitor Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6-3	FS_RATIO[3:0]	R	Fh	Detected SBCLK to FSYNC ratio. 00h = 16 01h = 24 02h = 32 03h = 48 04h = 64 05h = 96 06h = 128 07h = 192 08h = 256 09h = 384 0Ah = 512 0Bh-0Eh = Reserved 0F = Invalid ratio
2-0	FS_RATE[2:0]	R	7h	Detected sample rate of TDM bus. 000b = 7.35/8 KHz 001b = 14.7/16 KHz 010b = 22.05/24 KHz 011b = 29.4/32 KHz 100b = 44.1/48 KHz 101b = 88.2/96 kHz 110b = 176.4/192 kHz 111b = Error condition

9.5.20 LIM_CFG0 (page=0x00 address=0x12) [reset=12h]

Sets Limiter attack step size, attack rate and enable.

Figure 86. LIM_CFG0 Register Address: 0x12

7	6	5	4	3	2	1	0
Reserved	VBAT_LIM_TH_SELECTION	LIMB_ATK_ST[1:0]		LIMB_ATK_RT[2:0]			LIMB_EN
R-0h	RW-0h	RW-1h		RW-1h			RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 109. Limiter Configuration 0 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	VBAT_LIM_TH_SELECTION	RW	0h	Select source of threshold for VBAT based limiting 0b = User configured Thresholds 1b = PVDD based thresholds
5-4	LIMB_ATK_ST[1:0]	RW	1h	VBAT Limiter attack step size. 00b = 0.25 dB 01b = 0.5 dB 10b = 1 dB 11b = 2 dB
3-1	LIMB_ATK_RT[2:0]	RW	1h	VBAT Limiter attack rate. 000b = 1 step in 1 sample 001b = 1 step in 2 samples 010b = 1 step in 4 samples 011b = 1 step in 8 samples 100b = 1 step in 16 samples 101b = 1 step in 32 samples 110b = 1 step in 64 samples 111b = 1 step in 128 samples
0	LIMB_EN	RW	0h	Limiter enable. 0b = Disabled 1b = Enabled

9.5.21 LIM_CFG1 (page=0x00 address=0x13) [reset=76h]

Sets VBAT limiter release step size, release rate and hold time.

Figure 87. LIM_CFG1 Register Address: 0x13

7	6	5	4	3	2	1	0
LIMB_RLS_ST[1:0]		LIMB_RLS_RT[2:0]			LIMB_HLD_TM[2:0]		
RW-1h		RW-6h			RW-6h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 110. Limiter Configuration 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LIMB_RLS_ST[1:0]	RW	1h	VBAT Limiter/BOP/ICLA release step size. 00b = 0.25 dB 01b = 0.5 dB 10b = 1 dB 11b = 2 dB
5-3	LIMB_RLS_RT[2:0]	RW	6h	VBAT Limiter/BOP/ICLA release rate. 000b = 1 step in 10 ms 001b = 1 step in 20 ms 010b = 1 step in 40 ms 011b = 1 step in 80 ms 100b = 1 step in 160 ms 101b = 1 step in 320 ms 110b = 1 step in 640 ms 111b = 1 step in 1280 ms

Table 110. Limiter Configuration 1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	LIMB_HLD_TM[2:0]	RW	6h	VBAT Limiter hold time. 000b = 0 ms 001b = 10 ms 010b = 25 ms 011b = 50 ms 100b = 100 ms 101b = 250 ms 110b = 500 ms 111b = 1000 ms

9.5.22 DSP FREQUENCY & BOP_CFG0 (page=0x00 address=0x14) [reset=1h]

Sets BOP infinite hold clear, infinite hold enable, mute on brown out and enable.

Figure 88. DSP FREQUENCY & BOP_CFG0 Register Address: 0x14

7	6	5	4	3	2	1	0
Reserved			BOSD_EN	BOP_HLD_CLR	BOP_INF_HLD	BOP_MUTE	BOP_EN
R-0h			RW-0h	RW-0h	RW-0h	RW-0h	RW-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 111. Brown Out Prevention 0 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R	0h	Reserved
4	BOSD_EN	RW	0h	Brown out prevention enable. 0b = Disabled 1b = Enabled
3	BOP_HLD_CLR	RW	0h	BOP infinite hold clear (self clearing). 0b = Don't clear 1b = Clear
2	BOP_INF_HLD	RW	0h	Infinite hold on brown out event. 0b = Use BOP_HLD_TM after brown out event 1b = Don't release until BOP_HLD_CLR is asserted high
1	BOP_MUTE	RW	0h	Mute on brown out event. 0b = Don't mute 1b = Mute followed by device shutdown
0	BOP_EN	RW	1h	Brown out prevention enable. 0b = Disabled 1b = Enabled

9.5.23 BOP_CFG0 (page=0x00 address=0x15) [reset=2Eh]

BOP attack rate, attack step size and hold time.

Figure 89. BOP_CFG0 Register Address: 0x15

7	6	5	4	3	2	1	0
BOP_ATK_RT[2:0]			BOP_ATK_ST[1:0]		BOP_HLD_TM[2:0]		
RW-1h			RW-1h		RW-6h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 112. Brown Out Prevention 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	BOP_ATK_RT[2:0]	RW	1h	Brown out prevention attack rate. 000b = 1 step in 1 sample 001b = 1 step in 2 samples 010b = 1 step in 4 samples 011b = 1 step in 8 samples 100b = 1 step in 16 samples 101b = 1 step in 32 samples 110b = 1 step in 64 samples 111b = 1 step in 128 samples
4-3	BOP_ATK_ST[1:0]	RW	1h	Brown out prevention attack step size. 00b = 0.5 dB 01b = 1 dB 10b = 1.5 dB 11b = 2 dB
2-0	BOP_HLD_TM[2:0]	RW	6h	Brown out prevention hold time. 000b = 0 ms 001b = 10 ms 010b = 25 ms 011b = 50 ms 100b = 100 ms 101b = 250 ms 110b = 500 ms 111b = 1000 ms

9.5.24 BIL_and_ICLA_CFG0 (page=0x00 address=0x16) [reset=60h]

Boost Current limiter and ICLA

Figure 90. BIL_and_ICLA_CFG0 Register Address: 0x16

7	6	5	4	3	2	1	0
Reserved	BIL_HLD_TM[2:0]			Reserved			
R-0h	RW-6h			R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 113. Boost Current limiter and ICLA Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6-4	BIL_HLD_TM[2:0]	RW	6h	VBAT current limiter hold time 000b = 0 ms 001b = 10 ms 010b = 25 ms 011b = 50 ms 100b = 100 ms 101b = 250 ms 110b = 500 ms 111b = 1000 ms
3-0	Reserved	R	0h	Reserved

9.5.25 BIL_ICLA_CFG1 (page=0x00 address=0x17) [reset=0h]

ICLA starting time slot and enable.

Figure 91. BIL_ICLA_CFG1 Register Address: 0x17

7	6	5	4	3	2	1	0
Reserved							
RW-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 114. Inter Chip Limiter Alignment 0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	RW	0h	Reserved

9.5.26 GAIN_ICLA_CFG0 (page=0x00 address=0x18) [reset=0h]

ICLA starting time slot and enable.

Figure 92. GAIN_ICLA_CFG0 Register Address: 0x18

7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 115. Inter Chip Limiter Alignment 0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R	0h	Reserved

9.5.27 ICLA_CFG1 (page=0x00 address=0x19) [reset=0h]

ICLA time slot enables.

Figure 93. ICLA_CFG1 Register Address: 0x19

7	6	5	4	3	2	1	0
Reserved							
RW-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 116. Inter Chip Limiter Alignment 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	RW	0h	Reserved

9.5.28 INT_MASK0 (page=0x00 address=0x1A) [reset=FCh]

Interrupt masks.

Figure 94. INT_MASK0 Register Address: 0x1A

7	6	5	4	3	2	1	0
INT_MASK0[7]	INT_MASK0[6]	INT_MASK0[5]	INT_MASK0[4]	INT_MASK0[3]	INT_MASK0[2]	INT_MASK0[1]	INT_MASK0[0]
RW-1h	RW-1h	RW-1h	RW-1h	RW-1h	RW-1h	RW-0h	RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 117. Interrupt Mask 0 Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK0[7]	RW	1h	Limiter mute mask. 0b = Don't Mask 1b = Mask
6	INT_MASK0[6]	RW	1h	Limiter infinite hold mask. 0b = Don't Mask 1b = Mask
5	INT_MASK0[5]	RW	1h	Limiter max attenuation mask. 0b = Don't Mask 1b = Mask

Table 117. Interrupt Mask 0 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	INT_MASK0[4]	RW	1h	VBAT below limiter inflection point mask. 0b = Don't Mask 1b = Mask
3	INT_MASK0[3]	RW	1h	Limiter active mask. 0b = Don't Mask 1b = Mask
2	INT_MASK0[2]	RW	1h	TDM clock error mask. 0b = Don't Mask 1b = Mask
1	INT_MASK0[1]	RW	0h	Over current error mask. 0b = Don't Mask 1b = Mask
0	INT_MASK0[0]	RW	0h	Over temp error mask. 0b = Don't Mask 1b = Mask

9.5.29 INT_MASK1 (page=0x00 address=0x1B) [reset=A6h]

Interrupt masks.

Figure 95. INT_MASK1 Register Address: 0x1B

7	6	5	4	3	2	1	0
Reserved	Reserved	INT_MASK1[5]	INT_MASK1[4:3][1:0]		INT_MASK1[2]	INT_MASK1[1]	INT_MASK1[0]
RW-1h	RW-0h	RW-1h	RW-0h		RW-1h	RW-1h	RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 118. Interrupt Mask 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	1h	Reserved
6	Reserved	RW	0h	Reserved
5	INT_MASK1[5]	RW	1h	Load Diagnostic Completion Mask 0b = Don't Mask 1b = Masked
4-3	INT_MASK1[4:3]	RW	0h	Speaker open load mask 00b = Don't Mask 01b = Mask open Load detection 10b = Mask Short Load detection 11b = Mask both Open,Short Load detection
2	INT_MASK1[2]	RW	1h	Brownout device power down start mask 0b = Don't Mask 1b = Mask
1	INT_MASK1[1]	RW	1h	Brownout Protection Active mask 0b = Don't Mask 1b = Mask
0	INT_MASK1[0]	RW	0h	VBAT Brown out detected mask 0b = Don't Mask 1b = Mask

9.5.30 INT_MASK2 (page=0x00 address=0x1C) [reset=DFh]

Interrupt masks.

Figure 96. INT_MASK2 Register Address: 0x1C

7	6	5	4	3	2	1	0
INT_MASK2[7]	INT_MASK2[6]	INT_MASK2[5]	INT_MASK2[4]	INT_MASK2[3]	INT_MASK2[2]	INT_MASK2[1]	INT_MASK2[0]
RW-1h	RW-1h	RW-0h	RW-1h	RW-1h	RW-1h	RW-1h	RW-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 119. Interrupt Mask 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK2[7]	RW	1h	DAC MOD clock error mask 0b = Don't Mask 1b = Mask
6	INT_MASK2[6]	RW	1h	Boost Clock Error mask 0b = Don't Mask 1b = Mask
5	INT_MASK2[5]	RW	0h	VBAT POR mask 0b = Don't Mask 1b = Mask
4	INT_MASK2[4]	RW	1h	PLL Lock interrupt mask 0b = Don't Mask 1b = Mask
3	INT_MASK2[3]	RW	1h	DC DETECT mask 0b = Don't Mask 1b = Mask
2	INT_MASK2[2]	RW	1h	BOOST OV Clamp interrupt mask 0b = Don't Mask 1b = Mask
1	INT_MASK2[1]	RW	1h	CP PG mask 0b = Don't Mask 1b = Mask
0	INT_MASK2[0]	RW	1h	Device power up intp mask 0b = Don't Mask 1b = Mask

9.5.31 INT_MASK3 (page=0x00 address=0x1D) [reset=FFh]

Interrupt masks.

Figure 97. INT_MASK3 Register Address: 0x1D

7	6	5	4	3	2	1	0
INT_MASK3[7]	Reserved	Reserved	INT_MASK3[4]	INT_MASK3[3]	Reserved	Reserved	Reserved
RW-1h	RW-1h	RW-1h	RW-1h	RW-1h	RW-1h	RW-1h	RW-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 120. Interrupt Mask 3 Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK3[7]	RW	1h	Device power down intp mask 0b = Don't Mask 1b = Mask
6	Reserved	RW	1h	Reserved
5	Reserved	RW	1h	Reserved
4	INT_MASK3[4]	RW	1h	PDM mic clock error intp mask 0b = Don't Mask 1b = Mask
3	INT_MASK3[3]	RW	1h	ASI2 clock error intp mask 0b = Don't Mask 1b = Mask
2	Reserved	RW	1h	Reserved
1	Reserved	RW	1h	Reserved
0	Reserved	RW	1h	Reserved

9.5.32 INT_LIVE0 (page=0x00 address=0x1F) [reset=0h]

Live interrupt readback.

Figure 98. INT_LIVE0 Register Address: 0x1F

7	6	5	4	3	2	1	0
INT_LIVE0[7]	INT_LIVE0[6]	INT_LIVE0[5]	INT_LIVE0[4]	INT_LIVE0[3]	INT_LIVE0[2]	INT_LIVE0[1]	INT_LIVE0[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 121. Live Interrupt Readback 0 Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE0[7]	R	0h	Interrupt due to limiter mute. 0b = No interrupt 1b = Interrupt
6	INT_LIVE0[6]	R	0h	Interrupt due to limiter infinite hold. 0b = No interrupt 1b = Interrupt
5	INT_LIVE0[5]	R	0h	Interrupt due to limiter max attenuation. 0b = No interrupt 1b = Interrupt
4	INT_LIVE0[4]	R	0h	Interrupt due to VBAT below limiter inflection point. 0b = No interrupt 1b = Interrupt
3	INT_LIVE0[3]	R	0h	Interrupt due to limiter active. 0b = No interrupt 1b = Interrupt
2	INT_LIVE0[2]	R	0h	Interrupt due to TDM clock error. 0b = No interrupt 1b = Interrupt
1	INT_LIVE0[1]	R	0h	Interrupt due to over current error. 0b = No interrupt 1b = Interrupt
0	INT_LIVE0[0]	R	0h	Interrupt due to over temp error. 0b = No interrupt 1b = Interrupt

9.5.33 INT_LIVE1 (page=0x00 address=0x20) [reset=0h]

Live interrupt readback.

Figure 99. INT_LIVE1 Register Address: 0x20

7	6	5	4	3	2	1	0
Reserved	Reserved	INT_LIVE1[5]	INT_LIVE1[4]	INT_LIVE1[3]	INT_LIVE1[2]	INT_LIVE1[1]	INT_LIVE1[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 122. Live Interrupt Readback 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	Reserved	R	0h	Reserved
5	INT_LIVE1[5]	R	0h	Reserved
4	INT_LIVE1[4]	R	0h	Reserved
3	INT_LIVE1[3]	R	0h	Reserved
2	INT_LIVE1[2]	R	0h	Reserved
1	INT_LIVE1[1]	R	0h	Brownout Protection Active flag 0b = No interrupt 1b = Interrupt
0	INT_LIVE1[0]	R	0h	Interrupt due to VBAT brown out detected flag. 0b = No interrupt 1b = Interrupt

9.5.34 INT_LIVE3 (page=0x00 address=0x21) [reset=0h]

Live interrupt readback.

Figure 100. INT_LIVE3 Register Address: 0x21

7	6	5	4	3	2	1	0
INT_LIVE2[7]	INT_LIVE2[6]	INT_LIVE2[5]	INT_LIVE2[4]	INT_LIVE2[3]	INT_LIVE2[2]	INT_LIVE2[1]	INT_LIVE2[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 123. Live Interrupt Readback 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE2[7]	R	0h	DAC MOD clock error flag 0b = No interrupt 1b = Interrupt
6	INT_LIVE2[6]	R	0h	Boost Clock error flag 0b = No interrupt 1b = Interrupt
5	INT_LIVE2[5]	R	0h	VBAT_POR flag 0b = No interrupt 1b = Interrupt
4	INT_LIVE2[4]	R	0h	PLL LOCK flag 0b = No interrupt 1b = Interrupt
3	INT_LIVE2[3]	R	0h	DC DETECT flag 0b = No interrupt 1b = Interrupt
2	INT_LIVE2[2]	R	0h	BOOST OV Clamp flag 0b = No interrupt 1b = Interrupt
1	INT_LIVE2[1]	R	0h	CP PG flag 0b = No interrupt 1b = Interrupt
0	INT_LIVE2[0]	R	0h	Device powe up flag 0b = No interrupt 1b = Interrupt

9.5.35 INT_LIVE4 (page=0x00 address=0x22) [reset=0h]

Live interrupt readback.

Figure 101. INT_LIVE4 Register Address: 0x22

7	6	5	4	3	2	1	0
INT_LIVE3[7]	Reserved	Reserved	INT_LIVE3[4]	INT_LIVE3[3]	Reserved	Reserved	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 124. Live Interrupt Readback 3 Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE3[7]	R	0h	Device powe down flag 0b = No interrupt 1b = Interrupt
6	Reserved	R	0h	Reserved
5	Reserved	R	0h	Reserved
4	INT_LIVE3[4]	R	0h	PDM mic clock error flag 0b = No interrupt 1b = Interrupt

Table 124. Live Interrupt Readback 3 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INT_LIVE3[3]	R	0h	ASI2 clock error flag 0b = No interrupt 1b = Interrupt
2	Reserved	R	0h	Reserved
1	Reserved	R	0h	Reserved
0	Reserved	R	0h	Reserved

9.5.36 INT_LTCH0 (page=0x00 address=0x24) [reset=0h]

Latched interrupt readback.

Figure 102. INT_LTCH0 Register Address: 0x24

7	6	5	4	3	2	1	0
INT_LTCH0[7]	INT_LTCH0[6]	INT_LTCH0[5]	INT_LTCH0[4]	INT_LTCH0[3]	INT_LTCH0[2]	INT_LTCH0[1]	INT_LTCH0[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 125. Latched Interrupt Readback 0 Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH0[7]	R	0h	Interrupt due to limiter mute (cleared using CLR_INTP_LTCH). 0b = No interrupt 1b = Interrupt
6	INT_LTCH0[6]	R	0h	Interrupt due to limiter infinite hold (cleared using CLR_INTP_LTCH). 0b = No interrupt 1b = Interrupt
5	INT_LTCH0[5]	R	0h	Interrupt due to limiter max attenuation (cleared using CLR_INTP_LTCH). 0b = No interrupt 1b = Interrupt
4	INT_LTCH0[4]	R	0h	Interrupt due to VBAT below limiter inflection point (cleared using CLR_INTP_LTCH). 0b = No interrupt 1b = Interrupt
3	INT_LTCH0[3]	R	0h	Interrupt due to limiter active (cleared using CLR_INTP_LTCH). 0b = No interrupt 1b = Interrupt
2	INT_LTCH0[2]	R	0h	Interrupt due to TDM clock error (cleared using CLR_INTP_LTCH). 0b = No interrupt 1b = Interrupt
1	INT_LTCH0[1]	R	0h	Interrupt due to over current error (cleared using CLR_INTP_LTCH). 0b = No interrupt 1b = Interrupt
0	INT_LTCH0[0]	R	0h	Interrupt due to over temp error (cleared using CLR_INTP_LTCH). 0b = No interrupt 1b = Interrupt

9.5.37 INT_LTCH1 (page=0x00 address=0x25) [reset=0h]

Latched interrupt readback.

Figure 103. INT_LTCH1 Register Address: 0x25

7	6	5	4	3	2	1	0
Reserved	Reserved	INT_LTCH1[5]	INT_LTCH1[4:3][1:0]		INT_LTCH1[2]	INT_LTCH1[1]	INT_LTCH1[0]
R-0h	R-0h	R-0h	R-0h		R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 126. Latched Interrupt Readback 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	Reserved	R	0h	Reserved
5	INT_LTCH1[5]	R	0h	Interrupt due to Load Diagnostic Mode Completion(cleared using CLR_INTP_LTCH). 0b = Load Diagnostic Mode Not completed 1b = Load Diagnostic Mode Completed
4-3	INT_LTCH1[4:3]	R	0h	Interrupt due to Load Diagnostic Mode Fault Status(cleared using CLR_INTP_LTCH). 00b = Normal Load 01b = Open Load Detected 10b = Short Load Detected 11b = Reserved
2	INT_LTCH1[2]	R	0h	Interrupt due to Brownout Protection Triggered shutdown (cleared using CLR_INTP_LTCH) 0b = No interrupt 1b = Interrupt
1	INT_LTCH1[1]	R	0h	Interrupt due to Brownout Protection Active flag (cleared using CLR_INTP_LTCH) 0b = No interrupt 1b = Interrupt
0	INT_LTCH1[0]	R	0h	Interrupt due to VBAT brown out detected flag (cleared using CLR_INTP_LTCH). 0b = No interrupt 1b = Interrupt

9.5.38 INT_LTCH3 (page=0x00 address=0x26) [reset=0h]

Latched interrupt readback.

Figure 104. INT_LTCH3 Register Address: 0x26

7	6	5	4	3	2	1	0
INT_LTCH2[7]	INT_LTCH2[6]	INT_LTCH2[5]	INT_LTCH2[4]	INT_LTCH2[3]	INT_LTCH2[2]	INT_LTCH2[1]	INT_LTCH2[0]
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 127. Latched Interrupt Readback 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH2[7]	R	0h	Interrupt due to DAC MOD clock error (cleared using CLR_INTP_LTCH) 0b = No interrupt 1b = Interrupt
6	INT_LTCH2[6]	R	0h	Interrupt due to Boost Clock error (cleared using CLR_INTP_LTCH) 0b = No interrupt 1b = Interrupt
5	INT_LTCH2[5]	R	0h	Interrupt due to VBAT_POR (cleared using CLR_INTP_LTCH) 0b = No interrupt 1b = Interrupt
4	INT_LTCH2[4]	R	0h	Interrupt due to PLL LOCK (cleared using CLR_INTP_LTCH) 0b = No interrupt 1b = Interrupt

Table 127. Latched Interrupt Readback 2 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INT_LTCH2[3]	R	0h	Interrupt due to DC DETECT (cleared using CLR_INTP_LTCH) 0b = No interrupt 1b = Interrupt
2	INT_LTCH2[2]	R	0h	Interrupt due to BOOST OV Clamp (cleared using CLR_INTP_LTCH) 0b = No interrupt 1b = Interrupt
1	INT_LTCH2[1]	R	0h	Interrupt due to CP PG(cleared using CLR_INTP_LTCH) 0b = No interrupt 1b = Interrupt
0	INT_LTCH2[0]	R	0h	Interrupt due to DEVICE POWER UP(cleared using CLR_INTP_LTCH) 0b = No interrupt 1b = Interrupt

9.5.39 INT_LTCH4 (page=0x00 address=0x27) [reset=0h]

Latched interrupt readback.

Figure 105. INT_LTCH4 Register Address: 0x27

7	6	5	4	3	2	1	0
INT_LTCH3[7]	Reserved	Reserved	INT_LTCH3[4]	INT_LTCH3[3]	Reserved	Reserved	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 128. Latched Interrupt Readback 3 Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH3[7]	R	0h	Interrupt due to DEVICE POWER DOWN(cleared using CLR_INTP_LTCH) 0b = No interrupt 1b = Interrupt
6	Reserved	R	0h	Reserved
5	Reserved	R	0h	Reserved
4	INT_LTCH3[4]	R	0h	Interrupt due to PDM mic clock error(cleared using CLR_INTP_LTCH) 0b = No interrupt 1b = Interrupt
3	INT_LTCH3[3]	R	0h	Interrupt due to ASI2 clock error (cleared using CLR_INTP_LTCH). 0b = No interrupt 1b = Interrupt
2	Reserved	R	0h	Reserved
1	Reserved	R	0h	Reserved
0	Reserved	R	0h	Reserved

9.5.40 VBAT_MSB (page=0x00 address=0x2A) [reset=0h]

MSBs of SAR ADC VBAT conversion.

Figure 106. VBAT_MSB Register Address: 0x2A

7	6	5	4	3	2	1	0
VBAT_CNV[9:2]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 129. SAR ADC Conversion 0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VBAT_CNV[9:2]	R	0h	Returns SAR ADC VBAT conversion MSBs.

9.5.41 VBAT_LSB (page=0x00 address=0x2B) [reset=0h]

LSBs of SAR ADC VBAT conversion.

Figure 107. VBAT_LSB Register Address: 0x2B

7	6	5	4	3	2	1	0
VBAT_CNV[1:0]		Reserved					
R-0h		R-0h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 130. SAR ADC Conversion 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VBAT_CNV[1:0]	R	0h	Returns SAR ADC VBAT conversion LSBs.
5-0	Reserved	R	0h	Reserved

9.5.42 TEMP (page=0x00 address=0x2C) [reset=0h]

SARD ADC Temp conversion.

Figure 108. TEMP Register Address: 0x2C

7	6	5	4	3	2	1	0
TMP_CNV[7:0]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 131. SAR ADC Conversion 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TMP_CNV[7:0]	R	0h	Returns SAR ADC temp sensor conversion.

9.5.43 INT & CLK CFG (page=0x00 address=0x30) [reset=19h]

Figure 109. INT & CLK CFG Register Address: 0x30

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved			CLR_INTP_LTCH	IRQZ_PIN_CFG[1:0]	
RW-0h	RW-0h	RW-3h			RW-0h	RW-1h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 132. Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	0h	Reserved
6	Reserved	RW	0h	Reserved
5-3	Reserved	RW	3h	Reserved
2	CLR_INTP_LTCH	RW	0h	Clear INT_LTCH registers to clear interrupts (self clearing bit) 0b = Don't clear 1b = Clear INT_LTCH registers

Table 132. Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	IRQZ_PIN_CFG[1:0]	RW	1h	IRQZ interrupt configuration. 00b = IRQZ will assert on any unmasked live interrupts 01b = IRQZ will assert on any unmasked latched interrupts 10b = IRQZ will assert for 2-4ms one time on any unmasked live interrupt event 11b = IRQZ will assert for 2-4ms every 4ms on any unmasked latched interrupts

9.5.44 DIN_PD (page=0x00 address=0x31) [reset=40h]

Sets enables of input pin weak pull down.

Figure 110. DIN_PD Register Address: 0x31

7	6	5	4	3	2	1	0
DIN_PD[7]	Reserved	DIN_PD[5]	DIN_PD[4]	DIN_PD[3]	DIN_PD[2]	DIN_PD[1]	DIN_PD[0]
RW-0h	RW-1h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 133. Digital Input Pin Pull Down Field Descriptions

Bit	Field	Type	Reset	Description
7	DIN_PD[7]	RW	0h	Weak pull down for SBCLK2 0b = Disabled 1b = Enabled
6	Reserved	RW	1h	Reserved
5	DIN_PD[5]	RW	0h	Weak pull down for SPII2CZ_MISO 0b = Disabled 1b = Enabled
4	DIN_PD[4]	RW	0h	Weak pull down for ADDR_SPICLK 0b = Disabled 1b = Enabled
3	DIN_PD[3]	RW	0h	Weak pull down for SDOUT 0b = Disabled 1b = Enabled
2	DIN_PD[2]	RW	0h	Weak pull down for SDIN. 0b = Disabled 1b = Enabled
1	DIN_PD[1]	RW	0h	Weak pull down for FSYNC. 0b = Disabled 1b = Enabled
0	DIN_PD[0]	RW	0h	Weak pull down for SBCLK. 0b = Disabled 1b = Enabled

9.5.45 MISC (page=0x00 address=0x32) [reset=80h]

Set IRQZ pin active state

Figure 111. MISC Register Address: 0x32

7	6	5	4	3	2	1	0
IRQZ_POL	Reserved			Reserved		Reserved	Reserved
RW-1h	RW-0h			R-0h		RW-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 134. Misc Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7	IRQZ_POL	RW	1h	IRQZ pin polarity for interrupt. 0b = Active high (IRQ) 1b = Active low (IRQZ)
6-4	Reserved	RW	0h	Reserved
3-2	Reserved	R	0h	Reserved
1	Reserved	RW	0h	Reserved
0	Reserved	R	0h	Reserved

9.5.46 BOOST_CFG1 (page=0x00 address=0x33) [reset=34h]

Boost Configure 1

Figure 112. BOOST_CFG1 Register Address: 0x33

7	6	5	4	3	2	1	0
BST_MODE	BST_MODE	BST_EN	Reserved		BST_PFML[1:0]		BST_DYNAMIC_ILIM_EN
RW-0h	RW-0h	RW-1h	RW-2h		RW-2h		RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 135. Boost Configure 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	BST_MODE	RW	0h	Boost Mode
6	BST_MODE	RW	0h	Boost Mode 00b = Class-H 01b = Class-G 10b = Boost always ON 11b = Boost always OFF(Passthrough)
5	BST_EN	RW	1h	Boost enable 0b = Disabled 1b = Enabled
4-3	Reserved	RW	2h	Reserved
2-1	BST_PFML[1:0]	RW	2h	Boost active mode PFM lower limit 00b = No lower limit 01b = 25 kHz 10b = 50 kHz 11b = 100 kHz
0	BST_DYNAMIC_ILIM_EN	RW	0h	Dynamic Current Limiter based on VBAT 0b = Disabled 1b = Enabled

9.5.47 BOOST_CFG2 (page=0x00 address=0x34) [reset=4Bh]

Boost Configure 2

Figure 113. BOOST_CFG2 Register Address: 0x34

7	6	5	4	3	2	1	0
BST_IR[1:0]		BST_SYNC	BST_PA	BST_VREG[3:0]			
RW-1h		RW-0h	RW-0h	RW-Bh			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 136. Boost Configure 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BST_IR[1:0]	RW	1h	Boost inductor range 00b = less than 0.6 uH 01b = 0.6 uH to 1.3 uH 10b = 1.3 uH to 2.5 uH 11b = Reserved
5	BST_SYNC	RW	0h	Boost sync to clock 0b = Not synced 1b = Synced
4	BST_PA	RW	0h	Boost sync phase 0b = 0 deg 1b = 180 deg
3-0	BST_VREG[3:0]	RW	Bh	Boost Maximum Voltage(Default 11 V) 0000b = Reserved 0001b = 6 V 0010b = 6.5 V .... 1110b = 12.5 V 1111b = Reserved

9.5.48 BOOST_CFG3 (page=0x00 address=0x35) [reset=74h]

Boost Configure 3

Figure 114. BOOST_CFG3 Register Address: 0x35

7	6	5	4	3	2	1	0
BST_CLASSH_STEP_TIME[3:0]				BST_LR[1:0]		Reserved	Reserved
RW-7h				RW-1h		RW-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 137. Boost Configure 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BST_CLASSH_STEP_TIME[3:0]	RW	7h	Step Time for Boost if in Class-H mode 0000b = 9us 0001b = 18us 0010b = 36us 0011b = 54us 0100b = 72us 0101b = 90us 0110b = 108us 0111b = 135us 1000b = 162us 1001b = 198us 1010b = 252us 1011b = 342us 1100b = 477us 1101b = 612us 1110b = 792us 1111b = 990us
3-2	BST_LR[1:0]	RW	1h	Slope of boost load regulation. 00b = Reserved 01b = 3A/V; load regulation = 1V (default) 10b = 2A/V; load regulation = 1.5V 11b = Reserved
1	Reserved	RW	0h	Reserved
0	Reserved	R	0h	Reserved

9.5.49 MISC (page=0x00 address=0x3B) [reset=58h]

Figure 115. MISC Register Address: 0x3B

7	6	5	4	3	2	1	0
HAPTIC_EN	Reserved		Reserved		Reserved	Reserved	
RW-0h	RW-2h		RW-3h		RW-0h	RW-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 138. Field Descriptions

Bit	Field	Type	Reset	Description
7	HAPTIC_EN	RW	0h	Haptics mode is 0b = Disabled 1b = Enabled
6-5	Reserved	RW	2h	Reserved
4-3	Reserved	RW	3h	Reserved
2	Reserved	RW	0h	Reserved
1-0	Reserved	RW	0h	Reserved

9.5.50 TG_CFG0 (page=0x00 address=0x3F) [reset=0h]

Tone Generator

Figure 116. TG_CFG0 Register Address: 0x3F

7	6	5	4	3	2	1	0
TG1_EN[1:0]		TG1_PINEN[1:0]		Reserved			
RW-0h		RW-0h		R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 139. Tone Generator Field Descriptions

Bit	Field	Type	Reset	Description
7-6	TG1_EN[1:0]	RW	0h	Tone Generator 1 is 00b = Disabled or pin triggered 01b = Enabled - play tone 10b = audio level enabled 11b = reserved
5-4	TG1_PINEN[1:0]	RW	0h	Tone pin trigger 00b = Disabled 01b = SDIN 10b = GPIO 11b = AD1
3-0	Reserved	R	0h	Reserved

9.5.51 BST_ILIM_CFG0 (page=0x00 address=0x40) [reset=36h]

Boost ILIM configuration-0

Figure 117. BST_ILIM_CFG0 Register Address: 0x40

7	6	5	4	3	2	1	0
BST_SSL[7:6]		BST_ILIM[5:0]					
RW-0h		RW-36h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 140. Boost ILIM configuration-0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BST_SSL[7:0]	RW	0h	Boost peak current limit 00h = 0.99 A 01h = 1.045 A 02h = 1.1 A ... 36h = 3.96 A 37h = 4 A 38h-3Fh = Reserved

9.5.52 PDM_CONFIG0 (page=0x00 address=0x41) [reset=1h]

Figure 118. PDM_CONFIG0 Register Address: 0x41

7	6	5	4	3	2	1	0
Reserved	PDM_GATE_PAD0[6:6]	PDM_RATE_PAD0[5:5]	DIS_PDM_MIC_CLK_ERR_PAD0[4:4]	PDM_PAD0_CAP_EDGE[3:3]	PDM_MIC2_EN[2:2]	PDM_MIC1_EN[1:1]	PDM_MIC_SLV
R-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-0h	RW-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 141. Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R	0h	device in PDM MIC SLAVE or MASTER 0b=Device is in PDM MIC master mode 1b=Device is in PDM Slave mode

9.5.53 DIN_PD & PDM_CONFIG3 (page=0x00 address=0x42) [reset=F8h]

Figure 119. DIN_PD & PDM_CONFIG3 Register Address: 0x42

7	6	5	4	3	2	1	0
DIN_PD[14][7:7]	DIN_PD[13][6:6]	Reserved	wk_pulldown_pdmd_pad0[4:4]	wk_pulldown_pdmck_pad0[3:3]	Reserved		
RW-1h	RW-1h	R-1h	RW-1h	RW-1h	R-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 142. Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIN_PD[14]	RW	1h	Reserved

9.5.54 ASI2_CONFIG0 (page=0x00 address=0x43) [reset=8h]

Figure 120. ASI2_CONFIG0 Register Address: 0x43

7	6	5	4	3	2	1	0
tx_fill_asi2[7:7]	asi2_sbclk_fs_ratio[6:3]				Reserved		
RW-0h	RW-1h				R-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 143. Field Descriptions

Bit	Field	Type	Reset	Description
7-0	tx_fill_asi2[7:0]	RW	0h	Reserved

9.5.55 ASI2_CONFIG1 (page=0x00 address=0x44) [reset=0h]

Figure 121. ASI2_CONFIG1 Register Address: 0x44

7	6	5	4	3	2	1	0
asi2_auto_rate[7:7]	asi2_tx_lsb_half_cycle_reg[6:6]	rx_edge_asi2[5:5]	tx_edge_asi2[4:4]	Reserved			asi2_sbclk_master
RW-0h	RW-0h	RW-0h	RW-0h	R-0h			RW-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 144. Field Descriptions

Bit	Field	Type	Reset	Description
7-0	asi2_auto_rate[7:0]	RW	0h	ASI2 SBCLK master mode enable 0b = SBCLK2 in slave mode 1b = SBCLK2 in master mode

9.5.56 ASI2_CONFIG2 (page=0x00 address=0x45) [reset=1h]

Figure 122. ASI2_CONFIG2 Register Address: 0x45

7	6	5	4	3	2	1	0
tx_offset_asi2[7:5]			rx_offset_asi2[4:0]				
RW-0h			RW-1h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 145. Field Descriptions

Bit	Field	Type	Reset	Description
7-0	tx_offset_asi2[7:0]	RW	0h	TDM2 RX start of frame to time slot 0 offset (ASI2_SBCLK cycles)

9.5.57 ASI2_CONFIG3 (page=0x00 address=0x46) [reset=FCh]

Figure 123. ASI2_CONFIG3 Register Address: 0x46

7	6	5	4	3	2	1	0
Reserved	asi2_tx_keeper[6:6]	asi2_sdout_buskeeper_always_en[5:5]	num_slots[4:4]	num_devices[3:2]		my_device_num[1:0]	
R-1h	RW-1h	RW-1h	RW-1h	RW-3h		RW-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 146. Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R	1h	My device number on the common BUS 00b = 1st 01b = 2nd 10b = 3rd 11b = 4th

9.5.58 PVDD_MSB_DSP (page=0x00 address=0x49) [reset=0h]

MSBs of SAR ADC PVDD conversion.

Figure 124. PVDD_MSB_DSP Register Address: 0x49

7	6	5	4	3	2	1	0
PVDD_CNV_DSP[9:2]							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 147. SAR ADC Conversion 0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PVDD_CNV_DSP[9:2]	R	0h	Returns SAR ADC PVDD conversion MSBs.

9.5.59 PVDD_LSB_DSP (page=0x00 address=0x4A) [reset=0h]

LSBs of SAR ADC PVDD conversion.

Figure 125. PVDD_LSB_DSP Register Address: 0x4A

7	6	5	4	3	2	1	0
PVDD_CNV_DSP[1:0]		Reserved					
R-0h		R-0h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 148. SAR ADC Conversion 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PVDD_CNV_DSP[1:0]	R	0h	Returns SAR ADC PVDD conversion LSBs.
5-0	Reserved	R	0h	Reserved

9.5.60 REV_ID (page=0x00 address=0x7D) [reset=0h]

Returns REV and PG ID.

Figure 126. REV_ID Register Address: 0x7D

7	6	5	4	3	2	1	0
REV_ID[3:0]				PG_ID[3:0]			
R-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 149. Revision and PG ID Field Descriptions

Bit	Field	Type	Reset	Description
7-4	REV_ID[3:0]	R	0h	Returns the revision ID.
3-0	PG_ID[3:0]	R	0h	Returns the PG ID.

9.5.61 I2C_CKSUM (page=0x00 address=0x7E) [reset=0h]

Returns I2C checksum.

Figure 127. I2C_CKSUM Register Address: 0x7E

7	6	5	4	3	2	1	0
I2C_CKSUM[7:0]							
RW-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 150. I2C Checksum Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2C_CKSUM[7:0]	RW	0h	Returns I2C checksum. Writing to this register will reset the checksum to the written value. This register is updated on writes to other registers on all books and pages.

9.5.62 BOOK (page=0x00 address=0x7F) [reset=0h]

Device's memory map is divided into pages and books. This register sets the book.

Figure 128. BOOK Register Address: 0x7F

7	6	5	4	3	2	1	0
BOOK[7:0]							
RW-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 151. Device Book Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BOOK[7:0]	RW	0h	Sets the device book. 00h = Book 0 01h = Book 1 ... FFh = Book 255

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TAS2563 is a digital input high efficiency Class-D audio power amplifier with advanced battery current management and an integrated Class-H boost converter. In auto passthrough mode, the Class-H boost converter generates the Class-D amplifier supply rail. During low Class-D output power, the boost improves efficiency by deactivating and connecting VBAT directly to the Class-D amplifier supply. When high power audio is required, the boost quickly activates to provide louder audio than a stand-alone amplifier connected directly to the battery. To enable load monitoring, the TAS2563 constantly measures the current and voltage across the load and provides a digital stream of this information back to a processor. It is recommended to configure the TAS2563 using PurePath™ Console 3 Software.

10.2 Typical Application

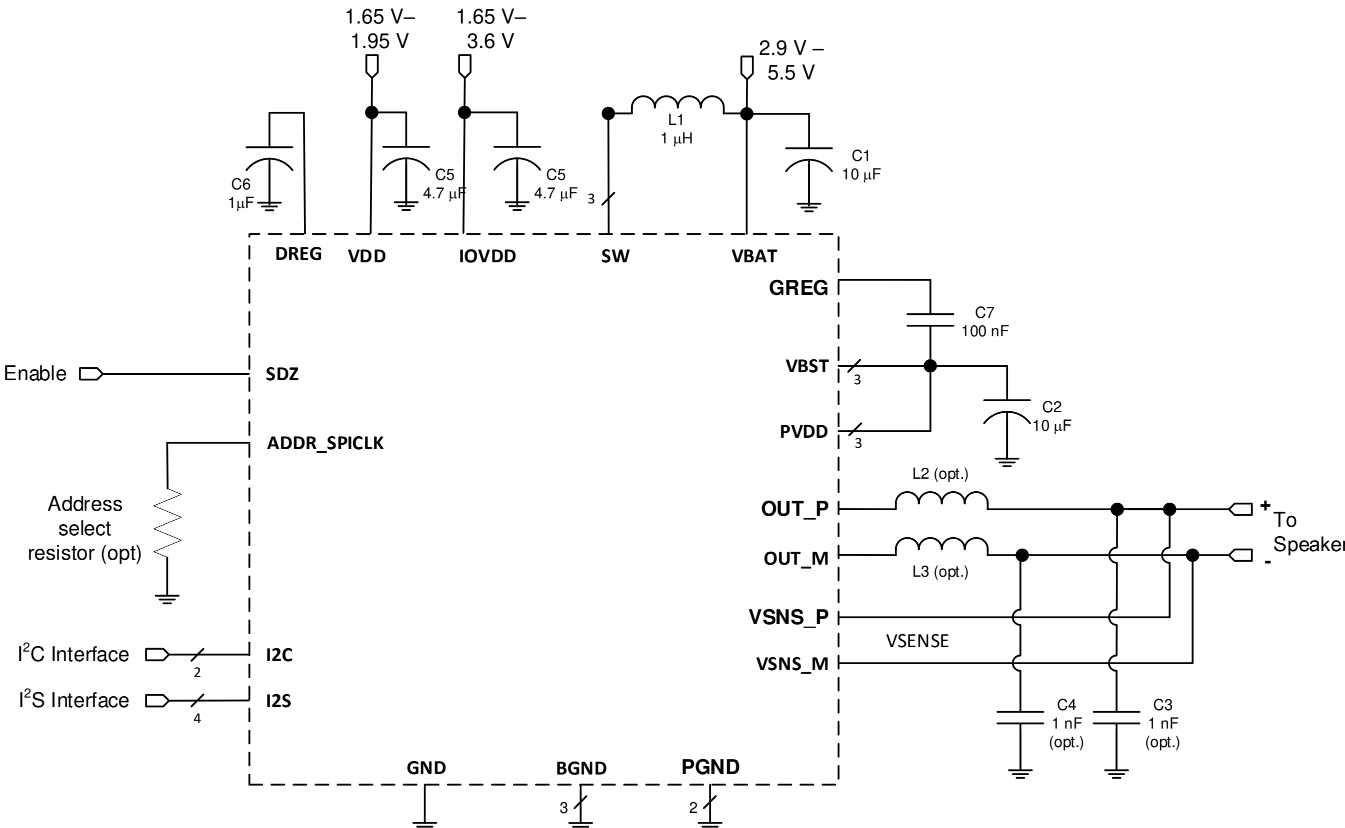


Figure 129. Typical Application - Digital Audio Input

Typical Application (continued)

Table 152. Recommended External Components

COMPONENT	DESCRIPTION	SPECIFICATION	MIN	TYP	MAX	UNIT
L1	Boost Converter Inductor(1)	Inductance, 20% Tolerance	0.47	1		µH
		Saturation Current		4.5		A
L2, L3	EMI Filter Inductors (optional). These are not recommended as it degrades THD+N performance. TAS2563 is a filter-less Class-D and does not require these bead inductors.	Impedance at 100 MHz		120		Ω
		DC Resistance			0.095	Ω
		DC Current			2	A
		Size		0402		EIA
C1	Boost Converter Input Capacitor(1)	Capacitance, 20% Tolerance	10			µF
C2	Boost Converter Output Capacitor	Type	X5R			
		Capacitance, 20% Tolerance	10		47	µF
		Rated Voltage	16			V
		Capacitance at 11.5 V derating	3.3			µF
C3, C4	EMI Filter Capacitors (optional, must use L2, L3 if C3, C4 used)	Capacitance		1		nF
C5	VDD Decoupling Capacitor	Capacitance	4.7			µF
C6	DREG Decoupling Capacitor	Capacitance	1			µF
C6	GREG Fly Capacitor	Capacitance	100			nF

(1) See section Boost Converter Passive Devices for additional requirements on derating, stability, and inductor value trade-offs.

10.2.1 Design Requirements

For this design example, use the parameters shown in Table 153.

Table 153. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Audio Input	Digital Audio, I^2S
Current and Voltage Data Stream	Digital Audio, I^2S
Mono or Stereo Configuration	Mono
Max Output Power at 1% THD+N	5.0 W

10.2.2 Detailed Design Procedure

10.2.2.1 Mono/Stereo Configuration

In this application, the device is assumed to be operating in mono mode. See Device Mode and Address Selection for information on changing the I^2C address of the TAS2563 to support stereo operation. Mono or stereo configuration does not impact the device performance.

10.2.2.2 Boost Converter Passive Devices

The boost converter requires three passive devices that are labeled L1, C1 and C2 in and whose specifications are provided in Table 152. These specifications are based on the design of the TAS2563 and are necessary to meet the performance targets of the device. In particular, L1 should not be allowed to enter in the current saturation region. The saturation current for L1 should be > ILIM to deliver Class-D peak power.

Additionally, the ratio of L1/C2 (the derated value of C2 at 11.5 V should be used in this ratio) has to be lesser than 1/3 for boost stability. This 1/3 ratio should be maintained including the worst case variation of L1 and C2. To satisfy sufficient energy transfer, L1 needs to be ≥ 0.47 µH at the boost switching frequency (100 kHz to 4 MHz). Using a 0.47µH will have more boost ripple than a 1.0µH or 2.2 µH but the high PSRR should minimize the effect from the additional ripple. Finally, the minimum C2 (derated value at programmed boost voltage) should be > 3.3 µF for Class-D power delivery specification.

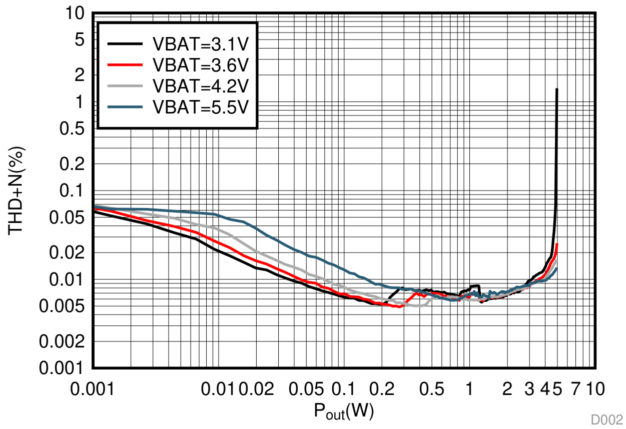
10.2.2.3 EMI Passive Devices

The TAS2563 supports edge-rate control to minimize EMI, but the system designer may want to include passive devices on the Class-D output devices. These passive devices that are labeled L2, L3, C3 and C4 in and their recommended specifications are provided in Table 152. If C3 and C4 are used, L2 and L3 must also be installed, and C3 and C4 must be placed after L2 and L3 respectively to maintain the stability of the output stage.

10.2.2.4 Miscellaneous Passive Devices

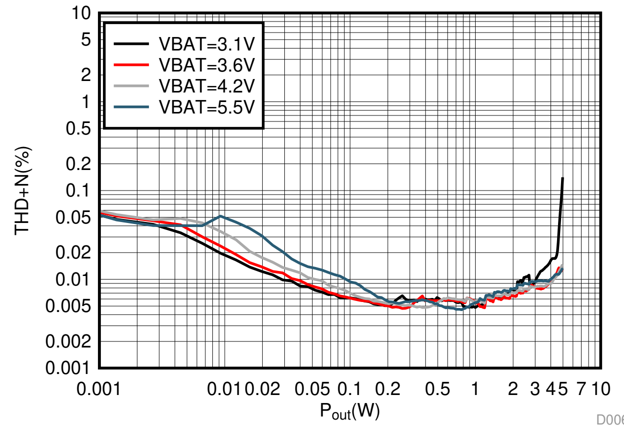
The GREG Capacitor requires 100 nF to meet boost and Class-D power delivery and efficiency specs. For best device performance, the GREG capacitor should be placed very close to the device and be routed with wide traces to minimize the impact of PCB parasitic effects.

10.2.3 Application Curves



RL = 4 Ω F_{IN} = 1 kHz

Figure 130. THD+N vs Output Power



F_{IN} = 20 Hz – 20 kHz P_{OUT} = 0.1 W   RL = 8 Ω

Figure 131. THD+N vs Frequency

11 Power Supply Recommendations

11.1 Power Supplies

The TAS2563 requires four power supplies:

- Boost Input (terminal: VBAT)
  - Voltage: 2.9 V to 5.5 V
  - Max Current: 5 A for ILIM = 4.0 A (default)
- Analog Supply (terminal: VDD)
  - Voltage: 1.65 V to 1.95 V
  - Max Current: 30 mA
- IO Supply (terminal: IOVDD)
  - Voltage: 1.65 V to 3.6 V
  - Max Current: 30 mA

The decoupling capacitors for the power supplies should be placed close to the device terminals.

11.2 Power Supply Sequencing

The power rail may be brought up and down in any order. There is no requirement on sequencing. However if VDD is present without VBAT an additional rise in VDD current will be observed until VBAT is present.

When the supplies have settled, the SDZ terminal can be set HIGH to operate the device. Additionally the SDZ pin can be tied to VDD and the internal POR will perform a reset of the device. After a hardware or software reset additional commands to the device should be delayed for 100uS to allow the OTP to load. The above sequence should be completed before any I^2C operation.

11.2.1 Boost Supply Details

The boost supply (VBAT) and associated passives need to be able to support the current requirements of the device. By default, the peak current limit of the boost is set to 4A. Refer to for information on changing the current limit. A minimum of a 10 µF capacitor is recommended on the boost supply to quickly support changes in required current. Refer to for the schematic.

The current requirements can also be reduced by lowering the gain of the amplifier, or in response to decreasing battery through the use of the battery-tracking feature of the TAS2563 described in Supply Tracking Limiters with Brown Out Prevention.

11.2.2 External Boost Mode (Boost Bypass Mode)

Its is very important that during external boost mode, VBAT and SW should be hard shorted on board.

12 Layout

12.1 Layout Guidelines

- Place the boost inductor between VBAT and SW close to device terminals with no VIAS between the device terminals and the inductor.
- Place the capacitor between VBST close to device terminals with no VIAS between the device terminals and capacitor.
- Place the capacitor between VBST/VBAT and GND close to device terminals with no VIAS between the device terminals and capacitor.
- Do not use VIAS for traces that carry high current. These include the traces for VBST, SW, VBAT, PGND and the speaker OUT_P, OUT_M.
- Use epoxy filled vias for the interior pads.
- Connect VSNS_P, VSNS_N as close as possible to the speaker.
  - VSNS_P, VSNS_N should be connected between the EMI ferrite and the speaker if EMI ferrites are used on OUT_P, OUT_M.
  - EMI ferrites must be used if EMI capacitors are used on OUT_P, OUT_M.
- Use a ground plane with multiple vias for each terminal to create a low-impedance connection to GND for minimum ground noise.
- Use supply decoupling capacitors as shown in and described in Power Supplies.
- Place EMI ferrites, if used, close to the device.

Table 154. Pin Layout Guidelines

PIN	MAX PARASITIC INDUCTANCE	LAYOUT RECOMMENDATIONS
BGND, GND, PGND, GNDD	150pH	Short BGND, GND, GNDD, PGDN below the package and connect them to PCB ground plane strongly through multiple vias. Minimize inductance as much as possible
DREG	500 pH	Bypass to GND with capacitor recommended in Table 152. Do not connect to external load. Both ends of decoupling cap should see as low inductance as possible between this pin and gnd pins.
GREG	200pH	Connect it to PVDD with a star connection and not to boost plane with recommended in Table 152. Do not connect to external load.
PVDD	100pH	Short it to VBST(boost) plane through strong conneciton. Connect it to GREG with a star connection and not to boost plane.
SW		Connect to VBAT with boost inductor recommended in Table 152. Reduce parasitic capacitor and resistance for efficiency. Boost inductor should be as close as possible to the SW pin. Inductor should be connected to SW through thick plane. Traces should support currents up to device over-current limit.
VBAT	500pH	Bypass to GND with capacitor recommended in Table 152. Should be connected to inductor through thick plane. Both ends of decoupling capacitor should see as low inductance as possible between VBAT pin and PGND pin.
VBST	100pH	Do not connect to external load. Bypass to GND with capacitor recommended in Table 152. Connect to PVDD through thick plane. Both ends of decoupling capacitor should see as low inductance as possible between VBST pin and BGND pin. Traces should support currents up to device over-current limit.
VDD	200pH	Bypass to GND with capacitor recommended in Table 152. Both the end of decoupling cap should see as low inductance as possible between this pin and GND pin

12.2 Layout Example

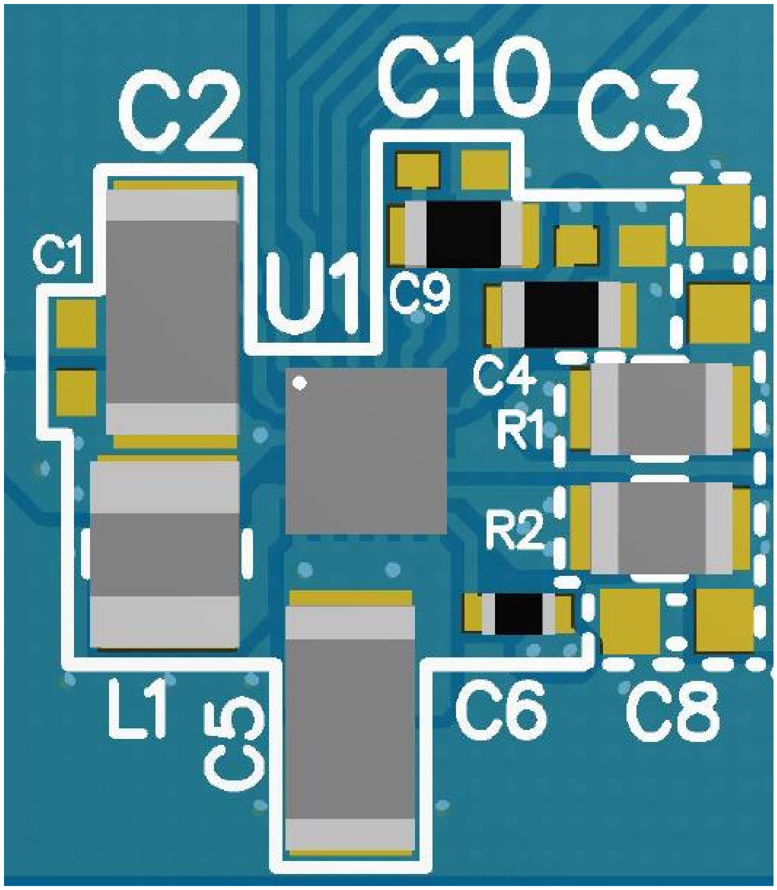


Figure 132. TAS2563 Board Layout

Layout Example (continued)

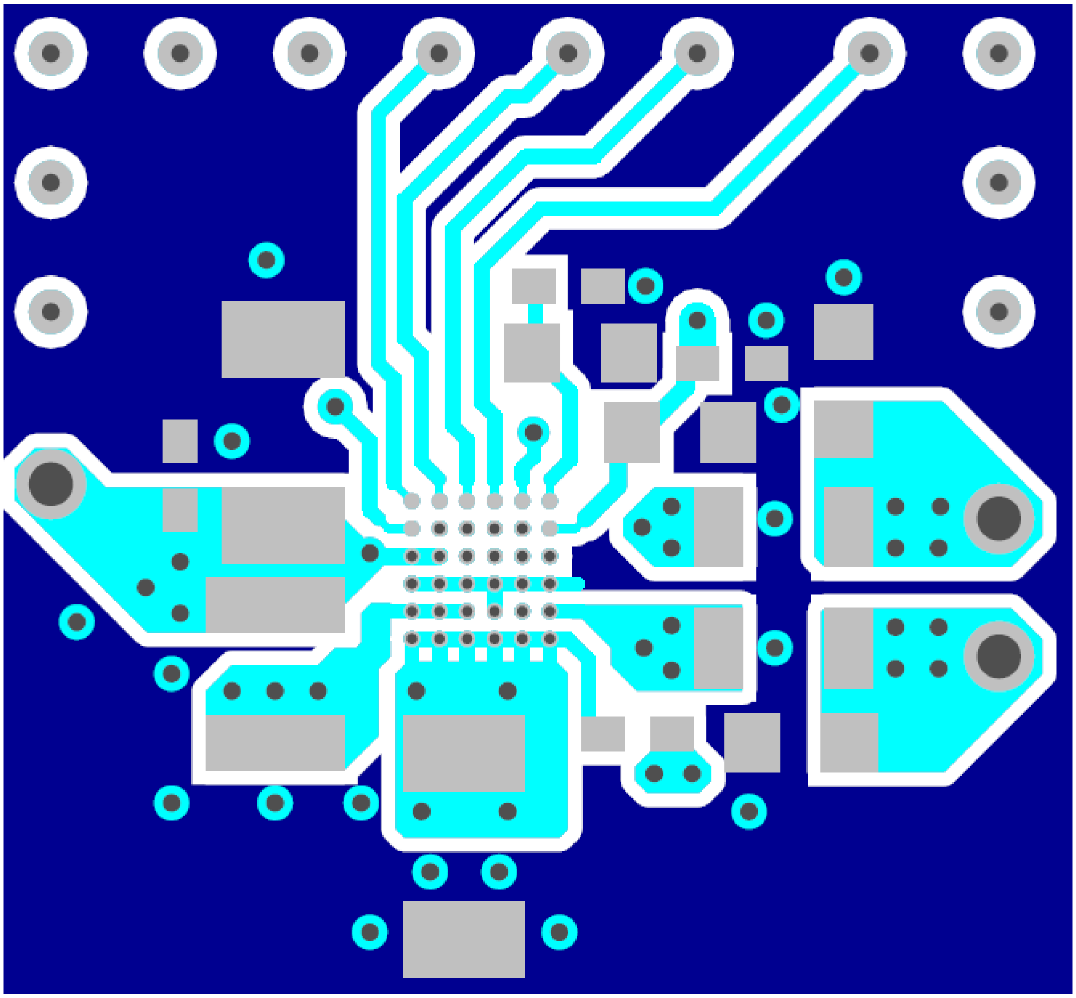


Figure 133. TAS2563 Top Copper Layout

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following: *TAS2563YBGEVM-DC Evaluation module user's guide*

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

PurePath, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

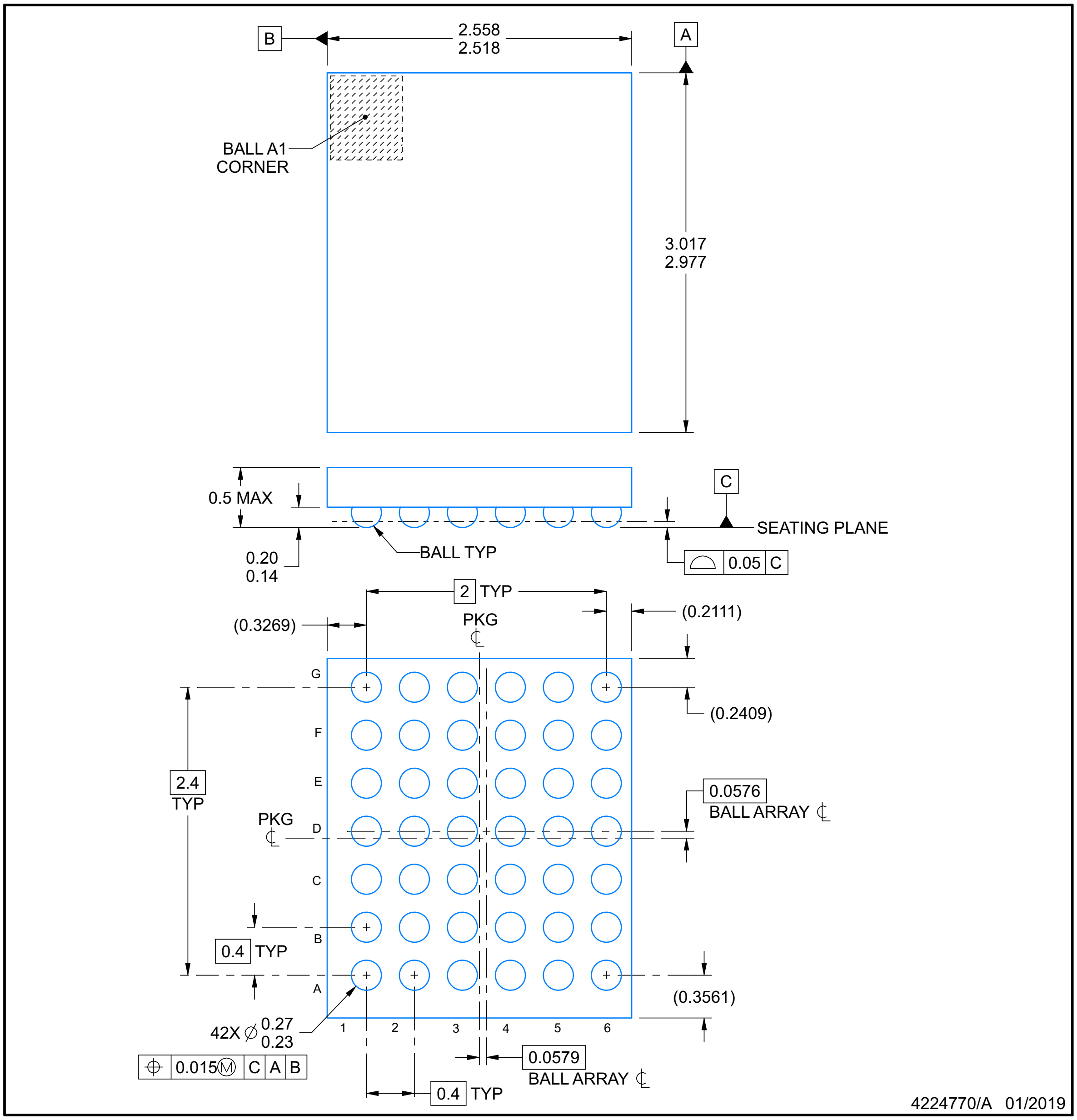
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAS2563YBG
YBG0042-C01

PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

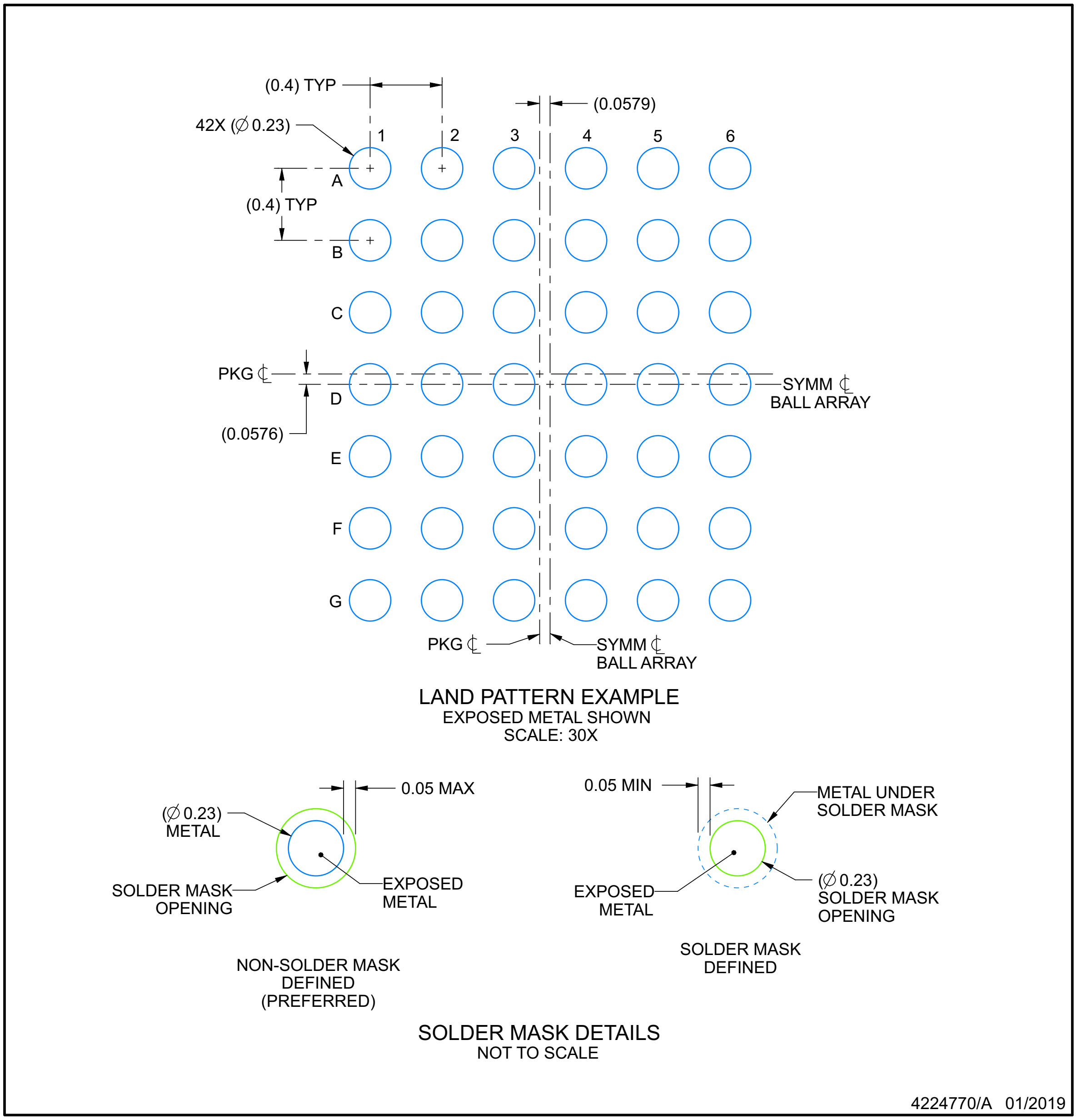
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

TAS2563YBG
YBG0042-C01

EXAMPLE BOARD LAYOUT

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

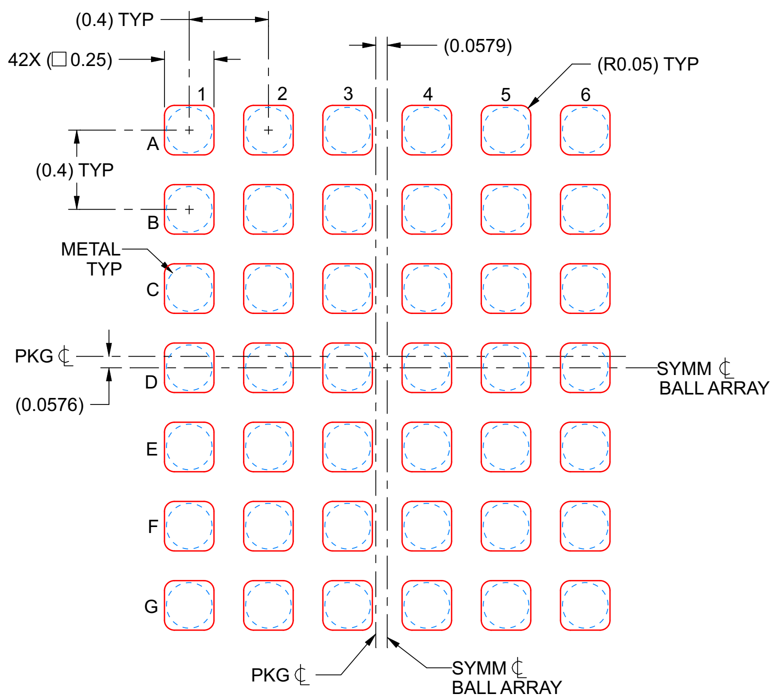
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

TAS2563YBG
YBG0042-C01

EXAMPLE STENCIL DESIGN

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4224770/A 01/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS2563YBGR	ACTIVE	DSBGA	YBG	42	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TAS2-DSA	Samples
TAS2563YBGT	ACTIVE	DSBGA	YBG	42	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TAS2-DSA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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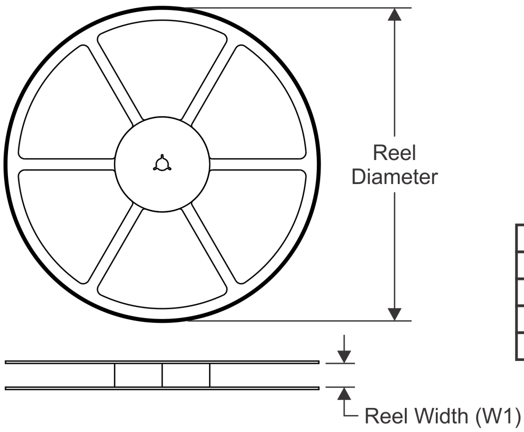
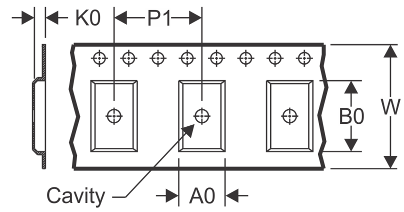
TAPE AND REEL INFORMATION

REEL DIMENSIONS

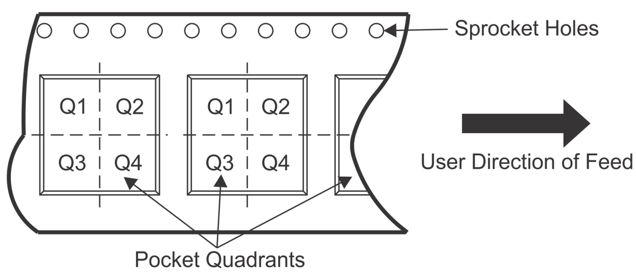


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

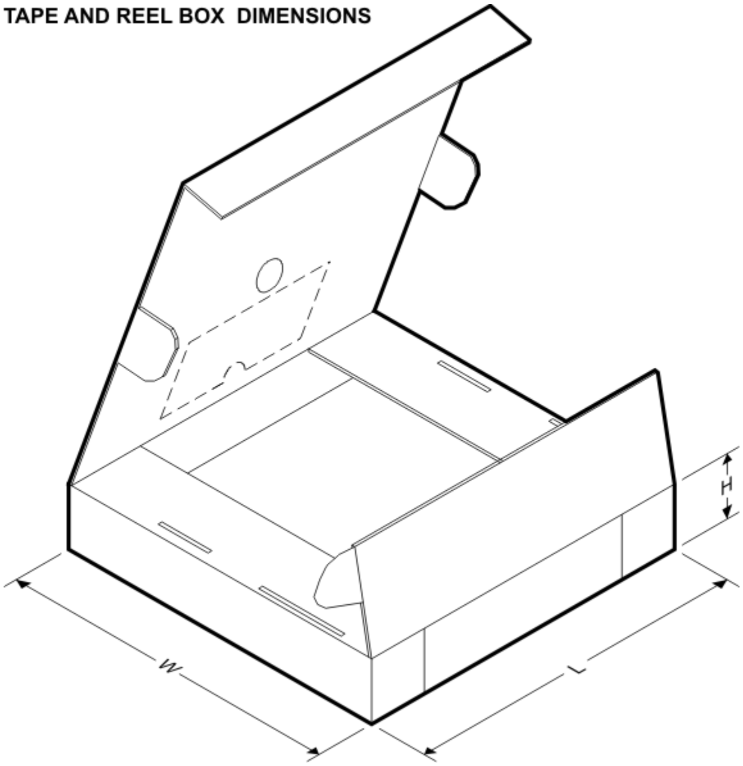
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS2563YBGR	DSBGA	YBG	42	3000	330.0	12.4	2.71	3.17	0.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS2563YBGR	DSBGA	YBG	42	3000	367.0	367.0	35.0