Application Report
SNAA021A–May 2004–Revised June 2004

AN-1192 Overture™ Series High Power Solutions

ABSTRACT

This application report discusses the different aspects of the Overture series high-power solutions, and discusses three application circuits: parallel, bridged, and bridged/parallel configurations.

Contents

List of Figures

List of Tables

1 Introduction

Texas Instruments has a broad portfolio of monolithic power integrated circuits covering power levels from a few hundred milliwatts up to 60W of non-clipped continuous average power. These ICs cover most audio applications by themselves, however, for really high power applications, other methods need to be employed because IC packages have limited power dissipation capabilities.

There are many different ways of obtaining over 100W of output power. Most high-end power amplifier manufacturers utilize discrete circuits which allows them to market their amplifiers as “specially designed.” However, there is a price to be paid for discrete amplifier designs; they are complex, difficult to design, require many components, lack the comprehensive protection mechanisms of integrated circuits and are not as reliable.

Other methods of obtaining output power greater than 100W include the use of power ICs as drivers for discrete power transistors. There are a number of these types of circuits, but they too possess all of the same flaws as discrete circuits, including a lack of comprehensive output stage protection.

2 Objective

The objective is to provide simple high-power solutions that are conservatively designed, highly reliable and have low part count. This document provides three specific, but not unique, application circuits that provide output power of 100W, 200W, and above. These circuits are the parallel, bridged, and bridged/parallel configurations.

These three circuits are simple to understand, simple to build and require very few external components compared to discrete power amplifier designs. Simplicity of design and few components make this solution much more reliable than discrete amplifiers. In addition, these circuits inherently possess the full protection of each individual IC that is very difficult and time consuming to design discretely. Finally, these circuits are well known and have been in industry for years.

3 Conclusion

The BR100 (100W Bridged Circuit), PA100 (100W parallel circuit), and the BPA200 (200W Bridged/Parallel Circuit) are high power solutions that can be used in many applications, but they are primarily targeted for home theater amplifier applications such as powered subwoofers, self-powered speakers, and surround sound amplifiers.

While bridged amplifier configurations are able to provide high power levels, they also consume four times more power than a conventional single-ended solution. However, it is feasible to conservatively design a 100W bridged amplifier solution, as will be shown here. The bridged solution is designed to drive an 8Ω nominal load for self-powered speaker or powered subwoofer applications.

The parallel amplifier is another configuration that can be used to obtain higher output power levels by combining two IC outputs and doubling output current drive capability. The parallel topology provides a great way of achieving higher power levels while keeping within IC power dissipation limits by driving low impedance loads, which is the case for many self-powered speaker and powered subwoofer designs. The main advantage of the parallel configuration is its ability to divide total power dissipation between ICs, since each amplifier is providing half of the load current. Another advantage of the parallel design is that unlike the bridge design, more than two ICs can be used. In fact, any number of ICs can be used in a parallel design and when configured the same will share the power dissipation equally. For example, using four ICs to drive a 1Ω load means that each IC dissipates 1/4 of the total power dissipation. In other words, the load to each IC looks like a 4Ω load (Number Of ICs in Parallel * Load Impedance = Load Impedance seen by each individual IC.) Odd numbers of ICs can also be used.

For lower impedance loads (<8Ω), the parallel circuit is a good solution for 100W power levels using just two devices. Power levels above 100W may be obtained by using more than two devices to increase output current capability and power dissipation limits along with lower impedance loads.

If the bridged and parallel configurations are combined, the outcome is a very high power amplifier solution that far exceeds the capabilities of one IC alone, while maintaining reasonable power dissipation levels within each IC. The bridged portion doubles the output voltage swing and quadruples the total power dissipation while the parallel portion halves the current between each IC set and divides the total power dissipation between each of the four ICs. The result is higher system output power with each IC not exceeding its individual power dissipation capabilities. Higher output power levels are attained, while the ICs run at a normal temperature, keeping long term reliability high. The schematic of the Bridged/Parallel Amplifier is shown in Figure 13.

The bridged/parallel circuit using four devices will produce the maximum output power (>200W) into loads with an impedance from 4Ω to 8Ω. For loads less than 4Ω, additional devices may need to be placed in parallel or the supply voltage reduced.

The data in the following sections will exemplify that the parallel, bridged, and bridged/parallel solutions using multiple power ICs can meet high fidelity specifications while providing output power from 100W up to 400W. The low noise and excellent linearity traits of the monolithic IC are transferred to the hig- power solution, making the circuit even more attractive. In addition, the protection mechanisms within the IC, which are not easily designed discretely, are inherently designed into the circuit.

While the data show what specs can be achieved by the configurations, as always, good design practices need to be followed to achieve the stated results. In addition to good electrical and layout design practices, the thermal design is equally critical with Overture™ ICs. The following section will expand on the thermal design aspects of Overture™ ICs. This concept of “design by power dissipation” is applicable to all types of high power solutions.

The PA100, BR100, and BPA200 schematics and test results exemplify what can be achieved with proper component selection, thermal design, and layout techniques.

4 Thermal Background

The voltage and current ratings of a power semiconductor are typically the first specs considered in designing high power amplifiers. The same is true for an integrated monolithic power amplifier. However, power dissipation ratings are equally important to the long term reliability of the power amplifier design. When using a monolithic IC in its intended application and within its specified capabilities, the thermal design is relatively straightforward. When an IC is used beyond is capabilities, as in high power circuits, power dissipation issues become more critical and not as straight-forward. Therefore, the designer must understand the IC's power dissipation capabilities before using the IC in a booster configuration.

4.1 Typical Characteristic Data

The power dissipation capabilities of a power IC are either specified in the datasheet or can be derived from its guaranteed output power specification. While the power dissipation rating for the LM3886T is 125W, this number can be misleading. Its power dissipation specification is derived from the IC's junction-to-case thermal resistance, θ_{JC} = 1°C/W, the maximum junction temperature, T_J = 150°C, and the ambient air, T_A = 25°C. As stated in the datasheet, the device must be derated based on these parameters while operating at elevated temperatures. The heat sinking requirements for the application are based on these parameters so that the IC will not go into Thermal Shutdown (TSD). The real problem for Overture™ ICs, however, comes from the sensitivity of the output stage's unique SPiKe™ Protection which dynamically monitors the output transistor's temperature. While the thermal shutdown circuitry is enabled at T_J = 150°C, SPiKe™ circuitry is enabled at T_J = 250°C for instantaneous power spikes in the output stage transistor. As the overall temperature of the IC increases, SPiKe™ circuitry becomes even more sensitive causing it to turn on before the 125W limit is reached. TSD circuitry will continue to function globally for the IC in conjunction with the SPiKe™ circuitry. However, protection circuitry should not be activated under normal operating conditions. The question then becomes, what is the power dissipation limit for the IC such that SPiKe™ circuitry is not enabled? Knowing the power dissipation limit and keeping the case temperature of the IC as cool as possible will expand the output power capability without activating SPiKe™ Protection.

The other way to determine IC power dissipation capabilities is to analyze the output power specification in the datasheet. In the case of the LM3886T, there are two output power specification guarantees: 60W (min) into a 4Ω load using ±28V supplies and 50W(typ) into an 8Ω load from ±35V supplies. Using these two conditions and the theoretical maximum power dissipation equation shown below, results in the following maximum power dissipations:

4.2 Single-ended Amplifier Pdmax Equation:

$$Pdmax = V_{CCtot}^2/2\pi^2R_L \quad (1)$$

Non-Isolated LM3886T:

1. $V_{CC} = \pm 28V$, $R_L = 4\Omega$ (2)

$$Pdmax = V_{CCtot}^2/2\pi^2R_L = (\pm 28V)^2/2\pi^2(4\Omega) = 39.7W \quad (3)$$

2. $V_{CC} = \pm 35V$, $R_L = 8\Omega$ (4)

$$Pdmax = V_{CCtot}^2/2\pi^2R_L = (\pm 35V)^2/2\pi^2(8\Omega) = 31.0W \quad (5)$$

These results show that the IC can handle a maximum of ≈ 40W of continuous power dissipation without SPiKe™ Protection being turned on under continuous sinusoidal input with proper heat sinking. The same theory applies to other Overture™ ICs as well, like the LM3876T, which is capable of dissipating 31W with proper heat sinking. It should be noted that the results shown above are for the non-isolated power package, where the back of the package is tied to the silicon substrate, or −Vee. The isolated power package has overmolded plastic on the back keeping the package electrically isolated from the silicon substrate. This extra amount of plastic increases the package thermal resistance from 1°C/W for the non-isolated version to ≈ 2°C/W for the isolated version. The result of increased thermal resistance is higher die temperature under the same conditions even though the heat sink temperature will not change.

There are two major points to note:

1. The maximum power dissipation analysis was taken into account using regulated power supplies. The IC for the whole analysis is being tested at the worst case power dissipation point for a constant full-load power supply voltage. When using an unregulated power supply, the no-load voltage will be somewhat higher (15%–35%) causing the overall maximum power dissipation to be higher than expected.
2. In the real “audio” application, the average music power dissipation is much less than the maximum power dissipation created by a sinusoidal input. Therefore, the IC will run cooler than expected due to the lower power dissipation.

However, when you put these two points together, they mostly cancel out, but only for music stimulus. Product qualifications may go through worse case power dissipation scenarios which implies that sinusoids will be used with unregulated power supplies. Therefore, when doing the thermal portion of the design, the higher supply voltages will increase the IC power dissipation and must be taken into account.

4.3 Bridged-output Amplifier Pdmax Equation

To determine the Pdmax equation for a bridged amplifier solution, the single-ended Pdmax equation is used as a starting point. A bridged amplifier solution requires two amplifiers and each amplifier will see 1/2 the total impedance. Adding these factors of 2 and 1/2 into the single-ended Pdmax equation results in the total Pdmax equation for a bridged amplifier.

$$Pdmax_{BTL} = 2*[V_{CCtot}^2/2\pi^2(/½R_L)] = 4*(V_{CCtot}^2/2\pi^2R_L) \quad (6)$$

The bridged-output Pdmax equation represents the bridged amplifier solution. If a dual amplifier IC is used, then the total Pdmax would need to be dissipated in the single IC package. However, if two individual ICs are used, then the total power dissipation is divided between each IC.

Two Non-Isolated LM3886Ts:

$$V_{CC} = \pm 28V,\ R_L = 4\Omega \tag{7}$$

$$Pdmax = 4V_{CCtot}{}^2/2\pi^2R_L = 4(\pm 28V)^2/2\pi^2(4\Omega) = 158.8W \tag{8}$$

$$Pdmax = 158.8W \tag{9}$$

$$Pdmax/IC = 79.4W \tag{10}$$

Therefore, using a bridged configuration, V_{cc} would have to be equal to ±20V to keep the IC's power dissipation within 40W/IC when driving a 4Ω load! This equates to about 110W of output power in bridged-mode driving a 4Ω load. When driving an 8Ω load, and using the same bridged pdmax equation and a maximum of 40W/IC of power dissipation, the supply voltages would have to be ±28V. This equates to about 120W of output power.

4.4 Parallel Amplifier Pdmax Equation

To determine the Pdmax equation for a parallel amplifier solution the single-ended Pdmax equation is used as a starting point. Since a parallel solution has the load connected the same as single-ended solution (one side to GND) just more devices driving the load, the equation does not change for total Pdmax.

$$Pdmax_{PA} = V_{CCtot}{}^2/2\pi^2R_L \tag{11}$$

The advantage of the parallel solution is total Pdmax is divided equally among each of the amplifiers in the parallel solution. By dividing up the total power dissipation among two or more ICs, lower impedance loads can be driven for much higher power solutions. National's Overture power amplifier series amplifiers will give the most output power and power dissipation will be kept within limits when each amplifier sees a load impedance of 4Ω – 8Ω.

Each amplifier in a parallel solution sees a load impedance equal to the total load impedance * the number of amplifiers used. So for a 4Ω solution using two amplifiers will result in each amplifier seeing an 8Ω load. Using National's LM3886 in a two-device parallel solution driving a 4Ω load will typically provide 110W of output power. For a 2Ω solution using two LM3886 ICs will result in each IC seeing a 4Ω load and typically provide 120W of output power. Or four LM3886 ICs may be used so each IC sees an 8Ω load typically providing 200W of output power. Three ICs may also be used so that each IC sees a 6Ω load typically providing 150W of output power.

4.5 Bridged/Parallel Amplifier Pdmax Equation

The bridged/parallel amplifier consist of two amplifiers in bridge mode then additional amplifiers in parallel to the amplifiers on each side of the bridge (see Figure 13 and Figure 17). To find the equation for $Pdmax_{BPA}$ the $Pdmax_{BTL}$ equation is used as a starting point. As discussed above, adding devices in parallel does not change the Pdmax equation so the total Pdmax for a bridged/parallel solution is the same as for a bridged solution.

$$Pdmax_{BPA} = 4*(V_{CCtot}{}^2/2\pi^2R_L) \tag{12}$$

This total power dissipation is divided equally among all of the amplifiers in the circuit. To determine the Pdmax equation for each amplifier in a bridged/parallel circuit the $Pdmax_{BPA}$ equation is used as a starting point. The $Pdmax_{BPA}$ equation calculates the total peak power dissipation for the entire circuit. To find the power for each side of the bridge the $Pdmax_{BPA}$ equation must be multiplied by a factor of 1/2 giving:

$$Pdmax_{BPA(IC)} = 4*(V_{CCtot}{}^2/2\pi^2R_L) * (½) = 2*(V_{CCtot}{}^2/2\pi^2R_L) \tag{13}$$

Adding one additional amplifier in parallel to each side of the bridge as shown in Figure 13 and Figure 17 divides the power between the two amplifiers in parallel on each side of the bridge. The equation must be multiplied by another factor of 1/2 giving:

$$Pdmax_{BPA(IC)} = 2*(V_{CCtot}^2/2\pi^2R_L) * (½) = V_{CCtot}^2/2\pi^2R_L \quad (14)$$

which is just the single-ended Pdmax equation. If more devices are added in parallel to each side of the bridge then instead of a factor of ½ a factor of 1/(Number of Amplifiers) would be used in the last step above.

An alternate way to arrive at the $Pdmax_{BPA(IC)}$ equation is to use the singled-ended Pdmax equation and determine the load impedance seen by each amplifier in the circuit. As discussed above, a bridge circuit means each side of the bridge will see 1/2 the load impedance and a parallel circuit results in each amplifier seeing a load impedance equal to the load * the number of amplifiers in parallel. Putting these two results together gives a general equation for $Pdmax_{BPA(IC)}$.

$$Pdmax_{BPA(IC)} = V_{CCtot}^2/2\pi^2[(\#\text{ of amps in parallel}/2)*R_L] \quad (15)$$

Where # of amps in parallel is the number of amplifiers in parallel on each side of the bridge and not the total number of amplifiers in parallel. As an example, if a 4Ω load is used and the number of amplifiers in parallel is three per side of the bridge (six amplifiers total) then the load seen by each amplifier is: 3/2 * 4Ω = 6Ω.

4.6 Thermal Conclusion

Because of National's portfolio of products and the capabilities of the bridged/parallel circuit, the bridged solution is applicable for a power output window between 80W and 120W. Trying to exceed this power level without a rigorous thermal design will be difficult to achieve. More caution needs to be applied along with better thermal management for bridged circuit designs. The proposed bridged/parallel solution is a more robust design than the bridged circuit, allowing higher output power levels to be obtained by paralleling the two bridged sets of ICs. Table 1 below summarizes the maximum supply voltages for each type of configuration and load impedance while keeping Pdmax per LM3886 IC to less than 40W. See Figure 3, Figure 6, and Figure 13 for detailed information on each circuit.

Table 1. Maximum Power Supply Voltages

	2Ω	4Ω	6Ω	8Ω	16Ω
BR100	NR(1)	±20V	±24V	±28V	±37V
PA100	±28V	±37V	±37V	NA(2)	NA(2)
BPA200	±20V	±28V	±32V	±37V	NA(2)

(1) NR = Not Recommended

(2) NA = No Advantage compared to single-ended or other configurations

In addition to better heat sinking, the application of a small fan can substantially increase the IC's continuous power dissipation capabilities. While the air flow of the fan used to take the data is not known, its air flow seemed to be consistent with a typical computer fan. The IC maximum power dissipation data for an individual LM3886 is summarized below in Table 2. The data shown below should only be used as a guideline of possible IC power dissipation capability. Your electrical design parameters and thermal management may be different, changing the achievable results. As always, lab testing is recommended to verify any solution.

Table 2. Power Dissipation Results

Power IC	Pdmax (No Fan)	Pdmax (With Fan)
LM3886T	40W	60W
LM3886TF	30W	45W

4.7 Thermal Testing Conditions

The data summarized in Table 2 was obtained by using the bridged/parallel configuration and the following conditions: The system was warmed up for an hour using a power dissipation of 30W per device with a 4Ω load. Four different temperature points were measured after stabilizing, then the supply voltages were incremented while insuring that SPiKe™ Protection was not enabled during each test by monitoring each amplifier output. The supply voltages continued to be incremented until SPiKe™ protection or thermal shutdown was enabled, providing the IC's power dissipation limits under those operating conditions.

The input stimulus was a 20Hz sinewave with an amplitude corresponding to the worst case power dissipation for the given load and supply voltage. The ICs were evenly spread out along the heatsink with dimensions of: 3.25″ high x 13.25″ long x 1.3125″ deep. The main body of the heatsink is 0.25″ thick with (10) 1.0625″ deep fins and the heatsink is black anodized. (See section 9.2 for detailed drawing.) Unfortunately, the fins ran horizontally, which hindered heat radiation without a fan, but helped with air flow and heat dissipation when a fan was used.

This same testing procedure can be used for any number of booster circuits, including variations of the bridged/parallel circuit. Another variation would be to add more ICs in parallel to further reduce power dissipation, allowing low impedance loads to be driven to obtain even higher output power levels.

5 BR100—100W Bridge Circuit

5.1 Audio Testing

The following graphs represent the performance level attainable from the bridged circuit found in Figure 3 with a well designed PCB and properly heat sinked. The testing focused on maximum output power capabilities and amplifier linearity. The low THD+N plots shown in Figure 1 and Figure 2 exemplify the high degree of linearity of the bridged circuit which directly translates into a cleaner sounding more transparent amplifier. Other bridged circuit topologies that use the output of one amplifier as the input to the second inverting amplifier inherently possess higher THD and noise that will degrade the solution's sound quality.

5.1.1 Linearity Tests

The linearity of the amplifier is represented by the low THD+N values shown in Figure 1 and Figure 2. Figure 1 represents the THD+N vs Frequency for 1W, 56W, and 100W power levels. The 20kHz THD+N is less than 0.02% for 1W and about 0.008% for 56W and above. For normal listening levels, the THD+N is about 0.004% for most of the audio band. Figure 2 represents the THD+N vs Output Power Level for 20Hz, 1kHz, and 20kHz. The THD+N between 20Hz and 1kHz is less than 0.004% from 1W to the clipping point. The 20kHz THD+N is less than 0.02% from 1W to the clipping point. The continuous clipping point power is around 105W while the power at 10% THD+N is about 140W. These THD+N graphs were obtained using relative THD units, which indicates that the noise level for the amplifier is quite low. Typically, the noise level becomes a significant THD+N contributor at low power levels and shows up as a linearly decreasing function of increasing input signal amplitude. The low power level THD+N for this amplifier is more than acceptable for home entertainment applications.

Figure 3 represents the bridged amplifier schematic. The design is extremely simple, consisting of a non-inverting power op amp configuration and an inverting power op amp configuration. The input to the amplifier solution goes to each individual configuration. While closed-loop gain matching is not critical, it is recommended to have fairly close values. The main functional point to note about this solution is that for a positive going input signal, amplifier U1 will have a positive changing output signal while U2 will have a negative changing output signal. The final voltage across the load is two times the peak amplitude of each individual amplifier output. Since output power is based on the square of the output voltage, the output power is theoretically quadrupled. This document will not go further into the functionality of the circuit as it is widely known in industry.

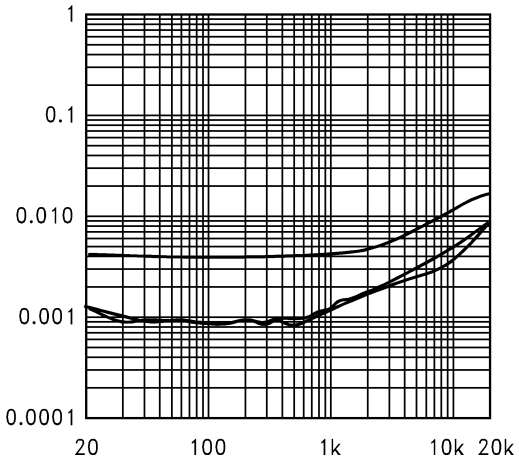


Figure 1. BR100 THD+N vs Frequency, R_L = 8Ω, V_{CC} ±25.5V, BW <80kHz, P_O = 1W, 56W, 100W

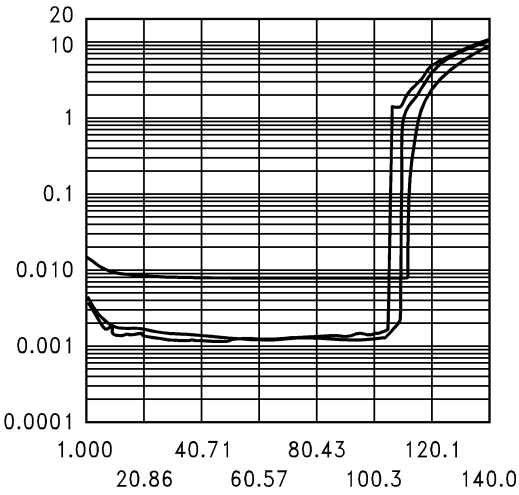


Figure 2. BR100 THD+N vs Output Power f = 20Hz, 1 kHz, 20kHz, R_L = 8Ω, V_{CC} = ±25.5V, BW <80kHz

5.2 Schematics

5.2.1 Bridged Amplifier Schematic

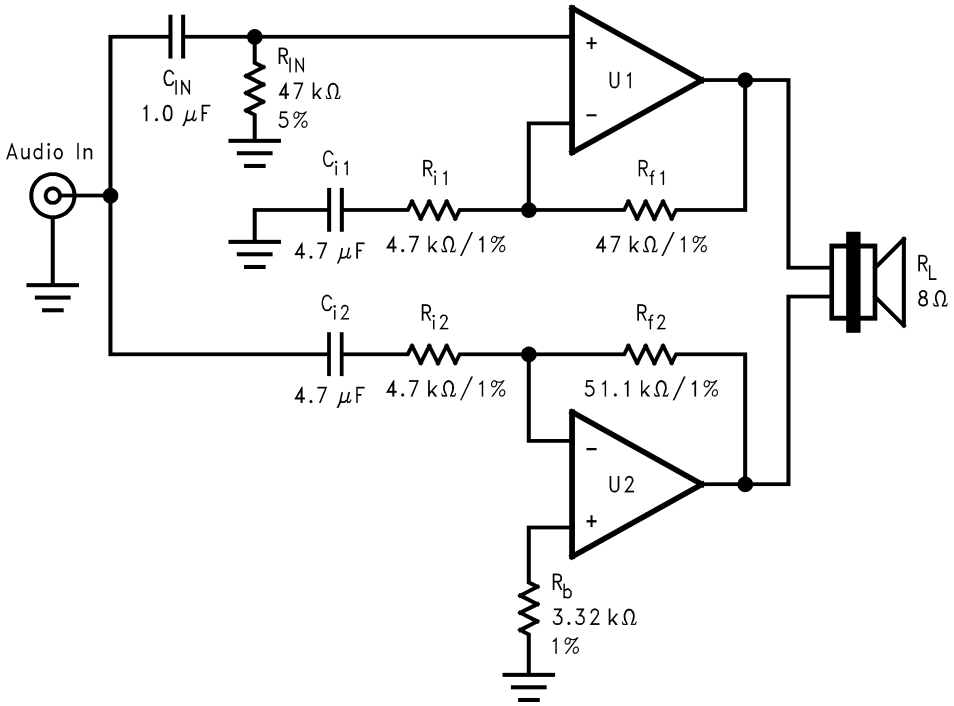


Figure 3. Bridged Amplifier Schematic

5.2.2 Electrical Design Notes

The following electrical design notes will aid in making the bridged amplifier design go more smoothly while also helping to achieve the highest level of performance.

- The input impedance of the inverting amplifier is essentially resistor, R_i. The value of this resistance affects the gain setting of the amplifier as well as the low frequency rolloff in conjunction with C_i. There is a tradeoff between having a low frequency rolloff, a high input impedance and a small capacitor size and value. It is critical to have a flat band response down to 20Hz while it is equally important to have a high enough input impedance so that heavy loading does not occur from the preamp stage. Using large valued low-cost capacitors implies the use of leaky electrolytics which affect the output offset voltage. Electrolytic capacitors are also less linear than other premium caps and should not be used in the signal path when not necessary. This tradeoff issue is the toughest portion of the design. The amplifier gain setting is just as one would expect for an inverting op amp. Of course, the input impedance issue can be quickly resolved by using a voltage follower as an input buffer, but it was omitted from this design to minimize cost and simplify the design. The values provided in the bridged schematic are at a good tradeoff point. There is sufficient input impedance for practically all audio op amps, the closed-loop gain setting is 11 for each amplifier, (gain of 22 overall) while the capacitor value of 4.7µF sets the low frequency −3dB rolloff at about 7Hz.
- The non-inverting input resistance, R_b, is used to create a voltage drop at the non-inverting terminal to offset the voltage at the inverting input terminal due to the input bias current flowing from the output to the inverting input. Generally, the value of this resistor equals the value of the feedback resistor so that the output offset voltage will be minimized close to zero. However, if this value is too large, noise can easily be picked up which will be amplified and seriously affect the THD+N performance. If the resistor is eliminated and the terminal is grounded, the THD+N performance will be much better, but it will not necessarily be optimized. By connecting the non-inverting input directly to a ground reference, any noise on that ground will be directly injected into the amplifier, amplified and thus will also affect the THD+N performance. The best solution is to use a value of resistance that is not too large that it picks up stray noise and not too small as to be affected by ground noise fluctuations. The value used in the previous plots was a 3.32kΩ resistor. It should be noted that this is not necessarily the optimized value and can change with varying circuit layouts.
- Low leakage signal path capacitors should be used where possible to reduce output offset voltages. This is not too big of an issue since each gain stage has only unity gain at DC. This is another reason why 1% resistor tolerances are not necessarily required. To obtain the highest quality amplifier, polypropylene capacitors should be employed in the signal path and supply bypassing.
- As always, the better the supply bypassing, the better the noise rejection and hence higher performance.

6 PA100—100W Parallel Circuit

6.1 Audio Testing

The following graphs are the same format as those presented in the BR100 analysis, namely THD+N verses Frequency at 1W, 56W and 100W and THD verses output power with plots at 20Hz, 1kHz, and 20kHz.

6.1.1 Linearity Test

The linearity of the amplifier is represented by the low THD+N values shown in Figure 4 and Figure 5. Figure 4 represents the THD+N vs Frequency for 1W, 56W and 100W power levels. The 20kHz THD+N is less than 0.05% for all power levels. Figure 5 represents the THD+N vs Output Power Level for 20Hz, 1kHz, and 20kHz. The THD+N between 20Hz and 1kHz is less than 0.01% for power levels above 1W up to the clipping point. The 20kHz THD+N is 0.04% from 0.1W to the clipping point. The 1% THD+N power point is around 110W while the 10% THD+N power point is near 150W. These THD+N graphs were obtained using relative THD+N units, which indicates that the noise level for the amplifier is very low. Typically, the noise level becomes a significant THD+N contributor at lower power levels and shows up as a linearly decreasing function of increasing input signal amplitude. The low power level THD+N for this amplifier configuration is more than acceptable for home entertainment applications.

Figure 6 represents the parallel amplifier schematic. The design is extremely simple, consisting of two power op amps configured identically and tied in parallel to the load each through a 0.1Ω/3W resistor. The closer matched the gain of each IC the more equal the current sharing between them as well as the temperature of each IC due to power dissipation being near equal. This document will not go further into the functionality of the circuit as it is well known in industry.

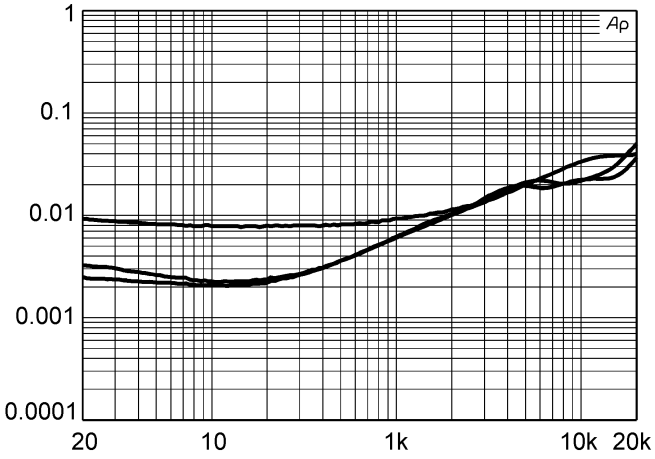


Figure 4. PA100 THD+N vs Frequency
R_L = 4Ω, V_{CC} = ±35V,
BW < 80kHz, P_O = 1W, 56W, 100W

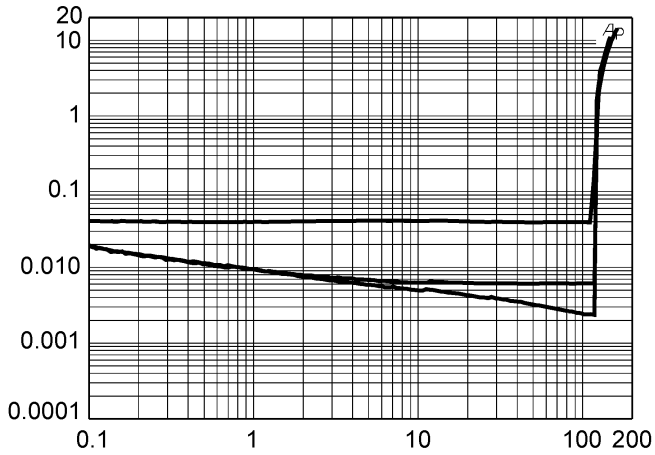


Figure 5. PA100 THD+N vs Output Power
f = 20Hz, 1kHz, 20kHz,
R_L = 4Ω, V_{CC} = ±35V, BW < 80kHz

6.2 Schematics

6.2.1 Parallel Amplifier Schematic

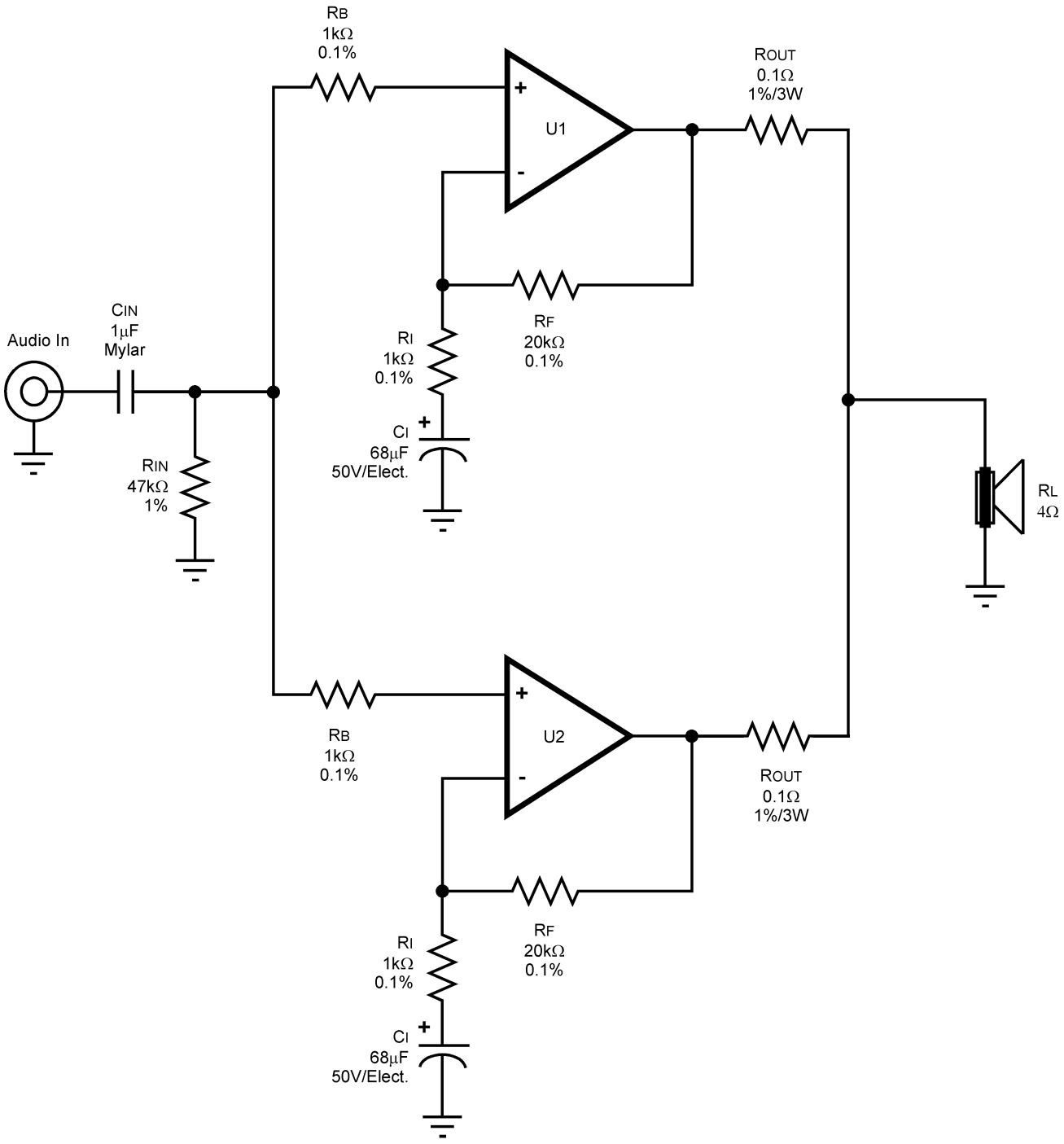


Figure 6. Parallel Amplifier Schematic

6.2.2 Electrical Design Notes

The following electrical design notes will aid in making the parallel amplifier design go more smoothly while also helping to achieve the highest level of performance.

- The input resistance is equal to R_{IN}.The value of R_{IN}should be high enough to eliminate any loading placed on the previous stage (i.e. pre-amplifier). The DC blocking input capacitor value should be calculated on the value of Rin to be sure the correct size is used so low frequency signals will be coupled in without severe attenuation. $f_{IN} = 1/(2\pi R_{IN}C_{IN})$.
- 1% gain setting resistors (R_i and R_f) will give good results but it is recommended 0.1% tolerance resistors be used for setting the gain of each op amp for closer matched gain and equal output current and power dissipation.
- The output resistors, R_{OUT}, wattage rating is based on the load impedance and the output current or maximum output power. As the load impedance is increased or reduced the output current is reduced or increased, respectively. The wattage rating of R_{OUT} should increase as output current increases and decrease as output current decreases. A very conservative design will use peak output current to calculate the needed wattage rating of R_{OUT} ($P = I^2R$).
- As always, the better the supply bypassing, the better the noise rejection and hence higher performance.

7 BPA200–200W Bridged/Parallel Circuit

7.1 Audio Testing

The following graphs represent the performance level attainable from the bridge/parallel circuit found in Figure 13 with a well designed PCB and properly heat-sinked. The testing focused on maximum output power capabilities, amplifier linearity and noise level.

7.1.1 Linearity Tests

The linearity of the amplifier is represented by the low THD+N values shown in Figure 7 and Figure 8. Figure 7 represents the THD+N vs Frequency for 1W, 56W, and 200W power levels. Figure 8 represents the THD+N vs Output Power Level for 20Hz, 1kHz, and 20kHz. The THD+N between 20Hz and 1 kHz is less than 0.004% from 1W to the clipping point. The 20kHz THD+N is less than 0.02% from 1W to the clipping point, The continuous clipping point power is around 210W while the power at 10% THD+N is 300W. These THD+N graphs were obtained using relative THD+N units, which indicates that the noise level for the amplifier is quite low. Typically, the noise level becomes a significant THD+N contributor at low power levels and shows up as a linearly decreasing function of increasing input signal amplitude. In Figure 8, the THD+N decreases from 0.004% to 0.001% from 1W to the clipping point for frequencies between 20Hz and 1kHz. The THD+N with a 20kHz input decreases from 0.02% to 0.009% from 1W to 50W and rises thereafter up to about 0.015%.

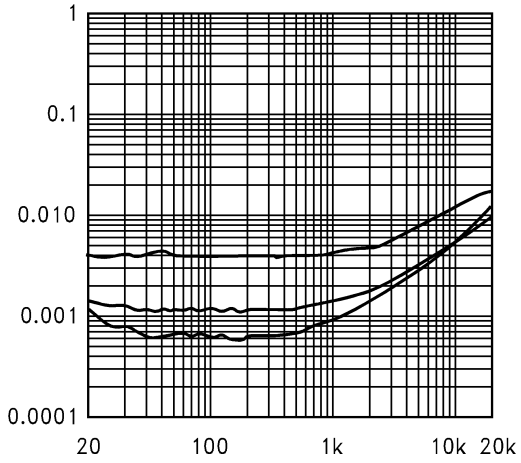


Figure 7. BPA200 THD+N vs Frequency P_O = 1W, 56W, 200W R_L = 8Ω, BW < 80 kHz, 9/16/97

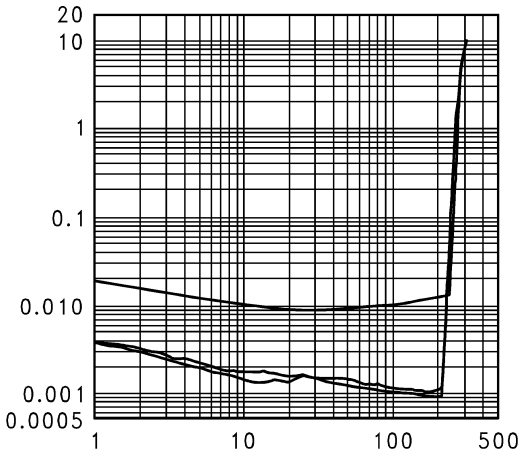


Figure 8. BPA200 THD+N vs Output Power f = 20Hz, 1kHz, 20kHz, R_L = 8Ω, BW < 80kHz, 9/16/97

7.1.2 Output Power Tests

Although the amplifier was deigned based on thermal dissipation capabilities using continuous sinusoidal inputs, the output power levels attainable are significantly greater with pulsed waveforms that more accurately reflect music material. The continuous clipping point power and burst power levels are shown in Table 3 below:

Table 3. BPA200 Maximum Output Power Levels

Load Impedance	Continuous Clipping Point Power	Burst Clipping Point Power
8Ω	225W	295W
4Ω	335W	450W

The burst power levels were obtained using a 20Hz sinewave with two cycles on and twenty cycles off. The output power capability of the BPA200 is further substantiated by the power bandwidth measurement. The amplifier is capable of producing 200W continuously into an 8Ω load up to f = 90.5kHz with little change in THD+N. The graph in Figure 9 shows the power bandwidth measurement. Also notice that the low frequency power in the graph is not rolled off as would normally occur with a DC blocking capacitor. The servo circuits allow the low frequency power to remain constant down to DC without high output offset voltage.

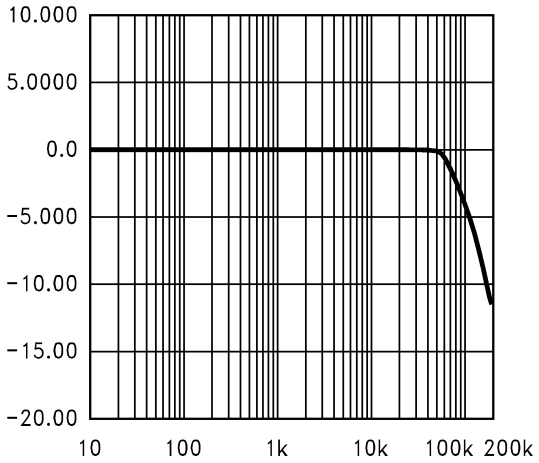


Figure 9. BPA200 Power Bandwidth
P_o = 200W, R_L = 8Ω, BW > 500kHz, 9/16/97

7.1.3 Noise Floor Tests

The following plots exemplify the low-noise aspects of the BPA200. Figure 10 was obtained using an 8k FFT relative to 1dBV with a measurement bandwidth of 22kHz. Figure 11 is the same measurement as Figure 10, but shown in a logarithmic scale.

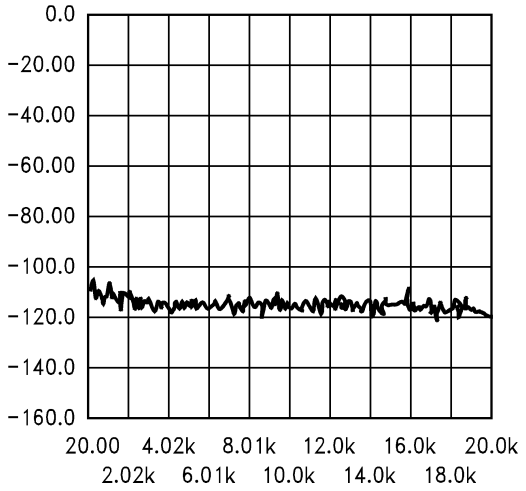


Figure 10. BPA200 Spot Noise Floor (dBV)
R_L = 8Ω, BW < 22kHz, 9/16/97
Linear-Scale

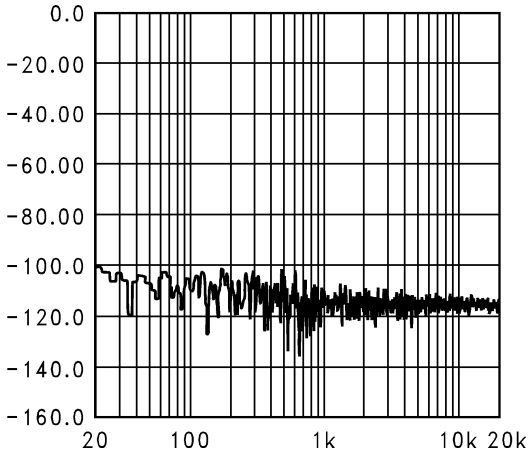


Figure 11. BPA200 Noise Floor (dBV)
R_L = 8Ω, BW < 22 kHz, 9/16/97 Log-Scale

An FFT analyzer is extremely handy in determining the noise culprit when debugging a new circuit and its layout, as well as evaluating the coupling effects of the 60Hz component and its harmonics. As shown in Figure 12, the noise level is quite low and the influence of the power supply is relatively small. The highest 60Hz components reach −105dBV, while the noise floor sits around −120dBV.

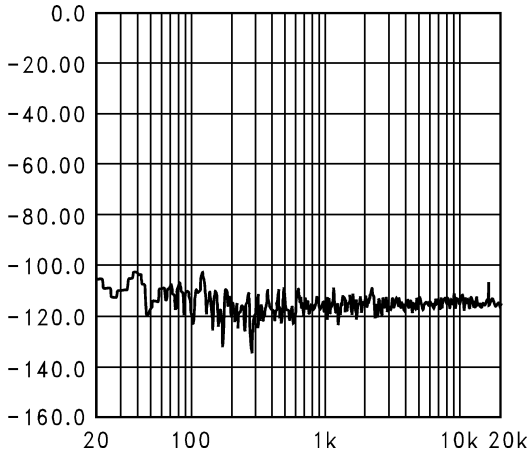


Figure 12. BPA200 Noise Floor (dBV)
R_L = 8Ω, BW < 22 kHz, 9/16/97 Log-Scale 60 Hz

Even with the limited number of graphs shown, the quality of this amplifier from a measurement perspective is quite good. However, with all audio equipment, nothing is really better than doing a listening test. It is recommended that listening test be done to confirm the audio quality of the different configurations presented.

7.1.4 Electrical Design Notes

The following electrical design notes will aid in obtaining a high performance amplifier solution.

- Input resistor values should be equal and have a 0.1% tolerance to minimize amplifier noise. These resistor pairs are R_{b1} & R_{i1}, R_{b2} & R_{i2}, R_{i3} & R_{c3}, and R_{i4} & R_{d3} as shown in Figure 13.
- 0.1% tolerance resistors for close gain matching should be used to minimize offset voltages when not using servo circuits.
- 1% tolerance high wattage ballast resistors are required when paralleling outputs to keep differently biased outputs from fighting each other. The wattage rating is dependent upon the amount of current expected to flow from each output and the resistance of the ballast resistor; $P = I^2R$. A good resistance value is 0.1Ω. Amplifier efficiency is lost if the resistor value is too large like 1Ω since 10A times 1Ω is 10V of output voltage drop.
- Low output offset voltage servo op amp is required to minimize solution output offset voltage.
- An input buffer is required because of the low input impedance from paralleling of the inputs. High valued gain setting resistors could be used at the risk of increasing noise susceptibility. The proposed solution with an input buffer (see Figure 13 and Figure 17) provides the easiest way around gain resistor matching and providing a high input impedance.

7.2 Schematics

7.2.1 Detailed Bridged/Parallel Amplifier Schematic

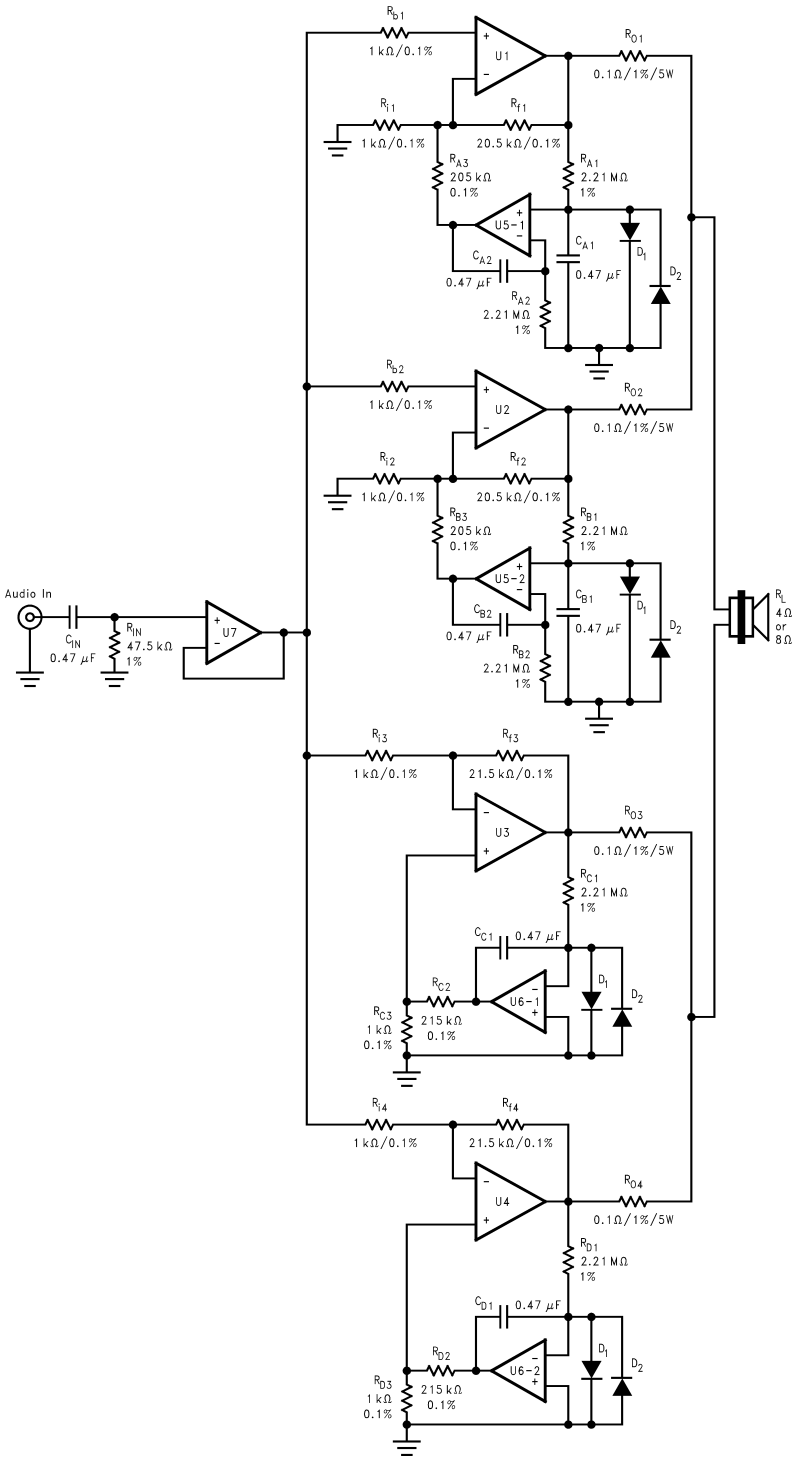


Figure 13. Detailed Bridged/Parallel Amplifier Schematic

7.2.2 Servo Circuits

While output ballast resistors in the basic bridge/parallel circuit work well to keep separately biased IC outputs from fighting each other, the addition of servo circuits will minimize output offset voltages that cause output voltage inequalities. Different output offset voltages cause a constant current to flow between outputs that increases IC power dissipation. By minimizing output offset voltages, all of the ICs will run cooler, expanding the IC's long term reliability and output power capability without activating sensitive protection circuits.

Typically, offset voltages are compensated for by using input and output coupling capacitors. Power amplifiers used in a single-supply configuration, utilize large value, large size electrolytic or polypropylene capacitors. This is because the load impedance is 4Ω or 8Ω and the RC combination creates a highpass filter that can rolloff audio frequencies. Since these output coupling capacitors have nonlinearities and are quite large, many designers choose to employ split power supplies. While split power supplies don't use these capacitors, a DC blocking capacitor is needed somewhere in the circuit to protect speakers. This capacitor is typically, C_{i1}, C_{i2}, C_{i3}, and C_{i4} as shown in Figure 13. With the application of a servo circuit, this capacitor can also be eliminated as shown in Figure 14 and Figure 15.

Servo circuits are essentially integrator op amp circuits that integrate offset voltage changes from the power op amp's output and feed back the integrated voltage to the opposite input of the power op amp. A servo circuit is required at each IC output of the bridge/parallel circuit to keep currents from flowing between IC outputs. Without each output compensated, one offset voltage will cause current to flow between ICs increasing power dissipation. If gain setting resistors are 0.1% and closely matched, the servo circuit may be left out, but DC blocking capacitors will be required.

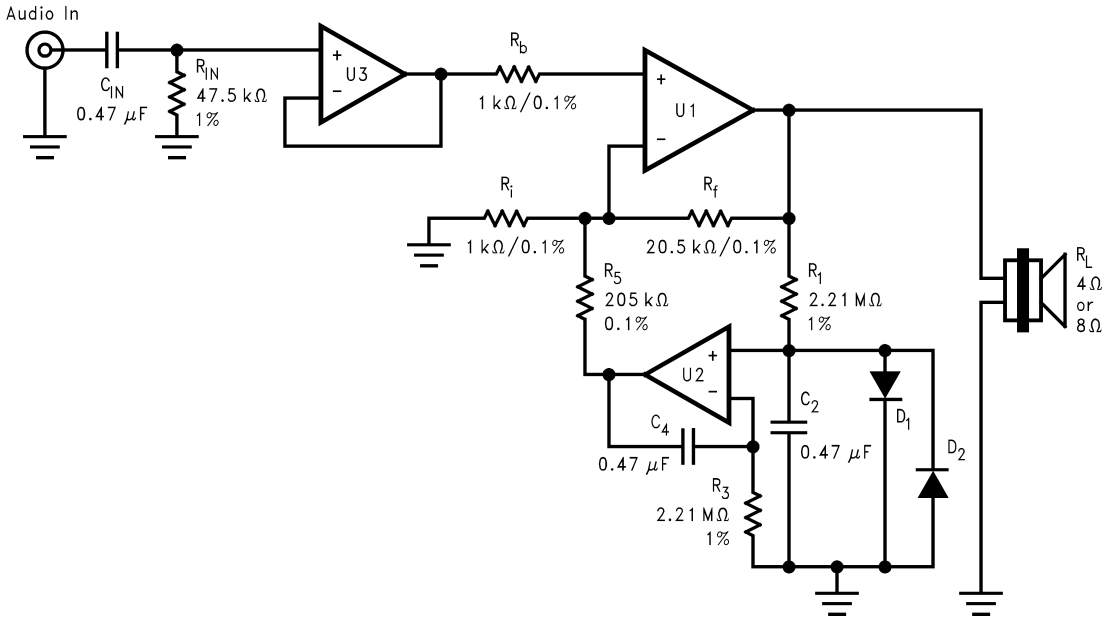


Figure 14. Non-Inverting Servo Amplifier Schematic

The inverting type servo amplifier applied to the inverting amplifier portion of the bridge/parallel circuit is shown in Figure 15. The non-inverting type servo circuit could be applied to the inverting input of U1 to achieve the same result, however, it uses an extra RC network that can be eliminated with the inverting type servo.

If a different power amplifier gain is desired, other component values can be used under the following conditions: In Figure 14, resistor R5 should be about 10 times the value of R_f, while R_i and R_b should be equal. In Figure 15, resistor R3 should be about 10 times the value of R_f, while R_4 and R_i should be equal. For both the Non-Inverting and Inverting Servo solutions, the input clamping diodes should be low-leakage, with low-leakage film capacitors having a high-quality dielectric such as polypropylene or polystyrene (mylar), and metal-film resistors.

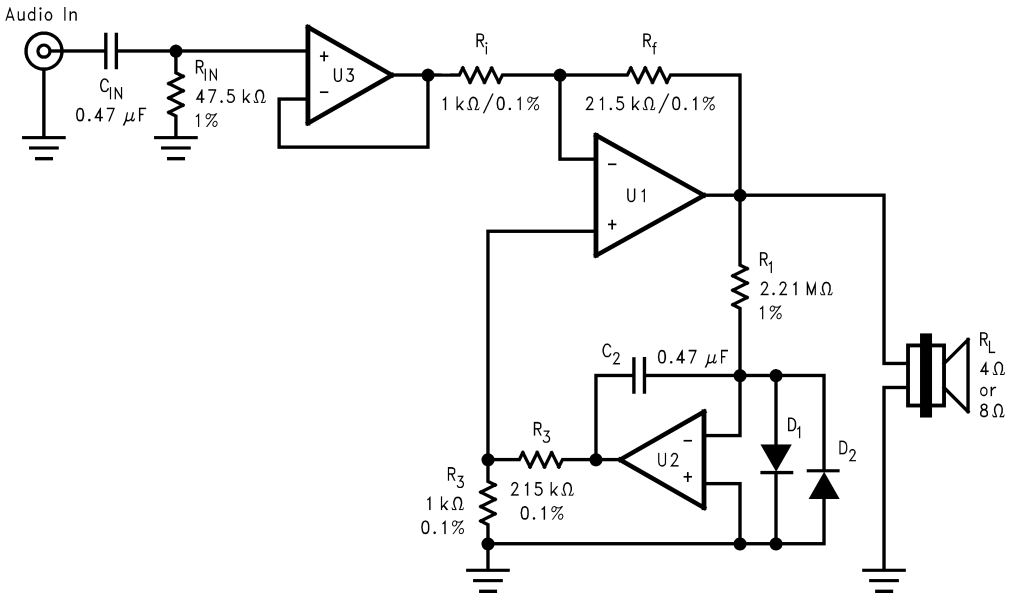


Figure 15. Inverting Servo Amplifier Schematic

7.2.3 Power Supply Circuit

The power supply portion of the amplifier is made up of a typical unregulated bipolar power supply. The supply is comprised of an input AC line filter, surge protecting MOVs, a separate 385VA toroidal transformer for each channel, and 40,000µF of supply reservoir capacitance for each supply voltage rail.

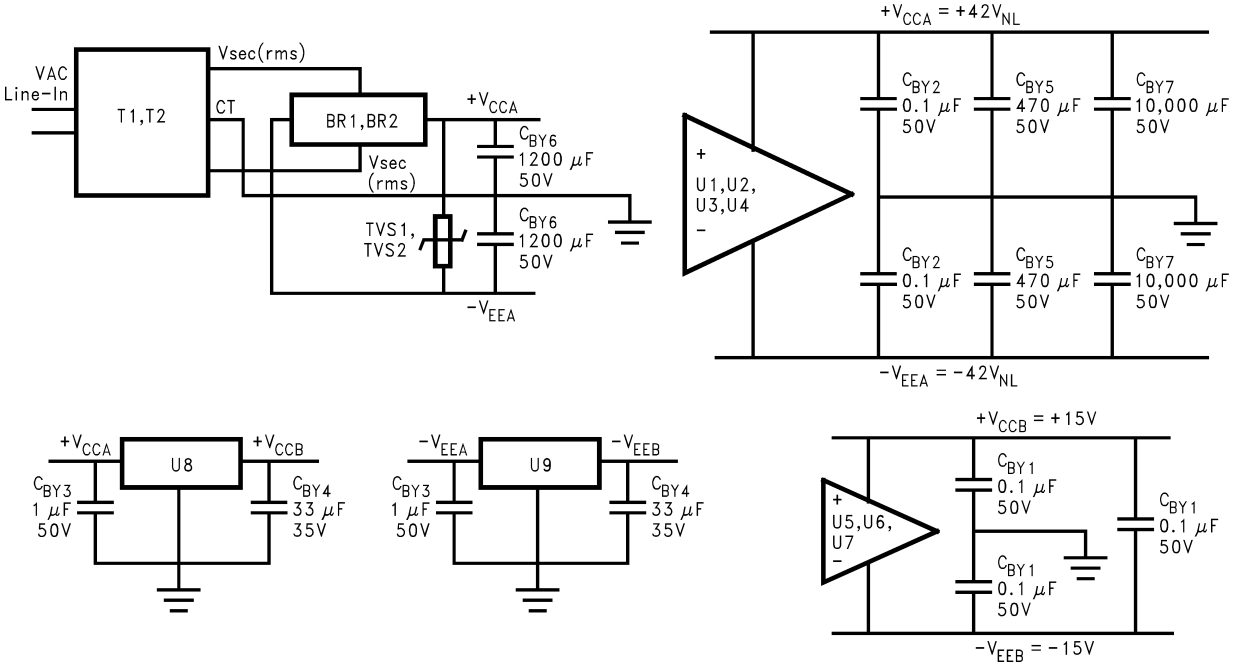


Figure 16. Power Supply Schematic

7.2.4 Basic Bridged/Parallel Amplifier Schematic

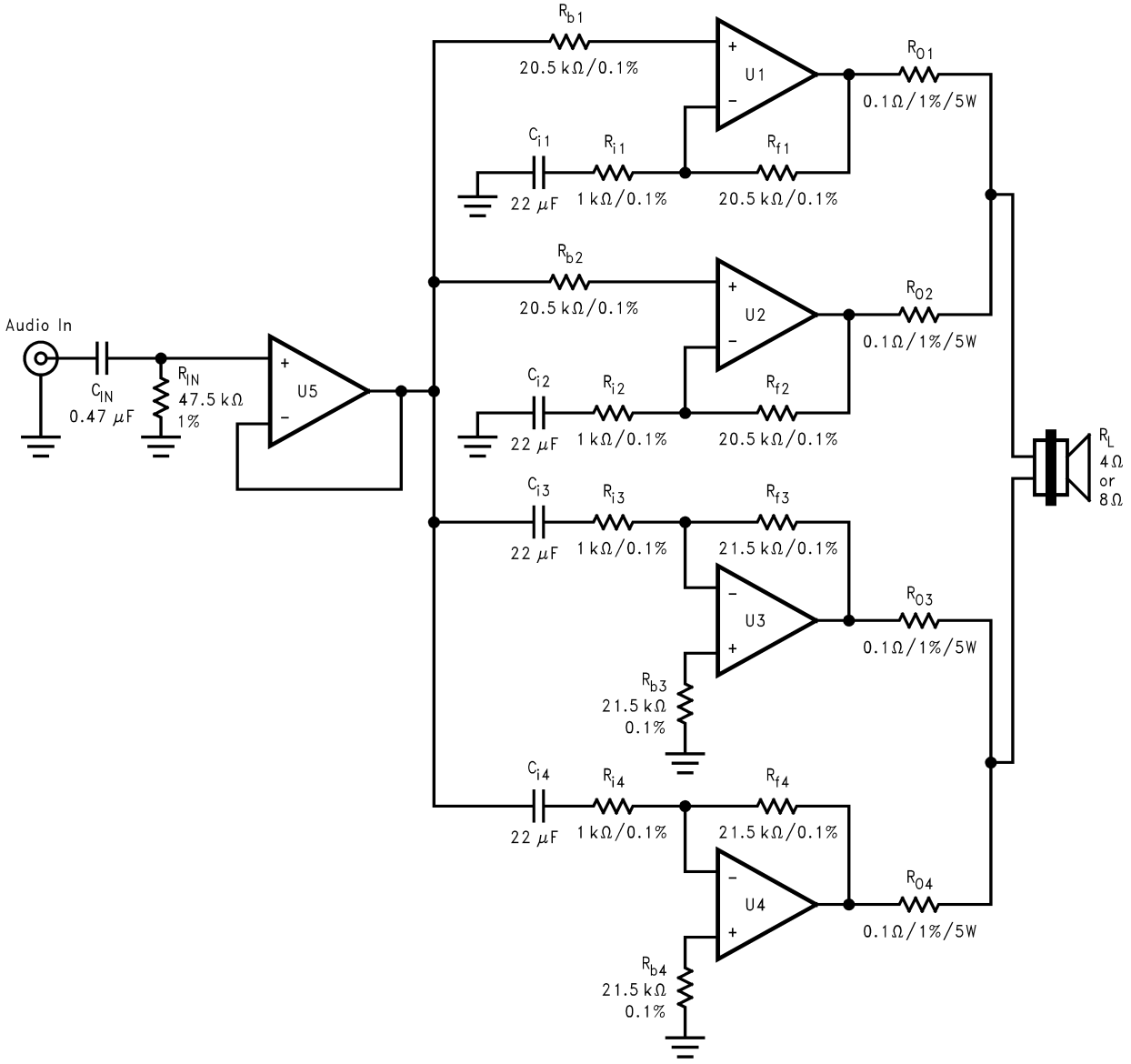


Figure 17. Basic Bridged/Parallel Amplifier Schematic

8 Parts List and Vendors

8.1 Build of Materials for BR100 Amplifier

(See Figure 3).

Description	Designator	Manufacturer's or Example Part Number
1.0µF/100V Metallized Polyester Fim Capacitor	C_{IN}	Panasonic,ECQ-E1105KF
4.7µF/35V/Electrolytic Capacitor	C_{i1}, C_{i2}	Panasonic, ECE-A1VN4R7U
47kΩ/1/4W/5% Resistor	R_{IN}	
4.7kΩ/1/4W/1% Resistor	R_{i1}, R_{i2}	
46.4kΩ/1/4W/1% Resistor	R_{f1}	
51.1kΩ/1/4W/1% Resistor	R_{f2}	
3.32kΩ/1/4W/1% Resistor	R_B	
Additional Externals on Demo Board Not Shown on Schematic		
Description	**Designator**	**Functional Description and Example Part Number**
0.1µF/50V/Monolithic Ceramic Capacitor	C_{B1}	IC Supply Bypass Capacitor
47µF/50V/Electrolytic Capacitor	C_{B2}	IC Supply Bypass Capacitor Panasonic, EEU-FC1H470
4,700µF/50V/Electrolytic Capacitor	C_{B3}	IC Supply Bypass Capacitor Panasonic,ECO-S1HP472BA
10µF/35V/Electrolytic Capacitor	C_M	Turn on Mute
15kΩ/1/4W/5% Resistor	R_{M1}	Turn on Mute
8.2kΩ/1/4W/5% Resistor	R_{M2}	Turn on Mute
2.7Ω/1/4W/5% Resistor	R_G	Signal GND to Power GND

8.2 Build of Materials for PA100 Amplifier

(See Figure 6).

Description	Designator	Manufacturer's or Example Part Number
1.0µF/100V Metallized Polyester Film Capacitor	C_{IN}	Panasonic, ECQ-E1105KF
68µF/50V Electrolytic Capacitor	C_i	Panasonic, EEU-FC1H680
47kΩ/1/4W/1% Resistor	R_{IN}	
1.0kΩ/1/4W/0.1% Resistor	R_i	
20.0kΩ/1/4W/0.1% Resistor	R_F	
1.0kΩ/1/4W/1% Resistor	R_B	
0.1Ω/1/3W/1% Resistor	R_{OUT}	
Additional Externals on Demo Board Not Shown on Schematic		
Description	**Designator**	**Functional Description and Example Part Number**
0.1µF/50V/Monolithic Ceramic Capacitor	C_1	IC Supply Bypass Capacitor
47µF/50V/Electrolytic Capacitor	C_2	IC Supply Bypass Capacitor Panasonic, EEU-FC1H470
2,200µF/50V/Electrolytic Capacitor	C_3	IC Supply Bypass Capacitor Panasonic,EEU-FC1H222
0.1µF/50V/Monolithic Ceramic Capacitor	C_{SN}	Snubber Network on Output
2.7Ω/1/4W/5% Resistor	R_{SN}	Snubber Network on Output
LM340T5, Fixed +5V Regulator	LM340L-5	5V PCB Supply

Description	Designator	Manufacturer's or Example Part Number
10µF/25V/Electrolytic Capacitor	C_{M1}	5V Output Bypass Capacitor
0.1µF/50V/Monolithic Ceramic Capacitor	C_{M2}	5V Input Bypass Capacitor
470Ω/1/2W/5% Resistor	R_{REG}	Voltage Reducer for LM340 Input Voltage
20kΩ/1/4W/5% Resistor	R_{M1}	Mute Circuit
1MΩ/1/4W/5% Resistor	R_{M2}	Mute Circuit
120Ω/1/4W/5% Resistor	R_{LED}	Current Limit for LED Indicators
2.7Ω/1/4W/5% Resistor	R_G	Signal GND to Power GND
Ultra Bright LED Lamp, T-1 ¾ Standard Size, Green	LED	Indicator LED

8.3 Build of Materials for BPA200 Amplifier

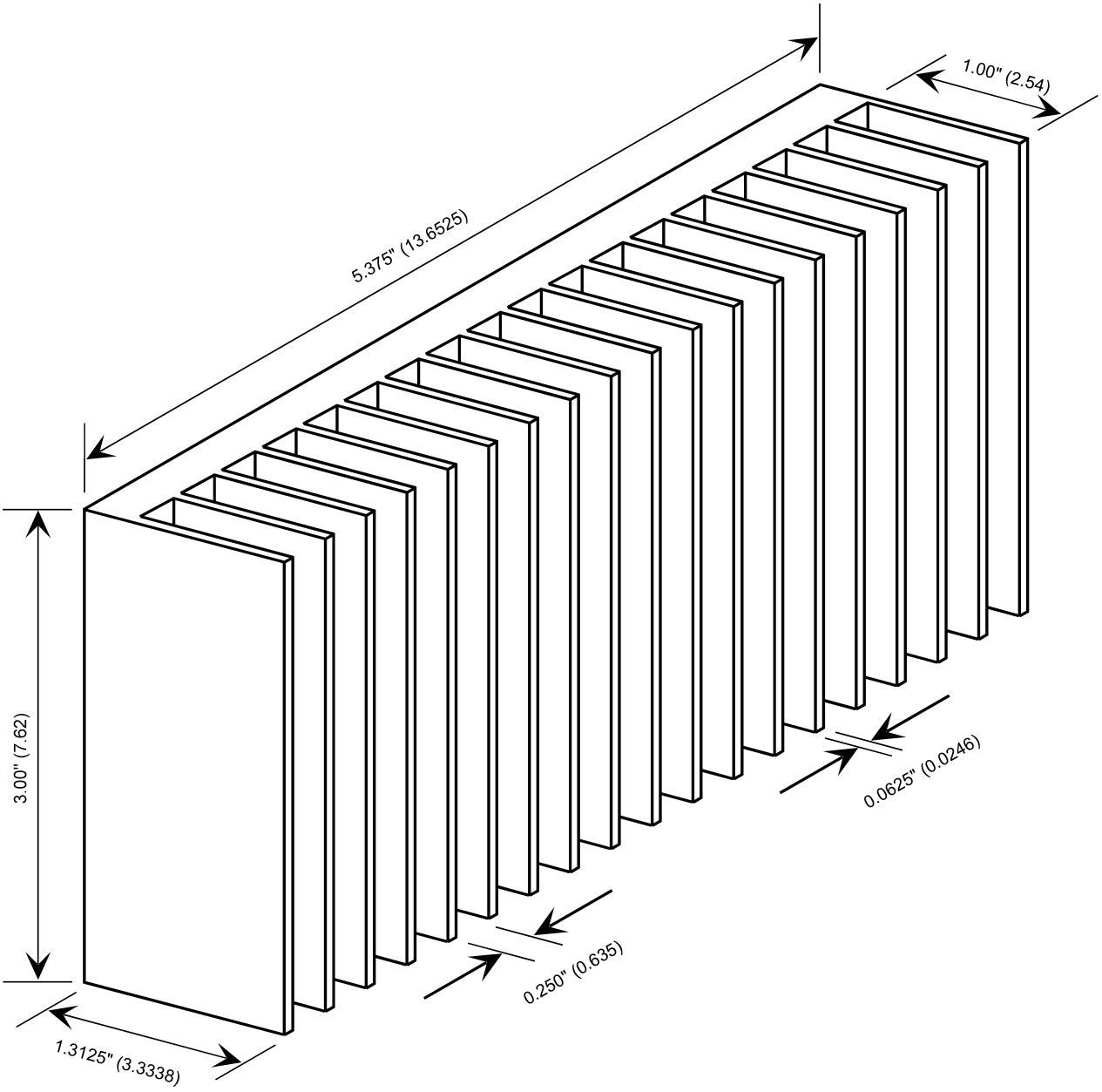
(See Figure 13 and Figure 16).

Description	Designator	Manufacturer's Part Number
PASSIVE COMPONENTS		
0.47µF/100V Mylar Capacitor	C_{A1}, C_{A2}, C_{B1}, C_{B2}, C_{C1}, C_{D1}, C_{IN}	Electrocube, 230B-0.47µF-100V-JB
0.1Ω/5W/1% Power Ballast Resistor	R_{O1}, R_{O2}, R_{O3}, R_{O4}	Dale, RS-5-0.1-1%
1kΩ/0.1% Metal Film Resistor	R_{b1}, R_{b2}, R_{i1}, R_{i2}, R_{i3}, R_{i4}, R_{C3}, R_{D3}	Dale, RN-55D-1000-B
47kΩ/1% Metal Film Resistor	R_{in}	Dale, RN-55D-4702
20.5kΩ/0.1% Metal Film Resistor	R_{f1}, R_{f2}	Dale, CMF-55-20.5k-.1%-T2
21.5kΩ/0.1% Metal Film Resistor	R_{f3}, R_{f4}	Dale, MF-55-21.5k-.1%-T2
205kΩ/0.1% Metal Film Resistor	R_{A3}, R_{B3}	Dale, CMF-55-205k-.1%-T2
215kΩ/0.1% Metal Film Resistor	R_{C2}, R_{D2}	Dale, CMF-55-215k-.1%-T2
2.21MΩ/1% Metal Film Resistor	R_{A1}, R_{A2}, R_{B1}, R_{B2}, R_{C1}, R_{D1}	Dale, CMF-55-2.21M-.5%-T9
1N456A Low Leakage Diodes	D_1, D_2	National Semiconductor (NSC) 1N456A
INTEGRATED COMPONENTS		
LM3886T, 50W Monolithic Power IC	U1, U2, U3, U4	NSC, LM3886T
LF412ACN, Dual JFET Input Op Amp	U5, U6	NSC, LF412ACN
LF411ACN, JFET Input Op Amp	U7	NSC, LF411ACN
LM78L15ACZ, +15V Linear Regulator	U8	NSC, LM78L15ACZ
LM79L15ACZ, −15V Linear Regulator	U9	NSC, LM79L15ACZ
POWER SUPPLY COMPONENTS		
385V A, 60 V_{rms} Sec. Transformer	T1, T2	Toroid Corp. of Maryland, #738.302
Bridge Rectifier	B_{R1}, B_{R2}	General Instrument, KBU8B
100V, 1.5kΩ Metal Oxide Varistor (Transient Voltage Surpressor)	TVS1, TVS2	Digikey, 1.5KE100CACT-ND
0.1µF/50V Ceramic Capacitor	C_{BY1}	Sprague, 1C25Z5U104M050B
0.1µF/50V Polypropylene	C_{BY2}	Panasonic, ECQ-P1H104GZ
1µF/50V Electrolytic Capacitor	C_{BY3}	
33µF/35V Electrolytic Capacitor	C_{BY4}	
470µF/50V Electrolytic Capacitor	C_{BY5}	Mallory, SKR471M1HJ21V
1200µF/50V Electrolytic Capacitor	C_{BY6}	Mallory, LP122M050A1P3
10,000µF/50V Electrolytic Capacitor	C_{BY7}	Panasonic, ECE-S1HU103U
AC Line Connector		Schurter, 34.3124
Power Switch (Bowden Cable)		Schurter, 886.0101
MISCELLANEOUS HARDWARE		
IC 11-Pin Sockets		Yamaichi, SMT-15420

9 Heat Sink Drawings

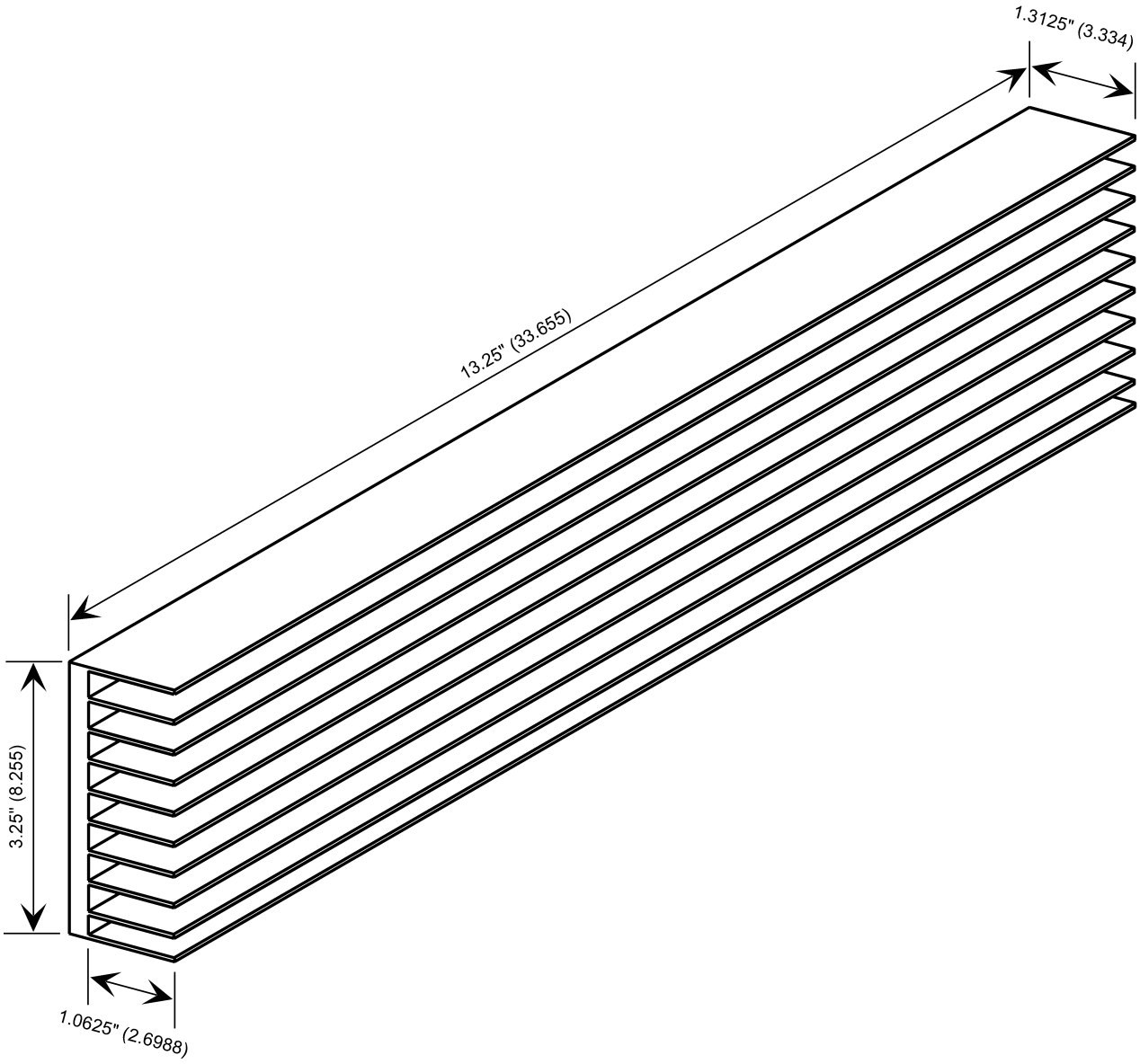
9.1 BR100 and PA100 Heat Sink Drawing

Inches (centimeters) unless otherwise noted.



9.2 BPA200 Heat Sink Drawing

Inches (centimeters) unless otherwise noted.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265