Modulation Frequency Check

During LF transmissions a FSK signal is transmitted. The resonance frequency of the trimmed antenna circuit (fL) represents a low bit and high bits are represented by a lower frequency (fH), which is achieved by switching in a Modulation Capacitor in parallel with the antenna resonance circuit. This frequency can be measured in the same way as the normal resonance frequency, but using Probe Test Mode 0x16 instead of 0x18.

CRC Calculation

A Cyclic Redundancy Check (CRC) generator is used in the TMS37157 during receipt and transmission of data to generate a 16-Bit Block Check Character (BCC), applying the CRC-CCITT algorithm as shown in Figure 51.

The CRC generator consists of 16 shift register cells with 3 exclusive OR (Xor) Gates. The first Xor gate (X^{16}) combines the input of the CRC generator with the output of the shift register (LSB first) and feeds back to the input of the shift register. The other two Xor gates combine certain cell outputs (X^{12}, X^{5}) with the output of the first Xor Gate and feed into the next cell input.

The CRC Generator is initialized with the value 0x3791 as shown in Figure 50).

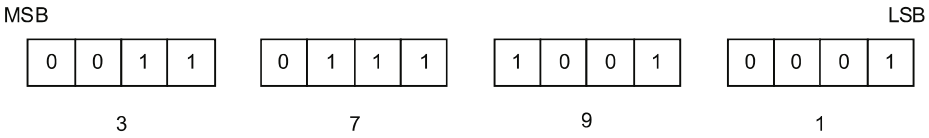

Figure 50. Initial CRC Value 0x3791

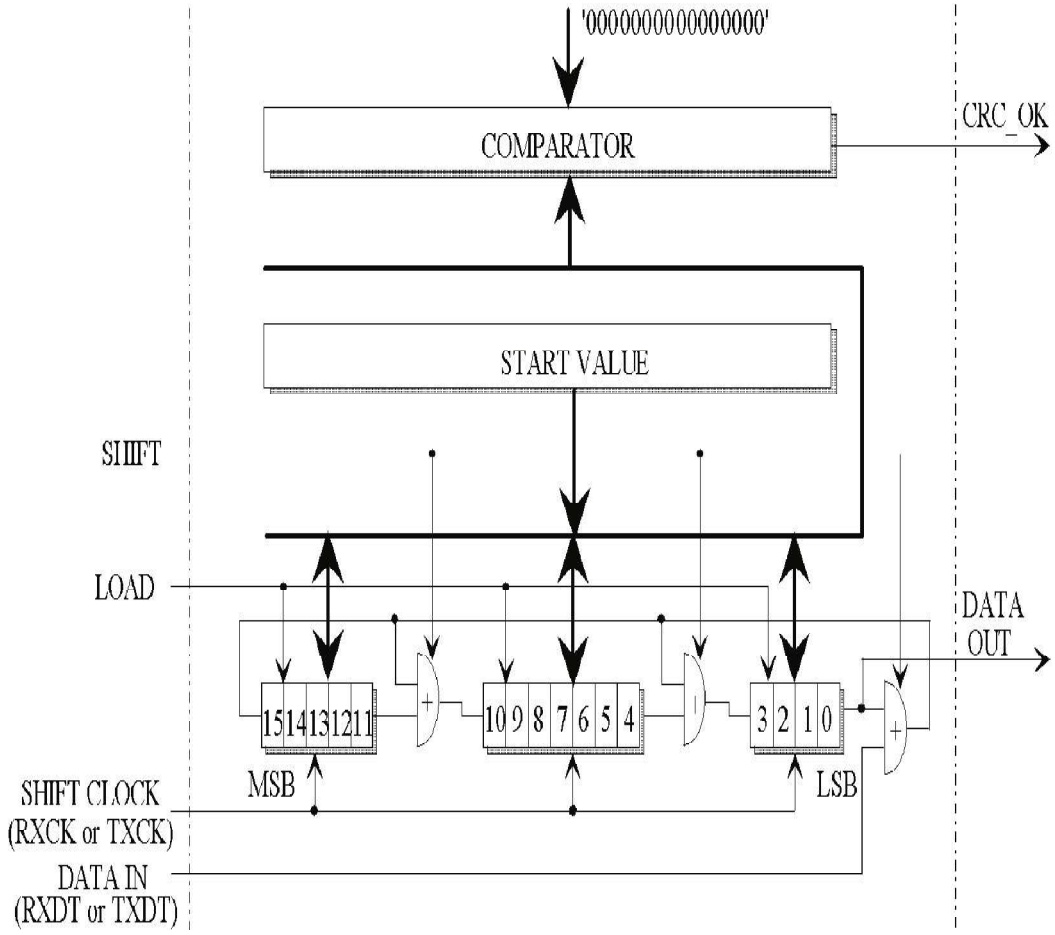

Figure 51. CRC Generator Block Schematic

The CRC generation is started with the first shifted bit, received during write phase RXCK, RXDT. After reception of program or lock command and the additional bits, including the write frame BCC, the CRC Generator content is compared to 0x0000 (CRC_OK).

During read function CRC generation is started after transmission of the start byte (0x7E). After the read data (6 bytes) and the read address byte, the CRC generator content is shifted out using the CRC generator as a normal shift register (SHIFT signal). DATA OUT represents the BCC which is added to read data and read address. The BCC format is one Word with LSB shifted out first.

From a mathematics point of view, the data, which are serially shifted through the CRC generator with LSB first, are multiplied by 16 and divided by the CRC-CCITT generator polynomial:

$$P(X) = X^{16} + X^{12} + X^{5} + 1 \quad (1)$$

The remainder from this division is the Read Frame Block Check Character (Read Frame BCC).

The interrogator control unit has to use the same algorithm to generate the Write Frame BCC and to check the Read Frame BCC received from the transponder. The response is checked by shifting the Read Frame BCC through the CRC generator in addition to the received data; the content of the CRC generator must be zero after this action.

Typically the CRC generator is realized in the Base Stations by means of software and not hardware. The algorithm can be handled on a bit-by-bit basis (see Figure 52) or by using look-up tables.

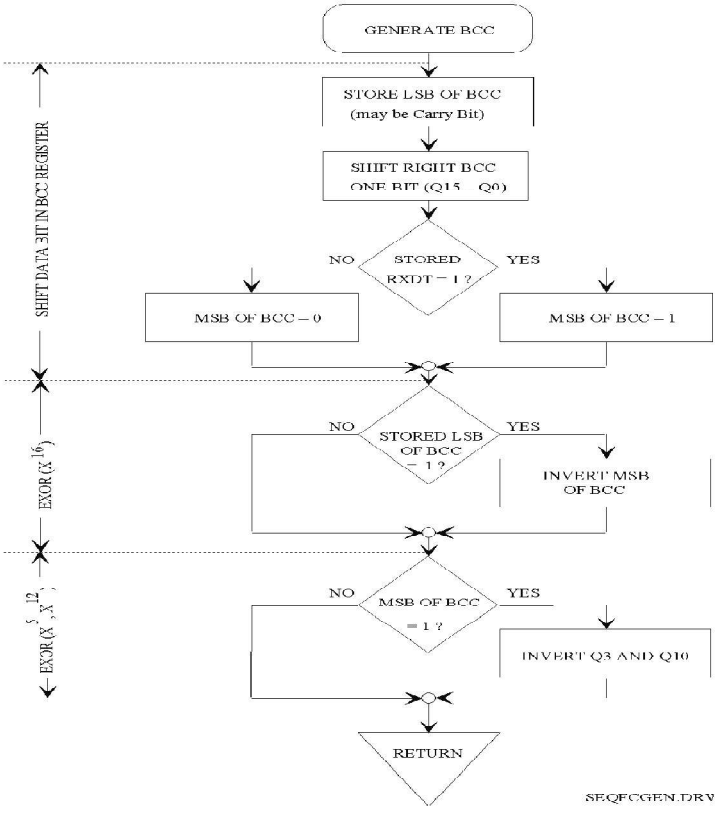

Figure 52. Routine - Generate Block Check Character Bit by Bit