



TMS370 Microcontroller Family

Data Book

1996

8-Bit Microcontroller Family





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INTRODUCTION

The TMS370 Microcontroller Family Data Book from Texas Instruments includes complete detailed specifications on the TMS370 8-Bit Microcontroller Family product line to include the following device groups: TMS370Cx0x, TMS370Cx1x, TMS370Cx2x, TMS370Cx32, TMS370Cx36, TMS370Cx4x, TMS370Cx5x, TMS370Cx6x, TMS370Cx7x, TMS370Cx8x, TMS370Cx9x, TMS370CxAx, TMS370CxBx, and TMS370CxCx.

The objective of this manual is to provide the user with complete information on all the device groups contained within the TMS370 Family, enabling selection of a particular device to suit the user's needs and application much easier.

The data book is divided into the following chapters, each of which is described briefly below:

Chapter 1. General Information – Introduces the TMS370 Family of devices, discusses the key features and major components of the device family, includes an alphanumeric index for finding device numbers, and contains an ordering guide showing the device-numbering convention for all fourteen device families. This chapter also includes a functional-block-diagram generalization and a Texas Instruments related documents section with further assistance information provided.

Chapter 2. Selection Guide – Provides an easy-to-use reference guide that includes specific device information by device groups: product family descriptions (device type, part number, package and temperature options, and pin count); memory (program and data memory and any capability of off-chip memory expansion); and any peripherals (timers, serial interfaces, A/D channels, I/O, clock generators, and OTP and reprogrammable devices). This chapter also identifies the development support tools available for each of the TMS370 devices.

Chapter 3. Operating Conditions and Characteristics/Timing Conventions/Glossary – Defines terms and standards used throughout the data book with respect to the TMS370 Family operating conditions and characteristics. Identifies and describes the timing conventions utilized. This chapter also contains a glossary that defines acronyms, key terms, signal names, and some general concepts.

Chapters 4 – 17. Data Sheets – Contains the data sheets for the TMS370 8-Bit Microcontroller Family.

Chapter 18. Mechanical Data – Shows the detailed mechanical drawing packages and the associated specifications for each package type utilized in the TMS370 family. This chapter also provides a cross-reference table to identify the mechanical package type(s) to a specific device family.

Chapter 19. Quality and Reliability – Details the selected processes, standards and philosophies that Texas Instruments uses to ensure the production of high quality products.

Chapter 20. Guidelines for Handling Electrostatic-Discharge-Sensitive Devices and Assemblies – Because the devices included in the TMS370 8-Bit Microcontroller Family are categorized as Class 2 ESD-sensitive, this section includes the guidelines for the handling of ESD-sensitive devices.

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introduction to the TMS370 family of devices

This chapter briefly discusses the key features and major components of the TMS370 8-Bit Microcontroller families (that is, 'x0x, 'x1x, 'x2x, 'x32, 'x36, 'x4x, ..., 'xCx). It includes a functional-block-diagram generalization that depicts all available modules, with the understanding that no one device contains all the available modules. The chapter concludes with an alphanumeric index, the device-numbering convention, and a list of other Texas Instruments related documents.

This chapter covers the following topics:

- Overview
- Typical Applications
- Device Categories
- Key Features of the TMS370 Microcontroller Family
- TMS370 Major Components Architecture
 - CPU
 - Register File (RF)
 - RAM
 - Data EEPROM
 - Program Memory (ROM/EPROM)
 - Input/Output Ports
 - Timer 1
 - Timer 2n (A and B)
 - Watchdog Timer
 - Programmable Acquisition and Control Timer (PACT)
 - Serial Communications Interfaces (SCI1 or SCI2)
 - Serial Peripheral Interface (SPI)
 - Analog-to-Digital Converter (ADC1, ADC2 or ADC3) Modules
- Summary of Components by Device Types
- Functional-Block-Diagram Generalization
- Alphanumeric Index
- Device-Numbering Conventions
- Available Development-System-Support Tools
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overview

The TMS370 family consists of very large scaled integration (VLSI), 8-bit, complementary metal oxide semiconductor (CMOS) microcontrollers with on-chip EEPROM storage and peripheral-support functions. These devices offer superior performance in complex, real-time control applications in demanding environments and are available in mask-programmable ROM and EPROM.

In a continual effort to improve its products, Texas Instruments has added new, more robust features to the TMS370 family of devices that are designed to enhance performance and enable new application technologies. These added features include new watchdog modes and low-power modes for mask-ROM devices. All family members are software compatible, so that many existing applications can be run on the improved devices without modification of software. (Refer to the associated data sheets for more information on compatibility.)

In expanding its powerful TMS370 family of microcontrollers, TI™ offers many new configurable devices for specific applications. As microcontrollers have evolved, TI has added multiple peripheral functions to chips that originally had only a central processing unit (CPU), memory, and I/O blocks. Now, with the high-performance, software-compatible TMS370 microcontrollers, over 80 standard products are available. Also, up to 27 function modules can be used to configure a new device quickly, easily, and cost-effectively for any applications.

The TMS370 family is supported fully by TI development tools that facilitate simplified software development for prompt market introduction of new products. These tools include an assembler, an optimizing C compiler, a linker, a C source debugger, a design kit, a starter kit, and a third-party microcontroller programmer from BP Microsystems. All of these tools work together by using an IBM™-compatible personal computer (PC) as the host and the central control element. This allows the user to select the host computer and text management as well as editing tools according to system requirements.

Additionally, the TMS370 in-circuit emulator [XDS™—extended development support, and CDT370 compact development tool (CDT™)] allows the user to immediately begin designing, testing, and debugging the system upon specification. The reason for this is straightforward: the emulator itself is modular and configurable, thereby eliminating the need to produce a new emulator for each TMS370 configuration.

typical applications

The TMS370 family of devices is the ideal choice for the applications shown in Table 1 because the newly added features (like the addition of multiple peripheral functions per device) have expanded the TMS370 family of microcontrollers, enhanced its performance, and opened up new application technologies.

Table 1. Typical Applications for TMS370 Family of Microcontroller Devices

APPLICATION AREA	APPLICATIONS	
Automotive	Climate control systems Cruise control Entertainment systems Instrumentation	Navigational systems Engine control Antilock braking
Computer	Keyboards Peripheral interface control	Disk controllers Terminals
Industrial	Motor control Temperature controllers Process control	Meter control Medical instrumentation Security systems
Telecommunications	Modems Intelligent phones Intelligent line card control	Telecopiers Debit cards

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device categories

The TMS370 category of devices is divided into fourteen families (see Table 2). All the families are supported by a full complement of development support tools. (For more information on the available development support tools, refer to the section on available development system support tools in Chapter 2.)

Table 2. TMS370 Family Categories and Their Corresponding Devices

FAMILY	DEVICES INCLUDED				
TMS370Cx0x	TMS370C002A	TMS370C302A	TMS370C702 [†]	SE370C702 [†]	
TMS370Cx1x	TMS370C010A TMS370C712A	TMS370C012A TMS370C712B	TMS370C310A SE370C712A [†]	TMS370C311A SE370C712B [†]	TMS370C312A
TMS370Cx2x	TMS370C020A SE370C722 [†]	TMS370C022A	TMS370C320A	TMS370C322A	TMS370C722
TMS370Cx32	TMS370C032A	TMS370C732A	TMS370C332A	SE370C732A [†]	
TMS370Cx36	TMS370C036A	TMS370C736A	SE370C736A [†]		
TMS370Cx4x	TMS370C040A SE370C742A [†]	TMS370C042A	TMS370C340A	TMS370C342A	TMS370C742A
TMS370Cx5x	TMS370C050A TMS370C150A TMS370C352A TMS370C456A SE370C756A [†]	TMS370C052A TMS370C156A TMS370C353A TMS370C756A SE370C758A [†]	TMS370C056A TMS370C250A TMS370C356A TMS370C758A SE370C758B [†]	TMS370C058A TMS370C256A TMS370C358A TMS370C758B SE370C759A [†]	TMS370C059A TMS370C350A TMS370C452A TMS370C759A
TMS370Cx6x	TMS370C067A SE370C768A [†]	TMS370C068A SE370C769A [†]	TMS370C069A	TMS370C768A	TMS370C769A
TMS370Cx7x	TMS370C077A	TMS370C777A	SE370C777A [†]		
TMS370Cx8x	TMS370C080A	TMS370C380A	TMS370C686A	SE370C686A [†]	
TMS370Cx9x	TMS370C090A	TMS370C792	SE370C792 [†]		
TMS370CxAx	TMS370C3A7A				
TMS370CxBx	TMS370C0B6A				
TMS370CxCx	TMS370C3C0A	TMS370C6C2A	SE370C6C2A [†]		

[†] These system evaluators are used only in a prototype environment. Their reliability has not been characterized.

key features

The TMS370 family is based on a register-to-register architecture that allows access to a register file (up to 256 bytes) in a single bus cycle. On-chip memory includes program memory (mask ROM or EPROM), static RAM, standby RAM, and data EEPROM.

The versatile on-chip peripheral functions include an analog-to-digital converter (ADC1, ADC2, or ADC3), a serial communications interface (SCI1 or SCI2), a serial peripheral interface (SPI), three different timer modules (T1, T2A, and T2B), and up to 55 digital input/output (I/O) pins. The number and type of peripheral functions (modules) is dependent on the TMS370 family of devices.

The following are key features of the TMS370 device family (not all features are available for all devices):

- Compatibility for supporting software migration between current and future microcontrollers
- CMOS EPROM technology for providing reprogrammable EPROM and one-time programmable (OTP) program memory for prototypes and for small-volume or quick-turn production
- CMOS EEPROM technology for providing EEPROM programming with a single 5-V supply
- ADC technology for converting analog signals to digital values
- Static RAM/registers that offer numerous memory options
- Standby RAM that offers data protection in power-off condition
- Programmable (asynchronous and isosynchronous[†]) built-in serial communications interface for control of timing, data format, and protocol
- Serial peripheral interface for providing single-mode synchronous data transmission from the CPUs to any external peripheral devices
- Flexible operating features:
 - Power-reduction-standby and halt modes
 - Temperature options:
 - 0°C to 70°C operating temperature (L)
 - 40°C to 85°C operating temperature (A)
 - 40°C to 105°C operating temperature (T)
 - Input clock frequency options:
 - Divide-by-4 (0.5 MHz to 5 MHz SYSCLK) standard oscillator
 - Divide-by-1 (2 MHz to 5 MHz SYSCLK) phase-locked loop (PLL)
 - Operating voltage range: 5 V +10%
- Flexible interrupt handling for design flexibility:
 - Two programmable interrupt levels
 - Programmable rising-edge or falling-edge detect
- System integrity features that increase flexibility during the software development phase:
 - Oscillator fault detection
 - Privileged mode lockout
 - Watchdog timer
 - Memory security (for ROM)

[†] Isosynchronous = isochronous

key features (continued)

- Memory-mapped ports for easy addressing
- An optimizing C compiler that translates ANSI C programs into '370 assembly language source
- A high-level language debugger that lets the user refine and correct code
- A modular library for quickly changing the device configurations
- Eighteen addressing modes that use eight formats, including:
 - Implied
 - Register-to-register arithmetic
 - Indirect addressing
 - Indexed and indirect branches and calls
 - PC relative
- 250-mA typical latch-up immunity at 25°C
- Electrostatic discharge (ESD) protection that exceeds 2,000 V per MIL-STD-883C method 3015, making the TMS370 families Class 2 ESD-sensitive devices

TMS370 major components architecture

In addition to the features listed in the key features section, the TMS370 family members have the following architectural features. Not all features (key or architectural) are applicable to all devices (see Table 1 in Chapter 2). The selection reference guide in Chapter 2, summarizes the following features and identifies the applicable devices associated with those features.

CPU

The TMS370 8-bit CPU has a status register, program-counter register, and stack pointer. The CPU uses the register file as working registers that are accessed on the internal bus in one bus cycle. The 8-bit internal bus also allows access to memory and to the peripheral interfaces. TMS370Cx5x, TMS370Cx6x, TMS370Cx7x, and TMS370CxBx devices all allow external memory expansion through ports A, B, C, and D.

register file (RF)

The register file is located at the beginning of the TMS370 memory map. Register-access instructions in the TMS370 instruction set allow access to any of the first 256 registers (if available) in one bus cycle. This segment of the memory map is used as general-purpose RAM and as the stack.

RAM

RAM modules, other than those contained in the register file, are mapped after the register file. The TMS370 accesses this RAM in two cycles.

data EEPROM

With the exception of the TMS370CxAx and TMS370CxCx families, certain devices in the TMS370 family have EEPROM. The data EEPROM modules provide in-circuit programmability and data retention in power-off mode. The modules contain 256 or 512 bytes of EEPROM. This memory is useful for storing constants and infrequently changed variables that are required by the application program. The EEPROM can be programmed and erased by using available EEPROM programmers or by the TMS370 device under program control.



program memory (ROM/EPROM)

The program memory provides alternatives to meet the needs of different applications. The program memory modules presently contain 2K, 4K, 8K, 16K, 24K, 32K, or 48K bytes of memory. The program memory in TMS370C6xx, SE370C6xx, TMS370C7xx, and SE370C7xx devices is EPROM. EPROM devices in a windowed ceramic package can be programmed, erased, and reprogrammed for prototyping. EPROM devices in a non-windowed plastic package are one-time programmable (OTP) devices that are used for small production runs. In the TMS370C0xx, TMS370C3xx, and TMS370C4xx devices, the program memory is mask-ROM that is programmed at the factory. ROM devices are appropriate for large-volume production.

input/output ports

The TMS370 family of devices has a varying number of I/O ports that have various port widths. Table 3 lists the available I/O port widths, by the number of bits, for each of the different TMS370 families.

Table 3. Bits Per Port for TMS370 Devices

FAMILIES†	BITS FOR PORTS A – H					
	A	B	C	D	G	H
x0x, x1x	8			5		
x2x	8	8	1	5		
x32	8			4		
x36	8			5		
x4x	8	3		5		
x5x – (64 pins)	8‡	8‡	8‡	6‡		
x5x – (68 pins)	8‡	8‡	8‡	8‡		
x6x	8‡	8‡	8‡	5‡		
x7x – (64 pins)	8‡	8‡	8‡	6‡	6	
x7x – (68 pins)	8‡	8‡	8‡	8‡	6	
x8x – (40 pins)	8	8	6	5		
x8x – (44 pins)	8	8	8	5		
x9x	8			5		
xAx	8	8	1	5		
xBx – (64 pins)	8‡	8‡	8‡	6‡	8	1
xBx – (68 pins)	8‡	8‡	8‡	8‡	8	1
xCx	8			4		

† For all families, the ports for these microcontrollers can be programmed, bit by bit, to function as either digital input or digital output.

‡ These ports can be configured by the software as the data, control, and address buses for external memory. Any bits not needed for external memory can be programmed to be either digital input or digital output.

timer 1

Timer 1 is a 16-bit timer that can be configured in the following ways:

- A programmable 8-bit prescaler (provide a 24-bit real-time timer) that determines the independent clock sources for the general-purpose timer and the watchdog (WD) timer
- A 16-bit event timer, to keep a cumulative total of the transitions
- A 16-bit pulse accumulator, to measure the pulse-input width
- A 16-bit input-capture function that latches the counter value on the occurrence of an external input
- Two 16-bit compare registers that trigger when the counter matches the contents of a compare register
- A self-contained pulse-width modulated (PWM) output control function

timer 1 (continued)

The results of these operations can generate an interrupt to the CPU, set flag bits, reset the timer counter, toggle an I/O line, or generate PWM outputs. Timer 1 can provide up to 200 ns of resolution with a 5-MHz system clock (SYSCLK).

timer 2n (A and B)

Timer 2A and 2B are 16-bit timers that can be configured in the following ways:

- Four independent clock sources for the general-purpose timer
- A 16-bit event timer, to keep a cumulative total of the transitions
- A 16-bit pulse accumulator, to measure the pulse-input width
- Two 16-bit input-capture devices that change a counter value on the occurrence of an external input
- Two 16-bit compare registers that trigger when a counter matches the contents of a compare register
- A self-contained PWM output controller

The results of these timer operations can generate an interrupt to the CPU, set flag bits, reset the timer counter, toggle an I/O line, or generate PWM outputs. Timers 2A and 2B can provide up to 200 ns of resolution with a 5-MHz system clock (SYSCLK).

watchdog timer

The watchdog timer helps ensure system integrity. It can be programmed to generate a hardware reset when it times out. This function provides a hardware monitor over the software to avoid losing a program. If not needed as a watchdog, this timer can be used as a general-purpose timer.

programmable acquisition and control timer (PACT)

The PACT module in the 'Cx32 and 'Cx36 device categories is a programmable timing module that uses some of the on-chip RAM to store its commands as well as the timer values. Only the TMS370Cx36 device offers the 256-byte standby RAM that protects stored data against power failures. The PACT module offers the following:

- Input capture on up to six pins, four of which may have a programmable prescaler
- One input-capture pin that can drive an 8-bit event counter
- Up to eight timer-driven outputs
- Timer capability of up to 20 bits
- Interaction between event counter and timer activity
- Eighteen independent interrupt vectors to allow better servicing of events
- Watchdog with selectable time-out period
- Mini-SCI (serial communications interface) that works as a full duplex UART (universal asynchronous receiver transmitter)

Once set up, the PACT requires no CPU overhead except to service interrupts.

serial communications interface (SCI1 or SCI2)

The term SCI is used frequently to refer to SCI1 and SCI2. The SCI1 and SCI2 modules are built-in serial interfaces. The SCI1 has a 3-pin configuration and SCI2 has a 2-pin configuration. Both offer the following features:

- Programmable to be asynchronous (up to 156 Kbps)
- Full duplex, double-buffered receive (Rx) and transmit (Tx)
- Programmable format with error-checking capabilities

The following feature is available only on the SCI1 module:

- Programmable to be isosynchronous (up to 2.5 Mbps)

The SCI1 and SCI2 modules program and control all timing, data format, and protocol factors. The CPU takes part in the serial communications only:

- To write data transmitted to the registers in the SCI
- To read received data from the registers in the SCI when interrupted

serial peripheral interface (SPI)

The SPI module is a built-in serial interface that facilitates communication between the network master, slave CPUs, and the external peripheral devices. The SPI module provides synchronous data transmission of up to 2.5 Mbps. Like the SCI, the SPI is set up by software. Once setup, the CPU takes no part in timing, data format, or protocol. Also, like the SCI, the CPU reads and writes to memory-mapped registers to receive and transmit data. An SPI interrupt alerts the CPU when received data is ready.

analog-to-digital converter (ADC1, ADC2, ADC3) modules

The 8-bit ADC modules perform successive approximation conversion. The term ADC is a general term used for ADC1, ADC2, and ADC3 modules. The ADCs offer the following number of input channels for each of the specified microcontroller families:

- ADC1 offers the following:
 - Four channels in the 40-pin devices of the 'x4x family,
 - Eight channels in the 44-pin devices of the 'x4x, 'x32, and 'x36 families
 - Eight channels in the 64-pin and 68-pin devices of the 'x5x, 'x6x, 'x7x, and 'xBx families
- ADC2 offers four channels in the 28-pin devices of the 'xCx family
- ADC3 offers 15 channels in the 40-pin and 44-pin devices of the 'x9x family

The reference source and input channel are selectable. The user can program the conversion result to be the ratio of the input voltage to the reference voltage or the ratio of one analog input to another. Input lines that are not required for analog-to-digital conversion can be programmed to be digital input lines.

For a detailed explanation on any of the major components of the TMS370 device family, refer to the TMS370 8-Bit Microcontroller User's Guide (literature number SPNU127) or to the specific data sheet in a device category.

For more details on the programming of the TMS370 family or for further expansion on the applications of these devices, refer to the section on related documentation from Texas Instruments.

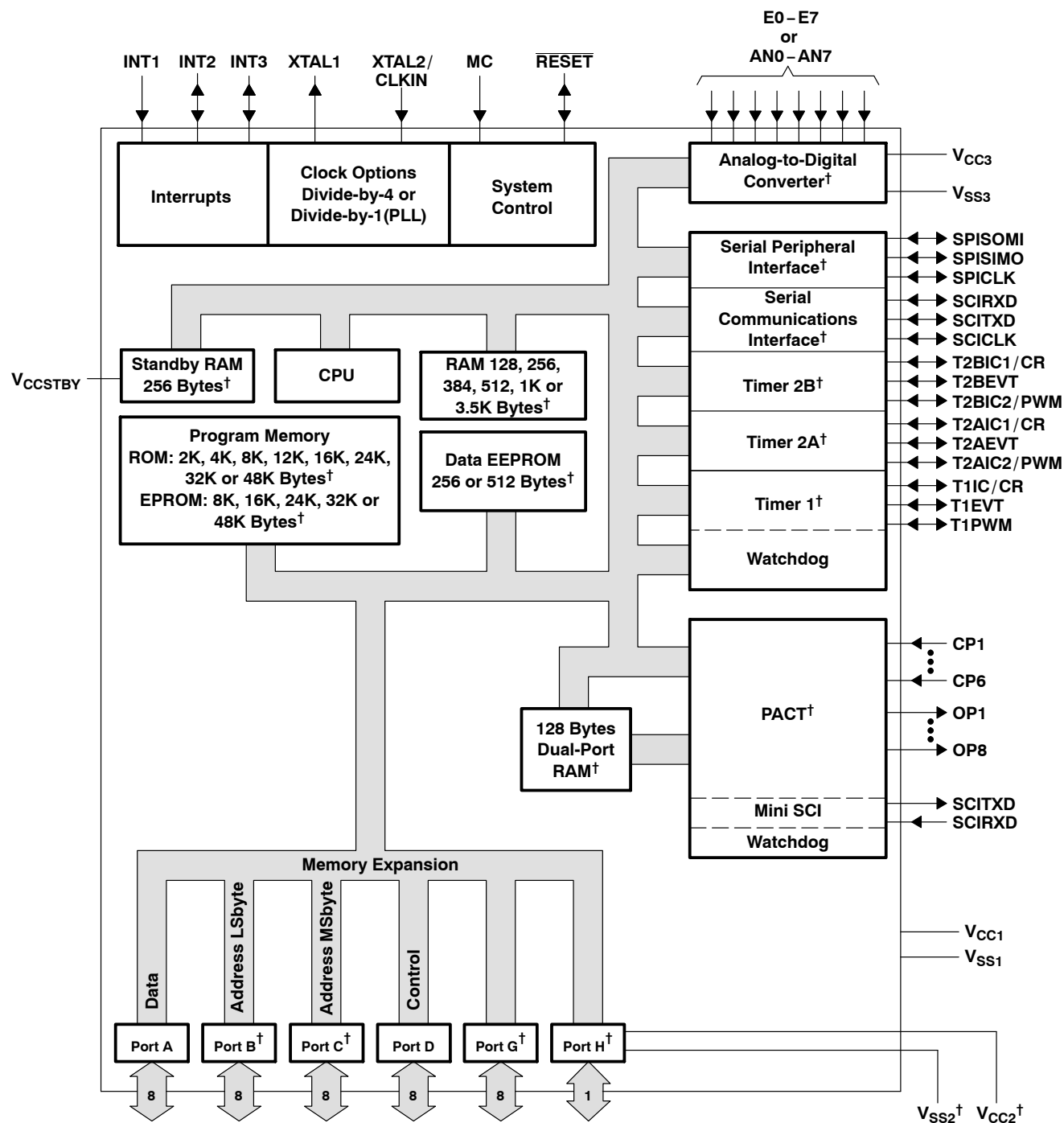
summary of components by device types

The major components of the TMS370 family devices (discussed in the TMS370 major components architecture section) are summarized in Chapter 2, Table 1 (selection reference guide) and Table 2 (development system support tools).

functional-block-diagram generalization

This section contains a functional-block-diagram generalization for the TMS370 microcontroller families (that is, 'x0x, 'x1x, 'x2x, 'x32, 'x36, 'x4x, ..., 'xCx). Because this diagram is a generalization, it depicts all the modules available for the TMS370 families, with the understanding that no one TMS370 device contains all available options. The diagram also shows the basic internal connections among the major architectural features that are identified in the selection guide in Chapter 2. For a functional block diagram of a specific TM370 family, the pinouts, the descriptions of the pinouts, and descriptions of the external connection names, refer to the applicable data sheet contained in Chapters 4 through 17.

functional-block-diagram generalization of the TMS370 families

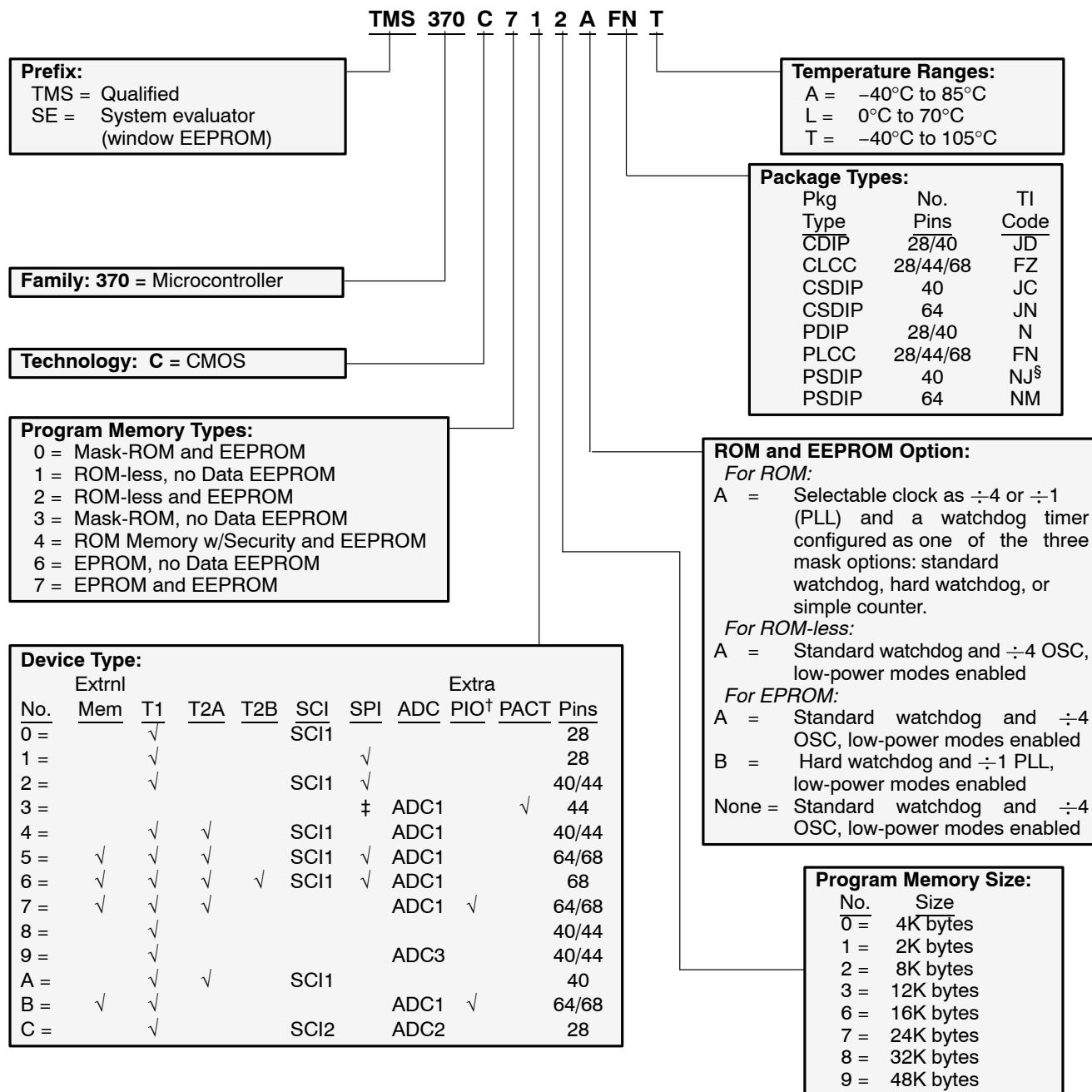


[†] Not available on all devices; see the selection reference guide (Chapter 2).

alphanumeric index of devices

SE370C686A	13-1	TMS370C050A	10-1	TMS370C352A	10-1
SE370C6C2A	17-1	TMS370C052A	10-1	TMS370C353A	10-1
SE370C702	4-1	TMS370C056A	10-1	TMS370C356A	10-1
SE370C712A	5-1	TMS370C058A	10-1	TMS370C358A	10-1
SE370C712B	5-1	TMS370C059A	10-1	TMS370C380A	13-1
SE370C722	6-1	TMS370C067A	11-1	TMS370C3A7A	15-1
SE370C732A	7-1	TMS370C068A	11-1	TMS370C3C0A	17-1
SE370C736A	8-1	TMS370C069A	11-1	TMS370C452A	10-1
SE370C742A	9-1	TMS370C077A	12-1	TMS370C456A	10-1
SE370C756A	10-1	TMS370C080A	13-1	TMS370C6C2A	17-1
SE370C758A	10-1	TMS370C090A	14-1	TMS370C686A	13-1
SE370C758B	10-1	TMS370C0B6A	16-1	TMS370C702	4-1
SE370C759A	10-1	TMS370C150A	10-1	TMS370C712A	5-1
SE370C768A	11-1	TMS370C156A	10-1	TMS370C712B	5-1
SE370C769A	11-1	TMS370C250A	10-1	TMS370C722	6-1
SE370C777A	12-1	TMS370C256A	10-1	TMS370C732A	7-1
SE370C792	14-1	TMS370C302A	4-1	TMS370C736A	8-1
TMS370C002A	4-1	TMS370C310A	5-1	TMS370C742A	9-1
TMS370C010A	5-1	TMS370C311A	5-1	TMS370C756A	10-1
TMS370C012A	5-1	TMS370C312A	5-1	TMS370C758A	10-1
TMS370C020A	6-1	TMS370C320A	6-1	TMS370C758B	10-1
TMS370C022A	6-1	TMS370C322A	6-1	TMS370C759A	10-1
TMS370C032A	7-1	TMS370C332A	7-1	TMS370C768A	11-1
TMS370C036A	8-1	TMS370C340A	9-1	TMS370C769A	11-1
TMS370C040A	9-1	TMS370C342A	9-1	TMS370C777A	12-1
TMS370C042A	9-1	TMS370C350A	10-1	TMS370C792	14-1

device-numbering conventions



[†] Extra peripheral I/O

[‡] For device type No. 3 the TMS370Cx32 device has no SPI; the TMS370Cx36 device has a SPI.

[§] NJ package was formerly known as N2.

Figure 1. TMS370C Family Nomenclature

available development-system-support tools

As previously stated, the TMS370 family is fully supported by TI development tools that facilitate simplified software development for prompt market introduction of new products. These tools include an assembler, an optimizing C compiler, a linker, a C source debugger, a design kit, a starter kit, and a third-party microcontroller programmer from BP Microsystems. All of these tools work together by using an IBM-compatible PC as the host and central control element. This allows the user to select the host computer and text management as well as editing tools according to system requirements.

Additionally, the TMS370 in-circuit emulator (XDS and CDT370 Compact Development Tool) allows the user to immediately begin designing, testing, and debugging the system upon specification. The reason for this is straightforward: the emulator itself is modular and configurable, thereby eliminating the need to produce a new emulator for each TMS370 configuration.

For a list of the available development-system-support tools, identified by device category, refer to the TMS370 Development System Support Tools table in Chapter 2 or to the specific TMS370 device data sheet.

For more detailed information on the development-system-support tools, refer to the TMS370 8-Bit Microcontroller User's Guide (literature number SPNU127) or to the documents listed in the section titled related documentation from Texas Instruments.



related documentation from Texas Instruments/Further Assistance Information

The following books describe the TMS370 family devices and related support tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924. When ordering, please identify the book by its title and literature number.

TMS370 Family Assembly Language Tools User's Guide (literature number SPNU010) describes the assembly language tools (assembler, linker, and other tools used to develop assembly code), assembler directives, macros, common object-file format, and symbolic debugging directives for the '370 family of devices.

TMS370 Family Optimizing C Compiler User's Guide (literature number SPNU022) describes the '370 C compiler. This C compiler accepts ANSI standard C source code and produces assembly language source code for the '370 family of devices.

TMS370 Family C Source Debugger User's Guide (literature number SPNU028) tells you how to invoke the TMS370 family application board and XDS versions of the C source debugger interface. This book discusses various aspects of the debugger interface, including window management, command entry, code execution, data management, and breakpoints. It also includes a tutorial that introduces basic debugger functionality.

TMS370 Microcontroller Family User's Guide (literature number SPNU127) describes the TMS 370 family of microcontroller devices and provides the user with the information needed to implement a microcontroller design using a TMS370 device.

TMS370 Microcontroller Family Applications Book (literature number SPNA017) provides examples of hardware interfaces and software routines for the TMS370 family of microcontrollers.

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Ask questions about product operation or report suspected problems	Call the Microcontroller Hotline: (713) 274-2370 Fax: (713) 274-4203
Product Information	View the Web Page: http://www.ti.com/sc/micro Call the Product Information Center: (214) 644-5580
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introduction to selection guide and development-systems-support tools

Chapter 2 contains a selection reference guide and a table listing of the available development support tools for the TMS370 family.

selection reference guide

The selection guide shown in Table 1 provides the user with an easy-to-use selection guide that includes the following specific device information by device groups: product family description (device type, part number, package and temperature options, and pin count); memory [program memory (ROM, EPROM), data memory (EEPROM, RAM) and any capability of off-chip memory expansion]; and peripherals (timers, serial interfaces, A/D channels, I/O, clock generators, and OTP and reprogrammable devices). The following symbol footnotes are used in Table 1:

- † Packages: FN = PLCC, FZ = CLCC, N = PDIP, JD = CDIP, NJ = PSDIP (formerly N2), JC = CSDIP, NM = PSDIP, JN = CSDIP
- ‡ Temperatures: ROM device types have L = 0°C to +70°C, A = – 40°C to +85°C, and T = – 40°C to +105°C temperature options; ROM-less, OTP and UV-EPROM device types only have T.
- § PACT SCI: PACT includes a mini-SCI. SCI1 module has 3-pin configuration while SCI2 module has 2-pin configuration.
- ¶ RAM: Includes 256 bytes of standby RAM
- # Memory: Includes secured memory feature
- || Max Freq: Supports maximum operating frequency of 3 MHz SYSCLK
- ☆ PACT WDOG: PACT includes a watchdog timer
- ADC1 Channels: 8 channels A/D for 44 pin package, 4 channels A/D for 40 pin package
- ◇ Timers: Timer 1 (T1) includes a watchdog timer programmable as a general purpose 16-bit timer
- Ψ 44/40 Packages: 44 pins for FN, FZ packages. 40 pins for N, JD, NJ (formerly N2), JC packages.
- Φ 68/64 Packages: 68 pins for FN, FZ packages. 64 pins for NM, JN packages
- ¥ TMS370Cx Cx SCI: Operable in asynchronous mode only
- Δ Converter Socket: Requires a TMDS37788OTP converter socket
- ♣ Requires software modification (refer to the *TMS370Cx Bx Data Sheet* (literature number SPNS038) – (Chapter 16)

Table 1 is a continuous table and only the applicable symbol footnotes are listed on each page.

development-systems-support tools

The TMS370 development system support tools listing shown in Table 2 identifies the available development support tools (by tool description and part number) for each of the TMS370 device families ('x0x, 'x1x, 'x2x, 'x32, 'x36, ..., 'xCx).

Table 1. TMS370 8-Bit Microcontroller Product Configurations

DEVICE TYPE‡	PART NUMBER “yy”= PACKAGE “z” =TEMP	PACAKGE OPTIONS “yy”†	PACKAGE PIN COUNT	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		OFF-CHIP MEM EXP (BYTES)	TIMERS◇	SERIAL INTERFACE§	A/D CHANNELS	I/O	CLOCK GENERATOR	OTP AND REPROGRAMMABLE DEVICES
				ROM	EPROM	EEPROM	RAM							
TMS370Cx0x														
ROM	TMS370C302Ayyz	FN	28	8K			256		T1	SCI1		22	÷4 or PLL	C702
ROM	TMS370C002Ayyz	FN	28	8K		256	256		T1	SCI1		22	÷4 or PLL	C702
OTP	TMS370C702yyz	FN	28		8K	256	256		T1	SCI1		22	÷4	—
UV-EPROM	SE370C702yyz	FZ	28		8K	256	256		T1	SCI1		22	÷4	—
TMS370Cx1x														
ROM	TMS370C311Ayyz	FN/N	28	2K			128		T1	SPI		22	÷4 or PLL	C712
ROM	TMS370C310Ayyz	FN/N	28	4K			128		T1	SPI		22	÷4 or PLL	C712
ROM	TMS370C010Ayyz	FN/N	28	4K		256	128		T1	SPI		22	÷4 or PLL	C712
ROM	TMS370C312Ayyz	FN/N	28	8K			128		T1	SPI		22	÷4 or PLL	C712
ROM	TMS370C012Ayyz	FN/N	28	8K		256	256		T1	SPI		22	÷4 or PLL	C712
OTP	TMS370C712Ayyz	FN/N	28		8K	256	256		T1	SPI		22	÷4	—
OTP	TMS370C712Byyz	FN/N	28		8K	256	256		T1	SPI		22	PLL	—
UV-EPROM	SE370C712Ayyz	FZ/JD	28		8K	256	256		T1	SPI		22	÷4	—
UV-EPROM	SE370C712Byyz	FZ/JD	28		8K	256	256		T1	SPI		22	PLL	—
TMS370Cx2x														
ROM	TMS370C320Ayyz	FN/N/NJ	44/40 ^Ψ	4K			256		T1	SPI/SCI1		34	÷4 or PLL	C722
ROM	TMS370C322Ayyz	FN/N/NJ	44/40 ^Ψ	8K			256		T1	SPI/SCI1		34	÷4 or PLL	C722
ROM	TMS370C020Ayyz	FN/N/NJ	44/40 ^Ψ	4K		256	256		T1	SPI/SCI1		34	÷4 or PLL	C722
ROM	TMS370C022Ayyz	FN/N/NJ	44/40 ^Ψ	8K		256	256		T1	SPI/SCI1		34	÷4 or PLL	C722
OTP	TMS370C722yyz	FN/N/NJ	44/40 ^Ψ		8K	256	256		T1	SPI/SCI1		34	÷4	—
UV-EPROM	SE370C722yyz	FZ/JD/JC	44/40 ^Ψ		8K	256	256		T1	SPI/SCI1		34	÷4	—

[†] Packages: FN = PLCC, FZ = CLCC, N = PDIP, JD = CDIP, NJ = PSDIP (formerly N2), JC = CSDIP, NM = PSDIP, JN = CSDIP

[‡] Temperatures: ROM device types have L = 0°C to +70°C, A = -40°C to +85°C, and T = -40°C to +105°C temperature options; ROM-less, OTP and UV-EPROM device types only have T.

[§] PACT SCI: PACT includes a mini-SCI. SCI1 module has 3-pin configuration while SCI2 module has 2-pin configuration.

[◇] Timers: Timer 1 (T1) includes a watchdog timer programmable as a general purpose 16-bit timer

^Ψ 44/40 Packages: 44 pins for FN, FZ packages. 40 pins for N, JD, NJ (formerly N2), JC packages.

Table 1. TMS370 8-Bit Microcontroller Product Configurations (Continued)

DEVICE TYPE‡	PART NUMBER “yy” = PACKAGE “z” =TEMP	PACAKGE OPTIONS “yy”†	PACKAGE PIN COUNT	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		OFF-CHIP MEM EXP (BYTES)	TIMERS◇	SERIAL INTERFACES§	A/D CHANNELS	I/O	CLOCK GENERATOR	OTP AND REPROGRAMMABLE DEVICES
				ROM	EPROM	EEPROM	RAM							
TMS370Cx3x														
ROM	TMS370C332Ayyz	FN	44	8K			256		PACT☆	PACT	ADC1/8	23	÷4 or PLL	C732
ROM	TMS370C032Ayyz	FN	44	8K		256	256		PACT☆	PACT	ADC1/8	23	÷4 or PLL	C732
ROM	TMS370C036Ayyz	FN	44	16K		256	512¶		PACT☆	SPI/PACT	ADC1/8	25	÷4 or PLL	C736
OTP	TMS370C732Ayyz	FN	44		8K	256	256		PACT☆	PACT	ADC1/8	23	÷4	—
OTP	TMS370C736Ayyz	FN	44		16K	256	512¶		PACT☆	SPI/PACT	ADC1/8	25	÷4	—
UV-EPROM	SE370C732Ayyz	FZ	44		8K	256	256		PACT☆	PACT	ADC1/8	23	÷4	—
UV-EPROM	SE370C736Ayyz	FZ	44		16K	256	512¶		PACT☆	SPI/PACT	ADC1/8	25	÷4	—
TMS370Cx4x														
ROM	TMS370C340Ayyz	FN/N/NJ	44/40Ψ	4K			256		T1/T2a	SCI1	ADC1/8, 4□	36/32	÷4 or PLL	C742
ROM	TMS370C342Ayyz	FN/N/NJ	44/40Ψ	8K			256		T1/T2a	SCI1	ADC1/8, 4□	36/32	÷4 or PLL	C742
ROM	TMS370C040Ayyz	FN/N/NJ	44/40Ψ	4K		256	256		T1/T2a	SCI1	ADC1/8, 4□	36/32	÷4 or PLL	C742
ROM	TMS370C042Ayyz	FN/N/NJ	44/40Ψ	8K		256	256		T1/T2a	SCI1	ADC1/8, 4□	36/32	÷4 or PLL	C742
OTP	TMS370C742Ayyz	FN/N/NJ	44/40Ψ		8K	256	256		T1/T2a	SCI1	ADC1/8, 4□	36/32	÷4	—
UV-EPROM	SE370C742Ayyz	FZ/JD/JC	44/40Ψ		8K	256	256		T1/T2a	SCI1	ADC1/8, 4□	36/32	÷4	—
TMS370Cx5x														
ROM-less	TMS370C150Ayyz	FN	68				256	56K	T1/T2a	SPI/SCI1	ADC1/8	55	÷4	C756
ROM-less	TMS370C250Ayyz	FN	68			256	256	56K	T1/T2a	SPI/SCI1	ADC1/8	55	÷4	C756
ROM-less	TMS370C156Ayyz	FN	68				512	56K	T1/T2a	SPI/SCI1	ADC1/8	55	÷4	C756
ROM-less	TMS370C256Ayyz	FN	68			512	512	56K	T1/T2a	SPI/SCI1	ADC1/8	55	÷4	C756
ROM	TMS370C350Ayyz	FN/NM	68/64Φ	4K			256	112K	T1/T2a	SPI/SCI1	ADC1/8	55/53	÷4 or PLL	C756
ROM	TMS370C050Ayyz	FN/NM	68/64Φ	4K		256	256	112K	T1/T2a	SPI/SCI1	ADC1/8	55/53	÷4 or PLL	C756
ROM	TMS370C352Ayyz	FN/NM	68/64Φ	8K			256	112K	T1/T2a	SPI/SCI1	ADC1/8	55/53	÷4 or PLL	C756
ROM	TMS370C052Ayyz	FN/NM	68/64Φ	8K		256	256	112K	T1/T2a	SPI/SCI1	ADC1/8	55/53	÷4 or PLL	C756
ROM	TMS370C452Ayyz	FN	68	8K#		256	256	112K	T1/T2a	SPI/SCI1	ADC1/8	55	÷4 or PLL	C756
ROM	TMS370C353Ayyz	FN	68	12K			1536	112K	T1/T2a	SPI/SCI1	ADC1/8	55	÷4 or PLL	C759

† Packages: FN = PLCC, FZ = CLCC, N = PDIP, JD = CDIP, NJ = PSDIP (formerly N2), JC = CSDIP, NM = PSDIP, JN = CSDIP

‡ Temperatures: ROM device types have L = 0°C to +70°C, A = - 40°C to +85°C, and T = - 40°C to +105°C temperature options; ROM-less, OTP and UV-EPROM device types only have T.

§ PACT SCI: PACT includes a mini-SCI. SCI1 module has 3-pin configuration while SCI2 module has 2-pin configuration.

¶ RAM: Includes 256 bytes of standby RAM

Memory: Includes secured memory feature

☆PACT WDOG: PACT includes a watchdog timer

□ADC1 Channels: 8 channels A/D for 44 pin package, 4 channels A/D for 40 pin package

◇ Timers: Timer 1 (T1) includes a watchdog timer programmable as a general purpose 16-bit timer

Ψ 44/40 Packages: 44 pins for FN, FZ packages. 40 pins for N, JD, NJ (formerly N2), JC packages.

Φ 68/64 Packages: 68 pins for FN, FZ packages. 64 pins for NM, JN packages

Table 1. TMS370 8-Bit Microcontroller Product Configurations (Continued)

DEVICE TYPE‡	PART NUMBER “yy” = PACKAGE “z” = TEMP	PACAKGE OPTIONS “yy”†	PACKAGE PIN COUNT	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		OFF- CHIP MEM EXP (BYTES)	TIMERS◇	SERIAL INTERFACE§	A/D CHANNELS	I/O	CLOCK GENERATOR	OTP AND REPROGRAMMABLE DEVICES
				ROM	EPROM	EEPROM	RAM							
TMS370Cx5x (CONTINUED)														
ROM	TMS370C356Ayyz	FN/NM	68/64Φ	16K			512	112K	T1/T2a	SPI/SCI1	ADC1/8	55/53	÷4 or PLL	C756
ROM	TMS370C456Ayyz	FN	68	16K#		512	512	112K	T1/T2a	SPI/SCI1	ADC1/8	55	÷4 or PLL	C756
ROM	TMS370C056Ayyz	FN/NM	68/64Φ	16K		512	512	112K	T1/T2a	SPI/SCI1	ADC1/8	55/53	÷4 or PLL	C756
ROM	TMS370C358Ayyz	FN/NM	68/64Φ	32K			1024	64K	T1/T2a	SPI/SCI1	ADC1/8	55/53	÷4 or PLL	C758
ROM	TMS370C058Ayyz	FN/NM	68/64Φ	32K		256	1024	64K	T1/T2a	SPI/SCI1	ADC1/8	55/53	÷4 or PLL	C758
ROM	TMS370C059Ayyz	FN	68	48K		256	3584	20K	T1/T2a	SPI/SCI1	ADC1/8	55	÷4 or PLL	C759
OTP	TMS370C756Ayyz	FN/NM	68/64Φ		16K	512	512	112K	T1/T2a	SPI/SCI1	ADC1/8	55/53	÷4	—
OTP	TMS370C758Ayyz	FN/NM	68/64Φ		32K	256	1024	64K	T1/T2a	SPI/SCI1	ADC1/8	55/53	÷4	—
OTP	TMS370C758Byyz	FN/NM	68/64Φ		32K	256	1024	64K	T1/T2a	SPI/SCI1	ADC1/8	55/53	PLL	—
OTP	TMS370C759Ayyz	FN	68		48K	256	3584	20K	T1/T2a	SPI/SCI1	ADC1/8	55	÷4	—
UV-EPROM	SE370C756Ayyz	FZ/JN	68/64Φ		16K	512	512	112K	T1/T2a	SPI/SCI1	ADC1/8	55/53	÷4	—
UV-EPROM	SE370C758Ayyz	FZ/JN	68/64Φ		32K	256	1024	64K	T1/T2a	SPI/SCI1	ADC1/8	55/53	÷4	—
UV-EPROM	SE370C758Byyz	FZ/JN	68/64Φ		32K	256	1024	64K	T1/T2a	SPI/SCI1	ADC1/8	55/53	PLL	—
UV-EPROM	SE370C759Ayyz	FZ	68		48K	256	3584	20K	T1/T2a	SPI/SCI1	ADC1/8	55	÷4	—
TMS370Cx6x														
ROM	TMS370C067Ayyz	FN	68	24K		256	1024	24K	T1/T2a/T2b	SPI/SCI1	ADC1/8	55	÷4 or PLL	C768
ROM	TMS370C068Ayyz	FN	68	32K		256	1024	24K	T1/T2a/T2b	SPI/SCI1	ADC1/8	55	÷4 or PLL	C768
ROM	TMS370C069Ayyz	FN	68	48K		256	3584	8K	T1/T2a/T2b	SPI/SCI1	ADC1/8	55	÷4 or PLL	C769
OTP	TMS370C768Ayyz	FN	68		32K	256	1024	24K	T1/T2a/T2b	SPI/SCI1	ADC1/8	55	÷4	—
OTP	TMS370C769Ayyz	FN	68		48K	256	3584	8K	T1/T2a/T2b	SPI/SCI1	ADC1/8	55	÷4	—
UV-EPROM	SE370C768Ayyz	FZ	68		32K	256	1024	24K	T1/T2a/T2b	SPI/SCI1	ADC1/8	55	÷4	—
UV-EPROM	SE370C769Ayyz	FZ	68		48K	256	3584	8K	T1/T2a/T2b	SPI/SCI1	ADC1/8	55	÷4	—

[†] Packages: FN = PLCC, FZ = CLCC, N = PDIP, JD = CDIP, NJ = PSDIP (formerly N2), JC = CSDIP, NM = PSDIP, JN = CSDIP

[‡] Temperatures: ROM device types have L = 0°C to +70°C, A = -40°C to +85°C, and T = -40°C to +105°C temperature options; ROM-less, OTP and UV-EPROM device types only have T.

[§] PACT SCI: PACT includes a mini-SCI. SCI1 module has 3-pin configuration while SCI2 module has 2-pin configuration.

^{||} Max Freq: Supports maximum operating frequency of 3 MHz SYSCLK

[◇] Timers: Timer 1 (T1) includes a watchdog timer programmable as a general purpose 16-bit timer

^Φ 68/64 Packages: 68 pins for FN, FZ packages. 64 pins for NM, JN packages

Table 1. TMS370 8-Bit Microcontroller Product Configurations (Continued)

DEVICE TYPE‡	PART NUMBER “yy” = PACKAGE “z” = TEMP	PACAKGE OPTIONS “yy”†	PACKAGE PIN COUNT	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		OFF-CHIP MEM EXP (BYTES)	TIMERS◇	SERIAL INTERFACE§	A/D CHANNELS	I/O	CLOCK GENERATOR	OTP AND REPROGRAMMABLE DEVICES
				ROM	EPROM	EEPROM	RAM							
TMS370Cx7x														
ROM	TMS370C077Ayyz	FN/NM	68/64 ^Φ	24K		256	512	64K	T1/T2a		ADC1/8	55/53	÷4 or PLL	C777
OTP	TMS370C777Ayyz	FN/NM	68/64 ^Φ		24K	256	512	64K	T1/T2a		ADC1/8	55/53	÷4	—
UV-EPROM	SE370C777Ayyz	FZ/JN	68/64 ^Φ		24K	256	512	64K	T1/T2a		ADC1/8	55/53	÷4	—
TMS370Cx8x														
ROM	TMS370C380Ayyz	FN	44	4K			128		T1			35	÷4 or PLL	C686
ROM	TMS370C080Ayyz	N	40	4K		256	128		T1			33	÷4 or PLL	C758 ^Δ
OTP	TMS370C686Ayyz	FN	44		16K		256		T1			35	÷4	—
UV-EPROM	SE370C686Ayyz	FZ	44		16K		256		T1			35	÷4	—
TMS370Cx9x														
ROM	TMS370C090Ayyz	FN/NJ	44/40 ^Ψ	4K		256	128		T1		ADC3/15	25	÷4 or PLL	C792
OTP	TMS370C792yyz	FN/NJ	44/40 ^Ψ		8K	256	128		T1		ADC3/15	25	÷4	—
UV-EPROM	SE370C792yyz	FZ/JC	44/40 ^Ψ		8K	256	128		T1		ADC3/15	25	÷4	—
TMS370CxAx														
ROM	TMS370C3A7Ayyz	N	40	24K			512		T1/T2a	SCI1		34	÷4 or PLL	C758 ^Δ
TMS370CxBx														
ROM	TMS370C0B6Ayyz	FN/NM	68/64 ^Φ	16K		256	384	112K	T1		8	55/53	÷4 or PLL	C758 [*]
TMS370CxCx														
ROM	TMS370C3C0Ayyz	FN/N	28	4K			128		T1	SCI2 [¥]	ADC2/4	22	÷4 or PLL	C6C2
OTP	TMS370C6C2Ayyz	FN/N	28		8K		128		T1	SCI2 [¥]	ADC2/4	22	÷4	—
UV-EPROM	SE370C6C2Ayyz	FZ/JD	28		8K		128		T1	SCI2 [¥]	ADC2/4	22	÷4	—

† Packages: FN = PLCC, FZ = CLCC, N = PDIP, JD = CDIP, NJ = PSDIP (formerly N2), JC = CSDIP, NM = PSDIP, JN = CSDIP

‡ Temperatures: ROM device types have L = 0°C to +70°C, A = – 40°C to +85°C, and T = – 40°C to +105°C temperature options; ROM-less, OTP and UV-EPROM device types only have T.

§ PACT SCI: PACT includes a mini-SCI. SCI1 module has 3-pin configuration while SCI2 module has 2-pin configuration.

◇ Timers: Timer 1 (T1) includes a watchdog timer programmable as a general purpose 16-bit timer

Ψ 44/40 Packages: 44 pins for FN, FZ packages. 40 pins for N, JD, NJ (formerly N2), JC packages.

Φ 68/64 Packages: 68 pins for FN, FZ packages. 64 pins for NM, JN packages

¥ TMS370CxCx SCI: Operable in asynchronous mode only

Δ Converter Socket: Requires a TMS37788OTP converter socket

♣ Requires software modification (refer to the *TMS370CxBx Data Sheet* (literature number SPNS038) – (Chapter 16)

Table 2. TMS370 Development System Support Tools

DEVELOPMENT TOOL DESCRIPTION	PART NUMBER	x0x	x1x	x2x	x32	x36	x4x	x5x	x6x	x7x	x8x	x9x	xAx	xBx	xCx
Assembler/Linker (PC)	TMDS3740850-02	√	√	√	√	√	√	√	√	√	√	√	√	√	√
C-Compiler, Assem/Link (PC)	TMDS3740855-02	√	√	√	√	√	√	√	√	√	√	√	√	√	√
C-Compiler, Assem/Link (WS)	TMDS3740555-09	√	√	√	√	√	√	√	√	√	√	√	√	√	√
TMS370 Starter Kit	TMDX37000	√	√	√	√	—	√	√	√	√	—	—	√	√	√
TMS370 Design Kit	TMDS3770110	√	√	—	—	—	—	√	—	—	—	—	—	—	√
TMS370 Compact Development Tool															
CDT370	EDSCDT370	√	√	√	—	—	√	√	—	—	√	—	√	—	√
CDT370 PACT	EDSCDT37P	—	—	—	√	√	—	—	—	—	—	√	—	—	—
CDT370 Timer	EDSCDT37T	—	—	—	—	—	—	—	√	√	—	—	—	√	—
CDT Target Cables															
28-Pin PLCC (x0x)	EDSTRG28PLCC02	√	—	—	—	—	—	—	—	—	—	—	—	—	—
28-Pin DIP (x1x)	EDSTRG28DIL	—	√	—	—	—	—	—	—	—	—	—	—	—	—
28-Pin PLCC (x1x)	EDSTRG28PLCC	—	√	—	—	—	—	—	—	—	—	—	—	—	—
40-Pin DIP (x2x)	EDSTRG40DILX	—	—	√	—	—	—	—	—	—	—	—	—	—	—
44-Pin PLCC (x2x)	EDSTRG44PLCCX	—	—	√	—	—	—	—	—	—	—	—	—	—	—
40-Pin SDIP (x2x)	EDSTRG40SDILX	—	—	√	—	—	—	—	—	—	—	—	—	—	—
44-Pin PLCC (x32)	EDSTRG44PLCC32	—	—	—	√	—	—	—	—	—	—	—	—	—	—
44-Pin PLCC (x36)	EDSTRG44PLCC36	—	—	—	—	√	—	—	—	—	—	—	—	—	—
40-Pin DIP (x4x)	EDSTRG40DIL	—	—	—	—	—	√	—	—	—	—	—	—	—	—
44-Pin PLCC (x4x)	EDSTRG44PLCC	—	—	—	—	—	√	—	—	—	—	—	—	—	—
40-Pin SDIP (x4x)	EDSTRG40SDIL	—	—	—	—	—	√	—	—	—	—	—	—	—	—
68-Pin PLCC (x5x, x6x, x7x, xBx)	EDSTRG68PLCC	—	—	—	—	—	—	√	√	√	—	—	—	√	—
64-Pin SDIP (x5x, x7x, xBx)	EDSTRG64SDIL	—	—	—	—	—	—	√	—	√	—	—	—	√	—
40-Pin DIP (x8x)	EDSTRG40DIL8X	—	—	—	—	—	—	—	—	—	√	—	—	—	—
44-Pin PLCC (x8x)	EDSTRG44PLCC8X	—	—	—	—	—	—	—	—	—	√	—	—	—	—
40-Pin SDIP (x9x)	EDSTRG40SDIL05	—	—	—	—	—	—	—	—	—	—	√	—	—	—
44-Pin PLCC (x9x)	EDSTRG44PLCC05	—	—	—	—	—	—	—	—	—	—	√	—	—	—
40-Pin DIP (xAx)	EDSTRG40DILAX	—	—	—	—	—	—	—	—	—	—	—	√	—	—
28-Pin PLCC (xCx)	EDSTRG28PLCCCX	—	—	—	—	—	—	—	—	—	—	—	—	—	√
28-Pin DIP (xCx)	EDSTRG28DILCX	—	—	—	—	—	—	—	—	—	—	—	—	—	√

Table 2. TMS370 Development System Support Tools (Continued)

DEVELOPMENT TOOL DESCRIPTION	PART NUMBER	x0x	x1x	x2x	x32	x36	x4x	x5x	x6x	x7x	x8x	x9x	xAx	xBx	xCx
TMS370 XDS/22 Emulator	TMD3762210	√	√	√	—	—	√	√	—	—	—	—	√	—	√
XDS Target Cable															
28-Pin DIP/PLCC	TMDS3788828	√	√	—	—	—	—	—	—	—	—	—	—	—	√
40-Pin DIP/SDIP, 44-Pin PLCC	TMDS3788844	—	—	√	—	—	√	—	—	—	—	—	√	—	—
68-Pin PLCC, 64-Pin SDIP	TMDS3788868	—	—	—	—	—	—	√	—	—	—	—	—	—	—
Converter Socket (from '758 to '080 or '3A7)	TMDS37788OTP	—	—	—	—	—	—	—	—	—	√	—	√	—	—
Programming Solutions															
BP1148TI Base	TMDS3760500A	√	√	√	√	√	√	√	√	√	√	√	√	√	√
Top/DIP (40-Pin DIP/SDIP, 28-Pin DIP, 64-Pin SDIP)	TMDS3780511A	—	√	√	—	—	√	√	—	√	√	—	√	√	√
Top/PLCC (44-Pin PLCC, 28-Pin PLCC, 68-Pin PLCC)	TMDS3780510A	√	√	√	√	—	√	√	√	√	√	—	—	√	√
Top/x36 (44-Pin PLCC x36)	TMDS3700572A	—	—	—	—	√	—	—	—	—	—	—	—	—	—
Top/x9x (44-Pin PLCC/ 40-Pin SDIP x9x)	TMDS3780513A	—	—	—	—	—	—	—	—	—	—	√	—	—	—

And for more information on the key features of the TMS370 Development Tools, and their current availability for PC-DOS and MS-DOS systems, refer to the TMS370 8-Bit Microcontroller User's Guide (literature number SPNU127).

third-party support

COMPANY	ADDRESS	PHONE NUMBER	TOOL	ENVIRONMENT
Allen Ashley	395 Sierra Madre Villa Pasadena, CA 91107	(818) 793-5748	Assembler/Linker	PC/MS-DOS
BP Microsystems	1000 North Post Oak Rd., Suite 225 Houston, TX 77055	(713) 688-4600 (800) 225-2102	Support (with adaptor top from TI) BP1148TI, BP1200 and BP2100 programmers	PC/MS-DOS
Data I/O	10525 Willows Rd., NE Redmond, WA 98073	(206) 881-6444	Programmers for TMS370; 3900, 2900 and Unisite	PC/MS-DOS
Logical Devices	130 Capitol Drive, Suites A & B Golden, CO 80401	(303) 279-6868	TMS370 Microcontroller Module for ALLPRO Programmers	ALLPRO Programmers
System General	1603 A South Main St. Milpitas, CA 95035	(408) 263-6667 (408) 263-6668	Support with Turpro-1/FX, Turpro-1/TX, Turpro-1, APRO, Turpro-832, and Turpro-840 programmers	PC/MS-DOS and Standalone

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Ops Cond/Timing/Glossary



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operating conditions and characteristics

current

high-level input current, I_{IH}

The current into an input when a high-level voltage is applied to that input.

high-level output current, I_{OH}

The current into an output with input conditions applied that, according to the product specification, establishes a high level at the output.

low-level input current, I_{IL}

The current into an input when a low-level voltage is applied to that input.

low-level output current, I_{OL}

The current into an output with input conditions applied that, according to the product specification, establishes a low level at the output.

supply current, I_{CC} , I_{CC2} , I_{CC3} , I_{PP} , I_{CCSTBY}

The current into, respectively, the ($V_{CC} = V_{CC1}$), V_{CC2} , V_{CC3} , V_{PP} , V_{CCSTBY} supply terminals.

operating free-air temperature, T_A

The temperature range over which the device operates and the range which meets the specified electrical characteristics.

voltage

high-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which of the logic element within specification limits is assured.

high-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that, according to the product specification, establishes a high level at the output.

low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values is used to represent the binary variables.

NOTE: The most positive value of low-level input voltage is specified for which operation of the logic element within specification limits is assured.

low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that, according to the product specification, establishes a low level at the output.

supply voltages, ($V_{CC} = V_{CC1}$), V_{CC2} , V_{CC3} , V_{PP} , and V_{CCSTBY}

The voltages supplied to the corresponding voltage pins that are required for the device to function. One to four of these supplies may be necessary, along with ground(s) ($V_{SS} = V_{SS1}$, V_{SS2} , and V_{SS3}).

time intervals

New or revised data sheets in this book use letter symbols in accordance with standards recently adopted by JEDEC, the IEEE, and the IEC. Two basic forms of symbols are used. The first form is used usually when intervals can be classified easily as cycle, hold, setup, transition, valid, or delay times and for pulse durations. The second form can be used generally, but in this book the second form is primarily for time intervals not easily classifiable. The second (unclassified) form is described first. Since some manufacturers use this form for all time intervals, symbols in the unclassified form are given with the examples for most of the classified time intervals.

unclassified time intervals

Generalized letter symbols can be used to identify almost any time interval without classifying it using traditional or contrived definitions. Symbols for unclassified time intervals identify two signal events listed in from-to sequence using the format:

$t_{(AB-CD)}$

Subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval.

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high

L = low or transition to low

V = a valid steady-state level

X = unknown, changing, or “don’t care” level

Z = high-impedance (off) state

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur.

classified time intervals

Because of the information contained in the definitions, frequently the identification of one or both of the two signal events that begin and end the intervals can be shortened significantly compared to the unclassified forms. For example, it is not necessary to indicate in the symbol that an access time ends with valid data at the output. However, if both signals are named (e.g., in a hold time), the from-to sequence is maintained.

cycle time

The time interval between the start and end of a cycle.

NOTE: For each cycle time (t_c), the value given represents the minimum time interval required to complete one cycle of the given function (e.g., read, write, etc.) correctly.

Example symbology:

Classified	Description
t_c	Cycle time, (SYSCLK)
$t_{c(SPC)}$	Cycle time, (SPICLK)
$t_{c(SCC)}$	Cycle time, (SCICLK)

hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is assured.
2. The hold time can have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is assured.

Example symbology:

Classified	Description
$t_{h(EH-A)}$	Hold time, address, R/ $\overline{W}$ and $\overline{OCF}$ from $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ high
$t_{h(EH-D)W}$	Hold time, write data time from $\overline{EDS}$ high
$t_{h(EH-D)R}$	Hold time, read time from $\overline{EDS}$ high
$t_{h(SCH-WT)}$	Hold time, $\overline{WAIT}$ time from SYSCLK high
$t_{h(AN)}$	Hold time, analog input from start of conversion

NOTE: The from-to sequence in the order of subscripts in the unclassified form is maintained in the classified form. In the case of hold times, this causes the order to seem reversed from what would be suggested by the terms.

pulse duration (width)

The time interval between the specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

Classified	Description
$t_w(CI)$	Pulse duration, XTAL2/CLKIN
$t_w(PGM)B$	Pulse duration, programming signal to ensure valid data is stored (byte mode)
$t_w(PGM)AR$	Pulse duration, programming signal to ensure valid data is stored (array mode)
$t_w(EPGM)$	Pulse duration, programming signal
$t_w(SCL)$	Pulse duration, SYSCLK low
$t_w(SCH)$	Pulse duration, SYSCLK high
$t_w(SCCL)$	Pulse duration, SCICLK low
$t_w(SCCH)$	Pulse duration, SCICLK high
$t_w(SPCL)$	Pulse duration, SPICLK low
$t_w(SPCH)$	Pulse duration, SPICLK high
$t_w(S)$	Pulse duration, sample time per kilohm of source impedance
t_w	Pulse duration, $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ low

setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is assured.

2. The setup time can have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is assured.

Example symbology:

Classified	Description
$t_{su(D)}$	Setup time, write data time to $\overline{EDS}$ high
$t_{su(WT-SCH)}$	Setup time, $\overline{WAIT}$ time to SYSCLK high
$t_{su(RXD-SCCH)}$	Setup time, SCIRXD to SCICLK high
$t_{su(SOMI-SPCH)}$	Setup time, SPISOMI to SPICLK high (polarity = 1)
$t_{su(SIMO-SPCH)}$	Setup time, SPISIMO to SPICLK high (polarity = 1)
$t_{su(S)}$	Setup time, analog to sample command

transition times (rise and fall times)

The time interval between two reference points (10% and 90% unless otherwise specified) on the same waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

Example symbology:

Classified	Description
t_r	Rise time
t_f	Fall time
$t_{r(Cl)}$	Rise time, XTAL2/CLKIN
$t_{f(Cl)}$	Fall time, XTAL2/CLKIN

valid time

- General. The time interval during which a signal is (or should be) valid.
- Output data-valid time. The time interval in which output data continues to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

Example symbology:

Classified	Description
$t_{v(A)}$	Valid time, address to $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$ and $\overline{CSPF}$ low
$t_{v(SCCH-TXD)}$	Valid time, SCITXD data valid after SCICLK high
$t_{v(SCCH-RXD)}$	Valid time, SCIRXD data valid after SCICLK high
$t_{v(SPCH-SOMI)}$	Valid time, SPISOMI data valid after SPICLK high (polarity = 1)
$t_{v(SPCH-SIMO)}$	Valid time, SPISIMO data valid after SPICLK high (polarity = 1)

$t_{v(AB-CD)}$ supersedes the older form t_{pVX} .

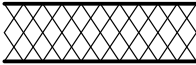
delay time

The time interval between two signals identified in the description column of the example symbology to follow.

Example symbology:

Classified	Description
$t_d(\text{CIH-SCL})$	Delay time, XTAL2/CLKIN rise to SYSCLK fall
$t_d(\text{CIH-SCH})$	Delay time, XTAL2/CLKIN rise to SYSCLK rise
$t_d(\text{SCL-A})$	Delay time, SYSCLK low to address $\overline{R/\overline{W}}$ and $\overline{OCF}$ valid
$t_d(\text{DZ-EL})$	Delay time, data bus high impedance to $\overline{EDS}$ low (read cycle)
$t_d(\text{EH-D})$	Delay time, $\overline{EDS}$ high to data bus enable (read cycle)
$t_d(\text{EL-DV})R$	Delay time, $\overline{EDS}$ low to read data valid
$t_d(\text{EL-WTV})$	Delay time, $\overline{EDS}$ low to $\overline{WAIT}$ valid
$t_d(\text{AV-DV})R$	Delay time, address valid to read data valid
$t_d(\text{AV-WTV})$	Delay time, address valid to $\overline{WAIT}$ valid
$t_d(\text{AV-EH})$	Delay time, address valid to $\overline{EDS}$ high (end of write)
$t_d(\text{SCCL-TXDV})$	Delay time, SCITXD valid after SCICLK low
$t_d(\text{SPCL-SIMOV})$	Delay time, SPISIMO valid after SPICLK low (polarity = 1)
$t_d(\text{SPCL-SOMIV})$	Delay time, SPISOMI valid after SPICLK low (polarity = 1)

timing diagrams conventions

Timing Diagram Symbol	Meaning	
	Input Forcing Functions	Output Response Functions
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated intervals
	Low-to-high changes permitted	Will be changing from low to high sometime during designated intervals
	Don't care	State unknown or changing

glossary

A

absolute addressing mode: An addressing mode in which code or operands produce the actual address

address: Any given memory location in which data can be stored or from which data can be retrieved

addressing mode: The method by which an instruction calculates the location of its required data

analog-to-digital converter (ADC): An 8-bit successive-approximation converter with internal sample-and-hold circuitry. Also referred to as ADC1, ADC2, or ADC3. ADC1 is an 8-channel ADC, except for the 40-pin TMS370Cx4x devices which have only four channels. ADC2 is a 4-channel ADC. And ADC3 is a 15-channel ADC.

ANSI C: A version of the C programming language that conforms to the C standards defined by the *American National Standards Institute*

archiver: A software program that allows the collection of several individual files into a single file called an archive library. The archiver also allows the addition, deletion, extraction, or replacement of members of the archive library.

assembler: A software program that creates a machine-language program from a source file containing assembly language instructions, directives, and macro directives. The assembler substitutes absolute operation codes for symbolic operation codes, and absolute or relocatable addresses for symbolic addresses.

assembly language: A symbolic language that describes the binary machine code in a more readable form. Each of the 73 unique instructions of the TMS370 family converts to one machine operation.

asynchronous-communications mode: An SCI mode that needs no synchronizing clock. This format consists of a start bit followed by data bits, an optional parity bit, and a stop bit. This format commonly is used with RS-232-C communications and PC serial ports.

B

baud: The communication speed for serial ports; equivalent to bits per second

BCD: *Binary coded decimal*. Each 4-bit nibble expresses a digit from 0–9 and usually packs two digits to a byte, giving a range of 0–99.

bit: Contraction of *binary digit* i.e., a 1 or a 0. In electrical terms, the value of a bit can be represented by the presence or absence of charge, voltage, or current.

breakpoint, trace, and timing (BTT) features: A set of features supported by the BTT board (included with the XDS/22 emulation system). These features allow the setting of hardware breakpoints, collecting of trace samples, and performing timing analysis.

buffer pointer: A 5-bit register in the PACT module peripheral frame that points to the next available location in the circular-capture buffer

byte: A sequence of eight adjacent bits operated upon as a unit

C

- C:** A high-level, general-purpose programming language that is useful for writing compilers and operating systems and for programming microprocessors
- C compiler:** A program that translates C source statements into assembly language source statements
- capture register:** A timer 2n register that is loaded with the 16-bit counter value on the occurrence of an external input transition. Either edge of the external input can be configured to trigger the capture.
- CDIP:** Ceramic Dual In-Line Package
- CDT370:** A low-cost code-development tool that is external to the target system and provides direct control over the TMS370 processor that is on the target system
- chip select:** For some blocks of the TMS370 memory map, the most significant bits of the address are pre-decoded to activate chip-select signals. These chip-select signals allow the TMS370 to access external addresses with a minimum of external logic and to perform memory bank selection under software control.
- circular buffer:** A variable length area in the PACT module dual-port RAM that stores the value of a PACT timer when a capture request is made. As new values are captured, they are put into successive locations in the buffer. When the buffer is full, the oldest captures are replaced with newer captures.
- CLCC:** Ceramic Leaded Chip Carrier
- CMOS:** A complementary MOS technology that uses transistors with electron (N-channel) and hole (P-channel) conduction
- code conversion utility:** A software program that translates a COFF file into one of several standard ASCII hexadecimal formats suitable for loading into an EPROM programmer
- COFF:** *Common Object File Format*. An implementation of the object file format of the same name developed by AT&T. The TMS370 compiler, assembler, and linker use and generate COFF files.
- command/definition area:** A variable length area in the PACT module dual-port RAM that is used to define the actions taken by the PACT module
- comment:** A source statement (or portion of a source statement) that documents or improves the readability of a source file. Comments are not compiled, assembled, or linked; they have no effect on the object file.
- compare register:** A timer 1 or timer 2n register that contains a value that is compared to the counter value. The compare function triggers when the counter matches the contents of the compare register.
- constant:** A value that does not change during execution
- CPU:** An 8-bit register-oriented processor with a status register, program counter, and stack pointer. The TMS370 CPU uses the register file, accessed in one bus cycle, as working registers.
- CSDIP:** Ceramic Shrink Dual In-Line Package
- $\overline{\text{CSE1}}$:** Chip-Select Eighth 1. This signal selects the first bank of memory. It has the same timing as $\overline{\text{EDS}}$. Setting this pin to a high-level general-purpose output disables the bank.
- $\overline{\text{CSE2}}$:** Chip-Select Eighth 2. This signal selects the second bank of memory. It has the same timing as $\overline{\text{EDS}}$. Setting this pin to a high-level general-purpose output disables the bank.
- $\overline{\text{CSH1}}$:** Chip-Select Half 1. This signal selects the first bank of memory. It has the same timing as $\overline{\text{EDS}}$. Setting this pin to a high-level general-purpose output disables the bank.
- $\overline{\text{CSH2}}$:** Chip-Select Half 2. This signal selects the second bank of memory. It has the same timing as $\overline{\text{EDS}}$. Setting this pin to a high-level general-purpose output disables the bank.
- $\overline{\text{CSH3}}$:** Chip-Select Half 3. This signal selects the third bank of memory. It has the same timing as $\overline{\text{EDS}}$. Setting this pin to a high-level general-purpose output disables the bank.

CSPF: Chip-Select Peripheral File. This signal has the same timing as $\overline{\text{EDS}}$, but it goes active only during access to external frames of the peripheral field (locations 10C0h – 10FFh).

D

data: Any information stored in or retrieved from a memory device.

debugger: A window-oriented software interface that helps the user to debug '370 programs running on an emulator, CDT370, or design kit.

dedicated-capture registers: An area in the PACT module dual-port RAM that stores the value of the default timer at the time of a specified edge on one of the PACT input-capture pins. Unlike the circular buffer, the location of the dedicated-capture register does not change.

default timer (also hardware timer): A 20-bit hardware counter in the PACT module that is incremented by the PACT prescaled clock

design kit: A low-cost tool that allows the user to analyze the hardware and software capabilities of the TMS370 family.

DIP: Dual In-line Package

dual-port RAM: An area in RAM that can be read from and written to by both the TMS370 CPU and the PACT module.

E

edge detection: A type of circuitry that senses an active pulse transition on a given timer input and provides appropriate output transitions to the rest of the module. The active transition can be configured to be low-to-high or high-to-low.

EDS: External Data Strobe. This signal goes low during external-memory operations. The rising edge of $\overline{\text{EDS}}$ validates the read-input data; the write data is available after the falling edge of $\overline{\text{EDS}}$.

EEPROM: *Electrically Erasable Programmable Read-Only Memory*. Memory that can be programmed and erased under direct program control.

EPROM: *Erasable Programmable Read-Only Memory*. Memory that can be programmed under direct program control.

Erase: Typically associated with EPROM and EEPROM. The procedure whereby programmed data is removed and the device returns to its unprogrammed state.

ESD: Electrostatic discharge

F

fully-static RAM: In a fully-static RAM, the periphery as well as the memory array is fully static. The periphery is therefore always active and ready to respond to input changes without the need of clocks. There is no precharge required for static periphery.

G

gang programmer: An interactive, menu-driven system that provides programming support for on-chip EEPROM or EPROM of the TMS370 microcontrollers in a production environment

H

HALT mode: An operating mode that reduces operating power by stopping the internal clock, which stops processing in all the modules. This is the lowest-power mode in which all register contents are preserved.

I

IDLE mode: An operating mode in which the CPU stops processing and waits for the next interrupt. It is not a low-power mode.

immediate operand: An operand whose actual constant value is specified in the instruction and placed after the opcode in the machine code

index: An 8-bit unsigned number added to a base address to give a final address

instruction: The basic unit of programming that causes the execution of one operation; consists of an opcode and operands, along with optional labels and comments

interrupt: A signal to the CPU that stops the flow of a program and forces the CPU to execute instructions at an address corresponding to the source of the interrupt. When the interrupt is finished, the CPU resumes execution at the point where it was interrupted.

isochronous: see **isosynchronous-communications mode**

isosynchronous-communications mode: An SCI mode in which data transmission is synchronized by a clock signal (SCICLK) common to both the sender and receiver. The format is identical to the asynchronous mode and consists of a start bit, data bits, an optional parity bit, and a stop bit.

K

K: When used in the context of specifying a given number of bits of information, $1K = 2^{10} = 1024$ bits. Thus, $64K = 64 \times 1024 = 65\,536$ bits.

L

label: A symbol that begins in column 1 of a source statement and corresponds to the address of that statement.

linker: A software tool that combines object files to form an object module that can be allocated into system memory and executed by the devices

LOW ADDR/HI ADDR: External memory address bus. Output only. Port B is the low address, and Port C is the high address.

low-power mode: An operating mode that reduces operating power by reducing or stopping the activity of various modules. There are two low-power modes: HALT and STANDBY.

LSB: *Least significant bit*

LSbyte: *Least significant byte*

M

machine code: The actual bytes read by the CPU during an instruction execution; usually read by a programmer as hexadecimal bytes

mask-programmed read-only memory (Mask-ROM): A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable

MC pin: *Mode control pin.* The pin that determines the operating mode of the TMS370 device, depending on the voltage applied to the pin. Twelve volts on the MC pin after reset places the processor in the write-protection override (WPO) mode.

memory: A medium capable of storing information that can be retrieved.

memory map: A description of the addresses of the various sections and features of the TMS370 processor. The map depends on the operating mode.

microcomputer mode with external expansion: An operating mode in which the address, control, and data memory extend off-chip to access external memory or peripherals

microcomputer single-chip mode: An operating mode in which the device uses only on-chip memory

microcontroller programmer: An interactive, menu-driven system that provides a method of programming TMS370 family devices and EPROMs directly or through an XDS™

microprocessor mode with internal-program memory: An operating mode in which the on-chip program memory is available to the processor

microprocessor mode without internal-program memory: An operating mode in which the on-chip program memory is not available to the processor. The processor must have external memory.

mini-SCI: The mini-UART function available in the PACT module.

mnemonic: A symbol that represents the opcode part of an assembly language instruction.

MSB: *Most significant bit*

MSbyte: *Most significant byte*

multiprocessor communications: An SCI format option that enables one processor to efficiently send blocks of data to other processors on the same serial link

N

nested interrupts: The ability of an interrupt to suspend the service routine of a prior interrupt. Nested interrupts are implemented in TMS370 devices by executing an interrupt-service routine that uses the EINT, EINTL, or EINTH instructions to set the global-interrupt-enable bits in the status register.

nonmaskable interrupt (NMI): An interrupt that causes the processor to execute the NMI routine. On TMS370 devices, INT1 can be configured as an NMI.

nonreturn to zero (NRZ) format: A communication format in which the inactive state is a logic state

nonvolatile memory: A memory in which the data content is maintained whether the power supply is connected or not

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O

OCF: Opcode Fetch. Goes low at the beginning of a memory read operation that fetches the first byte of an instruction. It then resumes its high level at the end of the opcode fetch(es).

offset: A signed value that is added to the base operand to give the final address

opcode: *Operation code.* The first byte of the machine code that describes to the CPU the type of operation and combination of operands. Some TMS370 instructions use 16-bit opcodes.

operand: The part of an instruction that tells the programmer where the CPU will fetch or store data

one-time programmable (OTP) read-only memory: a read-only memory that, after being manufactured, can have the data content of each memory cell altered once. Also referred to as OTP.

Output Enable: A control input that, when true, permits data to appear at the memory output, and when false, causes the output to assume a high-impedance state. (See also chip select.)

P

PACT: *Programmable acquisition and control timer module.* A timer coprocessor module for the TMS370 microcontroller family.

PDIP: Plastic Dual In-Line Package

peripheral file (PF): The 128 or 256 bytes of memory, starting at 1000h, that contain the registers that control the on-board peripherals and system configuration

peripheral-file frames: A set of sixteen contiguous peripheral file registers, usually related by function

PLCC: Plastic Leaded Chip Carrier

PPM: *Pulse-position modulation.* A serial signal in which the information is contained in the frequency of a signal with a constant-pulse width. By using the timer-compare features, a TMS370 device can output a PPM signal with a constant duty cycle without any program intervention.

prescaler: A circuit that slows the rate of a clocking source to the counter. The timer 1 prescaler can slow the clocking source by a factor of 4, 16, 64, or 256.

privilege mode: A mode immediately following reset in which the program can alter the privileged registers and bits. Once the privilege mode is disabled, these registers cannot be changed before another reset. This mode does not affect the EEPROM or the watchdog registers.

program: Typically associated with EPROM and OTP memories, the procedure whereby logical 0s (or 1s) are stored into various desired locations in a previously erased device

program counter (PC): A CPU register that identifies the current statement in the program

prototyping device: A device used before mask-ROM devices are available that has identical functions, pinout, size, and timings to those of the actual device. Programmable memory such as EEPROM or EPROM is used in place of the masked ROM.

PSDIP: Plastic Shrink Dual In-Line Package

pulse accumulation: A timer 1 or timer 2 mode that keeps a cumulative count of SYSCLK pulses gated by the T1EVT or T2EVT signal

PWM: *Pulse-width modulation.* A serial signal in which the information is contained in the width of a pulse of a constant-frequency signal. By using the timer-compare features, a TMS370 device can output a PWM signal with a constant-duty cycle without any program intervention.

R

R/ $\overline{W}$: Read or Write operation. Goes high at the beginning of read operations and low during write operations. This line is active during both internal and external accesses.

RAM: *Random access memory*

ratiometric conversion: An analog-to-digital conversion in which the conversion value is a ratio of the V_{REF} source to the analog input. As V_{REF} is increased, the input voltage needed to give a certain conversion value changes; however, all conversion values keep the same relationship to V_{REF} .

read: A memory operation whereby data is output from a desired address location

read-only memory (ROM): A memory in which the contents are not intended to be altered during normal operation. NOTE: Unless otherwise qualified, the term “read-only memory” implies that the contents are determined by its structure and are unalterable.

referred timer: The timer that a PACT command uses for time comparisons. This is the last timer defined in the PACT command/definition area before the command was encountered, or if no timer has been defined, it is the least significant 16 bits of the hardware timer.

register file (RF): The first 128 or 256 bytes of memory that can be accessed by the majority of the instructions

relative-addressing mode: An operating mode in which operands and code produce an absolute address at some distance from the current location

RESET pin: A pin that, when held low, starts hardware initialization and ensures an orderly software startup. If the MC pin is low when the $\overline{RESET}$ signal returns high, then the processor enters the microcomputer mode. If the MC pin is high when the $\overline{RESET}$ signal returns high, then it enters the microprocessor mode.

ROM security: Inhibits the reading of the ROM using any programmer

S

serial communications interface (SCI): Referred to as SCI1 or SCI2. SCI1 is a built-in serial interface that can be programmed to be asynchronous or isosynchronous. SCI2 is a built-in serial interface that can only be programmed to be asynchronous. Many timing, data format, and protocol factors are programmable and controlled by the SCI module in operation.

serial peripheral interface (SPI): A built-in serial interface that facilitates communication between networked master and slave CPUs. As in the SCI, the SPI is set up by software; from then on, the CPU takes no part in timing, data format, or protocol.

signed integer: A number system used to express positive and negative integers

SPI: *Serial Peripheral Interface module*

stack: The part of the register file used as last-in, first-out memory for temporary-variable storage. The stack is used during interrupts and calls to store the current program status. The area occupied by the stack is determined by the stack pointer and by the application program.

stack pointer (SP): An 8-bit CPU register that points to the last entry or top of the stack. The SP is incremented automatically before data is pushed onto the stack and decremented after data is popped from the stack.

standby RAM: Random-access memory which is powered through a separate power pin to protect the memory against power failures on the main power pin.

STANDBY mode: A power reduction mode in which the CPU stops processing, but the on-chip oscillator remains active. Timers remain active and can cause the CPU to exit the STANDBY mode.

static RAM (SRAM): A read/write random-access device within which information is stored as latched voltage levels. The memory cell is a static latch that retains data as long as power is applied to the memory array. No refresh is required. The type of peripheral circuitry sub-categorizes static RAMs.

status register (ST): A CPU register that monitors the operation of the instructions and contains the global-interrupt-enable bits

symbolic debugging: The ability of a software tool to retain symbolic information so that it can be used by a debugging tool such as an XDS/22, a design kit, or a CDT370

symbol table: A portion of a COFF file that contains information about the symbols that are defined and used by the file

SYSCLK: System Clock. This signal synchronizes external peripherals. It outputs one quarter of the crystal or external oscillator frequency.

T

T1: Timer 1 module contains a general-purpose timer and watchdog timer. Both timers allow program selection of input-clock source (real time, external event, or pulse accumulate) with multiple registers (input capture and compare) for special timer function control.

T2A: Timer 2A module is composed of a 16-bit resettable counter, 16-bit compare register with associated compare logic, a 16-bit capture register, and a 16-bit register that functions as a capture register in one mode and as a compare register in the other mode.

T2B: Timer 2B module is composed of a 16-bit resettable counter, 16-bit compare register with associated compare logic, a 16-bit capture register, and a 16-bit register that functions as a capture register in one mode and as a compare register in the other mode.

time slots: The internal cycles in which the PACT module can make a 32-bit access to the dual-port RAM. Each command or definition requires one, two, or three time slots. The number of time slots available is a function of the PACT prescaled clock and the frequency of access to the dual-port RAM by the CPU.

U

unsigned integer: A number system used to express positive integers

V

very-large-scale integration (VLSI): The description of an IC technology that is much more complex than large-scale integration (LSI) and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

virtual timer: An entry in the PACT command/definition area that creates an independent time base that is incremented by the PACT prescaled clock and cleared upon reaching a maximum value that is set by this definition.

volatile memory: A memory in which the data content is lost when the power supply is disconnected

W

WAIT pin: The pin that allows an external device to cause the processor to wait (holding the information on the expansion bus) for an indefinite number of clock cycles (one or more extra clockout cycles). When the wait line is released, the processor resynchronizes with the rising edge of the clockout signal (CLKOUT) after EDS goes active and continues with the program.

wait states, automatic: Extra clock cycles inserted automatically on every external-memory access to accommodate peripherals or expansion memory with slower access time than the TMS370 processor. These wait states are governed by two control bits: PF AUTOWAIT (SCCR0.5) and AUTOWAIT DISABLE (SCCR1.4).

watchdog (WD) timer: A timer option that can be programmed to generate an interrupt when it times out. This function serves as a hardware monitor over the software to prevent a “lost” program and is available in both the timer 1 and PACT modules. If timer 1 does not need a watchdog, this timer can be used as a general-purpose timer.

write: A memory operation whereby data is written into a desired address location

Write Enable: A control signal that when true causes the memory to assume the write mode, and when false causes it to assume the read mode

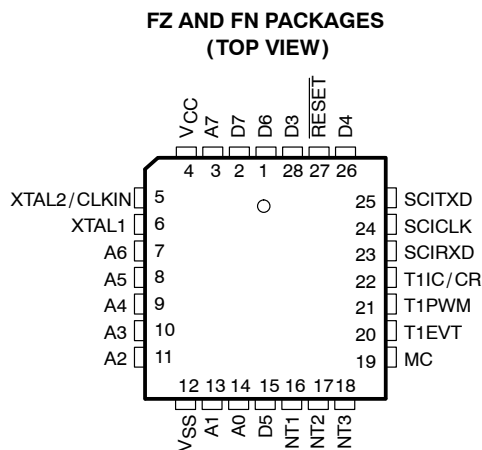
write-protect override (WPO): The only mode in which a TMS370 device can modify the on-board EEPROM. The WPO mode is entered when external circuitry applies 12 V to the MC pin after the device has been reset into one of its normal operating modes.

X

XDS/22: A code-development tool that is external to the target system and provides direct control over the TMS370 processor that is on the target system

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- **Serial Communications Interface 1 (SCI1)**
 - **Asynchronous Mode: 156K bps**
Maximum at 5 MHz SYSCLK
 - **Isosynchronous Mode: 25M bps**
Maximum at 5 MHz SYSCLK
 - **Full Duplex, Double-Buffered Receiver (RX) and Transmitter (TX)**
 - **Two Multiprocessor Communication Formats**
- **TMS370 Series Compatibility**
 - **Register-to-Register Architecture**
 - **256 General-Purpose Registers**
 - **14 Powerful Addressing Modes**
 - **Instructions Upwardly Compatible With All TMS370 Devices**
- **CMOS/TTL Compatible I/O Pins/Packages**
 - **All Peripheral Function Pins Software Configurable for Digital I/O**
 - **21 Bidirectional Pins, 1 Input Pin**
 - **28-Pin Plastic and Ceramic Leaded Chip Carrier Packages**
- **Workstation/Personal Computer-Based Development System**
 - **C Compiler and C Source Debugger**
 - **Real-time In-Circuit Emulation**
 - **Extensive Breakpoint/Trace Capability**
 - **Multi-Window User Interface**
 - **Microcontroller Programmer**



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TMS370Cx0x 8-BIT MICROCONTROLLER

SPNS029B – SEPTEMBER 1995 – REVISED MARCH 1996

Pin Descriptions

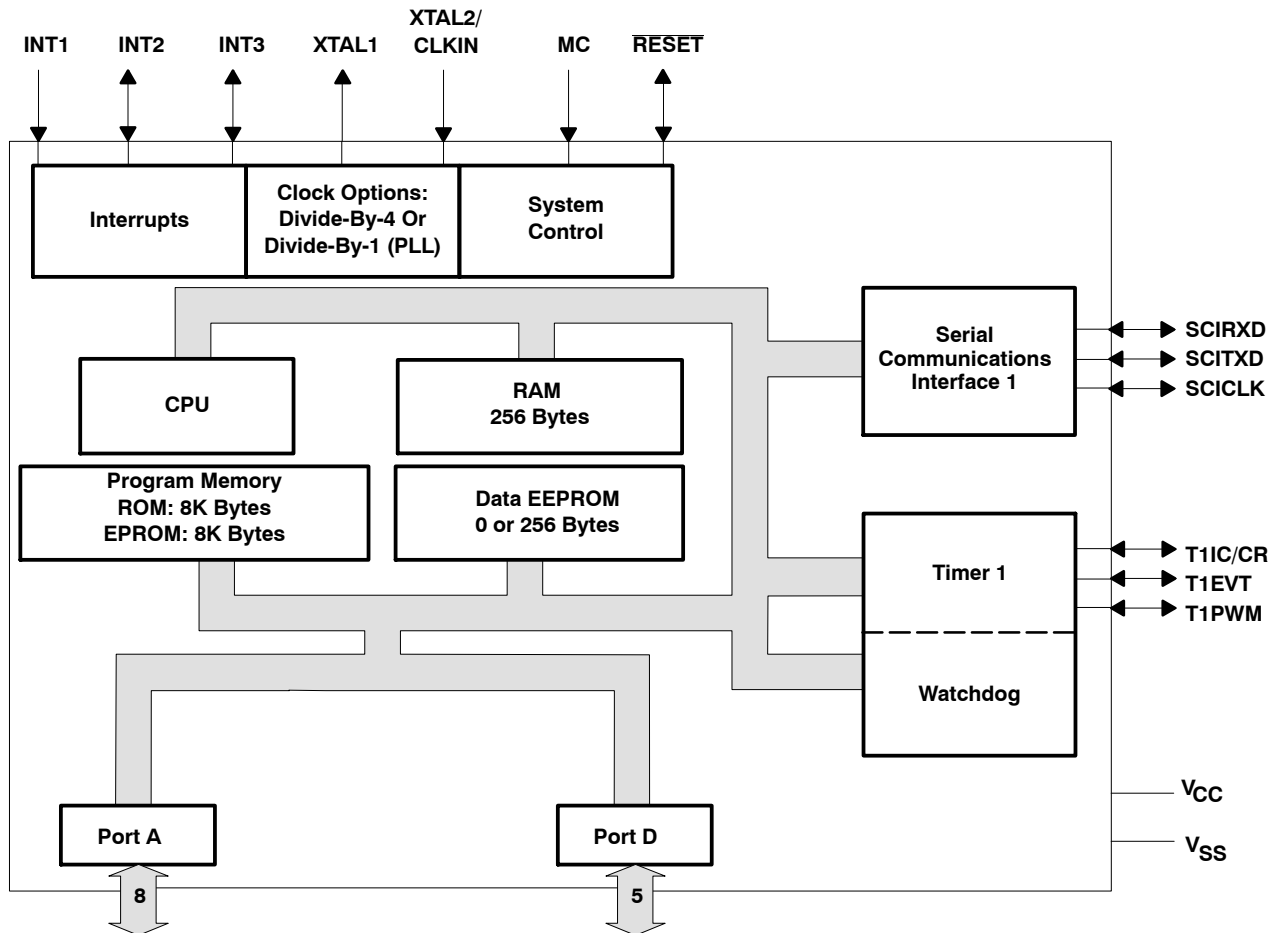
28 PINS LCC		I/O†	DESCRIPTION
NAME	NO.		
A0 A1 A2 A3 A4 A5 A6 A7	14 13 11 10 9 8 7 3	I / O	Port A is a general-purpose bidirectional I/O port.
D3 D4 D5 D6 D7	28 26 15 1 2	I / O	Port D is a general-purpose bidirectional I/O port. D3 is also configurable as SYSCLK.
INT1 INT2 INT3	16 17 18	I I / O I / O	External interrupt (non-maskable or maskable)/general-purpose input pin External maskable interrupt input/general-purpose bidirectional pin External maskable interrupt input/general-purpose bidirectional pin
T1IC/CR T1PWM T1EVT	22 21 20	I / O	Timer1 input capture/counter reset input pin /general-purpose bidirectional pin Timer1 PWM output pin/general-purpose bidirectional pin Timer1 external event input pin/general-purpose bidirectional pin
SCITXD SCIRXD SCICLK	25 23 24	I / O	SCI transmit data output pin, general-purpose bidirectional pin‡ SCI receive data input pin/general-purpose bidirectional pin SCI bidirectional serial clock pin/general-purpose bidirectional pin
RESET	27	I / O	System reset bidirectional pin; as input pin, RESET initializes the microcontroller; as open-drain output, RESET indicates that an internal failure was detected by watchdog or oscillator fault circuit.
MC	19	I	Mode control input pin; enables EEPROM write protection override (WPO) mode, also EPROM V _{PP}
XTAL2/CLKIN XTAL1	5 6	I O	Internal oscillator crystal input/External clock source input Internal oscillator output for crystal
V _{CC}	4		Positive supply voltage
V _{SS}	12		Ground reference

† I = input, O = output

‡ The three-pin SCI configuration is referred to as SCI1.



functional block diagram



description

The TMS370C002, TMS370C302, TMS370C702, and SE370C702 devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx0x refers to these devices. The TMS370 family provides cost-effective real-time system control through integration of advanced peripheral function modules and various on-chip memory configurations.

The TMS370Cx0x family of devices is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technologies. Low-operating power, wide-operating temperature range, and noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx0x devices attractive in system designs for automotive electronics, industrial motors, computer peripheral controls, telecommunications, and consumer applications.

All TMS370Cx0x devices contain the following on-chip peripheral modules:

- Serial communications interface 1 (SCI1)
- One 16-bit general-purpose timer with an 8-bit prescaler
- One 24-bit general-purpose watchdog timer

Table 1 provides a memory configuration overview of the TMS370Cx0x devices.

TMS370Cx0x 8-BIT MICROCONTROLLER

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description (continued)

Table 1. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		28-PIN PACKAGE
	ROM	EPROM	RAM	EEPROM	
TMS370C002A	8K	—	256	256	FN – PLCC
TMS370C302A	8K	—	256	—	FN – PLCC
TMS370C702	—	8K	256	256	FN – PLCC
SE370C702†	—	8K	256	256	FZ – CLCC

† System evaluators and development are for use only in prototype environment and their reliability has not been characterized.

The suffix letter (A) appended to the device name (shown in the first column of Table 1) indicates the configuration of the device. ROM and EPROM devices have different configurations as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 2. Suffix Letter Configuration

DEVICE	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM without A	Standard	Divide-by-4 (standard oscillator)	Enabled
ROM A	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

The 8K bytes of mask-programmable ROM in the associated TMS370Cx0x devices are replaced in the TMS370C702 with 8K bytes of EPROM. All other available memory and on-chip peripherals are identical, with the exception of no data EEPROM on the TMS370C302 devices. The one-time programmable (OTP) (TMS370C702) device and reprogrammable device (SE370C702) are available.

TMS370C702 OTP devices are available in plastic packages. This microcontroller is effective to use for immediate production updates for other members of the TMS370Cx0x family or for low-volume production runs when the mask charge or cycle time for low-cost mask ROM devices is not practical.

The SE370C702 has a windowed ceramic package to allow reprogramming of the program EPROM memory during the development-prototyping phase of design. The SE370C702 devices allow quick updates to breadboards and prototype systems while iterating initial designs.

The TMS370Cx0x family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all CPU activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator and the general purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx0x features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx0x family is fully instruction-set-compatible, providing easy transition between members of the TMS370 8-bit microcontroller family.

The TMS370Cx0x devices have two operational modes of serial communications provided by the SCI1 module. The SCI1 allows standard RS-232-C communications with other common data transmission equipment.



description (continued)

The TMS370Cx0x family provides the system designer with an economical, efficient solution to real-time control applications. The TMS370 family extended development system (XDS™) and compact development tool (CDT™) solve the challenge of efficiently developing the software and hardware required to design the TMS370Cx0x into an ever-increasing number of complex applications. The application source code can be written in assembly and C-language, and the output code can be generated by the linker. The TMS370 family XDS development tool communicates through a standard RS-232-C interface with an existing personal computer. This allows the use of the personal computer editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes ease-of-use through extensive menus and screen windowing so that a system designer with minimal training can begin developing software. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as reduced time-to-market cycle.

The TMS370Cx0x family together with the TMS370 family XDS/22, CDT370, design kit, starter kit, software tools, the SE370C712 reprogrammable devices, comprehensive product documentation, and customer support provide a complete solution to the needs of the system designer.

central processing unit (CPU)

The CPU used on the TMS370Cx0x device is the high-performance 8-bit TMS370 CPU module. The 'x0x implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'x0x instruction map is shown in Table 15 in the TMS370Cx0x instruction set overview section.

The '370Cx0x CPU architecture provides the following components:

CPU registers:

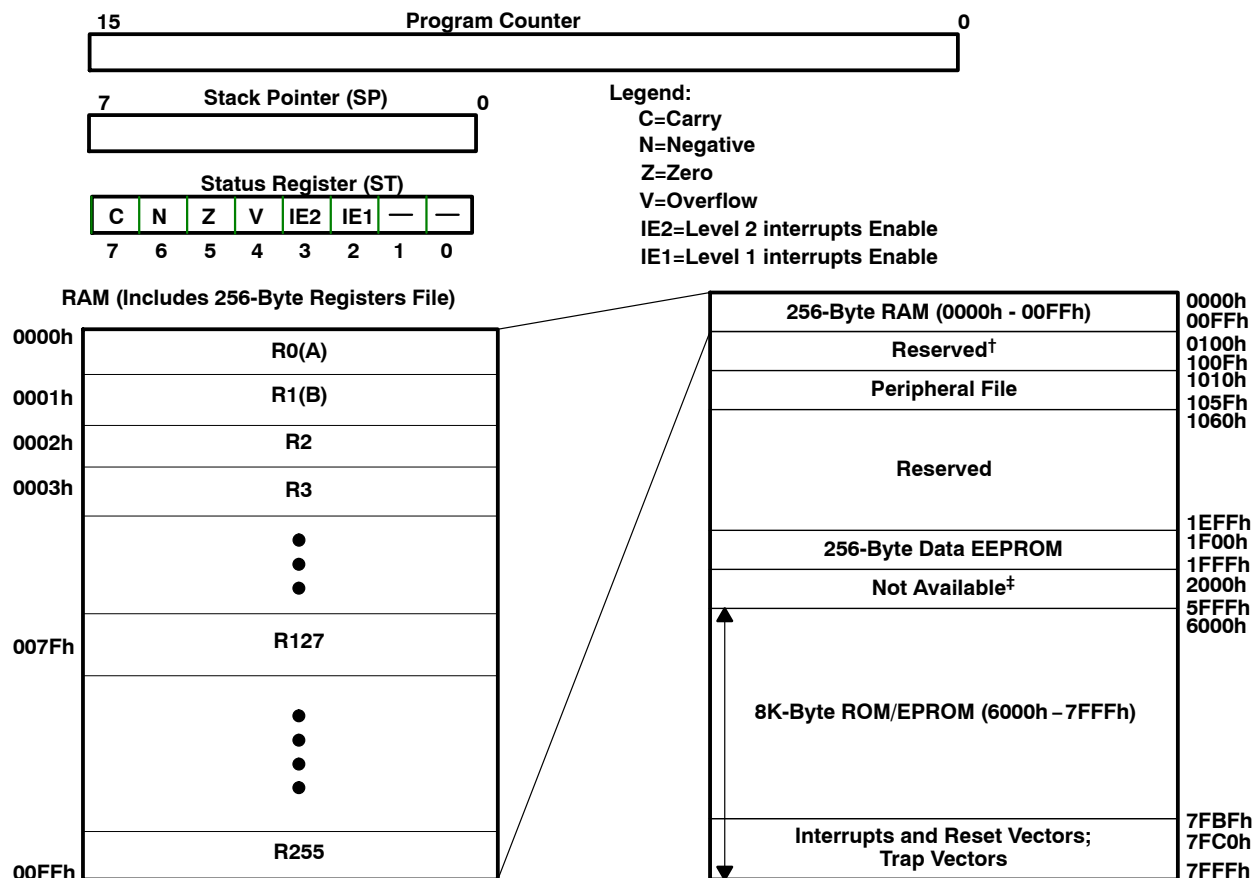
- A stack pointer that points to the last entry in the memory stack
- A status register that monitors the operation of the instructions and contains the global interrupt enable bits
- A program counter (PC) that points to the memory location of the next instruction to be executed

Figure 1 illustrates the CPU registers and memory blocks.

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central processing unit (CPU) (continued)



† Reserved means the address space is reserved for future expansion.

‡ Not available means the address space is not accessible.

Figure 1. Programmer's Model

A memory map that includes:

- 256-byte general-purpose RAM that can be used for data memory storage, program instructions, general-purpose register, or the stack
- A peripheral file that provides access to all internal peripheral modules, system-wide control functions and EEPROM/EPROM programming control
- 256-byte EEPROM module that provides in-circuit programmability and data retention in power-off conditions
- 8K-byte ROM or 8K-byte EPROM program memory

stack pointer (SP)

The SP is an 8-bit CPU register. Stack operates as a last-in, first-out, read/write memory. The stack is used typically to store the return address on subroutine calls as well as the status-register contents during interrupt sequences.

The SP points to the last entry or top of the stack. The SP is incremented automatically before data is pushed onto the stack and decremented after data is popped from the stack. The stack can be placed anywhere in the on-chip RAM memory.

central processing unit (CPU) (continued)

status register (ST)

The ST monitors the operation of the instructions and contains the global-interrupt-enable bits. The ST register includes four status bits (condition flags) and two interrupt-enable bits:

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional jump instructions) use the status bits to determine program flow.
- The two interrupt enable bits control the two interrupt levels.

The ST register, status-bit notation, and status-bit definitions are shown in Table 3.

Table 3. Status Registers (ST)

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most significant byte and least significant byte of a 16-bit address.

During reset, the contents of the reset vector (7FFEh, 7FFFh) are loaded into the program counter. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 6000h as the contents of the reset vector.

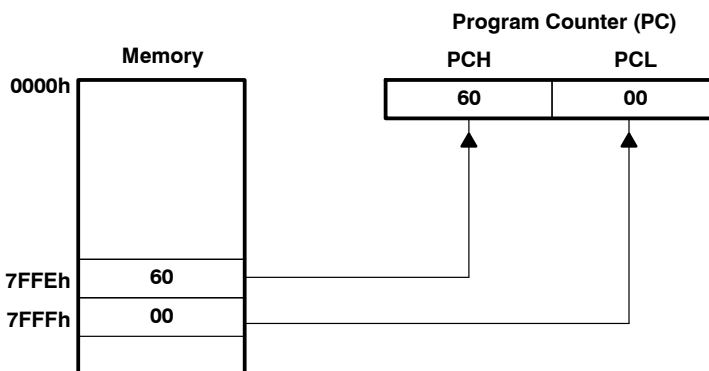


Figure 2. Program Counter After Reset

memory map

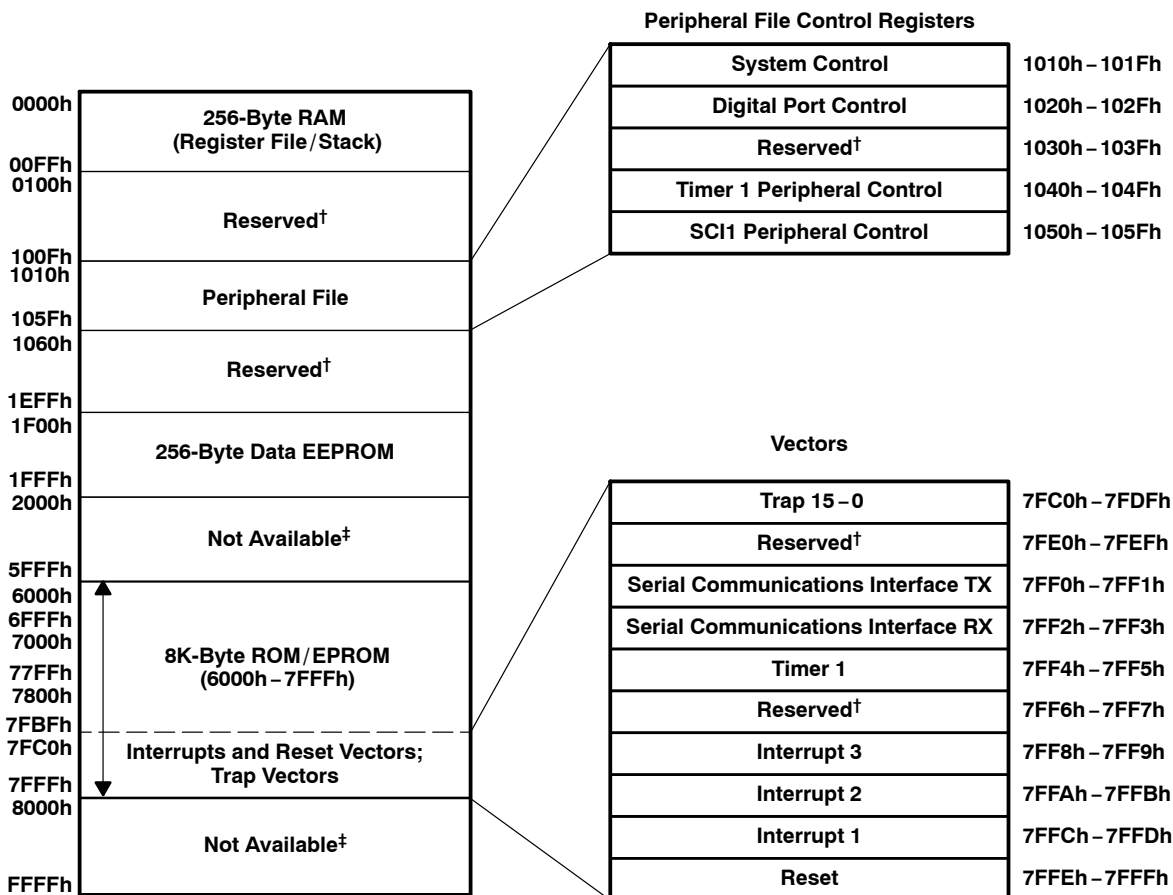
The TMS370Cx0x architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. As shown in Figure 3, the TMS370Cx0x provides memory-mapped RAM, ROM, Data EEPROM, input/output pins, peripheral functions, and system interrupt vectors.

The peripheral file contains all input/output port control, peripheral status and control, EEPROM, EPROM, and system-wide control functions. The peripheral file is located between 1010h to 105Fh and is divided logically into five peripheral-file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed.

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central processing unit (CPU) (continued)



† Reserved means the address space is reserved for future expansion.

‡ Not available means the address space is not accessible.

Figure 3. TMS370Cx0x Memory Map

RAM/register file (RF)

Locations within the RAM address space can serve as the RF, general-purpose read/write memory, program memory, or the stack instructions. The TMS370Cx0x devices contain 256 bytes of internal memory-mapped RAM beginning at location 0000h (R0) and continuing through location 00FFh (R255) which is shown in Figure 1.

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370Cx0x control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or P for a decimal designator. For example, the system control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 4 shows the TMS370Cx0x PF address map.

peripheral file (PF) (continued)

Table 4. TMS370Cx0x Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h – 100Fh	P000 – P00F	Reserved
1010h – 101Fh	P010 – P01F	System and EPROM/EEPROM control registers
1020h – 102Fh	P020 – P02F	Digital I/O port control registers
1030h – 103Fh	P030 – P03F	Reserved
1040h – 104Fh	P040 – P04F	Timer 1 registers
1050h – 105Fh	P050 – P05F	Serial communications interface registers
1060h – 10FFh	P060 – P0FF	Reserved

data EEPROM

The TMS370Cx0x devices, containing 256 bytes of data EEPROM, have their memory mapped beginning at location 1F00h and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B). The data EEPROM features include the following:

- Programming:
 - Bit-, byte-, and block-write/erase modes
 - Internal charge pump circuitry. No external EEPROM programming voltage supply is needed.
 - Control register: Data EEPROM programming is controlled by the DEECTL located in the PF frame beginning at location P01A. See Table 5.
 - In-circuit programming capability. There is no need to remove the device to program.
- Write protection. Writes to the data EEPROM are disabled during the following conditions.
 - Reset. All programming of the data EEPROM module is halted.
 - Write protection active. There is one write-protect bit per 32-byte EEPROM block.
 - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 5. Data EEPROM and Program EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME
P01A	DEECTL	Data EEPROM control register
P01B	—	Reserved
P01C	EPCTL	Program EPROM control register

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program EPROM

The TMS370C702 device contains 8K bytes of EPROM, mapped, at location 6000h and continuing through location 7FFFh as shown in Figure 3. Memory addresses 7FF0h through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh. Reading the program EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the EPROM control register (EPCTL). The program EPROM module features include:

- Programming
 - In-circuit programming capability if V_{PP} is applied to MC
 - Control register: EPROM programming is controlled by the EPROM control register (EPCTL) located in the peripheral file (PF) frame at location P01Ch as shown in Table 5.
- Write protection: Writes to the program EPROM are disabled under the following conditions:
 - Reset halts all programming to the EPROM module.
 - Low-power modes
 - 13 V not applied to MC

program ROM

The program read-only memory (ROM) consists of 8K bytes of mask-programmable ROM. The program ROM is used for permanent storage of data or instructions. Memory addresses 7FF0h through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh. Programming of the mask ROM is performed at the time of device fabrication. Refer to Figure 3 for ROM memory map.

system reset

The system reset operation ensures an orderly start-up sequence for the TMS370Cx0x CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are internally generated, while one ($\overline{\text{RESET}}$ pin) is controlled externally. These actions are as follows:

- External $\overline{\text{RESET}}$ pin. A low-level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.
- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer times out. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside the recommended operating range. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x0x device to reset external system components. Additionally, if a cold start (V_{CC} is off for several hundred milliseconds) condition or oscillator failure occurs or the $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator fault flag (OSC FLT FLAG, SCCR0.4), the cold start flag (COLD START, SCCR0.7), and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 6 lists the reset sources.



system reset (continued)

Table 6. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Registers A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

When an external reset circuit is connected to the $\overline{\text{RESET}}$ pin, the pin must be held low until the clock signal is valid and V_{CC} is within the operating range. Figure 4 shows a typical reset circuit.

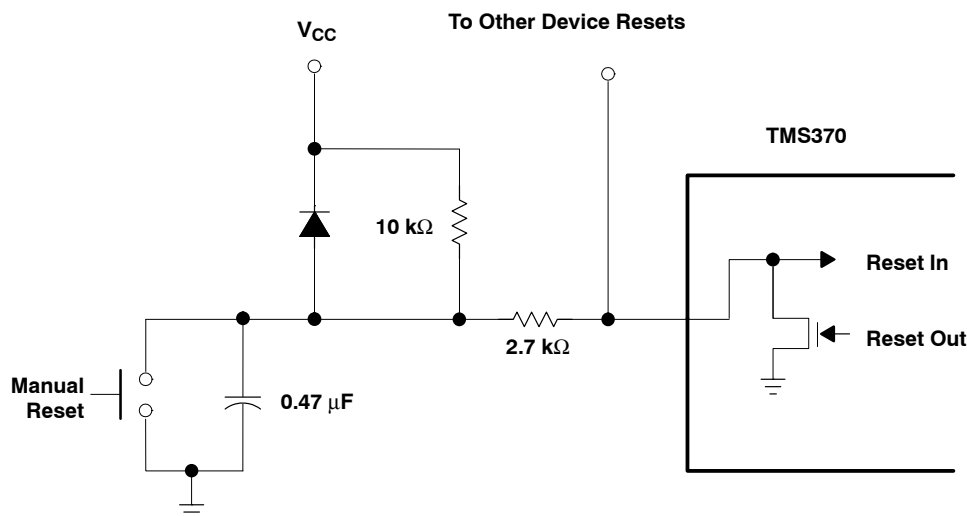


Figure 4. Typical Reset Circuit

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interrupts

The TMS370 family software programmable interrupt structure permits flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global-interrupt mask bits (IE1 and IE2) of the status register.

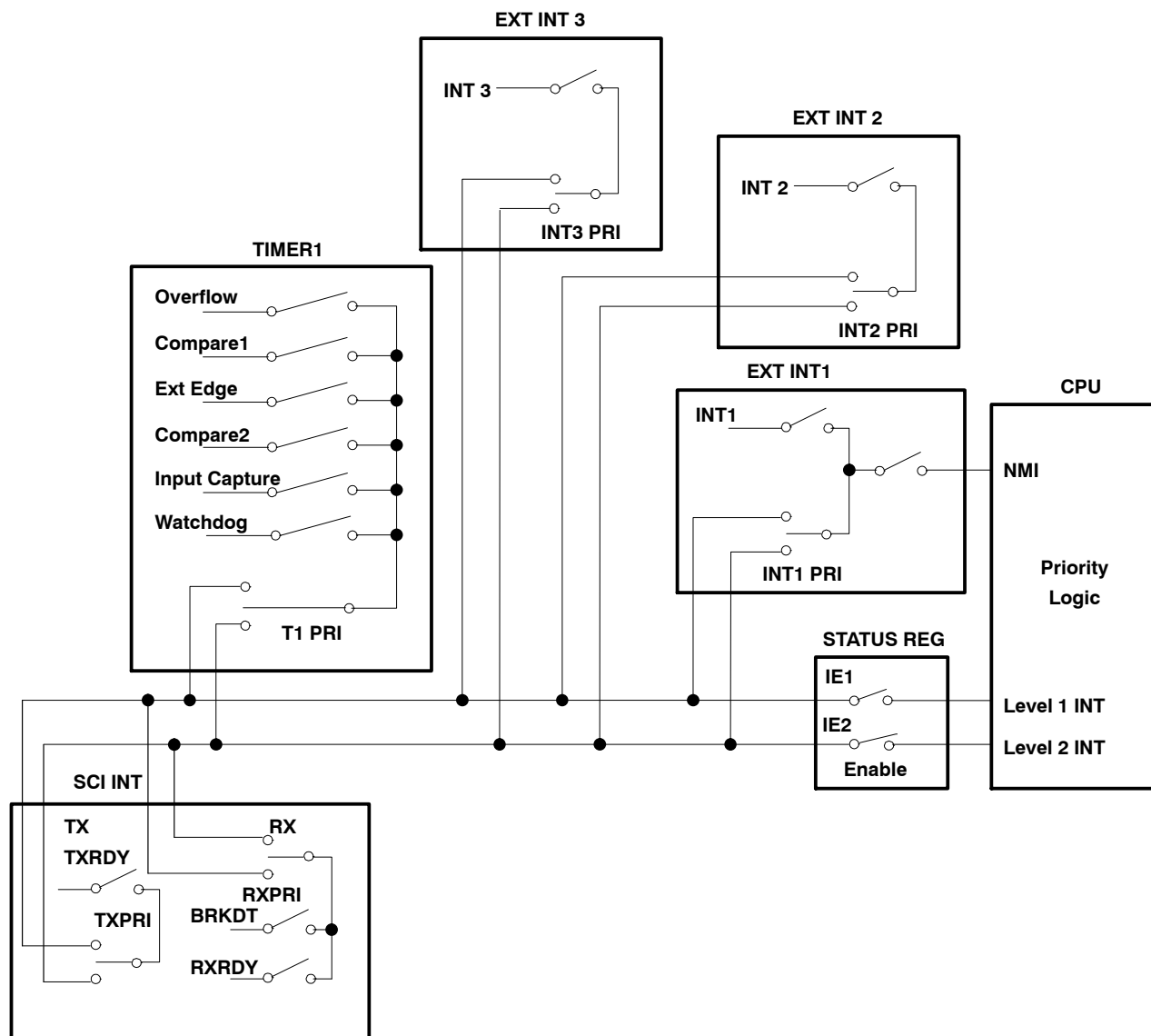


Figure 5. Interrupt Control

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is configured selectively on either the high- or low-priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority

interrupts (continued)

chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending-interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx0x has six hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 7. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. A system interrupt can have multiple interrupt sources. All of the interrupt sources are individually maskable by local interrupt enable control bits in the associated peripheral file. Each interrupt source FLAG bit is individually readable for software polling or for determining which interrupt source generated the associated system interrupt.

Three of the system interrupts are generated by on-chip peripheral functions, and three external interrupts are supported. Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in peripheral file frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual- or global-enable-mask bits. The INT1 NMI bit is protected during non-privileged operation and, therefore, should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software-configured as general-purpose input/output pins if the interrupt function is not required (INT1 can be similarly configured as an input pin).

Table 7. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY [†]
External $\overline{\text{RESET}}$ Watchdog Overflow Oscillator Fault Detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	$\overline{\text{RESET}}^{\ddagger}$	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1 [‡]	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2 [‡]	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3 [‡]	7FF8h, 7FF9h	4
Timer 1 Overflow Timer 1 Compare 1 Timer 1 Compare 2 Timer 1 External Edge Timer 1 Input Capture 1 Watchdog Overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT [§]	7FF4h, 7FF5h	5
SCI RX Data Register Full SCI RX Break Detect	RXRDY FLAG BRKDT FLAG	RXINT [‡]	7FF2h, 7FF3h	6
SCI TX Data Register Empty	TXRDY FLAG	TXINT	7FF0h, 7FF1h	7

[†] Relative priority within an interrupt level

[‡] Release microcontroller from STANDBY and HALT low-power modes.

[§] Release microcontroller from STANDBY low-power mode.

privileged operation and EEPROM write protection override

The TMS370Cx0x family has significant flexibility to enable the designer to software configure the system and peripherals to meet the requirements of a variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx0x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) is set to 1 to enter the

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privileged operation and EEPROM WPO (continued)

nonprivileged mode, thus disabling write operations to specific configuration control bits within the peripheral file. Table 8 lists the system configuration bits which are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

Table 8. Privileged Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCR0	P010.5 P010.6	PF AUTO WAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
SCIPRI	P05F.4 P05F.5 P05F.6 P05F.7	SCI ESPEN SCIRX PRIORITY SCITX PRIORITY SCI STEST
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST

† The privileged bits are shown in a bold typeface in Table 10.

The write protect override (WPO) mode is an external hardware method of overriding the write protection registers (WPR) of data EEPROM on the TMS370Cx0x. WPO mode is entered by applying a 12-V input to the MC pin after the **RESET** pin input goes high (logic 1). The high voltage (+ 12 V) on the MC pin during the WPO mode is not the programming voltage for the data EEPROM or program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware system level capability to modify the content of data EEPROM while the device remains in the application but only while requiring a 12-V external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power and IDLE modes

The TMS370Cx0x devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time the mask is manufactured.

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls the low-power mode selection.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity stops; however, the oscillator, internal clocks, timer 1 and the receive-start bit detection circuit of the serial communications interface remain active. System processing is suspended until a qualified interrupt (hardware **RESET**, external interrupt on INT1, INT2, INT3, timer 1 interrupt, or low level on the receive pin of the SCI1) is detected.

low-power and IDLE modes (continued)

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx0x is placed in its lowest power-consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware RESET, external interrupt on the INT1, INT2, INT3, or low level on the receive pin of the SCI1) is detected. The power-down mode selection bits are summarized in Table 9.

Table 9. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X [†]	IDLE

[†] Don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6-7 bits are ignored. In addition, if an idle instruction executes when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method of always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI is generated always, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing stops during the STANDBY and HALT modes, the clocking of the watchdog timer is inhibited.

clock modules

The 'x0x family provides two clock options that are referred to as divide-by-1 (phase-locked loop) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The 'x0x ROM-masked devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device. The '702A EPROM has only the divide-by-4.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 clock module option provides a one-to-one match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency, whereas the divide-by-4 option produces a SYSCLK which is one-fourth of the frequency of the external resonator. Inside of the divide-by-1 module, the frequency of the external resonator is multiplied by four, and the clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency.

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clock modules (continued)

These are formulated as follows:

$$\text{Divide-by-4 : SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 : SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the improved EMI performance. The harmonics of low-speed resonators extend through less of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 option provides the capability of reducing the resonator speed by four times, resulting in a steeper decay of emissions produced by the oscillator.

system configuration registers

Table 10 contains system configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in a bold typeface and shaded areas.

Table 10. Peripheral File Frame 1: System Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTO WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D to P01F	Reserved								

digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 11 shows the specific addresses, registers, and control bits within this peripheral file frame.

Table 11. Peripheral File Frame 2: Digital Port Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P020	Reserved								APOINT1
P021	Port A Control Register 2 (must be 0)								APOINT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPOINT1
P02D	Port D Control Register 2 (must be 0) [†]					—	—	—	DPOINT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 12. Port Configuration Register Setup

PORT	PIN	abcd 00q1	abcd 00y0
A	0 – 7	Data OUT q	Data In y
D	3 – 7	Data OUT q	Data In y
a = Port x Control Register 1 b = Port x Control Register 2 c = Data d = Direction			

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programmable timer 1

The programmable Timer 1 (T1) module of the TMS370Cx0x provides the designer with the enhanced timer resources required to perform real-time system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers (T1 and WD) allow program selection of input clock sources (real-time, external event, or pulse accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The timer 1 module includes three external device pins that can be used for multiple counter functions (operation mode dependent) or used as general-purpose I/O pins. The T1 module block diagram is shown in Figure 6.

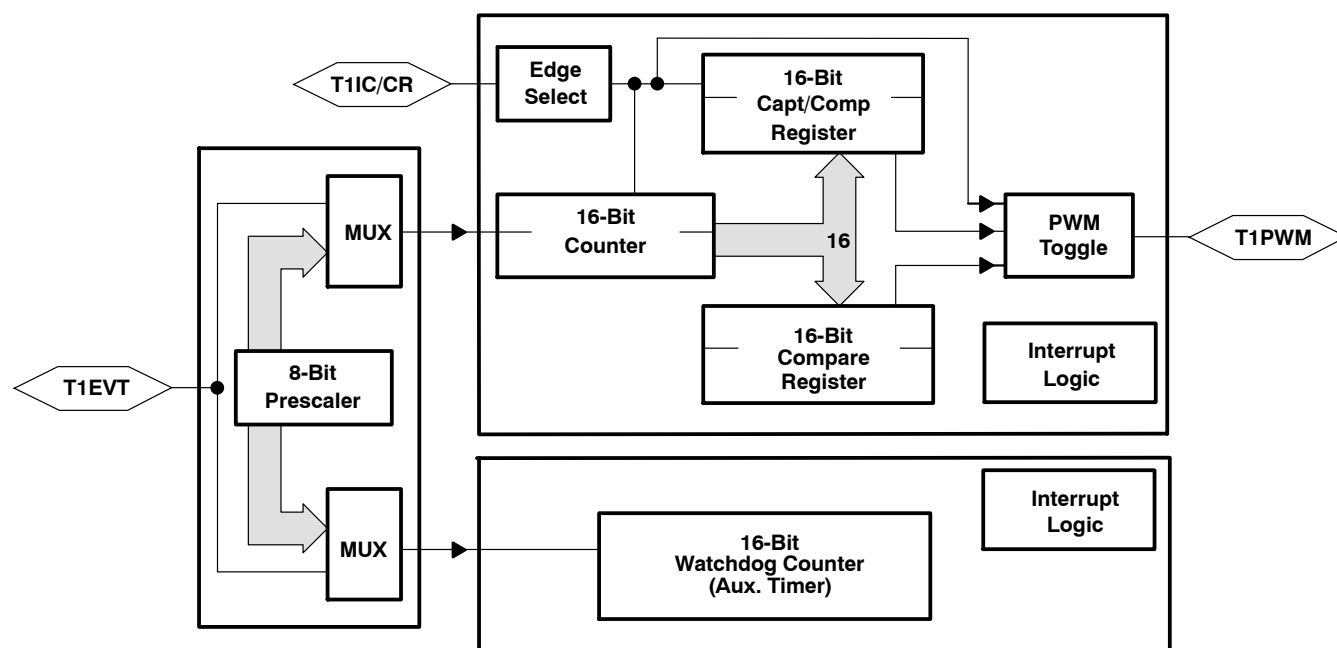


Figure 6. Timer 1 Block Diagram

- Three T1 I/O pins
 - T1IC/CR: Timer 1 input capture / counter reset input pin, or general-purpose bidirectional I/O pin
 - T1PWM: Timer 1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T1EVT: Timer 1 event input pin, or general-purpose bidirectional I/O pin
- Two operation modes:
 - Dual-compare mode: Provides PWM signal
 - Capture/compare mode: Provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register.
- One 16-bit watchdog counter can be used as an event counter, a pulse accumulator, or an interval timer if watchdog feature is not needed.
- Prescaler/clock sources that determine one of eight clock sources for general-purpose timer

programmable timer 1 (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC1/CR)
- Interrupts that can be generated on the occurrence of:
 - A capture
 - A compare equal
 - A counter overflow
 - An external edge detection
- Sixteen timer 1 module control registers located in the PF frame beginning at address P040.

The T1 module control registers are illustrated in Table 13.

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programmable timer 1 (continued)

Table 13. Timer 1 Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Dual-Compare and Capture/Compare									
P040	Bit 15 T1 Counter MSbyte							Bit 8	T1CNTR
P041	Bit 7 T1 Counter LSbyte							Bit 0	
P042	Bit 15 Compare Register MSbyte							Bit 8	T1C
P043	Bit 7 Compare Register LSbyte							Bit 0	
P044	Bit 15 Capture/Compare Register MSbyte							Bit 8	T1CC
P045	Bit 7 Capture/Compare Register LSbyte							Bit 0	
P046	Bit 15 Watchdog Counter MSbyte							Bit 8	WDCNTR
P047	Bit 7 Watchdog Counter LSbyte							Bit 0	
P048	Bit 7 Watchdog Reset Key							Bit 0	WDRST
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE=0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to the simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

programmable timer 1 (continued)

Figure 7 shows the timer 1 capture/compare mode block diagram. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

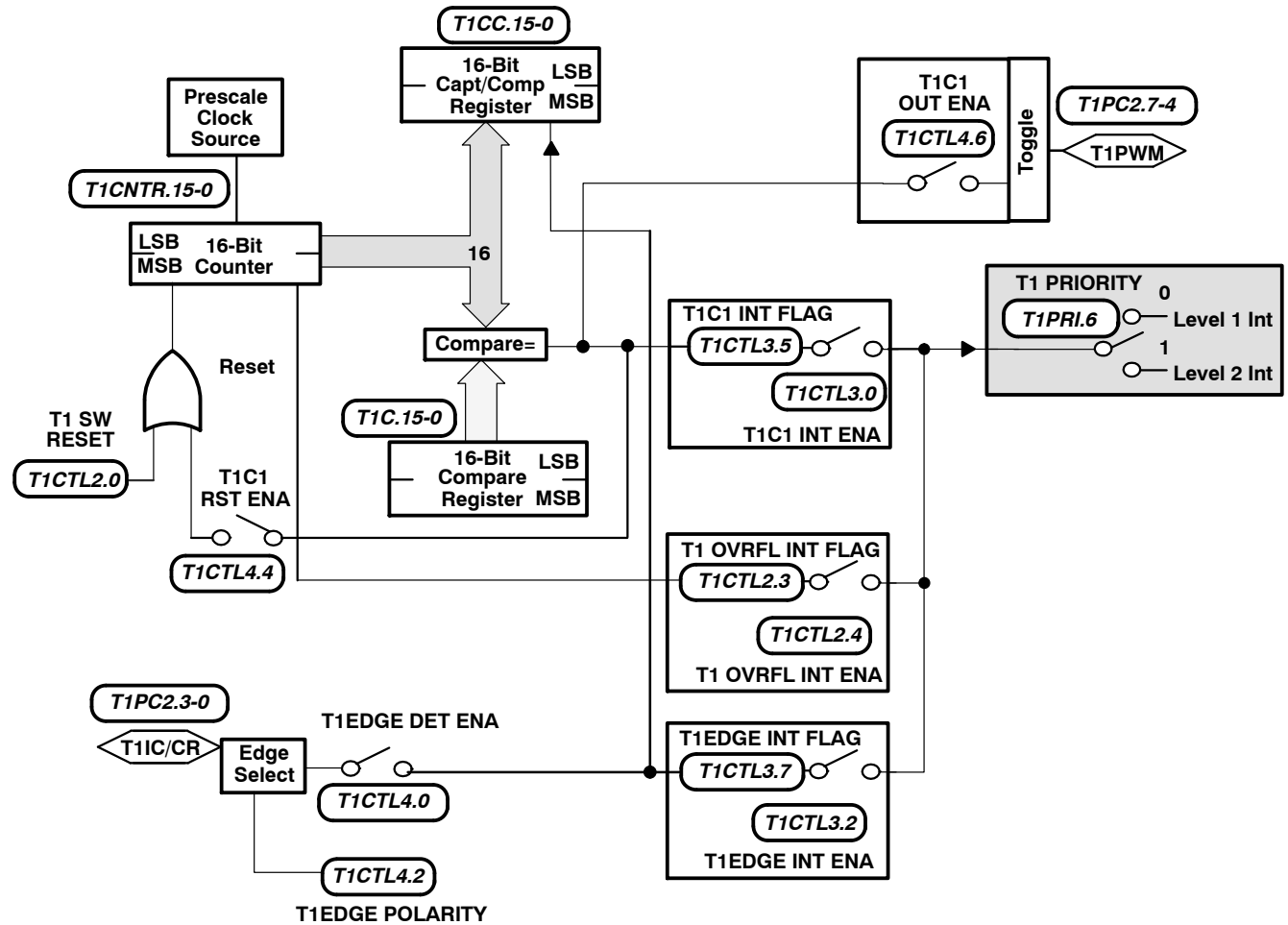


Figure 7. Capture/Compare Mode

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programmable timer 1 (continued)

Figure 8 shows the timer 1 dual-compare mode block diagram. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

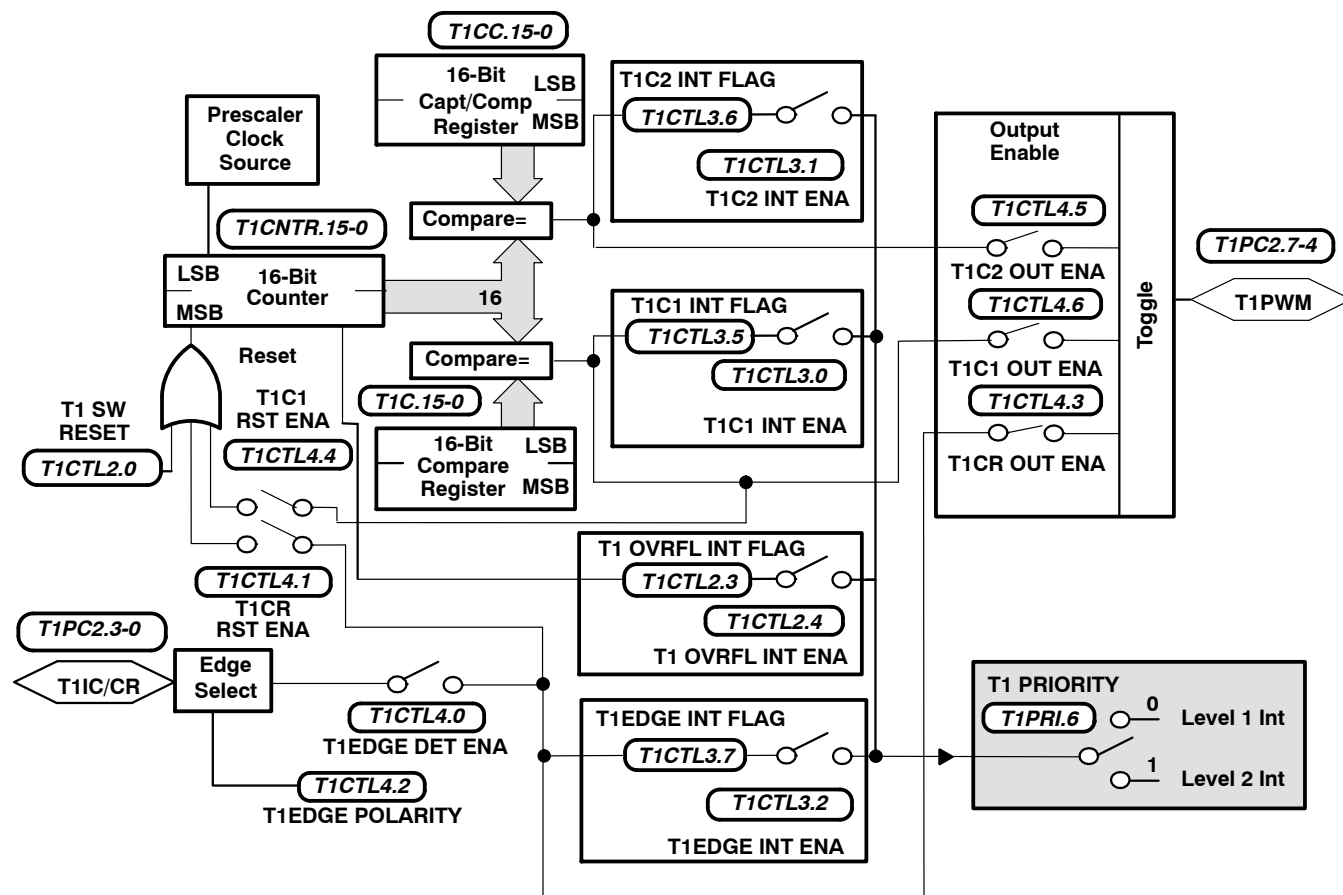


Figure 8. Dual-Compare Mode

programmable timer 1 (continued)

The TMS370Cx0x device includes a 24-bit watchdog (WD) timer, contained in the timer 1 module, which can be programmed as an event counter, pulse accumulator, or interval timer if the watchdog function is not used. The WD function is to monitor software and hardware operation and to implement a system reset when the WD counter is not properly serviced (WD counter overflow or WD counter is re-initialized by an incorrect value). The WD can be configured as one of three mask options as follows:

- Standard watchdog configuration (see Figure 9) – for EPROM and mask-ROM devices:
 - Watchdog mode
 - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows
 - A watchdog overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
 - Non-watchdog mode
 - Watchdog timer can be configured as an event counter, a pulse accumulator, or an interval timer

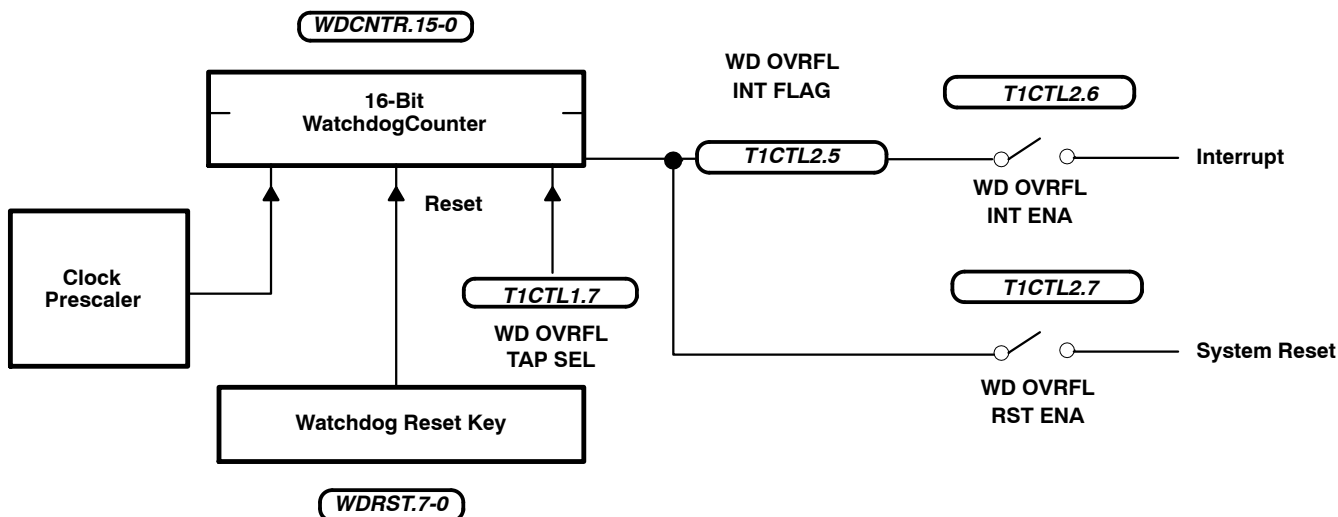


Figure 9. Standard watchdog

programmable timer 1 (continued)

- Hard watchdog configuration (see Figure 10) – for mask-ROM devices:
 - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows.
 - Automatic activation of the WD timer upon power-up reset
 - INT1 is enabled as a nonmaskable interrupt during low-power modes.
 - A watchdog overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset

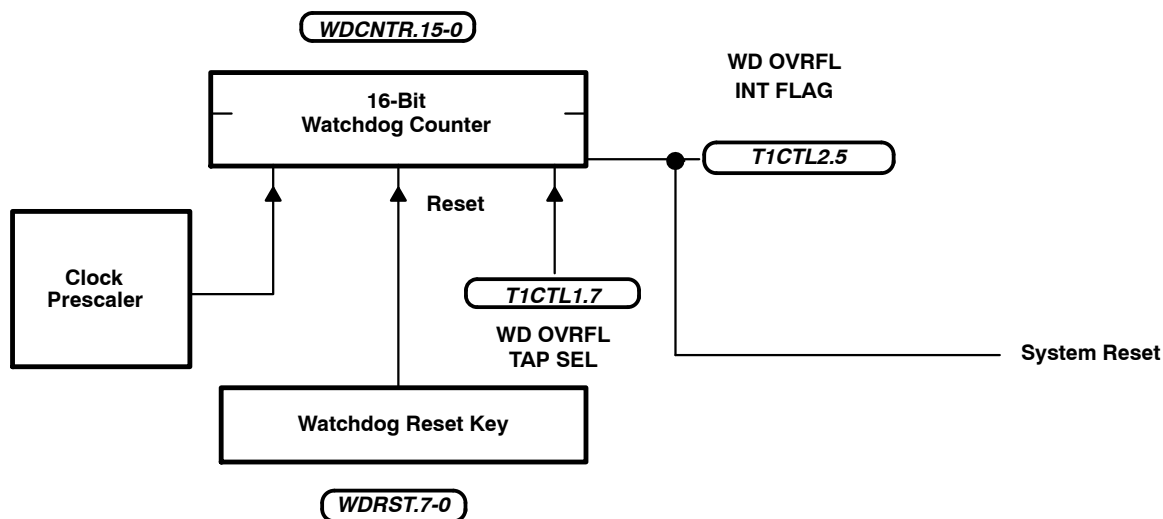


Figure 10. Hard Watchdog

- Simple counter configuration – for mask-ROM devices only (see Figure 11)
 - Simple counter can be configured as an event counter, pulse accumulator, or an internal timer.

programmable timer 1 (continued)

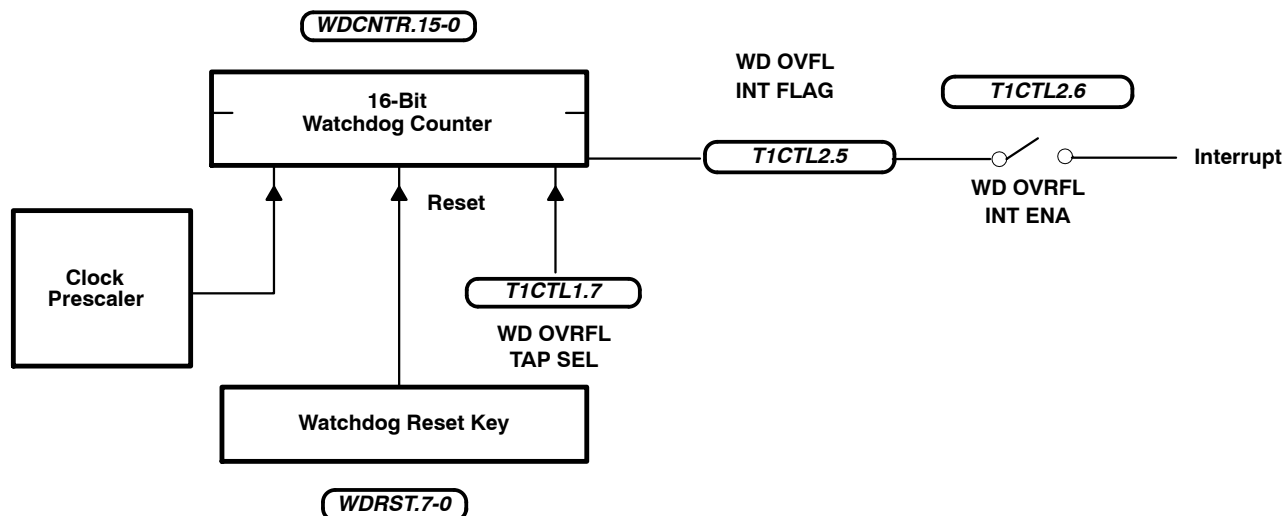


Figure 11. Simple Counter

serial communications interface 1 (SCI1) module

The TMS370Cx0x devices include a serial communications interface 1 (SCI1) module. The SCI1 module supports digital communications between the TMS370 devices and other asynchronous peripherals and uses the standard non-return-zero format (NRZ) format. The SCI1's receiver and transmitter are double buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full duplex mode. To ensure data integrity, the SCI1 checks received data for break detection, parity, overrun, and framing errors. The speed of bit rate (baud) is programmable to over 65,000 different speeds through a 16-bit baud-select register.

Features of the SCI1 module include:

- Three external pins:
 - SCITXD: SCI transmit-output pin or general-purpose bidirectional I/O pin
 - SCIRXD: SCI receive-input pin or general-purpose bidirectional I/O pin
 - SCICLK: SCI bidirectional serial-clock pin, or general-purpose bidirectional I/O pin
- Two communications modes: asynchronous and isosynchronous[†]
- Baud rate: 64K different programmable rates
 - Asynchronous mode: 3 bps to 156K bps at 5-MHz SYSCLK

$$\text{ASYNCHRONOUS BAUD} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 32}$$

- Isosynchronous mode: 39 bps to 2.5M bps at 5-MHz SYSCLK

$$\text{ISOSYNCHRONOUS BAUD} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 2}$$

[†] Isosynchronous = Isochronous

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serial communications interface 1 (SCI1) module (continued)

- Data word format:
 - One start bit
 - Data word length programmable from one to eight bits
 - Optional even/odd/no parity bit
 - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: Idle-line and address bit
- Half or full-duplex operation
- Double-buffered receiver and transmitter operations
- Transmitter and receiver operations can be accomplished through either interrupt-driven or polled-algorithms with status flags:
 - Transmitter: TXRDY flag (transmitter buffer register is ready to receive another character) and TX EMPTY flag (Transmitter shift register is empty)
 - Receiver: RXRDY flag (receive buffer register ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR monitoring four interrupt conditions
 - Separate enable bits for transmitter and receiver interrupts
 - NRZ (non return-to-zero) format
- Eleven SCI1 module control registers, located in control register frame beginning at address P050h



serial communications interface 1 (SCI1) module (continued)

The SCI1 module control registers are illustrated in Table 14.

Table 14. SCI1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNCR/ ISOSYNCR	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	Reserved								
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF
P05A P05B P05C	Reserved								
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	SCI STEST	SCITX PRIORITY	SCIRX PRIORITY	SCI ESPEN	—	—	—	—	SCIPRI

serial communications interface 1 (SCI1) module (continued)

The SCI1 module block diagram is illustrated in Figure 12.

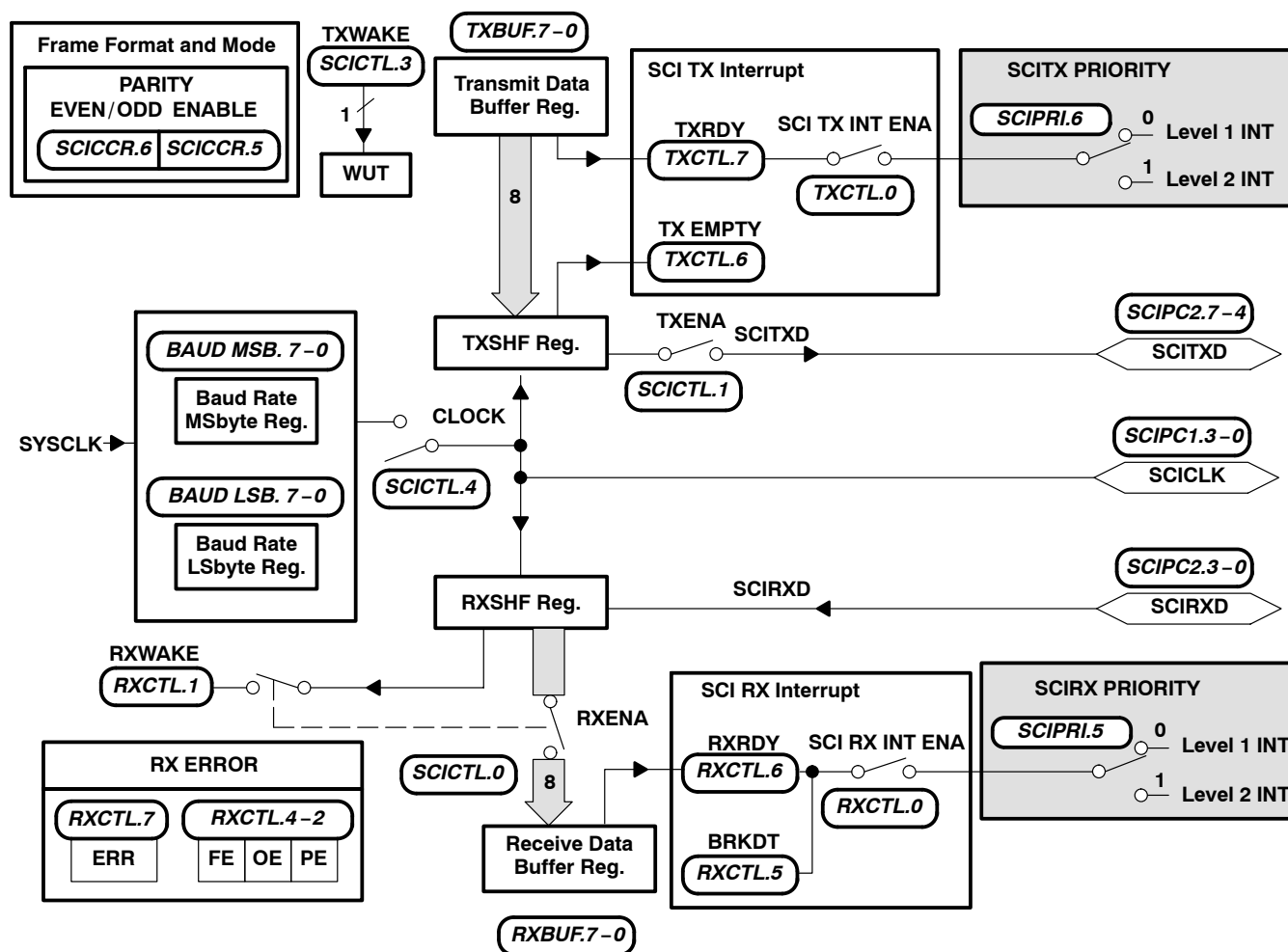


Figure 12. SCI1 Block Diagram

instruction set overview

Table 15 provides an opcode-to-instruction cross-reference of all 73 instructions and 274 opcodes of the '370Cx0x instruction set. The numbers at the top of this table represent the most significant nibble of the opcode while the numbers at the left side of the table represent the least significant nibble. The instructions for these two opcode nibbles contain the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

Table 15. TMS370 Family Opcode/Instruction Map†

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JMP #ra 2/7								INCW #ra,Rd 3/11	MOV Ps,A 2/8			CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
1	JN ra 2/5		MOV A,Pd 2/8				MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7
2	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8				MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7
3	JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8	
4	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes	
5	JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14		
6	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6	
7	JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10	
8	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7	
9	JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9	
A	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV A, lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12	
B	JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, lab 3/10	MOV A, *Rp 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8	

† All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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Table 15. TMS370 Family Opcode/Instruction Map[†] (Continued)

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C D E F	J N V r a 2/5	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
		JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
		JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
		JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):

F4

8

MOVW *n[Rn] 4/15	DIV Rn,A 3/14-63
JMPL *n[Rn] 4/16	
MOV *n[Rn],A 4/17	
MOV A,*n[Rn] 4/16	
BR *n[Rn] 4/16	
CMP *n[Rn],A 4/18	
CALL *n[Rn] 4/20	
CALLR *n[Rn] 4/22	

Legend:

- * = Indirect addressing operand prefix
- & = Direct addressing operand prefix
- # = immediate operand
- #16 = immediate 16-bit number
- lab = 16-label
- n = immediate 8-bit number
- Pd = Peripheral register containing destination type
- Pn = Peripheral register
- Ps = Peripheral register containing source byte
- ra = Relative address
- Rd = Register containing destination type
- Rn = **Register file**
- Rp = Register pair
- Rpd = Destination register pair
- Rps = Source Register pair
- Rs = Register containing source byte

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

development system support

The TMS370 family development support tools include an assembler, a C compiler, a linker, an in-circuit emulator (XDS/22 – extended development support), and compact development tool, and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
 - Includes extensive macro capability
 - Allows high-speed operation
 - Provides format conversion utilities for popular formats
- ANSI C Compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, Sun-3™ or Sun-4™)
 - Generates assembly code for the TMS370 that can be inspected easily
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables direct reference to the TMS370's port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (compact development tool) real-time in-circuit emulation
 - Base (Part Number EDSCDT370 – for PC, requires cable)
 - Cable for 28-pin PLCC (Part No. EDSTRG28PLCC02)
 - Includes EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Allows uploading/downloading program and data memory
 - Executes programs and software routines
 - Includes 1 024 samples trace buffer
 - Provides single-step executable instructions
 - Uses software breakpoints to halt program execution at selected address
- XDS/22 (extended development support) in-circuit emulator
 - Base (Part Number TMDS3762210 for PC, requires cable)
 - Cable for 28-pin PLCC (Part No. TMDS3788828)
 - Contains all the features of the CDT370 described previously but does not have the capability to program the data EEPROM and program EPROM
 - Contains sophisticated breakpoint trace and timing hardware that provides up to 2047 qualified trace samples with symbolic disassembly
 - Allows qualification of breakpoints by address and/or data on any type of memory acquisition. Up to four levels of events can be combined to cause a breakpoint

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development system support (continued)

- Provides timers for analyzing total and average time in routines
- Contains an eight-line logic probe for adding visibility of external signals to the breakpoint qualifier and for tracing display
- Microcontroller programmer
 - Base (Part No. TMDS3760500A – for PC, requires programmer head)
 - Single unit head for 28-pin PLCC (Part No. TMDS3780510A)
 - Personal computer based, window/function-key-oriented user interface for ease of use and rapid learning environment
- Design kit (Part No. TMDS3770110 – for PC)
 - Includes TMS370 Application Board and TMS370 Assembler diskette and documentation
 - Supports quick evaluation of TMS370 functionality
 - Provides capability to upload and download code
 - Provides capability to execute programs and software routines, and to single-step executable instructions
 - Provides software breakpoints to halt program execution at selected addresses
 - Includes wire-wrap prototype area
 - Includes reverse assembler
- Starter Kit (Part No. TMDX37000 – for PC)
 - Includes TMS370 Assembler diskette and documentation
 - Includes TMS370 Simulator
 - Includes programming adapter board and programming software
 - Does not include (to be supplied by the user):
 - + 5 V power supply
 - ZIF sockets
 - Nine-pin RS232 cable



device numbering conventions

Figure 13 illustrates the numbering and symbol nomenclature for the TMS370Cx0x family.

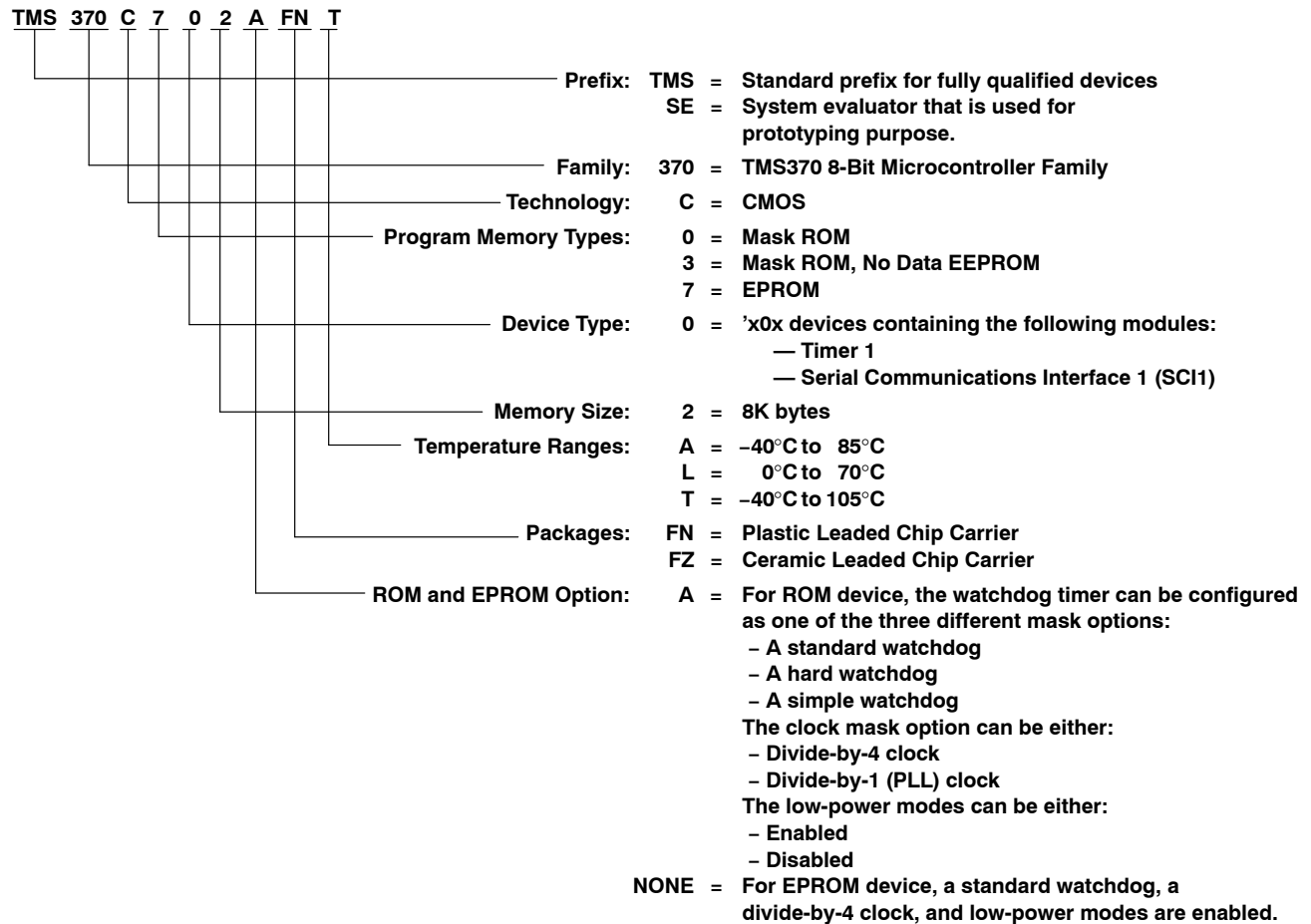


Figure 13. TMS370Cx0x Family Nomenclature

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device part numbers

Table 16 provides all of the 'x0x devices available. The device part number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog timer options desired. Each device can have only one of the three possible watchdog timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 16. Device Part Numbers

DEVICE PART NUMBERS FOR 28 PINS (LCC)
TMS370C002AFNA TMS370C002AFNL TMS370C002AFNT
TMS370C302AFNA TMS370C302AFNL TMS370C302AFNT
TMS370C702FNT
SE370C702FZT†

† System evaluators are for use in prototype environment and their reliability has not been characterized.

new code release form

Figure 14 shows a sample of the new code release form.

NEW CODE RELEASE FORM TEXAS INSTRUMENTS TMS370 MICROCONTROLLER PRODUCTS		DATE: _____																
To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information:																		
1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media) 2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.																		
Company Name: _____ Street Address: _____ Street Address: _____ City: _____ State _____ Zip _____ Customer Part Number: _____ Customer Application: _____		Contact Mr./Ms.: _____ Phone: (_____) _____ Ext.: _____ Customer Purchase Order Number: _____ Customer Print Number *Yes: _____ # _____ No: _____ (Std. spec to be followed) *If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.																
TMS370 Device: _____ TI Customer ROM Number: _____ (provided by Texas Instruments)																		
OSCILLATOR FREQUENCY <table border="0" style="width: 100%; margin-top: 5px;"> <tr> <td style="width: 30%;"></td> <td style="width: 10%; text-align: center;">MIN</td> <td style="width: 10%; text-align: center;">TYP</td> <td style="width: 10%; text-align: center;">MAX</td> </tr> <tr> <td>☐ External Drive (CLKIN)</td> <td>_____</td> <td>_____</td> <td>_____</td> </tr> <tr> <td>☐ Crystal</td> <td>_____</td> <td>_____</td> <td>_____</td> </tr> <tr> <td>☐ Ceramic Resonator</td> <td>_____</td> <td>_____</td> <td>_____</td> </tr> </table> ☐ Supply Voltage MIN: _____ MAX: _____ (std range: 4.5V to 5.5V)				MIN	TYP	MAX	☐ External Drive (CLKIN)	_____	_____	_____	☐ Crystal	_____	_____	_____	☐ Ceramic Resonator	_____	_____	_____
	MIN	TYP	MAX															
☐ External Drive (CLKIN)	_____	_____	_____															
☐ Crystal	_____	_____	_____															
☐ Ceramic Resonator	_____	_____	_____															
TEMPERATURE RANGE <table border="0" style="width: 100%; margin-top: 5px;"> <tr> <td style="width: 30%;">☐ 'L':</td> <td style="width: 70%;">0° to 70°C (standard)</td> </tr> <tr> <td>☐ 'A':</td> <td>-40° to 85°C</td> </tr> <tr> <td>☐ 'T':</td> <td>-40° to 105°C</td> </tr> </table>			☐ 'L':	0° to 70°C (standard)	☐ 'A':	-40° to 85°C	☐ 'T':	-40° to 105°C										
☐ 'L':	0° to 70°C (standard)																	
☐ 'A':	-40° to 85°C																	
☐ 'T':	-40° to 105°C																	
SYMBOLIZATION <table border="0" style="width: 100%; margin-top: 5px;"> <tr> <td style="width: 30%;">☐ TI standard symbolization</td> <td style="width: 70%;"></td> </tr> <tr> <td>☐ TI standard w/customer part number</td> <td></td> </tr> <tr> <td>☐ Customer symbolization</td> <td></td> </tr> <tr> <td colspan="2">(per attached spec, subject to approval)</td> </tr> </table>			☐ TI standard symbolization		☐ TI standard w/customer part number		☐ Customer symbolization		(per attached spec, subject to approval)									
☐ TI standard symbolization																		
☐ TI standard w/customer part number																		
☐ Customer symbolization																		
(per attached spec, subject to approval)																		
NON-STANDARD SPECIFICATIONS: ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.																		
RELEASE AUTHORIZATION: This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cycletime commences when this document is signed off and the verification code is approved by the customer.																		
<table border="0" style="width: 100%;"> <tr> <td style="width: 50%; vertical-align: top;"> 1. Customer: _____ Date: _____ </td> <td style="width: 50%; vertical-align: top;"> 2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____ </td> </tr> </table>			1. Customer: _____ Date: _____	2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____														
1. Customer: _____ Date: _____	2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____																	

CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS

Low Power Modes ☐ Enabled ☐ Disabled	Watchdog counter ☐ Standard ☐ Hard Enabled ☐ Simple Counter	Clock Type ☐ Standard (/4) ☐ PLL (/1)

NOTE:
 Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B).

PACKAGE TYPE

☐ 'N' 28-pin PDIP ☐ "FN" 28-pin PLCC ☐ "N" 40-pin PDIP ☐ "NJ" 40-pin PSDIP (formerly known as N2)	☐ "FN" 44-pin PLCC ☐ "FN" 68-pin PLCC ☐ "NM" 64-pin PSDIP

BUS EXPANSION

☐ YES	☐ NO

Figure 14. Sample New Code Release Form

TMS370Cx0x

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Table 17. Peripheral File Frame Compilation

Table 17 is a collection of all the peripheral file frames used in the 'Cx0x (provided for a quick reference).

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	System Configuration Registers								SCCR0
	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	
	—	—	—	AUTO WAIT DISABLE	—	MEMORY DISABLE	—	—	
P011	—	—	—	AUTO WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT / STANDBY	PWRDWN / IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D P01E P01F	Reserved								
P020	Digital Port Control Registers								APORT1 APORT2 ADATA ADIR DPORT1 DPORT2 DDATA DDIR
	Reserved								
	Port A Control Register 2 (must be 0)								
	Port A Data								
	Port A Direction								
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0) [†]					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR
P040	Timer Module Register Memory Map								T1CNTR T1C
	Modes: Dual-Compare and Capture/Compare								
	Bit 15 T1Counter MSbyte Bit 8								
	Bit 7 T1 Counter LSbyte Bit 0								
	Bit 15 Compare Register MSbyte Bit 8								
P043	Bit 7 Compare Register LSbyte Bit 0								

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 17. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Dual-Compare and Capture/Compare (Continued)									
P044	Capture/Compare Register MSbyte							Bit 8	T1CC
P045	Capture/Compare Register LSbyte							Bit 0	
P046	Watchdog Counter MSbyte							Bit 8	WDCNTR
P047	Watchdog Counter LSbyte							Bit 0	
P048	Watchdog Reset Key							Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE=0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI
SCI1 Module Control Memory Map									
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNC/ ISOSYNC	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	Reserved								

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

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Table 17. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF
P05A P05B P05C	Reserved								
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	SCI STEST	SCITX PRIORITY	SCIRX PRIORITY	SCI ESPEN	—	—	—	—	SCIPRI

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC}) (see Note 2)	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	500 mW
Operating free-air temperature range, T_A : L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS} .

2. Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 3)		3		5.5	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET	2		V_{CC}	V
		XTAL2/CLKIN	0.8 V_{CC}		V_{CC}	
		RESET	0.7 V_{CC}		V_{CC}	
V_{MC}	MC (mode control) voltage	EEPROM write protect override (WPO)	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	
		Microcomputer	V_{SS}		0.3	
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	
		T version	–40		105	

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS} .

3. RESET must be activated externally when V_{CC} or SYSCLK is not within the recommended operating range.

TMS370Cx0x

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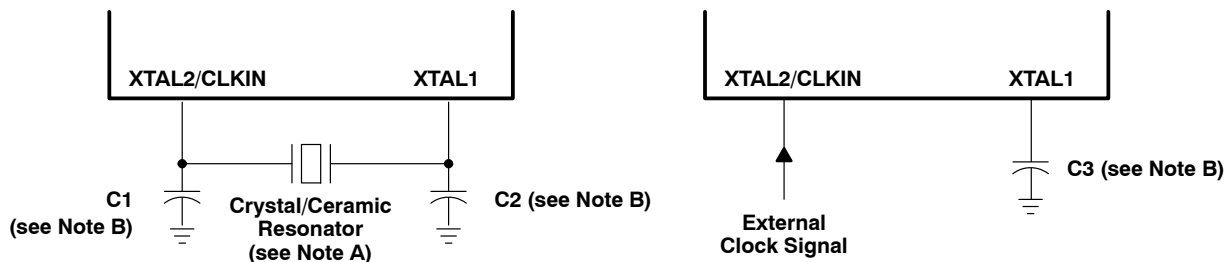
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OL}	Low-level output voltage	I _{OL} = 1.4 mA			0.4	V
V _{OH}	High-level output voltage	I _{OH} = -50 µA	0.9 V _{CC}			V
		I _{OH} = -2 mA	2.4			
I _I	Input current	0 V ≤ V _I ≤ 0.3 V			10	µA
		0.3 V < V _I ≤ 13 V			650	
		See Note 4 12 V ≤ V _I ≤ 13 V			50	mA
	I/O pins	0 V ≤ V _I ≤ V _{CC}			± 10	µA
I _{OL}	Low-level output current	V _{OL} = 0.4 V	1.4			mA
I _{OH}	High-level output current	V _{OH} = 0.9 V _{CC}	- 50			µA
		V _{OH} = 2.4 V	- 2			mA
I _{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 7)	See Notes 5 and 6 SYSCLK = 5 MHz		20	36	mA
		See Notes 5 and 6 SYSCLK = 3 MHz		13	25	
		See Notes 5 and 6 SYSCLK = 0.5 MHz		5	11	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 8)	See Notes 5 and 6 SYSCLK = 5 MHz		10	17	mA
		See Notes 5 and 6 SYSCLK = 3 MHz		6.5	11	
		See Notes 5 and 6 SYSCLK = 0.5 MHz		2	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 9)	See Notes 5 and 6 SYSCLK = 3 MHz		4.5	8.6	mA
		See Notes 5 and 6 SYSCLK = 0.5 MHz		1.5	3.0	
	Supply current (HALT mode)	See Note 5 XTAL2/CLKIN < 0.2 V		1	30	µA

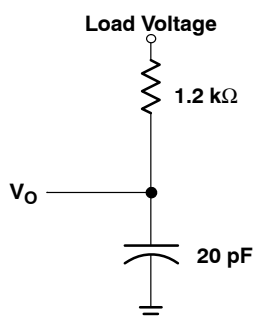
- NOTES: 4. Input current I_{pp} is a maximum of 50 mA only when programming EPROM.
5. Single chip mode, ports configured as inputs or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} - 0.2 V.
6. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = 0.01 mA x (total load capacitance + crystal capacitance in pF).
7. Maximum operating current = 5.6 (SYSCLK) + 8 mA.
8. Maximum standby current = 3 (SYSCLK) + 2 mA. (OSC POWER bit = 0).
9. Maximum standby current = 2.24 (SYSCLK) + 1.9 mA. (OSC POWER bit = 1, only valid up to 3 MHz of SYSCLK).





NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
B. The values of C1 and C2 are typically 15 pF and C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 15. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4 \text{ V}$; Load Voltage = 0 V

Case 2: $V_O = V_{OL} = 0.4 \text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 16. Typical Output Load Circuit (See Note A)

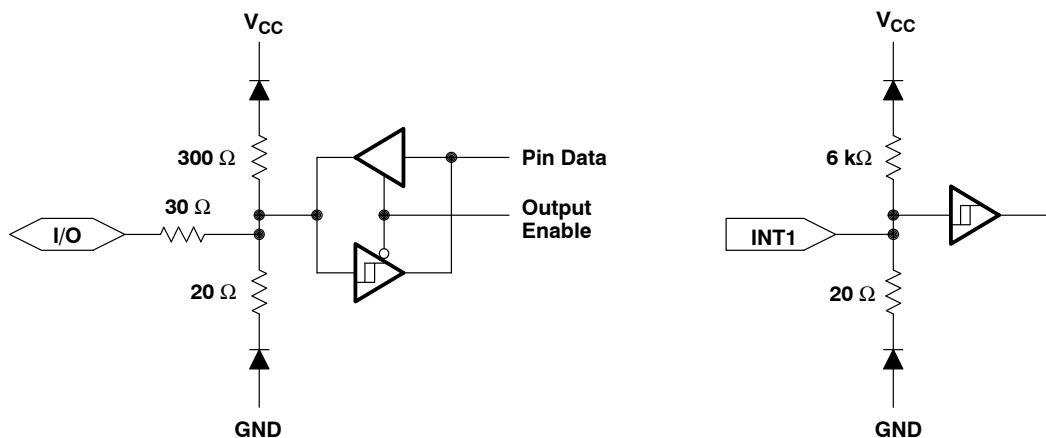


Figure 17. Typical Buffer Circuitry

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

AR	Array	SC	SYSCLK
B	Byte	SCC	SCICLK
CI	XTAL2/CLKIN	TXD	SCITXD
RXD	SCIRXD		

Lowercase subscripts and their meanings are:

c	cycle time (period)	su	setup time
d	delay time	v	valid time
f	fall time	w	pulse duration (width)
r	rise time		

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid

All timings are measured between high and low measurement points as indicated in Figure 18 and Figure 19.

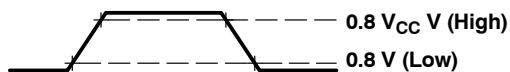


Figure 18. XTAL2/CLKIN Measurement Points

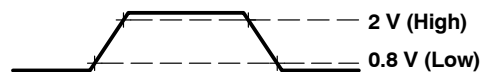


Figure 19. General Measurement Points

external clocking requirements for divide-by-4 clock (see Note 10 and Figure 20)

NO.		MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 11)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN Crystal operating frequency	2	20	MHz
	SYSCLK Internal system clock operating frequency†	0.5	5	MHz

† SYSCLK = CLKIN/4

NOTES: 10. For V_{IL} and V_{IH} , refer to recommended operating conditions.

11. This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

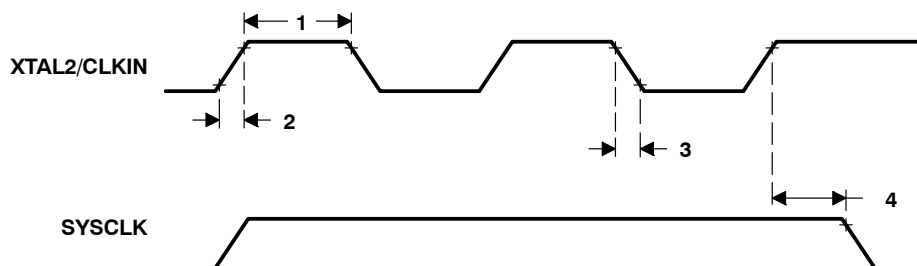


Figure 20. External Clock Timing for Divide-by-4

external clocking requirements for divide-by-1 clock (PLL) (see Note 10 and Figure 21)

NO.		MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 11)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN Crystal operating frequency	2	5	MHz
	SYSCLK Internal system clock operating frequency‡	2	5	MHz

‡ SYSCLK = CLKIN/1

NOTES: 10. For V_{IL} and V_{IH} , refer to recommended operating conditions.

11. This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

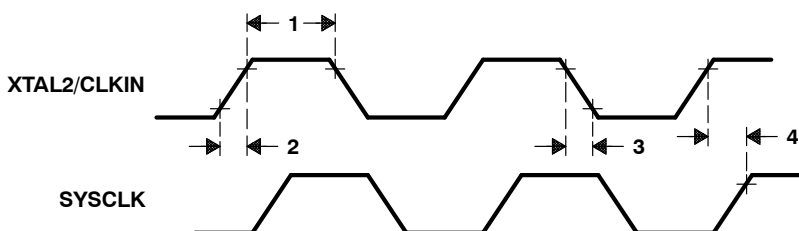


Figure 21. External Clock Timing for Divide-by-1

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switching characteristics and timing requirements (see Note 12 and Figure 22)

NO.	PARAMETER		MIN	MAX	UNIT
5	t_c	Cycle time, SYSCLK (system clock)	200	2000	ns
			200	500	
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low	$0.5 t_c - 20$	$0.5 t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high	$0.5 t_c$	$0.5 t_c + 20$	ns

NOTE 12: t_c = system-clock cycle time = $1 / \text{SYSCLK}$

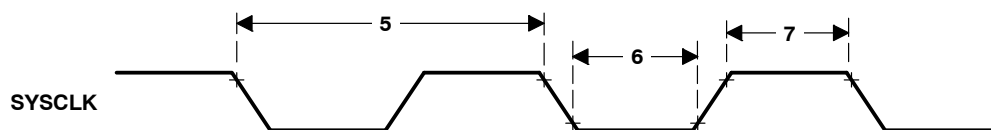


Figure 22. SYSCLK Timing

general purpose output signal switching time requirements (see Figure 23)

	MIN	NOM	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns

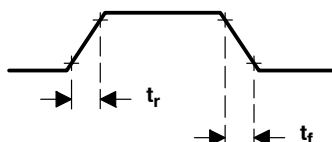


Figure 23. Signal Switching Time

recommended EEPROM timing requirements for programming

	MIN	MAX	UNIT
$t_{w(PGM)B}$ Pulse duration, programming signal to ensure valid data is stored (byte mode)	10		ms
$t_{w(PGM)AR}$ Pulse duration, programming signal to ensure valid data is stored (array mode)	20		ms

recommended EPROM operating conditions for programming

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5.5	6	V
V_{PP} Supply voltage at MC pin	13	13.2	13.5	V
I_{PP} Supply current at MC pin during programming ($V_{PP} = 13$ V)		30	50	mA
SYSCLK System clock operating frequency	Divide-by-4	0.5	5	MHz
	Divide-by-1	2	5	

recommended EPROM timing requirements for programming

	MIN	NOM	MAX	UNIT
$t_{w(EPGM)}$ Pulse duration, programming signal (see Note 13)	0.40	0.50	3	ms

NOTE 13: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.



SCI1 isosynchronous mode timing characteristics and requirements for internal clock
(see Note 12 and Figure 24)

NO.		MIN	MAX	UNIT
24	$t_c(\text{SCC})$ Cycle time, SCICLK	$2t_c$	$131\,072t_c$	ns
25	$t_w(\text{SCCL})$ Pulse duration, SCICLK low	$t_c - 45$	$0.5t_c(\text{SCC}) + 45$	ns
26	$t_w(\text{SCCH})$ Pulse duration, SCICLK high	$t_c - 45$	$0.5t_c(\text{SCC}) + 45$	ns
27	$t_d(\text{SCCL-TXDV})$ Delay time, SCITXD valid after SCICLK low	- 50	60	ns
28	$t_v(\text{SCCH-TXD})$ Valid time, SCITXD data valid after SCICLK high	$t_w(\text{SCCH}) - 50$		ns
29	$t_{su}(\text{RXD-SCCH})$ Setup time, SCIRXD to SCICLK high	$0.25 t_c + 145$		ns
30	$t_v(\text{SCCH-RXD})$ Valid time, SCIRXD data valid after SCICLK high	0		ns

NOTE 12: t_c = system-clock cycle time = $1/\text{SYSCLK}$

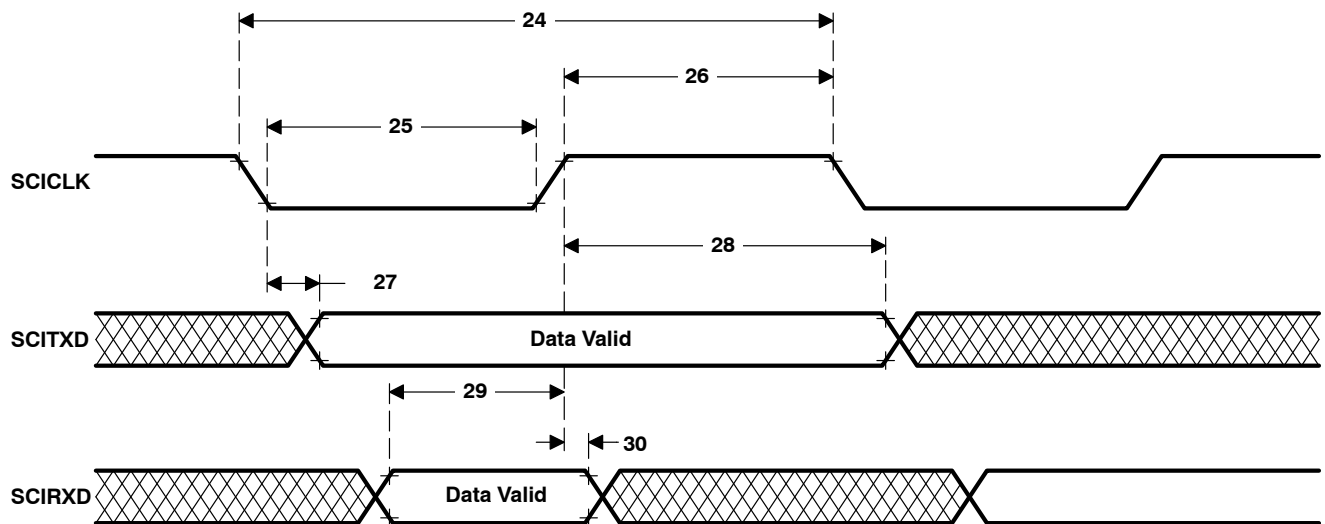


Figure 24. SCI1 Isosynchronous Mode Timing for Internal Clock

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SCI1 isosynchronous mode timing characteristics and requirements for external clock (see Note 12 and Figure 25)

NO.		MIN	MAX	UNIT
31	$t_c(\text{SCC})$ Cycle time, SCICLK	$10t_c$		ns
32	$t_w(\text{SCCL})$ Pulse duration, SCICLK low	$4.25t_c + 120$		ns
33	$t_w(\text{SCCH})$ Pulse duration, SCICLK high	$t_c + 120$		ns
34	$t_d(\text{SCCL-TXDV})$ Delay time, SCITXD valid after SCICLK low		$4.25t_c + 145$	ns
35	$t_v(\text{SCCH-TXD})$ Valid time, SCITXD data valid after SCICLK high	$t_w(\text{SCCH})$		ns
36	$t_{su}(\text{RXD-SCCH})$ Setup time, SCIRXD to SCICLK high	40		ns
37	$t_v(\text{SCCH-RXD})$ Valid time, SCIRXD data after SCICLK high	$2t_c$		ns

NOTE 12: t_c = system-clock cycle time = 1 / SYSCLK

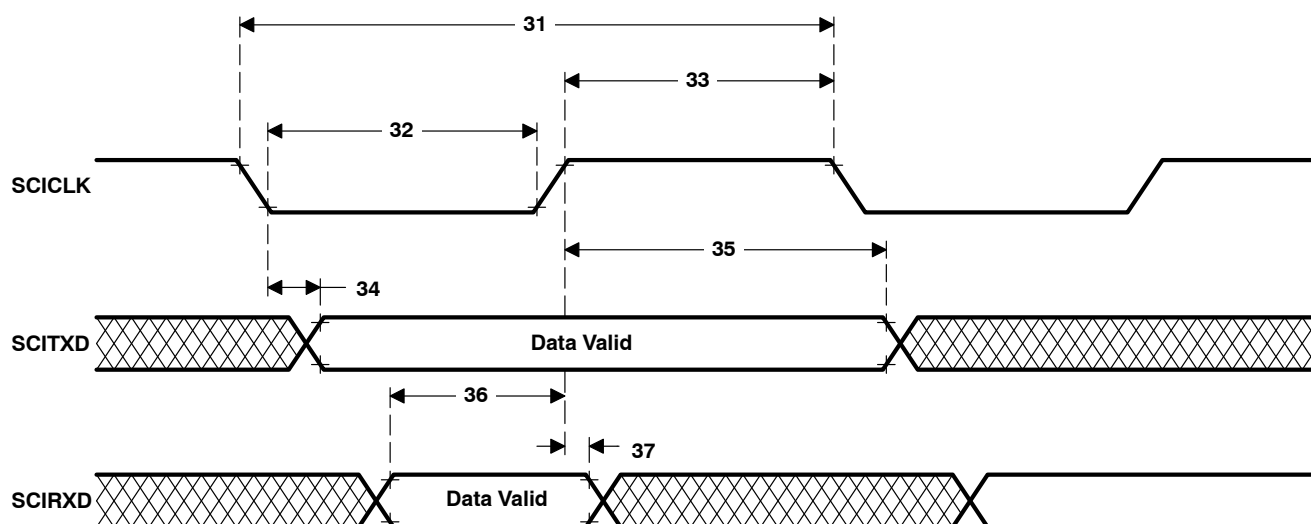


Figure 25. SCI1 Isosynchronous Timing for External Clock

Table 18 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

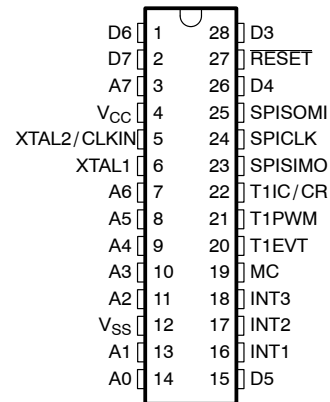
Table 18. TMS370Cx0x Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 28 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C002AFNA TMS370C002AFNL TMS370C002AFNT TMS370C302AFNA TMS370C302AFNL TMS370C302AFNT TMS370C702FNT
FZ – 28 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C702FZT

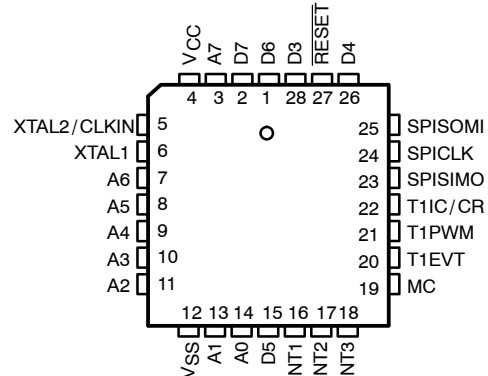
General Information	1
Selection Guide/Tools	2
Ops Cond/Timing/Glossary	3
TMS370Cx0x Data Sheet	4
TMS370Cx1x Data Sheet	5
TMS370Cx2x Data Sheet	6
TMS370Cx32 Data Sheet	7
TMS370Cx36 Data Sheet	8
TMS370Cx4x Data Sheet	9
TMS370Cx5x Data Sheet	10
TMS370Cx6x Data Sheet	11
TMS370Cx7x Data Sheet	12
TMS370Cx8x Data Sheet	13
TMS370Cx9x Data Sheet	14
TMS370CxAx Data Sheet	15
TMS370CxBx Data Sheet	16
TMS370CxCx Data Sheet	17
Mechanical Data	18
Quality and Reliability	19
Electrostatic Discharge Guidelines	20

- **CMOS/EEPROM/EPROM Technologies on a Single Device**
 - Mask-ROM Devices for High-Volume Production
 - One-Time-Programmable (OTP) EPROM Devices for Low-Volume Production
 - Reprogrammable-EPROM Devices for Prototyping Purposes
- **Internal System Memory Configurations**
 - On-Chip Program Memory Versions
 - ROM: 2K, 4K, or 8K Bytes
 - EPROM: 8K Bytes
 - Data EEPROM: 256 Bytes
 - Static RAM: 128 or 256 Bytes Usable as Registers
- **Flexible Operating Features**
 - Low-Power Modes: STANDBY and HALT
 - Commercial, Industrial, and Automotive Temperature Ranges
 - Clock Options
 - Divide-by-1 (2 MHz–5 MHz SYSCLK) Phase-Locked Loop (PLL)
 - Divide-by-4 (0.5 MHz–5 MHz SYSCLK)
 - Supply Voltage (V_{CC}) 5 V $\pm$ 10%
- **16-Bit General Purpose Timer**
 - Software Configurable as a 16-Bit Event Counter, or a 16-Bit Pulse Accumulator, or a 16-Bit Input Capture Functions, or Two Compare Registers, or a Self-Contained PWM Function
 - Software Programmable Input Polarity
 - 8-Bit Prescaler, Providing a 24-Bit Real-Time Timer
- **On-Chip 24-Bit Watchdog Timer**
 - EPROM/OTP Devices:
 - EPROM '712A Standard Watchdog
 - EPROM '712B Hard Watchdog
 - Mask-ROM Devices: Hard Watchdog, Simple Counter, or Standard Watchdog
- **Flexible Interrupt Handling**
 - Two Software Programmable Interrupt Levels
 - Global-and Individual-Interrupt Masking
 - Programmable Rising- or Falling-Edge Detect
 - Individual Interrupt Vectors
- **Serial Peripheral Interface (SPI)**
 - Variable-Length High-Speed Shift Register

**JD AND N PACKAGES
(TOP VIEW)**



**FZ AND FN PACKAGES
(TOP VIEW)**



- Synchronous Master/Slave Operation
- **TMS370 Series Compatibility**
 - Register-to-Register Architecture
 - 128 or 256 General-Purpose Registers
 - 14 Powerful Addressing Modes
 - Instructions Upwardly Compatible With All TMS370 Devices
- **CMOS/TTL Compatible I/O Pins/Packages**
 - All Peripheral Function Pins Software Configurable for Digital I/O
 - 21 Bidirectional Pins, 1 Input Pin
 - 28-Pin Plastic and Ceramic DIP, or Leaded Chip Carrier (LCC) Packages
- **Workstation/PC-Based Development System**
 - C Compiler and C Source Debugger
 - Real-Time In-Circuit Emulation
 - Extensive Breakpoint/Trace Capability
 - Multi-Window User Interface
 - Microcontroller Programmer



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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TMS370Cx1x

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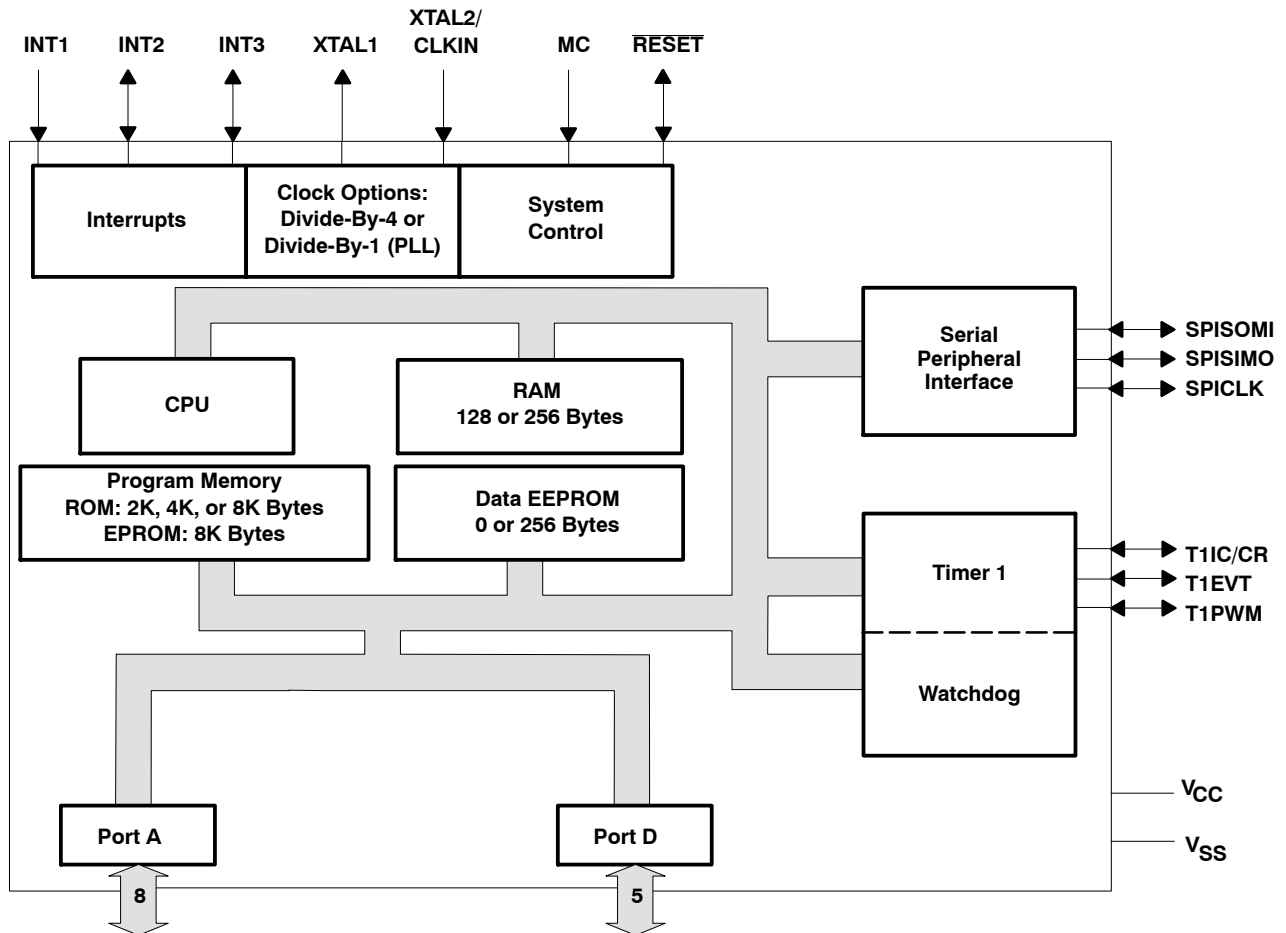
Pin Descriptions

28 PINS DIP and LCC		I/O†	DESCRIPTION
NAME	NO.		
A0 A1 A2 A3 A4 A5 A6 A7	14 13 11 10 9 8 7 3	I / O	Port A is a general-purpose bidirectional I/O port.
D3 D4 D5 D6 D7	28 26 15 1 2	I / O	Port D is a general-purpose bidirectional I/O port. D3 is also configurable as SYSCLK.
INT1 INT2 INT3	16 17 18	I I / O I / O	External interrupt (non-maskable or maskable)/general-purpose input pin External maskable interrupt input/general-purpose bidirectional pin External maskable interrupt input/general-purpose bidirectional pin
T1IC/CR T1PWM T1EVT	22 21 20	I / O	Timer1 input capture/counter reset input pin/general-purpose bidirectional pin Timer1 PWM output pin/general-purpose bidirectional pin Timer1 external event input pin/general-purpose bidirectional pin
SPISOMI SPISIMO SPICLK	25 23 24	I / O	SPI slave output pin, master input pin/general-purpose bidirectional pin SPI slave input pin, master output pin/general-purpose bidirectional pin SPI bidirectional serial clock pin/general-purpose bidirectional pin
RESET	27	I / O	System reset bidirectional pin; as input pin, RESET initializes the microcontroller; as open-drain output, RESET indicates that an internal failure was detected by watchdog or oscillator fault circuit.
MC	19	I	Mode control input pin; enables EEPROM write protection override (WPO) mode, also EPROM V_{PP}
XTAL2/CLKIN XTAL1	5 6	I O	Internal oscillator crystal input/External clock source input Internal oscillator output for crystal
V_{CC}	4		Positive supply voltage
V_{SS}	12		Ground reference

† I = input, O = output



functional block diagram



description

The TMS370C010, TMS370C012, TMS370C311, TMS370C310, TMS370C312, TMS370C712, and SE370C712 devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx1x refers to these devices. The TMS370 family provides cost-effective real-time system control through integration of advanced peripheral-function modules and various on-chip memory configurations.

The TMS370Cx1x family of devices is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technologies. Low-operating power, wide-operating temperature range, and noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx1x devices attractive for system designs for automotive electronics, industrial motors, computer peripheral controls, telecommunications, and consumer applications.

All TMS370Cx1x devices contain the following on-chip peripheral modules:

- Serial peripheral interface (SPI)
- One 24-bit general-purpose watchdog timer
- One 16-bit general-purpose timer with an 8-bit prescaler

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description (continued)

Table 1 provides a memory configuration overview of the TMS370Cx1x devices.

Table 1. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		28 PIN PACKAGES
	ROM	EPROM	RAM	EEPROM	
TMS370C010A	4K	—	128	256	FN – PLCC N – PDIP
TMS370C012A	8K	—	256	256	FN – PLCC N – PDIP
TMS370C311A	2K	—	128	–	FN – PLCC N – PDIP
TMS370C310A	4K	—	128	–	FN – PLCC N – PDIP
TMS370C312A	8K	—	128	–	FN – PLCC N – PDIP
TMS370C712A, TMS370C712B	—	8K	256	256	FN – PLCC N – PDIP
SE370C712A [†] , SE370C712B [†]	—	8K	256	256	FZ – CLCC JD – CDIP

[†] System evaluators and development are for use only in prototype environment and their reliability has not been characterized.

The suffix letter (A or B) appended to the device names shown in the device column of Tables 1 and 2 indicates the configuration of the device. ROM or EPROM devices have different configurations as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 2. Suffix Letter Configuration

DEVICE [‡]	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM A	Standard	Divide-by-4 (Standard oscillator)	Enabled
EPROM B	Hard	Divide-by-1 (PLL)	Enabled
ROM A	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

[‡] Refer to the “device numbering conventions” section for device nomenclature and to the “device part numbers” section for ordering.

The 2K bytes, 4K bytes, and 8K bytes of mask-programmable ROM in the associated TMS370Cx1x devices are replaced in the TMS370C712 with 8K bytes of EPROM. All other available memory and on-chip peripherals are identical, with the exception of no data EEPROM on the TMS370C311, TMS370C310, and TMS370C312 devices. The OTP (TMS370C712) device and reprogrammable (SE370C712) device are available.

TMS370C712 OTP devices are available in plastic packages. This microcontroller is effective to use for immediate production updates for other members of the TMS370Cx1x family or for low volume production runs when the mask charge or cycle time for the low-cost mask ROM devices is not practical.

The SE370C712 has a windowed ceramic package to allow reprogramming of the program EPROM memory during the development/prototyping phase of design. The SE370C712 devices allow quick updates to breadboards and prototype systems while iterating initial designs.



description (continued)

The TMS370Cx1x family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all CPU activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx1x features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx1x family is fully instruction-set-compatible, providing easy transition between members of the TMS370 8-bit microcontroller family.

The SPI provides a convenient method of serial interaction for high-speed communications between simpler shift register-type devices, such as display drivers, analog-to-digital (A/D) converters, PLL, input/output (I/O) expansion, or other microcontrollers in the system.

The TMS370Cx1x family provides the system designer with economical, efficient solution to real-time control applications. The TMS370 family extended development system (XDS™) and compact development tool (CDT™) solve the challenge of efficiently developing the software and hardware required to design the TMS370Cx1x into an ever-increasing number of complex applications. The application source code can be written in assembly and C language, and the output code can be generated by the linker. The TMS370 family XDS development tool communicates through a standard RS-232-C interface with an existing personal computer. This allows the use of the PC's editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes ease-of-use through extensive menus and screen windowing so that a system designer can begin developing software with minimal training. Precise real-time, in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as reducing the time-to-market cycle.

The TMS370Cx1x family together with the TMS370 family XDS22, CDT370, design kit, starter kit, software tools, the SE370C712 reprogrammable devices, comprehensive product documentation, and customer support provide a complete solution to the needs of the system designer.

central processing unit (CPU)

The CPU on the TMS370Cx1x device is the high-performance 8-bit TMS370 CPU module. The 'x1x implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'x1x instruction map is shown in Table 17 in the TMS370Cx1x instruction set overview section.

The '370Cx1x CPU architecture provides the following components:

CPU registers:

- A stack pointer that points to the last entry in the memory stack
- A status register that monitors the operation of the instructions and contains the global interrupt-enable bits
- A program counter (PC) that points to the memory location of the next instruction to be executed

central processing unit (CPU) (continued)

Figure 1 illustrates the CPU registers and memory blocks.

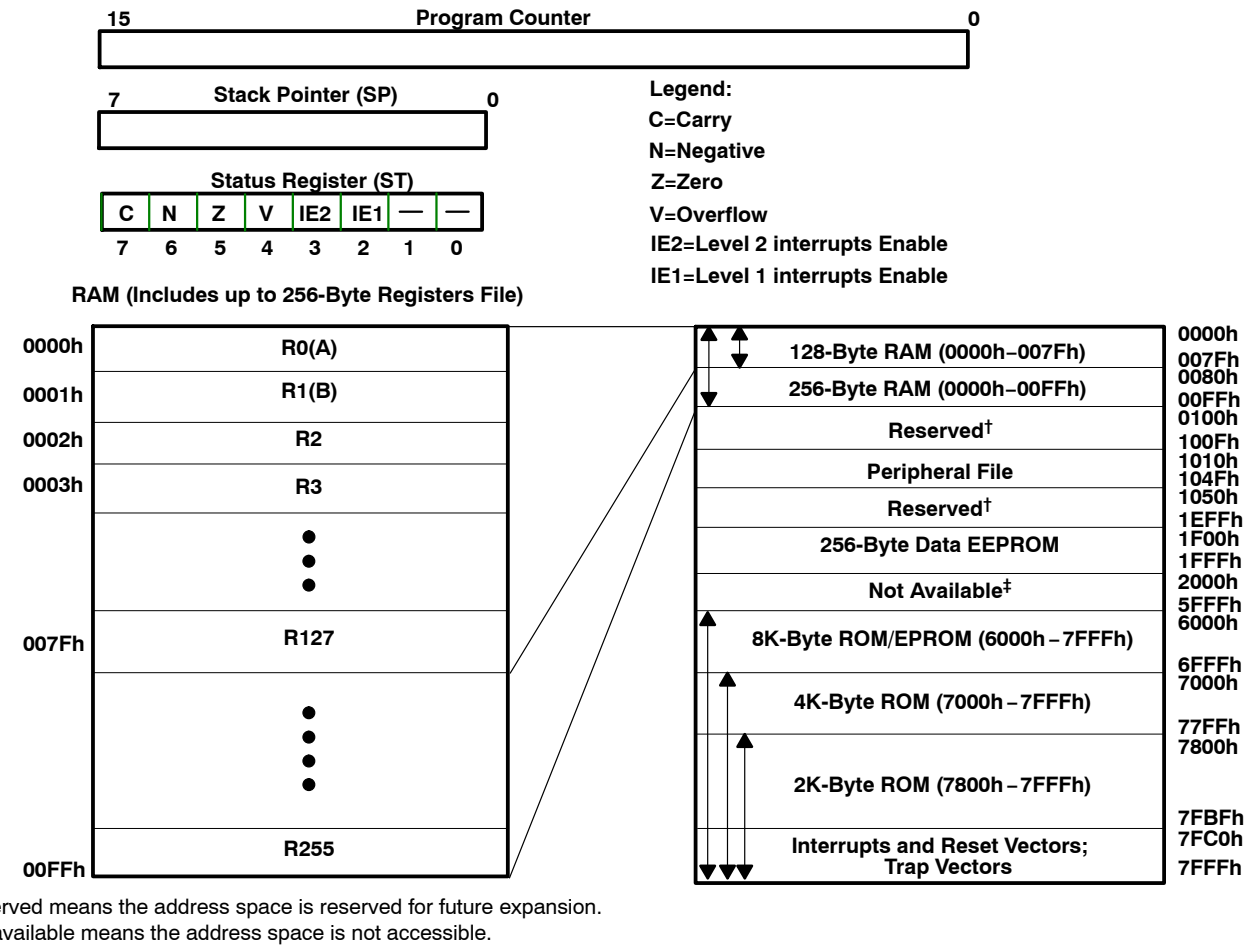


Figure 1. Programmer's Model

A memory map includes:

- 128- or 256-byte general-purpose RAM that can be used for data memory storage, program instructions, general purpose register, or the stack
- A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM/EPROM programming control
- 256-byte EEPROM module, that provides in-circuit programmability and data retention in power-off conditions
- 2K-, 4K-, or 8K-byte ROM or 8K-byte EPROM

stack pointer (SP)

The SP is an 8-bit CPU register. Stack operates as a last-in, first-out, read/write memory. Typically, the stack is used to store the return address on subroutine calls as well as the status register (ST) contents during interrupt sequences.

The SP points to the last entry or top of the stack. The SP is incremented automatically before data is pushed onto the stack and decremented after data is popped from the stack. The stack can be placed anywhere in the on-chip RAM.

central processing unit (CPU) (continued)

status register (ST)

The ST monitors the operation of the instructions and contains the global interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits.

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional-jump instructions) use the status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

The ST, status-bit notation, and status-bit definitions are shown in Table 3.

Table 3. Status Registers

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most significant byte (MSbyte) and least significant byte (LSbyte) of a 16-bit address.

During reset, the contents of the reset vector (7FFEh, 7FFFh) are loaded into the PC. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 6000h as the contents of the reset vector.

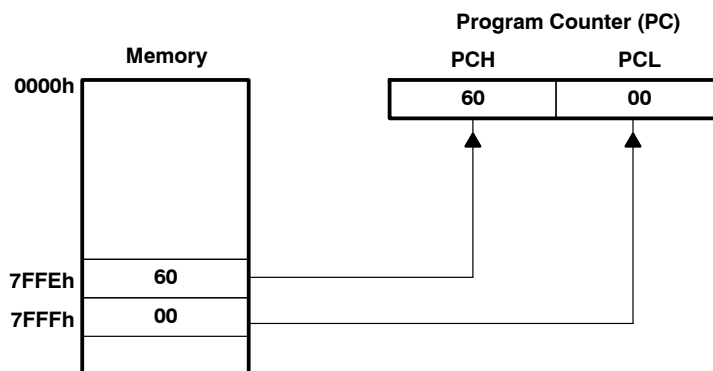


Figure 2. Program Counter After Reset

memory map

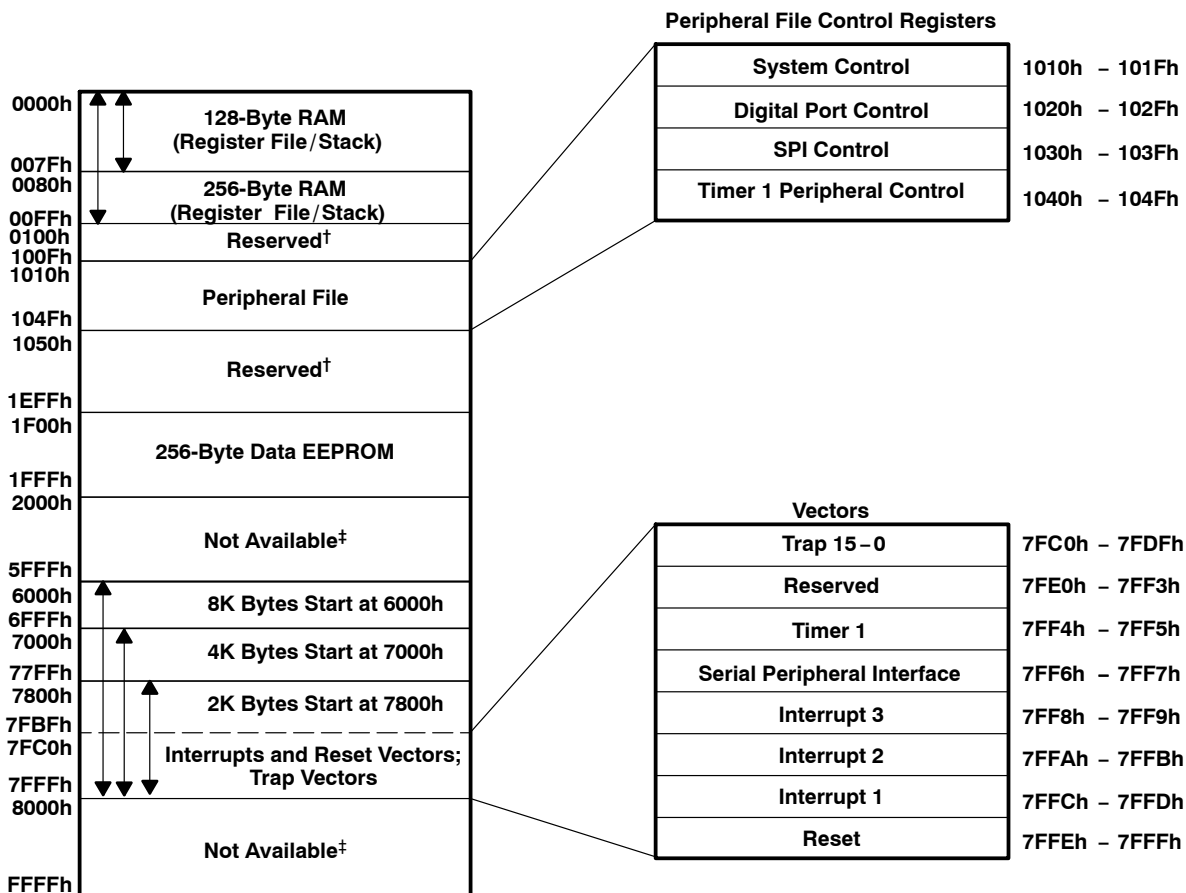
The TMS370Cx1x architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. As shown in Figure 3, the TMS370Cx1x provides memory-mapped RAM, ROM, data EEPROM, I/O pins, peripheral functions, and system-interrupt vectors.

The peripheral file contains all I/O port control, peripheral status and control, EEPROM, EPROM, and system-wide control functions. The peripheral file is located between 1010h to 104Fh and is divided logically into four peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed.

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TMS370Cx1x CPU (continued)



† Reserved means that the address space is reserved for future expansion.

‡ Not available means that the address space is not accessible.

Figure 3. TMS370Cx1x Memory Map

RAM/register file (RF)

Locations within the RAM address space can serve as the RF, general-purpose read/write memory, program memory, or the stack instructions. The TMS370Cx10, TMS370Cx11, and TMS370C312 contain 128 bytes of internal RAM mapped beginning at location 0000h (R0) and continuing through location 007Fh (R127) which is shown in Table 4 along with '712 devices.

Table 4. RAM Memory Map

	'x10, 'x11 AND '312	'712
RAM size	128 bytes	256 bytes
Memory mapped	0000h – 007Fh	0000h – 00FFh

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370Cx1x control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or P for a decimal designator. For example, the system-control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 5 shows the TMS370Cx1x PF address map.

Table 5. TMS370Cx1x Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h – 100Fh	P000 – P00F	Reserved
1010h – 101Fh	P010 – P01F	System and EPROM/EEPROM control registers
1020h – 102Fh	P020 – P02F	Digital I/O port control registers
1030h – 103Fh	P030 – P03F	SPI registers
1040h – 104Fh	P040 – P04F	Timer 1 registers
1050h – 10FFh	P050 – P0FF	Reserved

data EEPROM

The TMS370Cx1x devices, containing 256 bytes of data EEPROM, have memory mapped beginning at location 1F00h and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B). The data EEPROM features include the following:

- Programming:
 - Bit-, byte-, and block-write/erase modes
 - Internal charge pump circuitry. No external EEPROM programming voltage supply is needed.
 - Control register: Data EEPROM programming is controlled by the DEECTL located in the PF frame beginning at location P01A. See Table 6.
 - In-circuit programming capability. There is no need to remove the device to program.
- Write protection. Writes to the data EEPROM are disabled during the following conditions.
 - Reset. All programming of the data EEPROM module is halted.
 - Write protection active. There is one write-protect bit per 32-byte EEPROM block.
 - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 6. Data EEPROM and PROGRAM EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME
P01A	DEECTL	Data EEPROM Control Register
P01B	—	Reserved
P01C	EPCTL	Program EPROM Control Register

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program EPROM[†]

The TMS370C712 device contains 8K bytes of EPROM mapped, beginning at location 6000h and continuing through location 7FFFh as shown in Figure 3. Reading the program EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the EPROM control register (EPCTL). The program EPROM module features include:

- Programming
 - In-circuit programming capability if V_{PP} is applied to MC
 - Control register: EPROM programming is controlled by the EPROM control register (EPCTL) located in the peripheral file (PF) frame at location P01Ch as shown in Table 6.
- Write protection: Writes to the program EPROM are disabled under the following conditions:
 - Reset: All programming to the EPROM module is halted
 - Low-power modes
 - 13 V not applied to MC

program ROM[†]

The program ROM consists of 2K to 8K bytes of mask programmable read-only memory (see Table 7). The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication.

Table 7. Program ROM Memory Map

	'x11	'x10	'x12
ROM size	2K bytes	4K bytes	8K bytes
Memory mapped	7800h – 7FFFh	7000h – 7FFFh	6000h – 7FFFh

system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx1x CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are generated internally, while one ($\overline{\text{RESET}}$ pin) is controlled externally. These actions are as follows:

- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside of the recommended operating range. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.
- External $\overline{\text{RESET}}$ pin. A low level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x1x device to reset external system components. Additionally, if a cold start (V_{CC} is off for several hundred milliseconds) condition or oscillator failure occurs or the $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

[†] Memory addresses 7FF8h through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions are located between addresses 7FC0h and 7FDFh.

system reset (continued)

After a reset, the program can check the oscillator-fault flag (OSC FLT FLAG, SCCR0.4), the cold-start flag (COLD START, SCCR0.7) and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 8 depicts the reset sources.

Table 8. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Register A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

When an external reset circuit is connected to the **RESET** pin, the pin must be held low until the clock signal is valid and V_{CC} is within the operating range. Figure 4 shows a typical reset circuit.

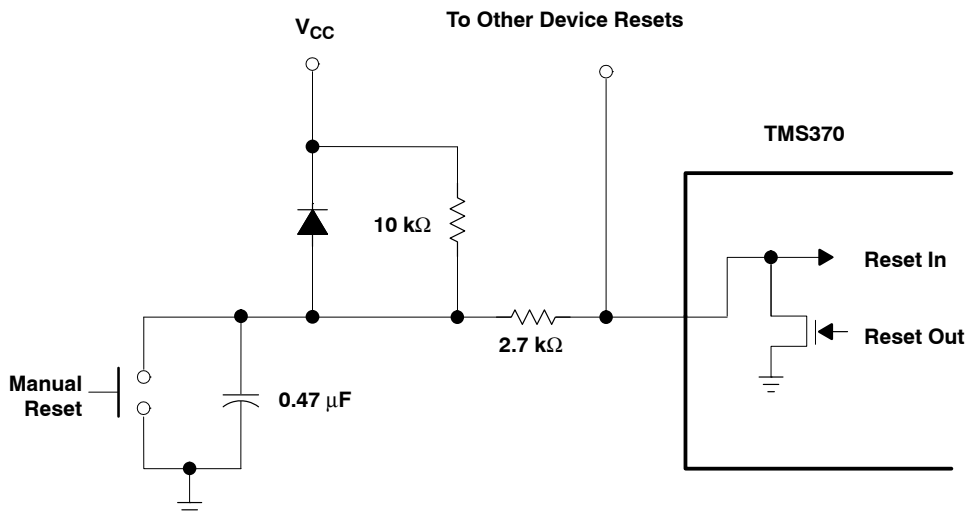


Figure 4. Typical Reset Circuit

interrupts

The TMS370 family software-programmable interrupt structure permits flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global interrupt mask bits (IE1 and IE2) of the ST.

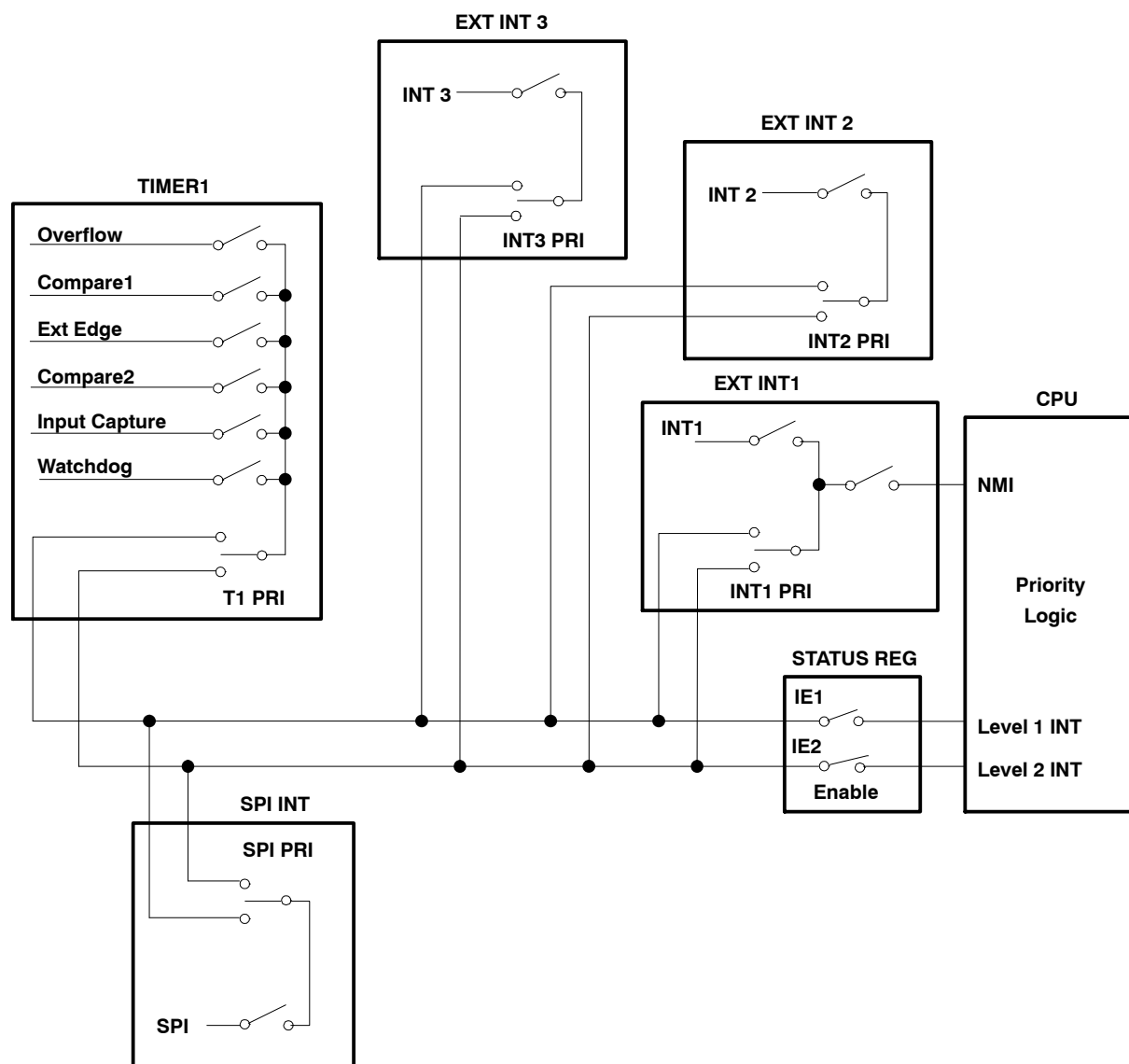


Figure 5. Interrupt Control

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is selectively configured on either the high- or low-priority-interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority

interrupts (continued)

chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending-interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx1x has five hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 9. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. A system interrupt may have multiple interrupt sources. All of the interrupt sources are individually maskable by local interrupt enable control bits in the associated peripheral file. Each interrupt source FLAG bit is individually readable for software polling or to determine which interrupt source generated the associated system interrupt.

Two of the system interrupts are generated by on-chip peripheral functions, and three external interrupts are supported. Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in peripheral file frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual or global enable mask bits. The INT1 NMI bit is protected during non-privileged operation and, therefore, should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software configured as general purpose input/output pins if the interrupt function is not required (INT1 can be similarly configured as an input pin).

Table 9. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY†
External $\overline{\text{RESET}}$ Watchdog Overflow Oscillator Fault Detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	$\overline{\text{RESET}}^\ddagger$	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1 ‡	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2 ‡	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3 ‡	7FF8h, 7FF9h	4
SPI Receiver (Rx)/Transmitter (Tx) Data Complete	SPI INT FLAG	SPIINT	7FF6h, 7FF7h	5
Timer 1 Overflow Timer 1 Compare 1 Timer 1 Compare 2 Timer 1 External Edge Timer 1 Input Capture 1 Watchdog Overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT §	7FF4h, 7FF5h	6

† Relative priority within an interrupt level

‡ Release microcontroller from STANDBY and HALT low-power modes

§ Release microcontroller from STANDBY low-power mode

privileged operation and EEPROM write protection override

The TMS370Cx1x family is designed with significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx1x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) is

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privileged operation and EEPROM write protection override (continued)

set to 1 to enter the nonprivileged mode, disabling write operations to specific configuration-control bits within the PF. Table 10 displays the system-configuration bits which are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

Table 10. Privilege Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCRO	P010.6	OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
SPIPRI	P03F.5 P03F.6 P03F.7	SPI ESPEN SPI PRIORITY SPI STEST
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST

† The privilege bits are shown in a bold typeface in the peripheral file frame 1 section.

The write protect override (WPO) mode provides an external hardware method of overriding the write protection registers (WPRs) of data EEPROM on the TMS370Cx1x. WPO mode is entered by applying a 12-V input to the MC pin after the **RESET** pin input goes high (logic 1). The high voltage on the MC pin during the WPO mode is not the programming voltage for the data EEPROM or Program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware system level capability to modify the content of data EEPROM while the device remains in the application but only while requiring a 12 V external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power and IDLE modes

The TMS370Cx1x devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time when the mask is manufactured.

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls the low-power mode selection.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, and Timer 1 remain active. System processing is suspended until a qualified interrupt (hardware **RESET**, external interrupt on INT1, INT2, INT3, or timer 1 interrupt) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx1x is placed in its lowest power consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware **RESET**, external interrupt on the INT1, INT2, or INT3) is detected. The power-down mode-selection bits are summarized in Table 11.

low-power and IDLE modes (continued)

Table 11. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X †	IDLE

† Don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6-7 bits is ignored. In addition, if an IDLE instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method for always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI is generated always, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (SP, PC, and ST), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the WD timer is inhibited.

clock modules

The 'x1x family provides two clock options that are referred to as divide-by-1 (phase-locked loop) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 MCU. The 'x1x masked ROM devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device. The '712A EPROM has only the divide-by-4, while the '712B has divide-by-1.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a one-to-one match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency, whereas the divide-by-4 produces a SYSCLK which is one-fourth the frequency of the external resonator. Inside of the divide-by-1 module, the frequency of the external resonator is multiplied by four, and the clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. These are formulated as follows:

$$\text{Divide-by-4 option : } \text{SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option : } \text{SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the improved EMI performance. The harmonics of low-speed resonators extend through fewer of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 provides the capability of reducing the resonator speed by four times, and this results in a steeper decay of emissions produced by the oscillator.

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system configuration registers

Table 12 contains system-configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in a bold typeface and shaded areas.

Table 12. Peripheral File Frame 1: System-Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTO WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	V _{PPS}	—	—	—	—	W0	EXE	EPCTL
P01D to P01F	Reserved								

digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 13 shows the specific addresses, registers, and control bits within this peripheral file frame. Table 14 shows the port configuration register setup.

Table 13. Peripheral File Frame 2: Digital Port-Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0) [†]					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

[†] D3 as SYSCLK, set port D control register 2 = 08h.

Table 14. Port Configuration Register Setup

PORT	PIN	abcd 00q1	abcd 00y0
A	0 – 7	Data Out q	Data In y
D	3 – 7	Data Out q	Data In y
a = Port x Control Register 1 b = Port x Control Register 2 c = Data d = Direction			

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programmable timer 1

The programmable Timer 1 (T1) module of the TMS370Cx1x provides the designer with the enhanced timer resources required to perform real-time system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers, T1 and WD, allow program selection of input clock sources (real-time, external event, or pulse accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The Timer 1 module includes three external device pins that can be used for multiple counter functions (operation-mode dependent), or used as general-purpose I/O pins. The T1 module block diagram is shown in Figure 6.

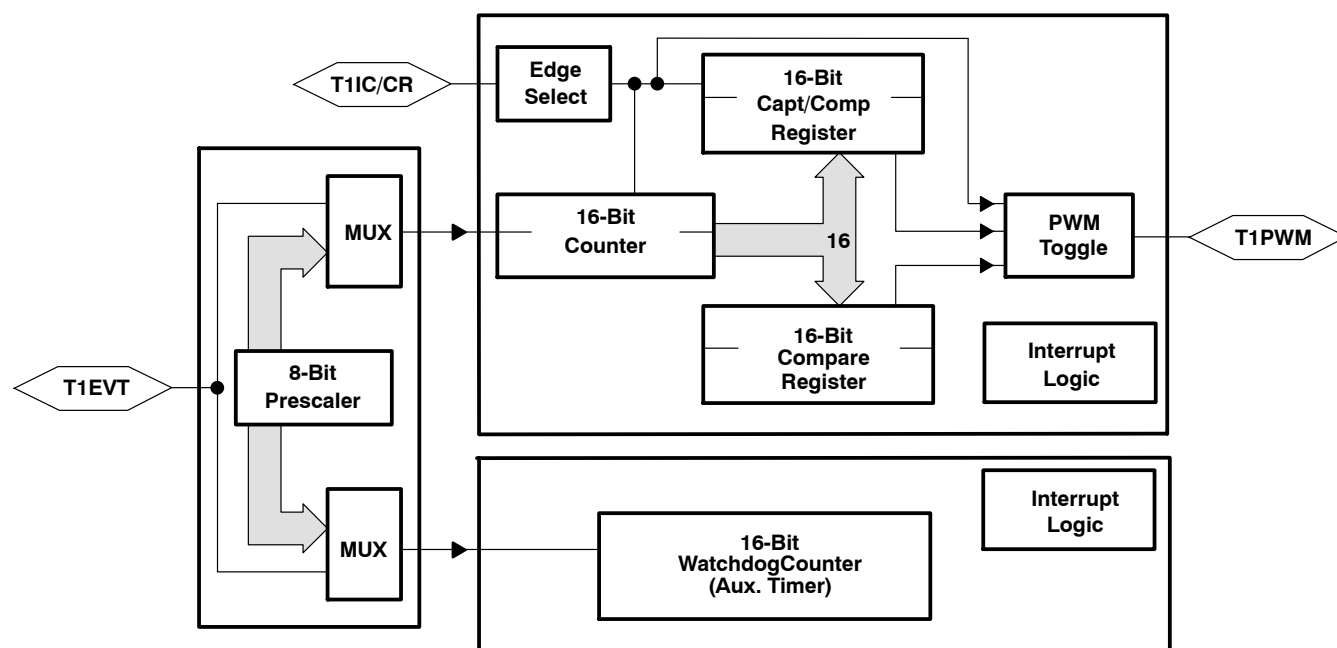


Figure 6. Timer 1 Block Diagram

- Three T1 I/O pins
 - T1IC/CR: T1 input capture / counter-reset input pin, or general-purpose bidirectional I/O pin
 - T1PWM: T1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T1EVT: T1 event input pin, or general-purpose bidirectional I/O pin
- Two operational modes:
 - Dual-compare mode: Provides PWM signal
 - Capture/compare mode: Provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either capture or compare registers.
- One 16-bit WD counter can be used as an event counter, a pulse accumulator, or an interval timer if WD feature is not needed.
- Prescaler/clock sources that determine one of eight clock sources for general-purpose timer

programmable timer 1 (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR)
- Interrupts that can be generated on the occurrence of:
 - A capture
 - A compare equal
 - A counter overflow
 - An external edge detection
- Sixteen T1 module control registers located in the PF frame beginning at address P040

The T1 module control registers are illustrated in Table 15.

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programmable timer 1 (continued)

Table 15. Timer 1 Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Dual-Compare and Capture/Compare									
P040	T1 Counter MSbyte							Bit 8	T1CNTR
P041	T1 Counter LSbyte							Bit 0	
P042	Compare Register MSbyte							Bit 8	T1C
P043	Compare Register LSbyte							Bit 0	
P044	Capture/Compare Register MSbyte							Bit 8	T1CC
P045	Capture/Compare Register LSbyte							Bit 0	
P046	Watchdog Counter MSbyte							Bit 8	WDCNTR
P047	Watchdog Counter LSbyte							Bit 0	
P048	Watchdog Reset Key							Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE=0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

Figure 7 shows the Timer 1 capture/compare mode block diagram. The annotations on the diagram identify the register and the bit(s) in the PF. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.



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programmable timer 1 (continued)

Figure 8 shows the Timer 1 dual-compare mode block diagram. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

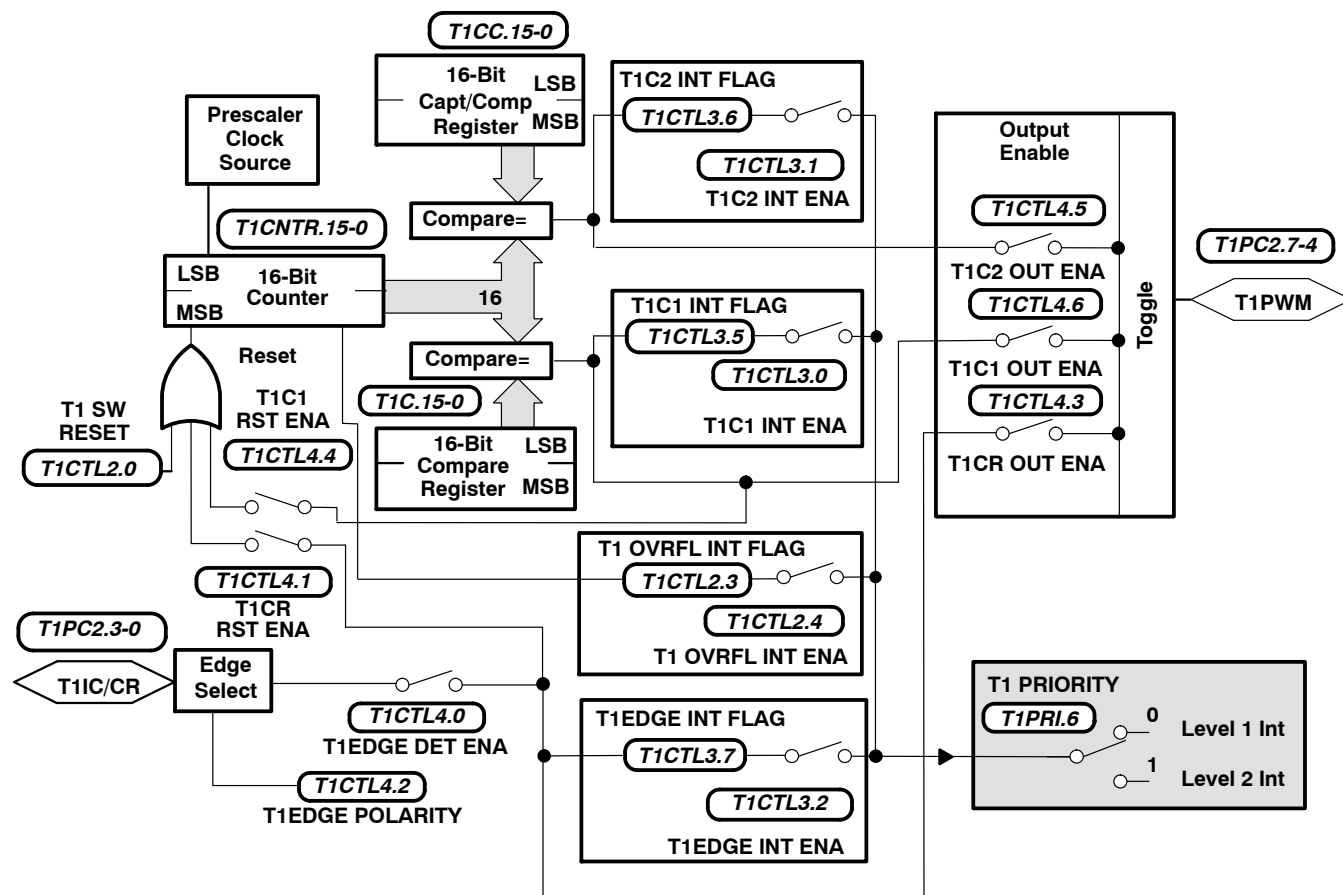


Figure 8. Dual-Compare Mode

programmable timer 1 (continued)

The TMS370Cx1x device includes a 24-bit WD timer, contained in the T1 module, which can be programmed as an event counter, pulse accumulator, or interval timer if the WD function is not used. The WD function is to monitor software and hardware operation and to implement a system reset when the WD counter is not properly serviced (WD counter overflow or WD counter is re-initialized by an incorrect value). The WD can be configured as one of three mask options as follows: standard watchdog, hard WD, or simple counter.

- Standard watchdog configuration (see Figure 9) for 'C712A EPROM and mask-ROM devices:
 - Watchdog mode
 - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the WD reset key or if the counter overflows
 - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
 - Non-watchdog mode
 - Watchdog timer can be configured as an event counter, pulse accumulator or an interval timer

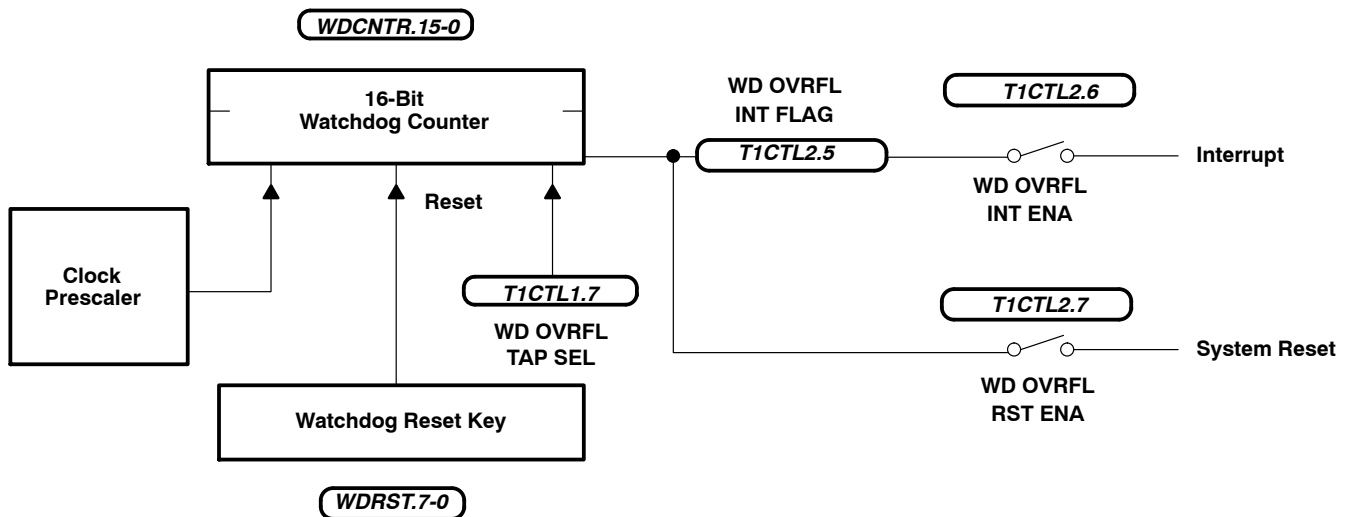


Figure 9. Standard Watchdog

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programmable timer 1 (continued)

- Hard watchdog configuration (see Figure 10) for 'C712B EPROM and mask-ROM devices:
 - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the WDRST or if the counter overflows
 - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
 - Automatic activation of the WD timer upon power-up reset
 - INT1 is enabled as a nonmaskable interrupt during low power modes.

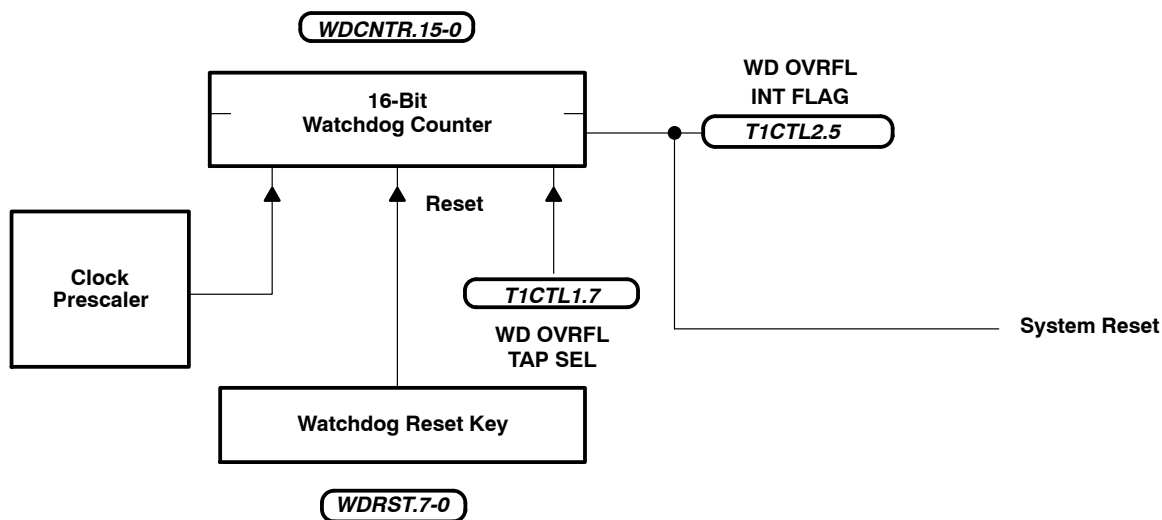


Figure 10. Hard Watchdog

programmable timer 1 (continued)

- Simple counter configuration (see Figure 11) for mask-ROM devices only
 - Simple counter can be configured as an event counter, pulse accumulator, or an internal timer.

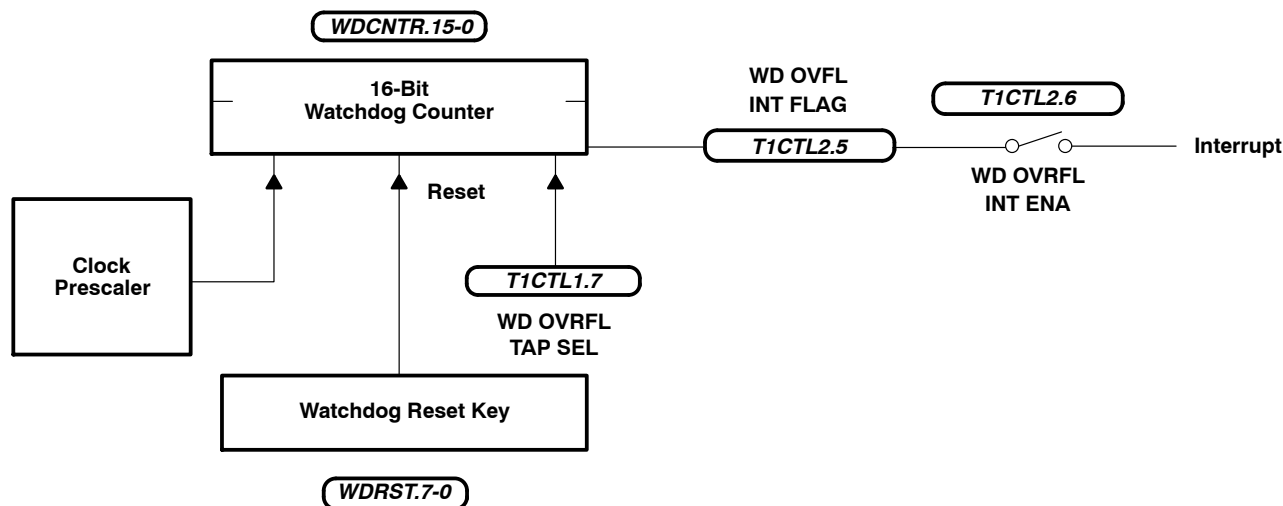


Figure 11. Simple Counter

serial peripheral interface

The SPI is a high-speed synchronous serial I/O port that allows a serial bit stream of programmed length (one to eight bits) to be shifted into and out of the device at a programmable bit transfer rate. The SPI normally is used for communications between the microcontroller and external peripherals or another microcontroller. Typical applications include external I/O or peripheral expansion by way of devices such as shift registers, display drivers, and A/D converters. Multi-device communications are supported by the master/slave operation of the SPI. The SPI module features include the following:

- Three external pins
 - SPISOMI: SPI slave output/master input pin or general-purpose bidirectional I/O pin
 - SPISIMO: SPI slave input/master output pin or general-purpose bidirectional I/O pin
 - SPICLK: SPI serial clock pin or general-purpose bidirectional I/O pin
- Two operational modes: Master and slave
- Baud rate: Eight different programmable rates
 - Maximum baud rate in master mode: 2.5M bps at 5-MHz SYSCLK

$$\text{SPI BAUD RATE} = \frac{\text{SYSCLK}}{2 \times 2^b}$$

where b=bit rate in SPICCR.5-3 (range 0–7)

- Maximum baud rate in slave mode: 625K bps at 5-MHz SYSCLK
for maximum slave SPI BAUD RATE < SYSCLK/8
- Data word format: one to eight data bits
- Simultaneous receiver and transmitter operations (transmit function can be disabled in software)

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serial peripheral interface (continued)

- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Seven SPI module control registers located in control register frame beginning at address P030h

The SPI module-control registers are illustrated in Table 16.

Table 16. SPI Module-Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/SLAVE	TALK	SPI INT ENA	SPICTL
P032 to P036	Reserved								
P037	RCVD7	RCVD6	RCVD5	RCVD4	RCVD3	RCVD2	RCVD1	RCVD0	SPIBUF
P038	Reserved								
P039	SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0	SPIDAT
P03A to P03C	Reserved								
P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
P03F	SPI TEST	SPI PRIORITY	SPI ESPEN	—	—	—	—	—	SPIPRI

The SPI block diagram is illustrated in Figure 12.

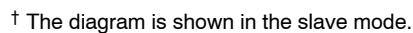


Figure 12. SPI Block Diagram

Table 17 provides an opcode to instruction cross reference of all 73 instructions and 274 opcodes of the '370Cx1x instruction set. The numbers at the top of this table represent the most significant nibble of the opcode while the numbers at the left side of the table represent the least significant nibble (LBN). The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

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Table 17. TMS370 Family Opcode/Instruction Map†

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JMP	ra							INCW	MOV			CLRC /	MOV	MOV	TRAP	LDST
	ra	2/7							#n,Rd	Ps,A			TST A	A,B	A,Rd	15	n
1	JN	ra		MOV			MOV		MOV		MOV				MOV	TRAP	MOV
	ra	2/5		A,Pd			B,Pd		Rs,Pd		Ps,B				B,Rd	14	*n[SP],A
2	JZ	ra	MOV	MOV	MOV	MOV	MOV	MOV				MOV	DEC	DEC	DEC	TRAP	MOV
	ra	2/5	Rs,A	#n,A	Rs,B	Rs,Rd	#n,B	B,A	#n,Rd			Ps,Rd	A	B	Rn	13	A,*n[SP]
3	JC	ra	AND	AND	AND	AND	AND	AND	AND	AND	AND	AND	INC	INC	INC	TRAP	CMP
	ra	2/5	Rs,A	#n,A	Rs,B	Rs,Rd	#n,B	B,A	#n,Rd	A,Pd	B,Pd	#n,Pd	A	B	Rn	12	*n[SP],A
4	JP	ra	OR	OR	OR	OR	OR	OR	OR	OR	OR	OR	INV	INV	INV	TRAP	extend
	ra	2/5	Rs,A	#n,A	Rs,B	Rs,Rd	#n,B	B,A	#n,Rd	A,Pd	B,Pd	#n,Pd	A	B	Rn	11	inst,2
5	JPZ	ra	XOR	XOR	XOR	XOR	XOR	XOR	XOR	XOR	XOR	XOR	CLR	CLR	CLR	TRAP	
	ra	2/5	Rs,A	#n,A	Rs,B	Rs,Rd	#n,B	B,A	#n,Rd	A,Pd	B,Pd	#n,Pd	A	B	Rn	10	
6	JNZ	ra	BTJO	BTJO	BTJO	BTJO	BTJO	BTJO	BTJO	BTJO	BTJO	BTJO	XCHB	XCHB A /	XCHB	TRAP	IDLE
	ra	2/5	Rs,A,ra	#n,A,ra	Rs,B,ra	Rs,Rd,ra	#n,B,ra	B,A,ra	#n,Rd,ra	A,Pd,ra	B,Pd,ra	#n,Pd,ra	A	TST B	Rn	9	1/6
7	JNC	ra	BTJZ	BTJZ	BTJZ	BTJZ	BTJZ	BTJZ	BTJZ	BTJZ	BTJZ	BTJZ	SWAP	SWAP	SWAP	TRAP	MOV
	ra	2/5	Rs,A,ra	#n,A,ra	Rs,B,ra	Rs,Rd,ra	#n,B,ra	B,A,ra	#n,Rd,ra	A,Pd,ra	B,Pd,ra	#n,Pd,ra	A	B	Rn	8	#n,Pd
8	JV	ra	ADD	ADD	ADD	ADD	ADD	ADD	ADD	MOVW	MOVW	MOVW	PUSH	PUSH	PUSH	TRAP	SETC
	ra	2/5	Rs,A	#n,A	Rs,B	Rs,Rd	#n,B	B,A	#n,Rd	#16,Rd	Rs,Rd	#16[B],Rd	A	B	Rs	7	1/7
9	JL	ra	ADC	ADC	ADC	ADC	ADC	ADC	ADC	JMPL	JMPL	JMPL	POP	POP	POP	TRAP	RTS
	ra	2/5	Rs,A	#n,A	Rs,B	Rs,Rd	#n,B	B,A	#n,Rd	lab	*Rd	*lab[B]	A	B	Rd	6	1/9
A	JLE	ra	SUB	SUB	SUB	SUB	SUB	SUB	SUB	MOV	MOV	MOV	DJNZ	DJNZ	DJNZ	TRAP	RTI
	ra	2/5	Rs,A	#n,A	Rs,B	Rs,Rd	#n,B	B,A	#n,Rd	& lab,A	*Rs,A	*lab[B],A	A,ra	B,ra	Rn,ra	5	1/12
B	JHS	ra	SBB	SBB	SBB	SBB	SBB	SBB	SBB	MOV	MOV	MOV	COMPL	COMPL	COMPL	TRAP	PUSH
	ra	2/5	Rs,A	#n,A	Rs,B	Rs,Rd	#n,B	B,A	#n,Rd	A, & lab	A, *Rd	A,*lab[B]	A	B	Rn	4	ST

† All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

Table 17. TMS370 Family Opcode/Instruction Map †(Continued)

	MSN															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rd 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rn 2/6	TRAP 3 1/14	POP ST 1/8
D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rs,A 2/10	CMP *lab[B].A 3/13	RRC A 1/8	RRC B 1/8	RRC Rn 2/6	TRAP 2 1/14	LDSP 1/7
E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rd 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rn 2/6	TRAP 1 1/14	STSP 1/8
F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rd 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rn 2/6	TRAP 0 1/14	NOP 1/7

Legend:

* = Indirect addressing operand prefix
 & = Direct addressing operand prefix
 # = immediate operand
 #16 = immediate 16-bit number
 lab = 16-label
 n = immediate 8-bit number
 Pd = Peripheral register containing destination type
 Pn = Peripheral register
 Ps = Peripheral register containing source byte
 ra = Relative address
 Rd = Register containing destination type
 Rn = Register file
 Rp = Register pair
 Rpd = Destination register pair
 Rps = Source Register pair
 Rs = Register containing source byte

Second byte of two-byte instructions (F4xx):

F4	8	MOVW *n[Rn] 4/15	DIV Rn,A 3/14-63
F4	9	JMPL *n[Rn] 4/16	
F4	A	MOV *n[Rn].A 4/17	
F4	B	MOV A,*n[Rn] 4/16	
F4	C	BR *n[Rn] 4/16	
F4	D	CMP *n[Rn].A 4/18	
F4	E	CALL *n[Rn] 4/20	
F4	F	CALLR *n[Rn] 4/22	

† All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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development system support

The TMS370 family development support tools include an assembler, a C-compiler, a linker, an in-circuit emulator XDS/22, CDT and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
 - Includes extensive macro capability
 - Provides high-speed operation
 - Includes format conversion utilities for popular formats
- ANSI C Compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, Sun-3™ or Sun-4™)
 - Generate assembly code for the TMS370 that can be inspected easily
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables direct reference the TMS370's port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (Compact Development Tool) real-time in-circuit emulation
 - Base (Part Number EDSCDT370 – for PC, requires cable)
 - Cable for 28-pin DIP (Part No. EDSTRG28DIL)
 - Cable for 28-pin PLCC (Part No. EDSTRG28PLCC)
 - EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Includes compatibility to upload/download program and data memory
 - Execute programs and software routines
 - Includes 1 024 samples trace buffer
 - Includes single-step executable instructions
 - Uses software breakpoints to halt program execution at selected address
- XDS/22 in-circuit emulator
 - Base (Part Number TMDS3762210 for PC, requires cable)
 - Cable for 28-pin DIP/PLCC (Part No. TMDS3788828)
 - Contains all the features of the CDT370 described previously but does not have the capability to program the data EEPROM and program EPROM
 - Contains sophisticated breakpoint trace and timing hardware that provides up to 2047 qualified trace samples with symbolic disassembly
 - Allows qualification of breakpoints by address and/or data on any type of memory acquisition. Up to four levels of events can be combined to cause a breakpoint

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development system support (continued)

- Provides timers for analyzing total and average time in routines
- Contains an eight-line logic probe for adding visibility of external signals to the breakpoint qualifier and to trace display
- Microcontroller programmer
 - Base (Part No. TMDS3760500A – for PC, requires programmer head)
 - Single unit head for 28-pin PLCC (Part No. TMDS3780510A)
 - Single unit head for 28-pin DIP (Part No. TMDS3780511A)
 - PC-based, window/function-key-oriented user interface for ease of use and rapid learning environment
- Design kit (Part No. TMDS3770110 – for PC)
 - Includes TMS370 Application Board and TMS370 Assembler diskette and documentation
 - Supports quick evaluation of TMS370 functionality
 - Capability to upload and download code
 - Capability to execute programs and software routines, and to single-step executable instructions
 - Software breakpoints to halt program execution at selected addresses
 - Wire-wrap prototype area
 - Reverse assembler
- Starter Kit (Part No. TMDX37000 – for PC)
 - Includes TMS370 Assembler diskette and documentation
 - Includes TMS370 Simulator
 - Includes programming adapter board and programming software
 - Does not include (to be supplied by the user)
 - + 5 V power supply
 - ZIF sockets
 - Nine-pin RS232 cable

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device numbering conventions

Figure 13 illustrates the numbering and symbol nomenclature for the TMS370Cx1x family.

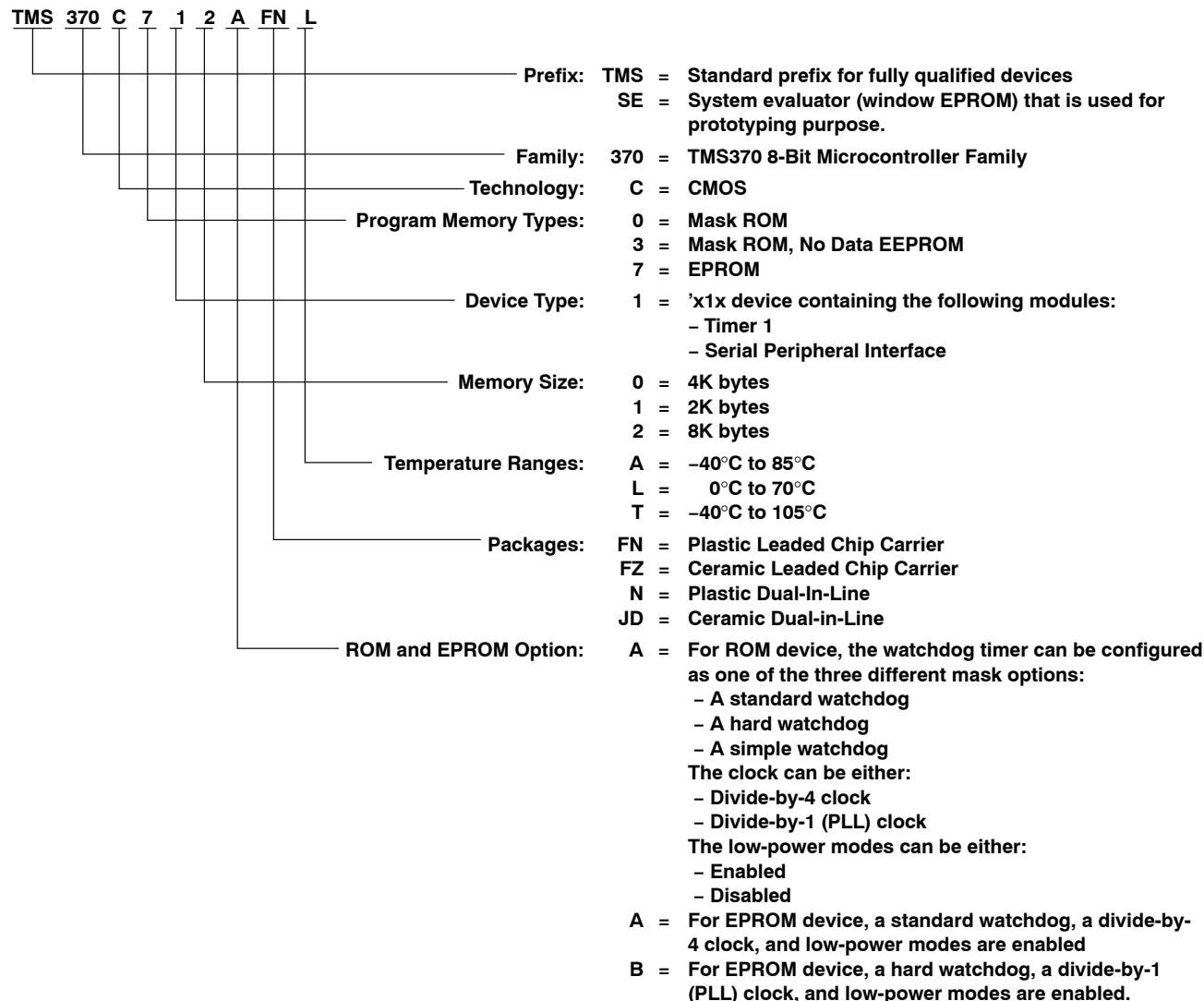


Figure 13. TMS370Cx1x Family Nomenclature

device part numbers

Table 18 provides all of the 'x1x devices available. The device part number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog timer options desired. Each device can have only one of the three possible watchdog timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 18. Device Part Numbers

DEVICES PART NUMBERS FOR 28 PINS (LCC)	DEVICES PART NUMBERS FOR 28 PINS (DIP)
TMS370C010AFNA TMS370C010AFNL TMS370C010AFNT	TMS370C010ANA TMS370C010ANL TMS370C010ANT
TMS370C012AFNA TMS370C012AFNL TMS370C012AFNT	TMS370C012ANA TMS370C012ANL TMS370C012ANT
TMS370C310AFNA TMS370C310AFNL TMS370C310AFNT	TMS370C310ANA TMS370C310ANL TMS370C310ANT
TMS370C311AFNA TMS370C311AFNL TMS370C311AFNT	TMS370C311ANA TMS370C311ANL TMS370C311ANT
TMS370C312AFNA TMS370C312AFNL TMS370C312AFNT	TMS370C312ANA TMS370C312ANL TMS370C312ANT
TMS370C712AFNT TMS370C712BFNT	TMS370C712ANT TMS370C712BNT
SE370C712AFZT [†] SE370C712BFZT [†]	SE370C712AJDT [†] SE370C712BJDT [†]

[†] System evaluators are for use in prototype environment and their reliability has not been characterized.

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new code release form

Figure 14 shows a sample of the new code release form.

NEW CODE RELEASE FORM TEXAS INSTRUMENTS TMS370 MICROCONTROLLER PRODUCTS				DATE: _____																
To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information: 1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media) 2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.																				
Company Name: _____ Street Address: _____ Street Address: _____ City: _____ State _____ Zip _____		Contact Mr./Ms.: _____ Phone: (_____) _____ Ext.: _____ Customer Purchase Order Number: _____ Customer Print Number *Yes: _____ # _____ No: _____ (Std. spec to be followed) *If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.																		
Customer Part Number: _____ Customer Application: _____																				
TMS370 Device: _____ TI Customer ROM Number: _____ (provided by Texas Instruments)																				
OSCILLATOR FREQUENCY <table border="1" style="width: 100%; border-collapse: collapse;"><thead><tr><th></th><th style="text-align: center;">MIN</th><th style="text-align: center;">TYP</th><th style="text-align: center;">MAX</th></tr></thead><tbody><tr><td>☐ External Drive (CLKIN)</td><td>_____</td><td>_____</td><td>_____</td></tr><tr><td>☐ Crystal</td><td>_____</td><td>_____</td><td>_____</td></tr><tr><td>☐ Ceramic Resonator</td><td>_____</td><td>_____</td><td>_____</td></tr></tbody></table> ☐ Supply Voltage MIN: _____ MAX: _____ (std range: 4.5V to 5.5V)						MIN	TYP	MAX	☐ External Drive (CLKIN)	_____	_____	_____	☐ Crystal	_____	_____	_____	☐ Ceramic Resonator	_____	_____	_____
	MIN	TYP	MAX																	
☐ External Drive (CLKIN)	_____	_____	_____																	
☐ Crystal	_____	_____	_____																	
☐ Ceramic Resonator	_____	_____	_____																	
CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS <table style="width: 100%;"><tr><td>Low Power Modes</td><td>Watchdog counter</td><td>Clock Type</td></tr><tr><td>☐ Enabled</td><td>☐ Standard</td><td>☐ Standard (/4)</td></tr><tr><td>☐ Disabled</td><td>☐ Hard Enabled</td><td>☐ PLL (/1)</td></tr><tr><td></td><td>☐ Simple Counter</td><td></td></tr></table> NOTE: Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the <i>TMS370 Family User's Guide</i> (literature number SPNU127) or the <i>TMS370 Family Data Manual</i> (literature number SPNS014B).					Low Power Modes	Watchdog counter	Clock Type	☐ Enabled	☐ Standard	☐ Standard (/4)	☐ Disabled	☐ Hard Enabled	☐ PLL (/1)		☐ Simple Counter					
Low Power Modes	Watchdog counter	Clock Type																		
☐ Enabled	☐ Standard	☐ Standard (/4)																		
☐ Disabled	☐ Hard Enabled	☐ PLL (/1)																		
	☐ Simple Counter																			
TEMPERATURE RANGE <table style="width: 100%;"><tr><td>☐ 'L': 0° to 70°C (standard)</td></tr><tr><td>☐ 'A': -40° to 85°C</td></tr><tr><td>☐ 'T': -40° to 105°C</td></tr></table>					☐ 'L': 0° to 70°C (standard)	☐ 'A': -40° to 85°C	☐ 'T': -40° to 105°C													
☐ 'L': 0° to 70°C (standard)																				
☐ 'A': -40° to 85°C																				
☐ 'T': -40° to 105°C																				
PACKAGE TYPE <table style="width: 100%;"><tr><td>☐ 'N' 28-pin PDIP</td><td>☐ "FN" 44-pin PLCC</td></tr><tr><td>☐ "FN" 28-pin PLCC</td><td>☐ "FN" 68-pin PLCC</td></tr><tr><td>☐ "N" 40-pin PDIP</td><td>☐ "NM" 64-pin PSDIP</td></tr><tr><td colspan="2">☐ "NJ" 40-pin PSDIP (formerly known as N2)</td></tr></table>					☐ 'N' 28-pin PDIP	☐ "FN" 44-pin PLCC	☐ "FN" 28-pin PLCC	☐ "FN" 68-pin PLCC	☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP	☐ "NJ" 40-pin PSDIP (formerly known as N2)									
☐ 'N' 28-pin PDIP	☐ "FN" 44-pin PLCC																			
☐ "FN" 28-pin PLCC	☐ "FN" 68-pin PLCC																			
☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP																			
☐ "NJ" 40-pin PSDIP (formerly known as N2)																				
SYMBOLIZATION <table style="width: 100%;"><tr><td>☐ TI standard symbolization</td></tr><tr><td>☐ TI standard w/customer part number</td></tr><tr><td>☐ Customer symbolization (per attached spec, subject to approval)</td></tr></table>					☐ TI standard symbolization	☐ TI standard w/customer part number	☐ Customer symbolization (per attached spec, subject to approval)													
☐ TI standard symbolization																				
☐ TI standard w/customer part number																				
☐ Customer symbolization (per attached spec, subject to approval)																				
BUS EXPANSION <table style="width: 100%;"><tr><td>☐ YES</td><td>☐ NO</td></tr></table>					☐ YES	☐ NO														
☐ YES	☐ NO																			
NON-STANDARD SPECIFICATIONS: ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.																				
RELEASE AUTHORIZATION: This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cycletime commences when this document is signed off and the verification code is approved by the customer.																				
1. Customer: _____ Date: _____		2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____																		

Figure 14. Sample New Code Release Form



Table 19 is a collection of all the peripheral file frames used in the 'Cx1x (provided for a quick reference).

Table 19. Peripheral File Frame Compilation

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	System Configuration Registers								
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTO WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT / STANDBY	PWRDWN / IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D P01E P01F	Reserved								
	Digital Port Control Registers								
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0) [†]					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR
	SPI Module Control Register Memory Map								
P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/SLAVE	TALK	SPI INT ENA	SPICTL
P032 to P036	Reserved								
P037	RCVD7	RCVD6	RCVD5	RCVD4	RCVD3	RCVD2	RCVD1	RCVD0	SPIBUF
P038	Reserved								

[†] D3 as SYSCLK, set port D control register 2 = 08h.

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Table 19. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P039	SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0	SPIDAT
P03A to P03C	Reserved								
P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
P03F	SPI STEST	SPI RRIORITY	SPI ESPEN	—	—	—	—	—	SPIPRI
Timer1 Module Register Memory Map									
Modes: Dual-Compare and Capture/Compare									
P040	Bit 15	T1Counter MSbyte						Bit 8	T1CNTR
P041	Bit 7	T1 Counter LSbyte						Bit 0	
P042	Bit 15	Compare Register MSbyte						Bit 8	T1C
P043	Bit 7	Compare Register LSbyte						Bit 0	
P044	Bit 15	Capture/Compare Register MSbyte						Bit 8	T1CC
P045	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P046	Bit 15	Watchdog Counter MSbyte						Bit 8	WDCNTR
P047	Bit 7	Watchdog Counter LSbyte						Bit 0	
P048	Bit 7	Watchdog Reset Key						Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE=0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC}) (see Note 2)	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	500 mW
Operating free-air temperature range, T_A : L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS} .

2. Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 3)		3		5.5	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET	2		V_{CC}	V
		XTAL2/CLKIN	0.8 V_{CC}		V_{CC}	
		RESET	0.7 V_{CC}		V_{CC}	
V_{MC}	MC (mode control) voltage	EEPROM write protect override (WPO)	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	
		Microcomputer	V_{SS}		0.3	
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	
		T version	–40		105	

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS} .

3. RESET must be externally activated when V_{CC} or SYSCLK is not within the recommended operating range.

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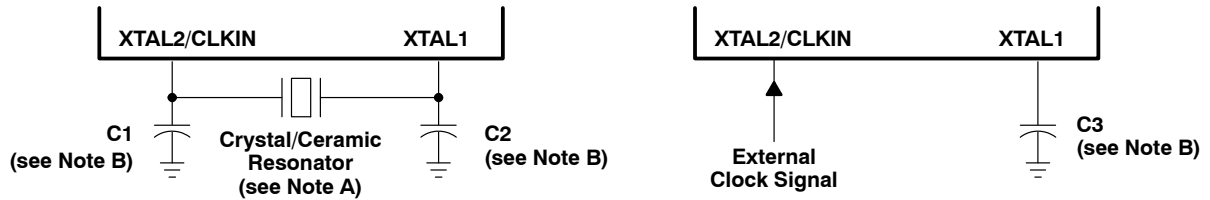
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OL}	Low-level output voltage	I _{OL} = 1.4 mA			0.4	V
V _{OH}	High-level output voltage	I _{OH} = -50 µA	0.9 V _{CC}			V
		I _{OH} = -2 mA	2.4			
I _I	Input current	0 V ≤ V _I ≤ 0.3 V			10	µA
		0.3 V < V _I ≤ 13 V			650	
		See Note 4 12 V ≤ V _I ≤ 13 V			50	mA
	I/O pins	0 V ≤ V _I ≤ V _{CC}			± 10	µA
I _{OL}	Low-level output current	V _{OL} = 0.4 V	1.4			mA
I _{OH}	High-level output current	V _{OH} = 0.9 V _{CC}	- 50			µA
		V _{OH} = 2.4 V	- 2			mA
I _{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 7)	See Notes 5 and 6 SYSCLK = 5 MHz		20	36	mA
		See Notes 5 and 6 SYSCLK = 3 MHz		13	25	
		See Notes 5 and 6 SYSCLK = 0.5 MHz		5	11	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 8)	See Notes 5 and 6 SYSCLK = 5 MHz		10	17	mA
		See Notes 5 and 6 SYSCLK = 3 MHz		6.5	11	
		See Notes 5 and 6 SYSCLK = 0.5 MHz		2	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 9)	See Notes 5 and 6 SYSCLK = 3 MHz		4.5	8.6	mA
		See Notes 5 and 6 SYSCLK = 0.5 MHz		1.5	3.0	
	Supply current (HALT mode)	See Note 5 XTAL2/CLKIN < 0.2 V		1	30	µA

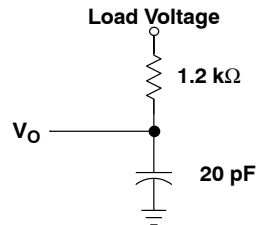
- NOTES:
- Input current I_{pp} is a maximum of 50 mA only when you are programming EPROM.
 - Single chip mode, ports configured as inputs or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} - 0.2V.
 - XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = 0.01 mA x (total load capacitance + crystal capacitance in pF).
 - Maximum operating current = 5.6 (SYSCLK) + 8 mA.
 - Maximum standby current = 3 (SYSCLK) + 2 mA. (OSC POWER bit = 0).
 - Maximum standby current = 2.24 (SYSCLK) + 1.9 mA. (OSC POWER bit = 1, only valid up to 3 MHz SYSCLK).





NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
 B. The values of C1 and C2 are typically 15 pF and the value of C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 15. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4 \text{ V}$; Load Voltage = 0 V

Case 2: $V_O = V_{OL} = 0.4 \text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 16. Typical Output Load Circuit (See Note A)

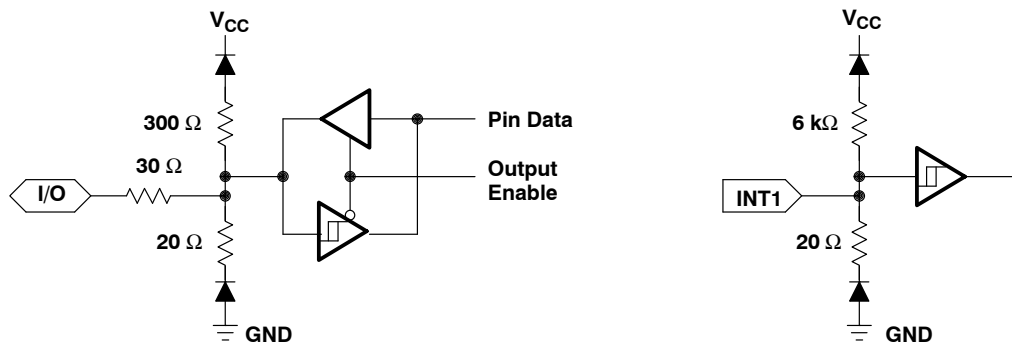


Figure 17. Typical Buffer Circuitry

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PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

AR	Array	SC	SYSCLK
B	Byte	SIMO	SPISIMO
CI	XTAL2/CLKIN	SOMI	SPISOMI
M	Master mode	SPC	SPICLK
S	Slave mode		

Lowercase subscripts and their meanings are:

c	cycle time (period)	su	setup time
d	delay time	v	valid time
f	fall time	w	pulse duration (width)
r	rise time		

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid

All timings are measured between high and low measurement points as indicated in Figure 18 and Figure 19.

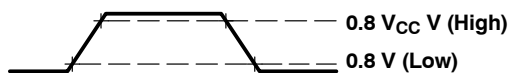


Figure 18. XTAL2/CLKIN Measurement Points

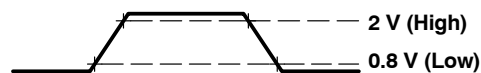


Figure 19. General Measurement Points

external clocking requirements for clock divided by 4 (see Note 10 and Figure 20)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 11)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN Crystal operating frequency	2	20	MHz
	SYSCLK Internal system clock operating frequency [†]	0.5	5	MHz

[†] SYSCLK = CLKIN/4

NOTES: 10. For V_{IL} and V_{IH} , refer to recommended operating conditions.

11. This pulse may be either a high pulse which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

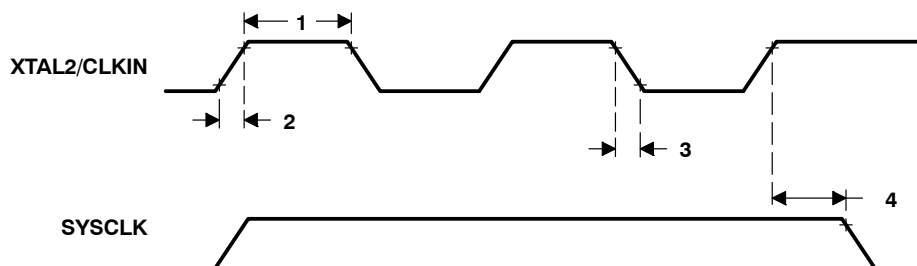


Figure 20. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL) (see Note 10 and Figure 21)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 11)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN Crystal operating frequency	2	5	MHz
	SYSCLK Internal system clock operating frequency [‡]	2	5	MHz

[‡] SYSCLK = CLKIN/1

NOTES: 10. For V_{IL} and V_{IH} , refer to recommended operating conditions.

11. This pulse can be either a high pulse which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

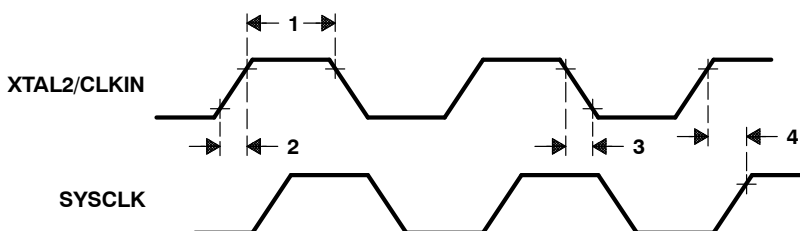


Figure 21. External Clock Timing for Divide-by-1

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switching characteristics and timing requirements (see Note 12 and Figure 22)

NO.	PARAMETER		MIN	MAX	UNIT
5	t_c	Cycle time, SYSCLK	200	2000	ns
			200	500	
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low	$0.5 t_c - 20$	$0.5 t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high	$0.5 t_c$	$0.5 t_c + 20$	ns

NOTE 12: t_c = system-clock cycle time = $1 / \text{SYSCLK}$

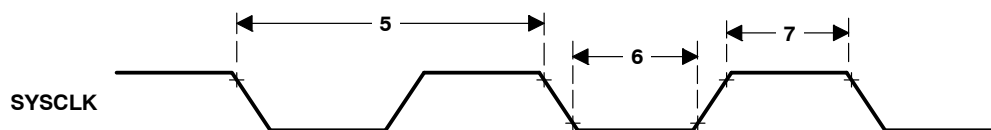


Figure 22. SYSCLK Timing

general purpose output signal switching time requirements (see Figure 23)

	MIN	NOM	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns

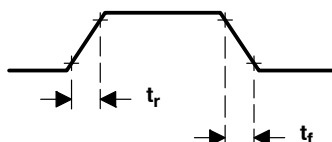


Figure 23. Signal Switching Timing

recommended EEPROM timing requirements for programming

	MIN	MAX	UNIT
$t_{w(PGM)B}$ Pulse duration, programming signal to ensure valid data is stored (byte mode)	10		ms
$t_{w(PGM)AR}$ Pulse duration, programming signal to ensure valid data is stored (array mode)	20		ms

recommended EPROM operating conditions for programming

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5.5	6	V
V_{PP} Supply voltage at MC pin	13	13.2	13.5	V
I_{PP} Supply current at MC pin during programming ($V_{PP} = 13 \text{ V}$)		30	50	mA
SYSCLK System clock	Divide by 4	0.5	5	MHz
	Divide by 1	2	5	

recommended EPROM timing requirements for programming

	MIN	NOM	MAX	UNIT
$t_{w(EPGM)}$ Pulse duration, programming signal (see Note 13)	0.40	0.50	3	ms

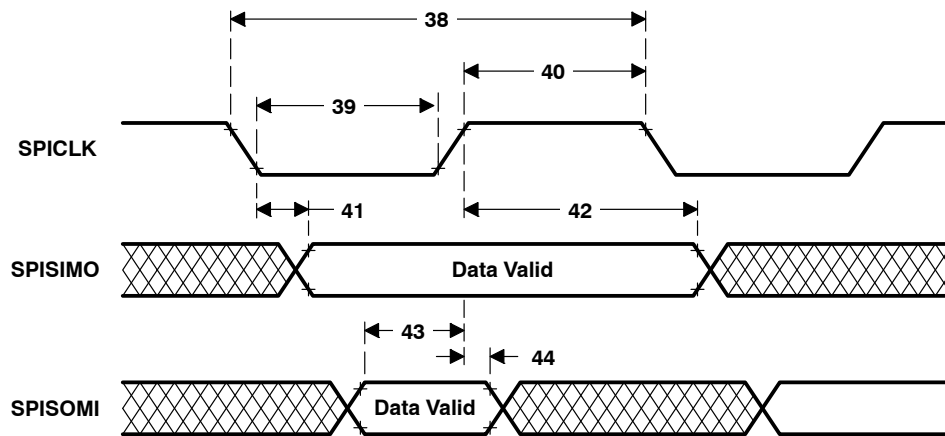
NOTE 13: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.



SPI master mode external timing characteristics and requirements (see Note 12 and Figure 24)

NO.		MIN	MAX	UNIT
38	$t_{c(SPC)M}$ Cycle time, SPICLK	$2t_c$	$256t_c$	ns
39	$t_{w(SPCL)M}$ Pulse duration, SPICLK low	$t_c - 45$	$0.5t_{c(SPC)} + 45$	ns
40	$t_{w(SPCH)M}$ Pulse duration, SPICLK high	$t_c - 55$	$0.5t_{c(SPC)} + 45$	ns
41	$t_{d(SPCL-SIMOV)M}$ Delay time, SPISIMO valid after SPICLK low (polarity = 1)	- 65	50	ns
42	$t_{v(SPCH-SIMO)M}$ Valid time, SPISIMO data valid after SPICLK high (polarity = 1)	$t_{w(SPCH)} - 50$		ns
43	$t_{su(SOMI-SPCH)M}$ Setup time, SPISOMI to SPICLK high (polarity = 1)	$0.25 t_c + 150$		ns
44	$t_{v(SPCH-SOMI)M}$ Valid time, SPISOMI data valid after SPICLK high (polarity = 1)	0		ns

NOTE 12: t_c = system-clock cycle time = $1/\text{SYSCLK}$



NOTE A: The diagram is for polarity = 1. SPICLK is inverted when polarity = 0.

Figure 24. SPI Master External Timing

TMS370Cx1x

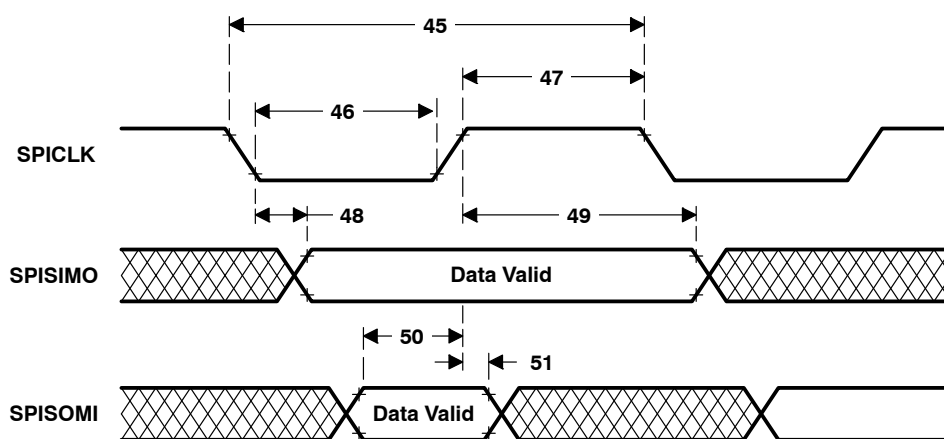
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SPI slave mode external timing characteristics and requirements (see Note 12 and Figure 25)

NO.		MIN	MAX	UNIT
45	$t_{c(SPC)}S$ Cycle time, SPICLK	$8t_c$		ns
46	$t_{w(SPCL)}S$ Pulse duration, SPICLK low	$4t_c - 45$	$0.5t_{c(SPC)}S + 45$	ns
47	$t_{w(SPCH)}S$ Pulse duration, SPICLK high	$4t_c - 45$	$0.5t_{c(SPC)}S + 45$	ns
48	$t_{d(SPCL-SOMI)}S$ Delay time, SPISOMI valid after SPICLK low (polarity = 1)		$3.25t_c + 130$	ns
49	$t_{v(SPCH-SOMI)}S$ Valid time, SPISOMI data valid after SPICLK high (polarity = 1)	$t_{w(SPCH)}S$		ns
50	$t_{su(SIMO-SPCH)}S$ Setup time, SPISIMO to SPICLK high (polarity = 1)	0		ns
51	$t_{v(SPCH-SIMO)}S$ Valid time, SPISIMO data after SPICLK high (polarity = 1)	$3t_c + 100$		ns

NOTE 12: t_c = system-clock cycle time = 1 / SYSCLK



NOTE A: The diagram is for polarity = 1. SPICLK is inverted when polarity = 0.

Figure 25. SPI Slave External Timing

Table 20 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

Table 20. TMS370Cx1x Family Package Type and Mechanical Cross-Reference

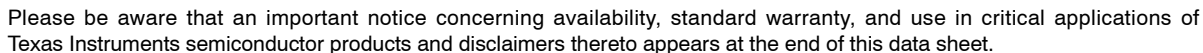
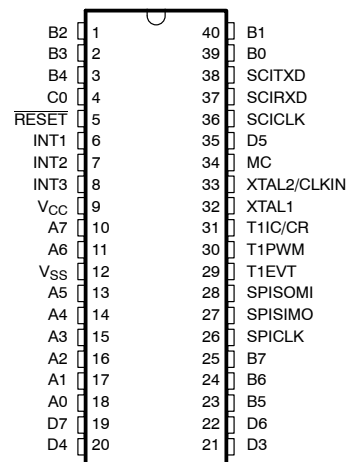
PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 28 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C010AFNA TMS370C010AFNL TMS370C010AFNT TMS370C012AFNA TMS370C012AFNL TMS370C012AFNT TMS370C310AFNA TMS370C310AFNL TMS370C310AFNT TMS370C311AFNA TMS370C311AFNL TMS370C311AFNT TMS370C312AFNA TMS370C312AFNL TMS370C312AFNT TMS370C712AFNT TMS370C712BFNT
FZ – 28 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C712AFZT SE370C712BFZT
JD – 28 pin (100-mil pin spacing)	CERAMIC DUAL-IN-LINE PACKAGE (CDIP)	JD(R-CDIP-T**) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE	SE370C712AJDT SE370C712BJDT
N – 28 pin (100-mil pin spacing)	PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	N(R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE	TMS370C010ANA TMS370C010ANL TMS370C010ANT TMS370C012ANA TMS370C012ANL TMS370C012ANT TMS370C310ANA TMS370C310ANL TMS370C310ANT TMS370C311ANA TMS370C311ANL TMS370C311ANT TMS370C312ANA TMS370C312ANL TMS370C312ANT TMS370C712ANT TMS370C712BNT

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- **CMOS/TTL Compatible I/O Pins/Packages**
 - All Peripheral Function Pins Software Configurable for Digital I/O
 - 33 Bidirectional Pins, 1 Input Pin
 - 44-Pin Plastic and Ceramic Leaded Chip Carrier (LCC) Packages
 - 40-Pin Plastic and Ceramic Dual-In-Line (DIP) Packages
- **Workstation/PC-Based Development System**
 - C Compiler and C Source Debugger
 - Real-Time In-Circuit Emulation
 - Extensive Breakpoint/Trace Capability
 - Multi-Window User Interface
 - Microcontroller Programmer



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Pin Descriptions

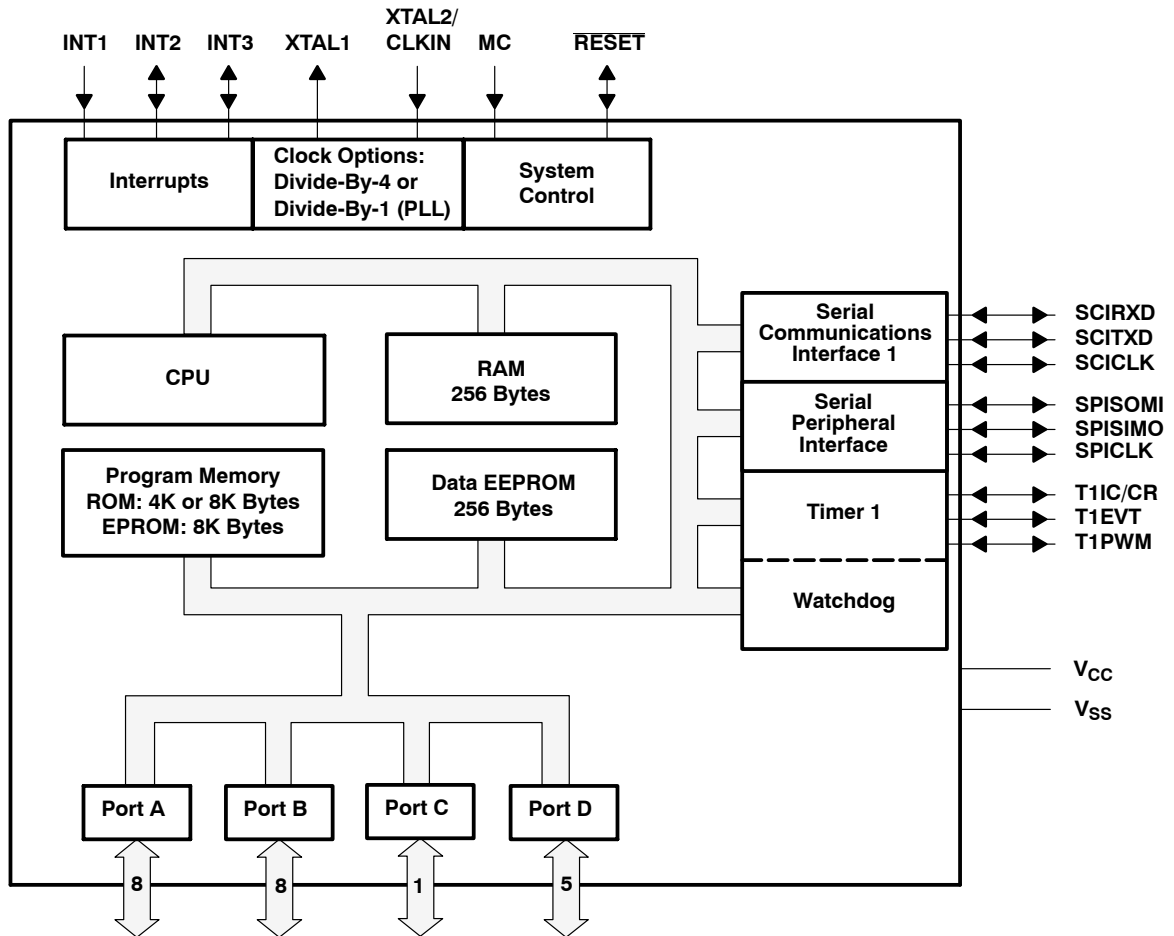
PIN			TYPE†	DESCRIPTION
NAME	DIP (40)	PLCC (44)		
A0 A1 A2 A3 A4 A5 A6 A7	18 17 16 15 14 13 11 10	20 19 18 17 16 15 13 12	I/O	Port A pins are general-purpose bidirectional I/O ports.
B0 B1 B2 B3 B4 B5 B6 B7	39 40 1 2 3 23 24 25	44 1 2 3 4 26 27 28	I/O	Port B pins are general-purpose bidirectional I/O ports.
C0	4	5	I/O	Port C pin is a general-purpose bidirectional I/O port.
D3 D4 D5 D6 D7	21 20 35 22 19	23 22 40 24 21	I/O	Port D pins are general-purpose bidirectional I/O ports. D3 is also configurable as SYSCLK.
INT1 INT2 INT3	6 7 8	7 8 9	I I/O I/O	External interrupt (non-maskable or maskable) general-purpose input pin External maskable interrupt input/general-purpose bidirectional pin External maskable interrupt input/general-purpose bidirectional pin
T1IC/CR T1PWM T1EVT	31 30 29	36 35 34	I/O	Timer 1 input-capture/counter-reset input pin/general-purpose bidirectional pin Timer 1 pulse width modulation output pin/general-purpose bidirectional pin Timer 1 external event-input pin/general-purpose bidirectional pin
SPISOMI SPISIMO SPICLK	28 27 26	32 31 30	I/O	SPI slave output pin, master input pin/general-purpose bidirectional pin SPI slave input pin, master output pin/general-purpose bidirectional pin SPI bidirectional serial clock pin/general-purpose bidirectional pin
SCITXD SCIRXD SCICLK	38 37 36	43 42 41	I/O	SCI transmit data output pin/general-purpose bidirectional pin‡ SCI receive data input pin/general-purpose bidirectional pin SCI bidirectional serial clock pin/general-purpose bidirectional pin
RESET	5	6	I/O	System reset bidirectional pin; as input, RESET initializes microcontroller; as open-drain output, RESET indicates an internal failure was detected by the watchdog or oscillator fault circuit.
MC	34	39	I	Mode control-input pin. MC enables the EEPROM write-protection override (WPO) mode and EPROM V _{PP} .
XTAL2/CLKIN XTAL1	33 32	38 37	I O	Internal oscillator crystal input/external clock source input Internal oscillator output for crystal
V _{CC}	9	10		Positive supply voltage
V _{SS}	12	14		Ground reference
NC	– – – –	11 25 29 33		No connections

† I = input, O = output

‡ The three-pin configuration SCI is referred to as SCI1.



functional block diagram



TMS370Cx2x 8-BIT MICROCONTROLLER

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description

The TMS370C020A, TMS370C022A, TMS370C320A, TMS370C322A, TMS370C722, and SE370C722 devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx2x refers to these devices. The TMS370 family provides cost-effective real-time system control through integration of advanced peripheral modules and various function on-chip memory configurations.

The TMS370Cx2x family uses high-performance silicon-gate CMOS EPROM and EEPROM technology. Low operating power, wide operating temperature range, and noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx2x devices attractive in system designs for automotive electronics, industrial motor, computer peripheral controls, telecommunications, and consumer applications.

All TMS370Cx2x devices contain the following on-chip peripheral modules:

- Serial peripheral interface (SPI)
- Serial communications interface 1 (SCI1)
- One 24-bit general-purpose watchdog (WD) timer
- One 16-bit general-purpose timer with an 8-bit prescaler

Table 1 lists memory configurations of the TMS370Cx2x devices.

Table 1. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		PIN/PACKAGES
	ROM	EPROM	RAM	EEPROM	
TMS370C020A	4K	—	256	256	44/FN-PLCC 40/N-DIP 40/NJ [‡] -PSDIP
TMS370C022A	8K	—	256	256	44/FN-PLCC 40/N-DIP 40/NJ [‡] -PSDIP
TMS370C320A	4K	—	256	—	44/FN-PLCC 40/N-DIP 40/NJ [‡] -PSDIP
TMS370C322A	8K	—	256	—	44/FN-PLCC 40/N-DIP 40/NJ [‡] -PSDIP
TMS370C722	—	8K	256	256	44/FN-PLCC 40/N-DIP 40/NJ [‡] -PSDIP
SE370C722 [†]	—	8K	256	256	44/FZ-CLCC 40/JD-CDIP 40/JC-CSDIP

[†] System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.

[‡] The NJ designator for the 40-pin plastic shrink DIP package was formerly known as N2. The mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

The suffix letter A appended to the device names in Table 1 indicates the configuration of the devices. ROM or EPROM devices have different configurations as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.



description (continued)

Table 2. Suffix Letter Configuration

DEVICE†	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM without A	Standard	Divide-by-4 (Standard oscillator)	Enabled
ROM A	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

† Refer to the “device numbering conventions” section for device nomenclature and the “device part numbers” section for ordering.

The 4K bytes and 8K bytes of mask-programmable ROM in the TMS370C020, TMS370C022, TMS370C320, and TMS370C322 are replaced in the TMS370C722 and SE370C722 with 8K bytes of EPROM. All other available memory and on-chip peripherals are identical, except there are no data EEPROMs on the TMS370C320 and TMS370C322 devices. OTP (TMS370C722) devices and the reprogrammable device (SE370C722) are available.

TMS370C722 (OTP) devices are in plastic packages. This microcontroller is effective to use for immediate production updates for other members of the TMS370Cx2x family or for low-volume production runs when the mask charge or cycle time for the low-cost mask ROM devices is not practical.

The SE370C722 has a windowed ceramic package to allow reprogramming of the program EPROM memory during the prototyping phase of design. These SE370C722 devices allow quick updates to breadboards and prototype systems while creating multiple initial designs.

The TMS370Cx2x family provides two low-power modes (STANDBY and HALT) for applications where low power consumption is critical. Both modes stop all central processing unit (CPU) activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator, the general-purpose timer, and the SCI receiver start-bit detection remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx2x features advanced register-to-register architecture that allows arithmetic and logical operations without requiring an accumulator (e.g., ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx2x family is fully instruction-set-compatible, providing easy transition between members of the TMS370 8-bit microcontroller family.

The SPI provides a convenient method of serial interaction for high speed communications between simpler shift-register type devices, such as display drivers, analog-to-digital (A/D) converter, PLL, I/O expansion, or other microcontrollers in the system.

The TMS370Cx2x devices have two operational modes of serial communications provided by the SCI1 module. The SCI1 allows standard RS-232-C communications with other common data transmission equipment.

The TMS370Cx2x family provides the system designer with an economical, efficient solution to real-time control applications. The TMS370 family extended development system (XDS™) and compact development tool (CDT™) meet the challenge of efficiently developing the software and hardware required to design the TMS370Cx2x into complex applications. The application source code can be written in assembly and C language, and the output code can be generated by the linker. The TMS370 family XDS development tool communicates through a standard RS-232-C interface with a personal computer. This allows the use of the personal computer editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes ease-of-use through extensive menus and screen windowing so that a system designer can begin developing software with minimal training. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as a reduced time-to-market cycle.

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central processing unit (CPU)

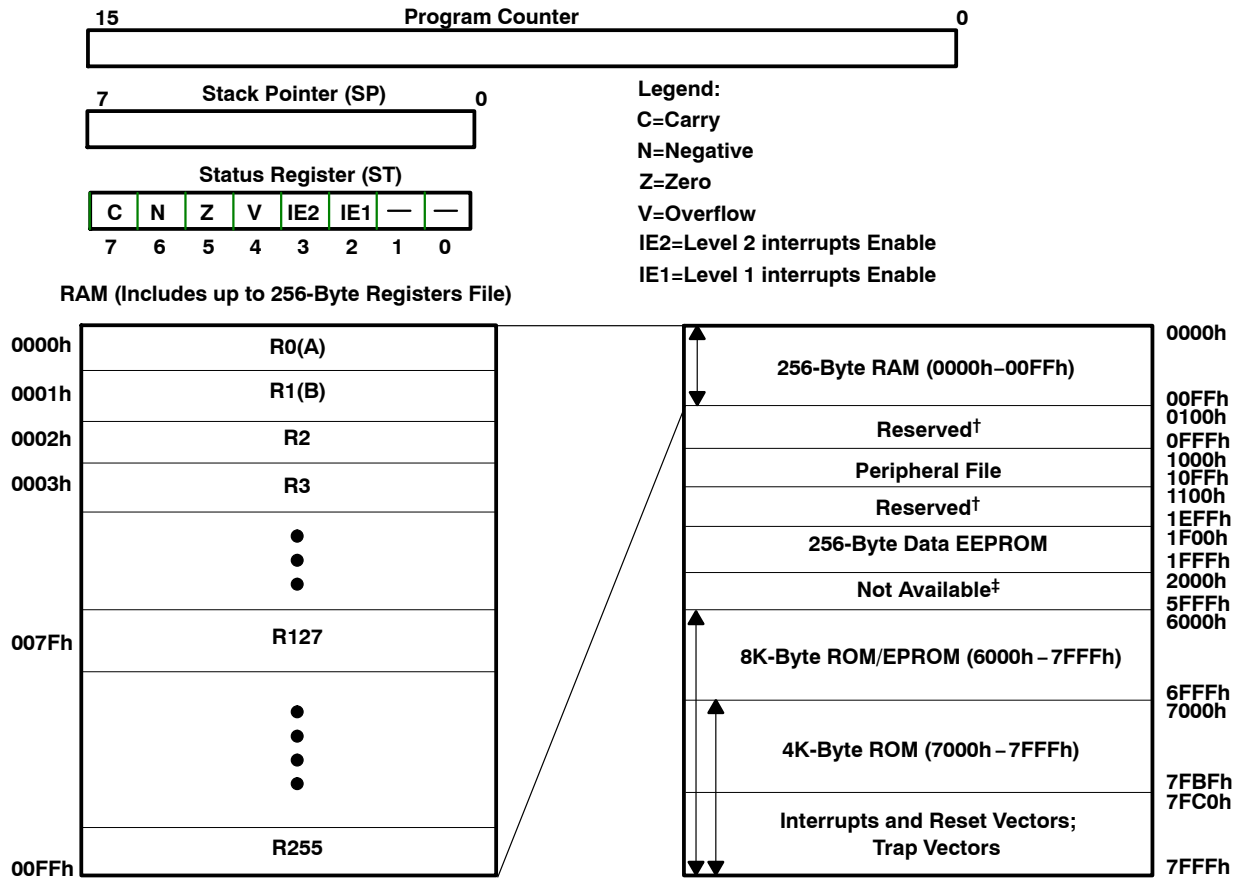
The TMS370Cx2x device uses the high-performance 8-bit TMS370 CPU module. The 'x2x uses an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'x2x instruction map is shown in Table 17 in the instruction set overview section.

The '370Cx2x CPU architecture provides the following components:

- CPU registers:
 - A stack pointer that points to the last entry in the memory stack
 - A status register that monitors the operation of the instructions and contains the global interrupt-enable bits
 - A program counter that points to the memory location of the next instruction to be executed
- Memory blocks:
 - 256-byte general-purpose RAM that can be used for data memory storage, program instructions, general purpose register, or the stack
 - A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM/EPROM programming control
 - 256-byte EEPROM module, that provides in-circuit programmability and data retention in power-off conditions
 - 4K- or 8K-byte ROM or 8K-byte EPROM

Figure 1 illustrates the CPU registers and memory blocks.

central processing unit (CPU) (continued)



† Reserved means the address space is reserved for future expansion.

‡ Not available means the address space is not accessible.

Figure 1. Programmer's Model

stack pointer (SP)

The SP is an 8-bit CPU register. Stack operates as a last-in, first-out, read/write memory. Typically the stack is used to store the return address on subroutine calls as well as the status register contents during interrupt sequences.

The SP points to the last entry or top of the stack. The SP is incremented automatically before data is pushed onto the stack and decremented after data is popped from the stack. The stack can be placed anywhere in the on-chip RAM.

status register (ST)

The ST monitors the operation of the instructions and contains the global interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits.

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional-jump instructions) use the status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

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central processing unit (CPU) (continued)

The ST, status-bit notation, and status-bit definitions are shown in Table 3.

Table 3. Status Registers

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most significant byte (MSbyte) and least significant byte (LSbyte) of a 16-bit address.

During reset, the contents of the reset vector (7FFEh, 7FFFh) are loaded into the PC. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 6000h as the contents of the reset vector.

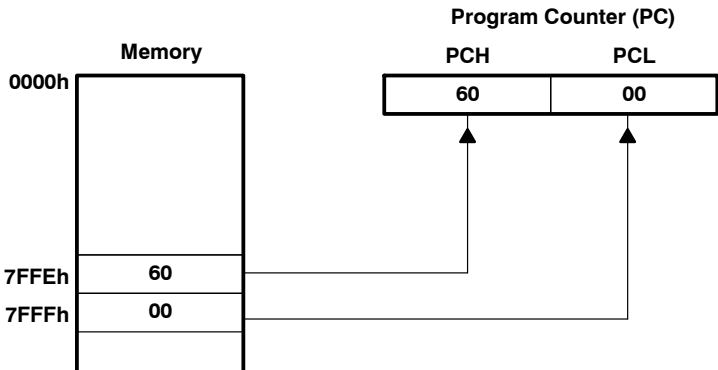


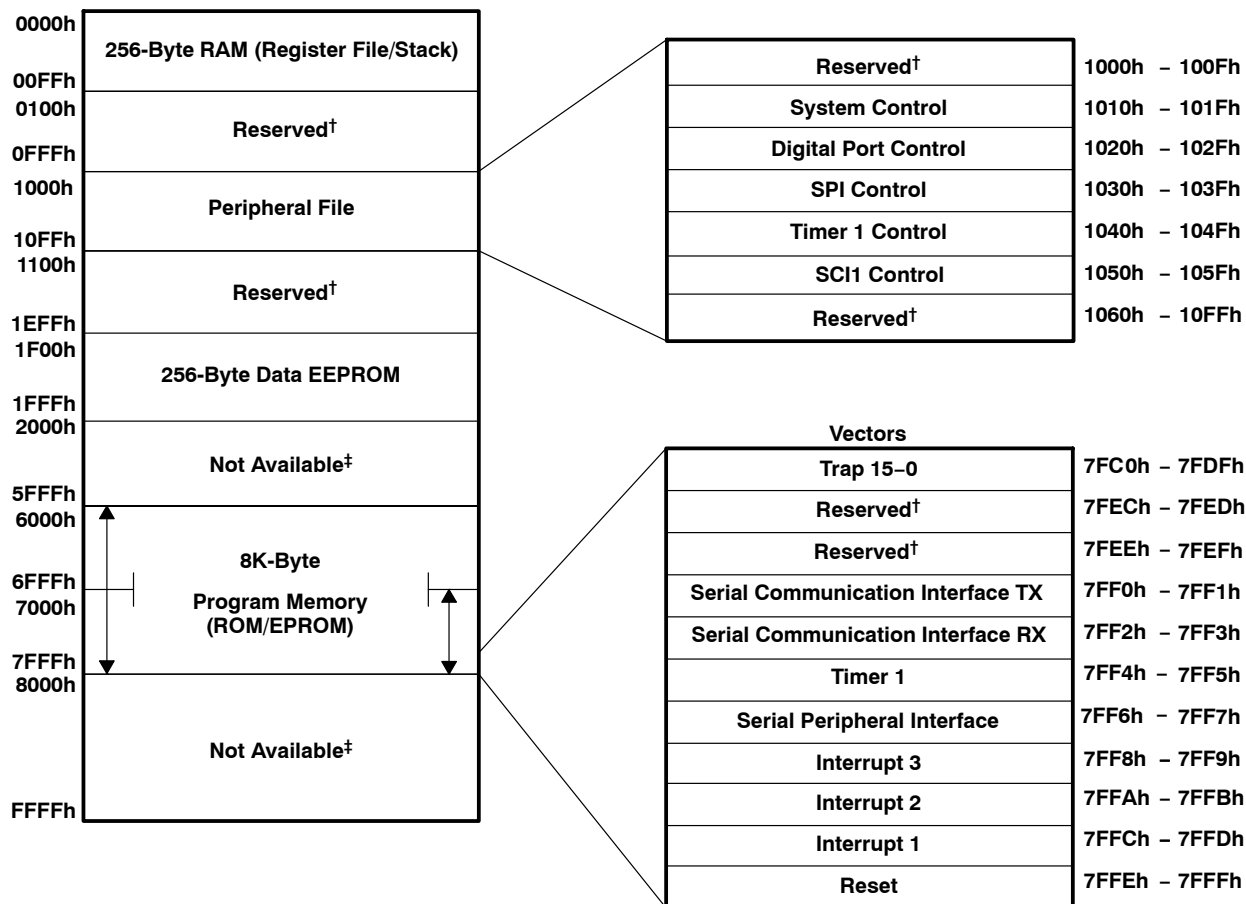
Figure 2. Program Counter After Reset

memory map

The TMS370Cx2x architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. As shown in Figure 3, the TMS370Cx2x provides memory-mapped RAM, ROM, EPROM, data EEPROM, I/O pins, peripheral functions, and system-interrupt vectors.

The peripheral file contains all I/O port control, peripheral status and control, EEPROM, EPROM, and system-wide control functions. The peripheral file is located between 1010h to 105Fh and is divided logically into five peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed.

memory map (continued)



† Reserved means the address space is reserved for future expansion.

‡ Not available means the address space is not accessible.

Figure 3. TMS370Cx2x Memory Map

RAM/register file (RF)

Locations within the RAM address space can serve as the RF, general-purpose read/write memory, program memory, or stack instructions. The TMS370Cx2x contains 256 bytes of internal RAM mapped beginning at location 0000h (R0) and continuing through location 00FFh (R255).

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370Cx2x control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or P for a decimal designator. For example, the system-control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 4 shows the TMS370Cx2x PF address map.

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peripheral file (PF) (continued)

Table 4. TMS370Cx2x Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h–100Fh	P000–P00F	Reserved
1010h–101Fh	P010–P01F	System and EPROM/EEPROM control registers
1020h–102Fh	P020–P02F	Digital I/O port control registers
1030h–103Fh	P030–P03F	SPI peripheral control registers
1040h–104Fh	P040–P04F	Timer 1 registers
1050h–105Fh	P050–P05F	SCI1 peripheral control registers
1060h–10FFh	P060–P0FF	Reserved

data EEPROM

The TMS370Cx2x devices contain 256 bytes of data EEPROM and are memory mapped beginning at location 1F00h and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B). The data EEPROM features include the following:

- Programming:
 - Bit-, byte-, and block-write/erase modes
 - Internal charge pump circuitry. No external EEPROM programming voltage supply is needed.
 - Control register: Data EEPROM programming is controlled by the DEECTL located in the PF frame beginning at location P01A. See Table 5.
 - In-circuit programming capability. There is no need to remove the device to program it.
- Write protection. Writes to the data EEPROM are disabled during the following conditions.
 - Reset. All programming of the data EEPROM module is halted.
 - Write protection active. There is one write-protect bit per 32-byte EEPROM block.
 - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 5. Data EEPROM and Program EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME
P01A	DEECTL	Data EEPROM Control Register
P01B	—	Reserved
P01C	EPCTL	Program EPROM Control Register

program EPROM[†]

The TMS370C722 and SE370C722 devices contain 8K bytes of program EPROM mapped, beginning at location 6000h and continuing through location 7FFFh, as shown in Figure 3. Reading the program EPROM modules is identical to reading other internal memory. During programming, the program EPROM is controlled by the EPROM control register (EPCTL). The program EPROM module features include:

- Programming
 - In-circuit programming capability if V_{PP} is applied to MC
 - Control register: EPROM programming is controlled by the EPROM control register (EPCTL) located in the peripheral file (PF) frame at location P01C as shown in Table 5.
- Write protection: Writes to the program EPROM are disabled under the following conditions:
 - Reset: All programming to the EPROM module is halted
 - Low-power modes
 - 13 V not applied to MC

program ROM[†]

The program ROM consists of 4K or 8K bytes of mask programmable read-only memory (see Table 6). The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication.

Table 6. Program ROM Memory Map

	'x20A	'x22A
ROM size	4K bytes	8K bytes
Memory mapped	7000h – 7FFFh	6000h – 7FFFh

system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx2x CPU-based device. Three actions can cause a system reset. Two of these actions are internally generated, while one ($\overline{\text{RESET}}$) is controlled externally. These actions are as follows:

- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside the recommended operating range. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B) for more information.
- External $\overline{\text{RESET}}$ Pin. A low-level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x2x device to reset external system components. Additionally, if a cold start (V_{CC} is off for several hundred milliseconds) condition or oscillator failure occurs or $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

[†] Memory addresses 7FF0h through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions are located between addresses 7FC0h and 7FDFh.

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system reset (continued)

After a reset, the program can check the oscillator fault flag, the cold start flag and the watchdog reset to determine the source of the reset. A reset does not clear these flags. Table 7 lists the reset sources.

Table 7. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Registers A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to by the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

RESET must be held low until the clock signal is valid and V_{CC} is within the operating range, when an external reset circuit is connected to **RESET**. Figure 4 shows a typical reset circuit.

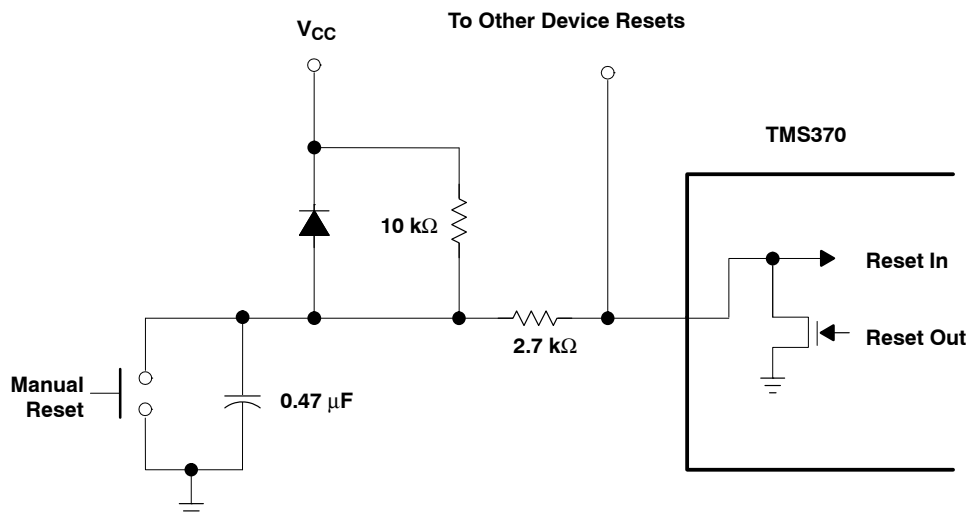


Figure 4. Typical Reset Circuit

interrupts

The TMS370 family software-programmable interrupt structure supports flexible on-chip and external-interrupt configurations to meet real-time interrupt-driven application requirements. The hardware-interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be enabled independently by the global-interrupt enable bits (IE1 and IE2) of the status register.

Each system interrupt is configured independently on either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is configured selectively on either the high- or low-priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority chains is performed within the peripheral modules to support interrupt expansion to future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx2x has seven hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 8. Each system interrupt has a dedicated interrupt vector located in program memory through which control is passed to the interrupt service routines. A system interrupt can have multiple interrupt sources (e.g., SCI RXNT has two interrupt sources). All of the interrupt sources are individually maskable by local interrupt-enable control bits in the associated peripheral file. Each interrupt source FLAG bit is individually readable for software polling or for determining which interrupt source generated the associated system interrupt.

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interrupts (continued)

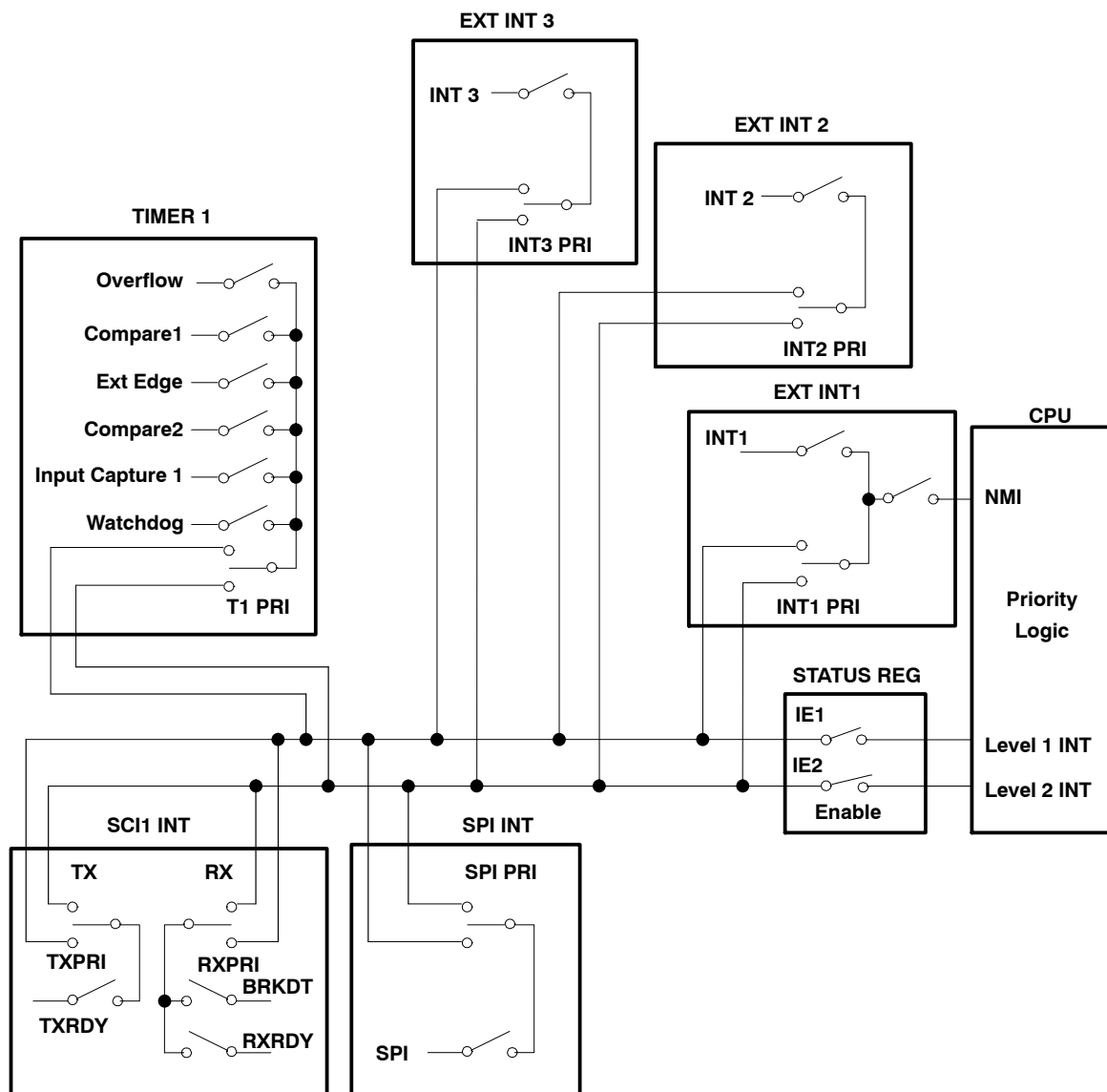


Figure 5. Interrupt Control

Four of the system interrupts are generated by on-chip peripheral functions, and three external interrupts are supported. Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in peripheral file frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual- or global-enable mask bits. The INT1 NMI bit is protected during non-privileged operation and therefore should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software configured as general-purpose input/output pins if the interrupt function is not required (INT1 can be similarly configured as an input pin).

interrupts (continued)

Table 8. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY [†]
External RESET Watchdog Overflow Oscillator Fault Detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	RESET [‡]	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1 [‡]	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2 [‡]	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3 [‡]	7FF8h, 7FF9h	4
SPI RX/TX Complete	SPI INT FLAG	SPIINT	7FF6h, 7FF7h	5
Timer 1 Overflow Timer 1 Compare 1 Timer 1 Compare 2 Timer 1 External Edge Timer 1 Input-Capture Watchdog Overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC INT FLAG WD OVRFL INT FLAG	T1INT [§]	7FF4h, 7FF5h	6
SCI RX Data Register Full SCI RX Break Detect	RXRDY FLAG BRKDT FLAG	RXINT [‡]	7FF2h, 7FF3h	7
SCI TX Data Register Empty	TXRDY FLAG	TXINT	7FF0h, 7FF1h	8

[†] Relative priority within an interrupt level.

[‡] Releases microcontroller from STANDBY and HALT low-power modes.

[§] Releases microcontroller from STANDBY low-power mode.

privileged operation and EEPROM write-protection override

The TMS370Cx2x family enables the designer to software-configure the system and peripherals to meet the requirements of a broad variety of applications. The non-privileged mode of operation ensures the integrity of the system configuration once defined for an end application. Following a hardware reset, the TMS370Cx2x operates in the privileged mode where all peripheral file registers have unrestricted read/write access and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) is set to 1, causing the device to enter the non-privileged mode, thus disabling write operations to specific configuration control bits within the peripheral file. The system configuration bits listed in Table 9 are write-protected during the non-privileged mode and must be configured by software prior to exiting the privileged mode.

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privileged operation and EEPROM write-protection override (continued)

Table 9. Privileged Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCR0	P010.5 P010.6	PF AUTO WAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
SCIPRI	P05F.4 P05F.5 P05F.6 P05F.6	SCI ESPEN SCI RX PRIORITY SCI TX PRIORITY SCI STEST
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST
SPIPRI	P03F.5 P03F.6 P03F.7	SPI ESPEN SPI PRIORITY SPI STEST

† The privileged bits are shown in a bold typeface in Table 11.

The WPO mode provides an external hardware method of overriding the WPR of data EEPROM on the TMS370Cx2x. WPO mode is entered by applying a 12-V input to the MC pin after the RESET pin input goes high. The high voltage on the MC pin during the WPO mode is not the programming voltage for the data EEPROM or program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware system level capability to modify the personality or calibration information in the data EEPROM while the device remains in the application, but only while a 12-V external input is present on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power operating modes

The TMS370Cx2x devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact when the mask is manufactured.

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls the low-power mode selection.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity stops; however, the oscillator, internal clocks, timer 1, and receive start-bit detection circuit of the SCI1 remain active. System processing is suspended until a qualified interrupt (hardware RESET, external interrupt on INT1, INT2, INT3, timer 1 interrupt, or low level on the receive pin of the SCI1) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx2x is in its lowest power consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware RESET, external interrupt on the INT1, INT2, INT3, or low level on the receive pin of the SCI1) is detected. The power-down mode-selection bits are summarized in Table 10.



low-power operating modes (continued)

Table 10. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X [†]	IDLE

[†] Don't care

When low-power modes are disabled through a programmable contact, writing to the SCCR2.6-7 bits is ignored. In addition, if an IDLE instruction is executed when low-power modes are disabled, the device always enters the IDLE mode.

To provide a method for always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI always is generated, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (SP, PC, and ST), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the WD timer is inhibited.

clock modules

The 'x2x family provides two clock options that are referred to as divide-by-1 (phase-locked loop) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 MCU. The 'x2x masked ROM devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device.

The divide-by-1 clock module option provides reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a one-to-one match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency, whereas the divide-by-4 produces a SYSCLK which is one-fourth the frequency of the external resonator. Inside of the divide-by-1 module, the frequency of the external resonator is multiplied by four, and the clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. These are formulated as follows:

$$\text{Divide-by-4 option : } \text{SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option : } \text{SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of a divide-by-1 oscillator is the improved EMI performance. The harmonics of low-speed resonators extend through fewer of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 reduces the resonator speed by four, and this results in a steeper decay of emissions produced by the oscillator.

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system configuration registers

Table 11 contains peripheral file frame 1 system configuration and control register functions for controlling EEPROM programming. The privileged bits are shown in bold typeface and shaded.

Table 11. Peripheral File Frame 1: System Configuration and Control Registers†

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTOWAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D to P01F	Reserved								

† Privileged bits are shown in bold typeface.

peripheral file frame 2

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 12 and Table 13 detail the specific addresses, registers, and control bits within the peripheral file frame.

Table 12. Peripheral File Frame 2: Digital Port Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
P020	Reserved								APOINT1
P021	Port A Control Register 2 (must be 0)								APOINT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPOINT1
P025	Port B Control Register 2 (must be 0)								BPOINT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPOINT1
P029	—	—	—	—	—	—	—	Port C Control Register 2 (must be 0)	CPOINT2
P02A	—	—	—	—	—	—	—	Port C Data	CDATA
P02B	—	—	—	—	—	—	—	Port C Direction	CDIR
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPOINT1
P02D	Port D Control Register 2 (must be 0) [†]					—	—	—	DPOINT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 13. Port Configuration Register Setup

PORT	PIN	abcd 00q1	abcd 00y0
A	0–7	Data out q	Data in y
B	0–7	Data out q	Data in y
C	0	Data out q	Data in y
D	3–7	Data out q	Data in y
a = Port × Control Register 1 [‡] b = Port × Control Register 2 c = Data d = Direction			

[‡] DPORT only

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programmable timer 1

The programmable timer module of the TMS370Cx2x provides the enhanced timer resources required to perform real-time system control. The Timer 1 module contains the general-purpose timer T1 and the watchdog (WD) timer. The two independent 16-bit timers (T1 and WD) allow program selection of input clock sources (real-time, external event, or pulse-accumulate) with multiple 16-bit registers (input-capture and compare) for special timer function control. The timer 1 module includes three external device pins that can be used for multiple counter functions (operation-mode dependent), or used as general-purpose I/O pins. The T1 module is shown in Figure 6.

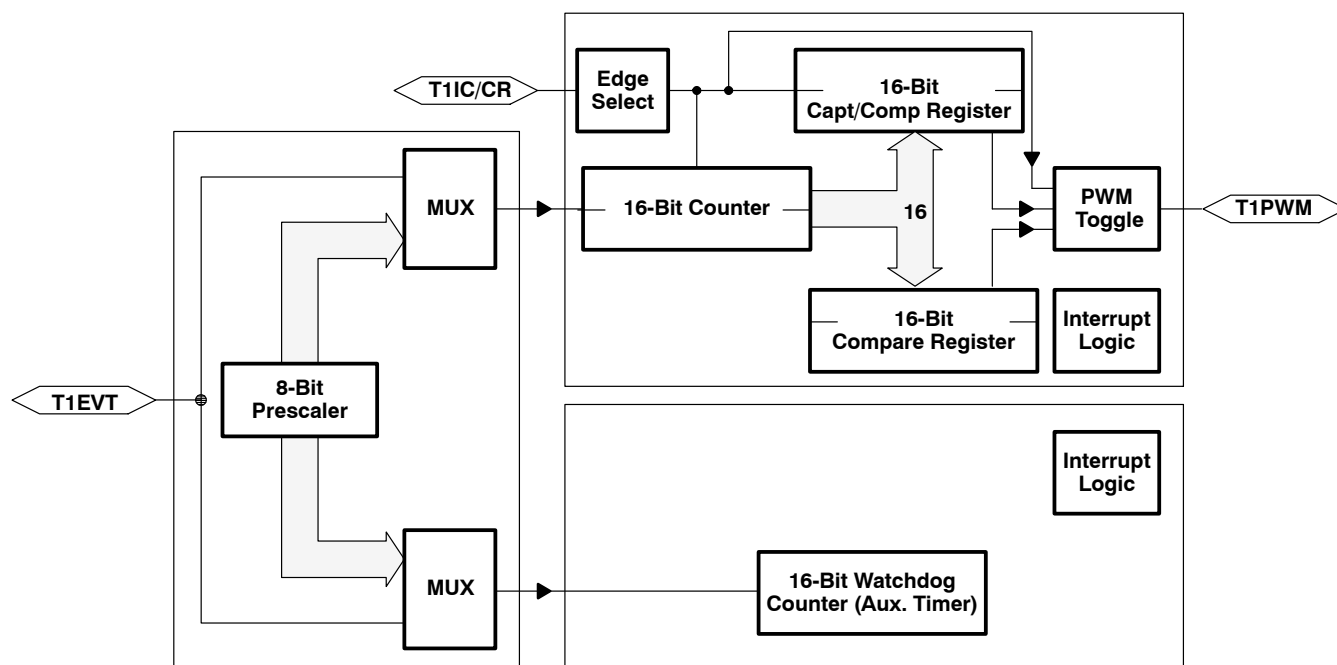


Figure 6. Timer 1 Block Diagram

- Three T1 I/O pins
 - T1IC/CR: T1 input capture / counter-reset input pin, or general-purpose bidirectional I/O pin
 - T1PWM: T1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T1EVT: T1 event input pin, or general-purpose bidirectional I/O pin
- Two operational modes:
 - Dual-compare mode: Provides PWM signal
 - Capture/compare mode: Provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either capture or compare register
- One 16-bit WD counter can be used as an event counter, a pulse accumulator, or an interval timer if WD feature is not needed.
- Prescaler/clock sources that determine one of eight clock sources for general-purpose timer

programmable timer 1 (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR)
- Interrupts that can be generated on the occurrence of:
 - A capture
 - A compare equal
 - A counter overflow
 - An external edge detection
- Sixteen T1 module control registers located in the PF frame beginning at address P040

The T1 module control registers are listed in Table 14.

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programmable timer 1 (continued)

Table 14. Timer Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Dual-Compare and Capture/Compare									
P040	Bit 15 T1 Counter MSbyte							Bit 8	T1CNTR
P041	Bit 7 T1 Counter LSbyte							Bit 0	
P042	Bit 15 Compare Register MSbyte							Bit 8	T1C
P043	Bit 7 Compare Register LSbyte							Bit 0	
P044	Bit 15 Capture/Compare Register MSbyte							Bit 8	T1CC
P045	Bit 7 Capture/Compare Register LSbyte							Bit 0	
P046	Bit 15 Watchdog Counter MSbyte							Bit 8	WDCNTR
P047	Bit 7 Watchdog Counter LSbyte							Bit 0	
P048	Bit 7 Watchdog Reset Key							Bit 0	WDRST
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE=0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

programmable timer 1 (continued)

Figure 7 shows the Timer 1 capture/compare mode block diagram. The annotations on the diagram identify the register and the bit(s) in the PF. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

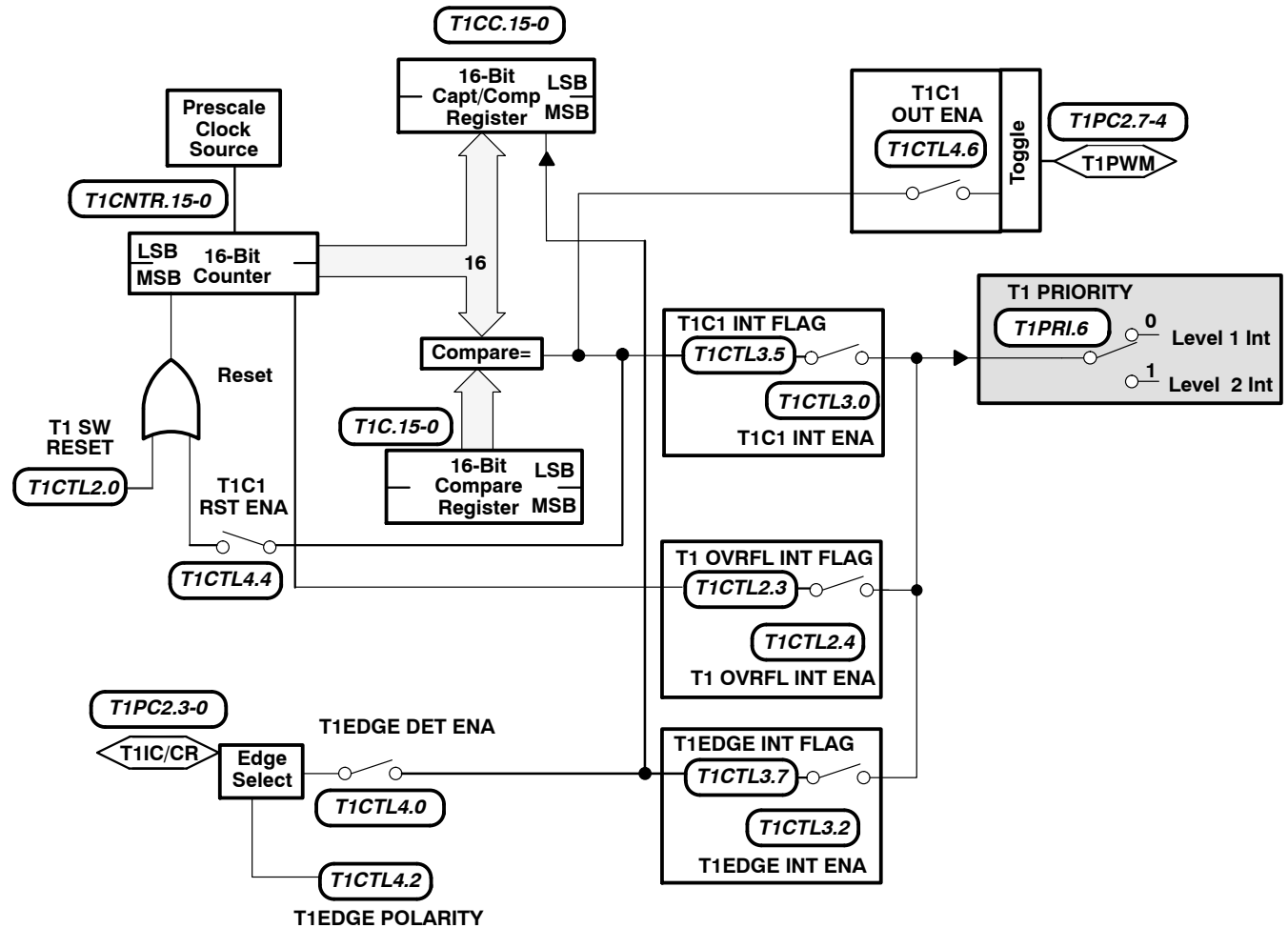


Figure 7. Capture/Compare Mode

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programmable timer 1 (continued)

Figure 8 shows the Timer 1 dual-compare mode block diagram. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

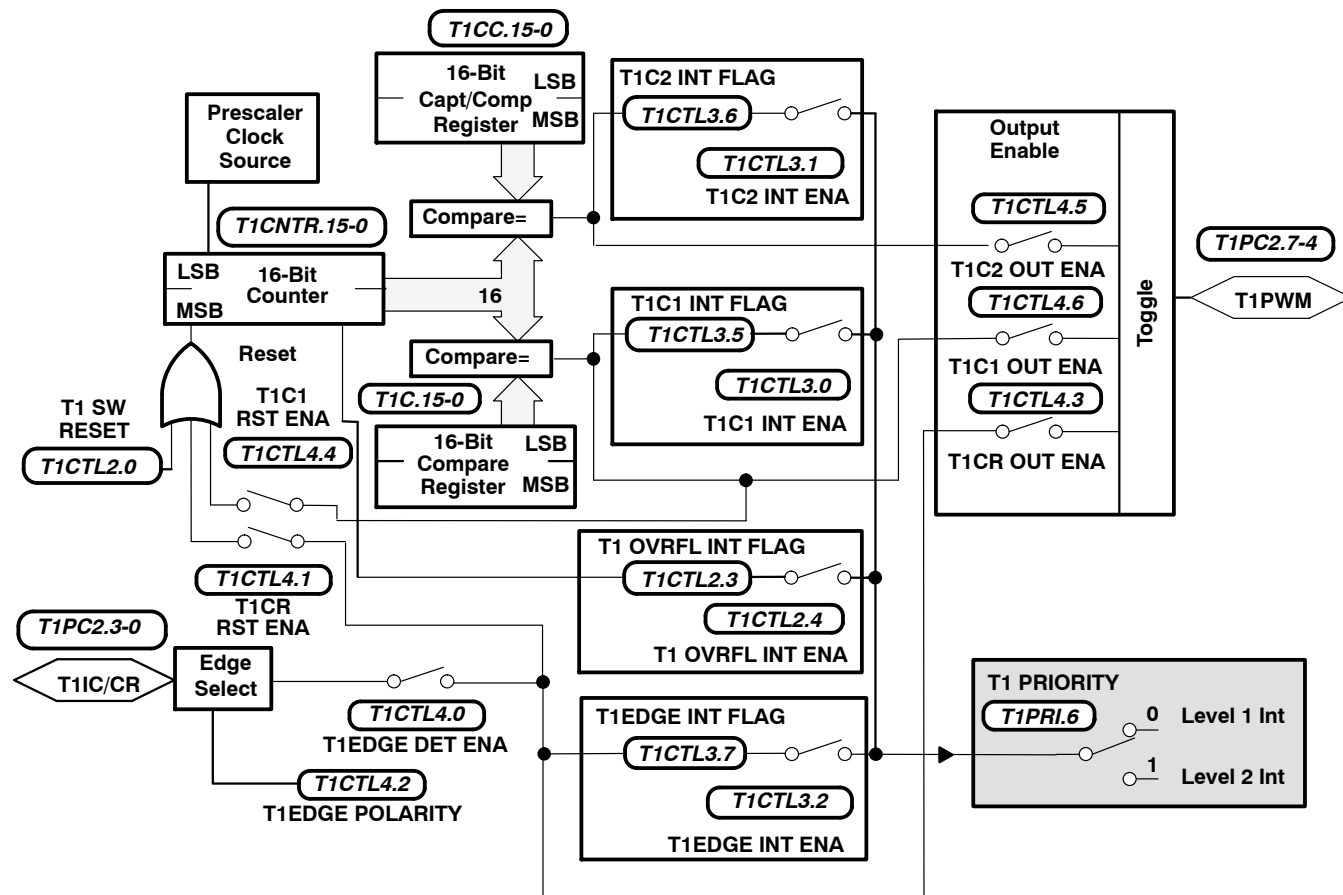


Figure 8. Dual-Compare Mode

programmable timer 1 (continued)

The TMS370Cx2x device includes a 24-bit WD timer, contained in the T1 module, which can be programmed as an event counter, pulse accumulator, or interval timer if the watchdog function is not used. The WD monitors software and hardware operation, and implements a system reset when the WD counter is not serviced properly (WD counter overflow or WD counter is re-initialized by an incorrect value). The WD can be configured as one of the three mask options as follows: standard watchdog, hard WD, or simple counter.

- Standard watchdog configuration (see Figure 9) for 'C722 EPROM and mask-ROM devices:
 - Watchdog mode
 - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register clears the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows
 - A watchdog overflow flag (WD OVRFL INT FLAG) bit indicates whether the WD timer initiated a system reset.
 - Non-watchdog mode
 - Watchdog timer can be configured as an event counter, pulse accumulator or an interval timer.

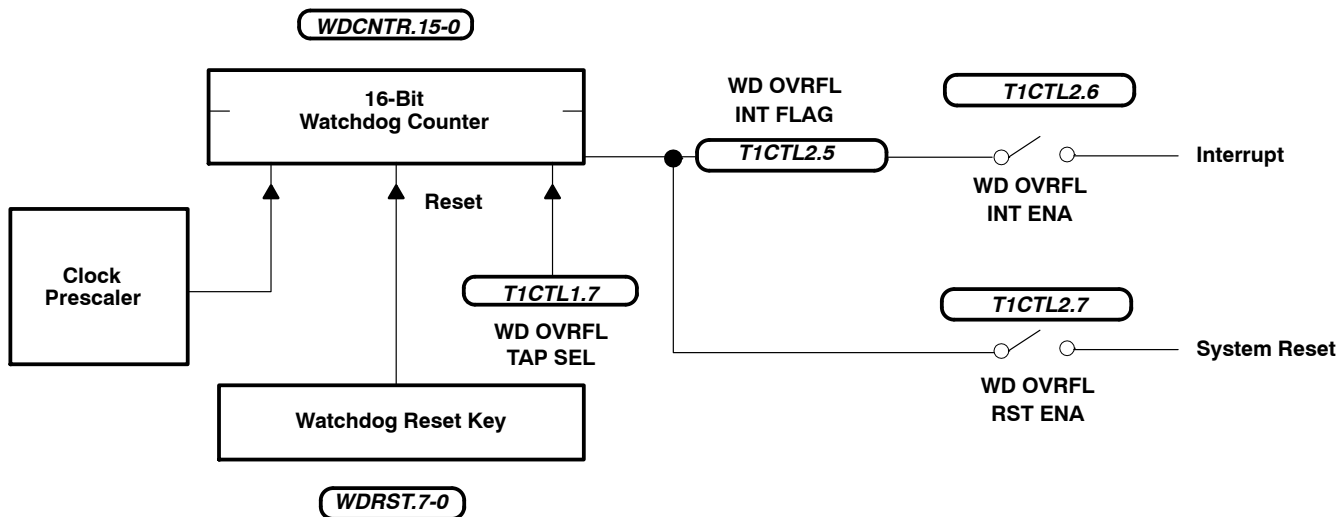


Figure 9. Standard Watchdog

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programmable timer 1 (continued)

- Hard watchdog configuration (see Figure 10) for 'C722 EPROM and mask-ROM devices:
 - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register clears the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the WDRST or if the counter overflows
 - A WD overflow flag (WD OVRFL INT FLAG) bit indicates whether the WD timer initiated a system reset.
 - Automatic activation of the WD timer upon power-up reset
 - INT1 is enabled as a nonmaskable interrupt during low power modes.

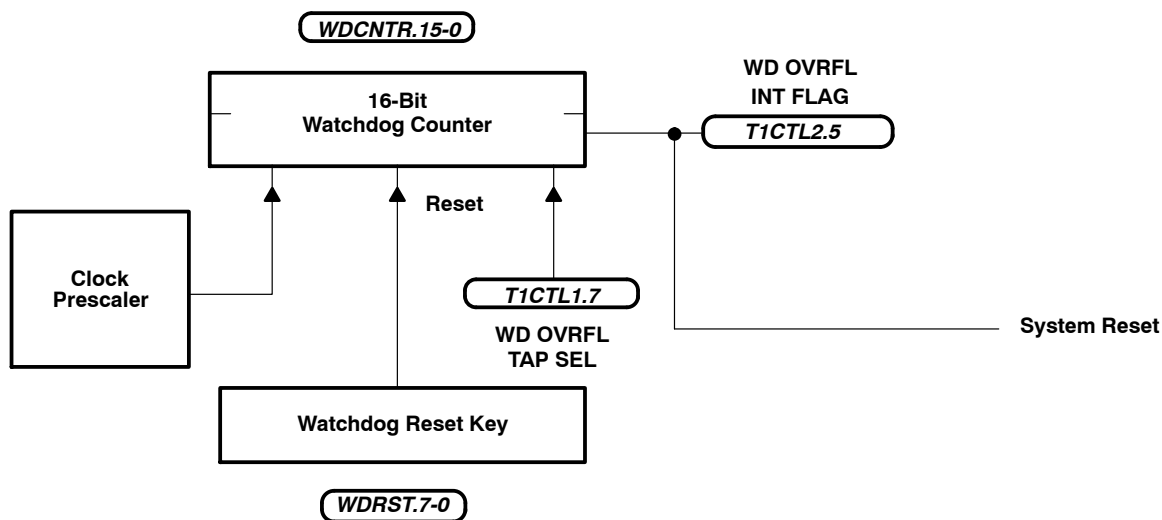


Figure 10. Hard Watchdog

programmable timer 1 (continued)

- Simple counter configuration (see Figure 11) for mask-ROM devices only
 - Simple counter can be configured as an event counter, pulse accumulator, or internal timer.

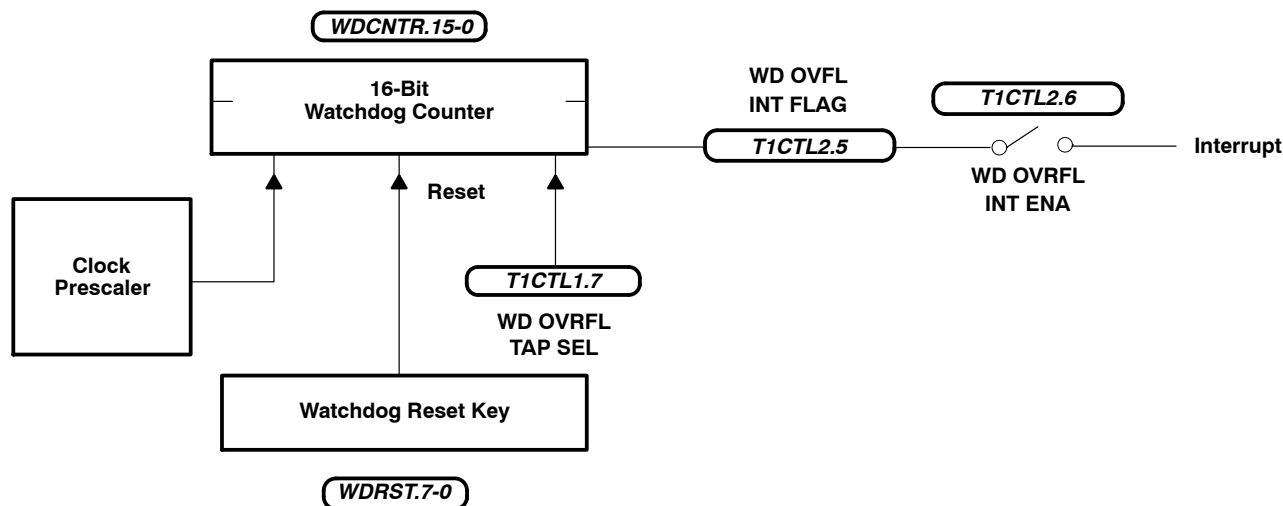


Figure 11. Simple Counter

serial peripheral interface

The SPI is a high-speed synchronous serial I/O port that allows a serial bit stream of programmed length (1 to 8 bits) to be shifted into and out of the device at a programmable bit transfer rate. The SPI normally is used for communications between the microcontroller and external peripherals or another microcontroller. Typical applications include external I/O or peripheral expansion by way of devices such as shift registers, display drivers, and A/D converters. Multi-device communications are supported by the master/slave operation of the SPI. The SPI module features include the following:

- Three external pins
 - SPISOMI: SPI slave output/master input pin or general-purpose bidirectional I/O pin
 - SPISIMO: SPI slave input/master output pin or general-purpose bidirectional I/O pin
 - SPICLK: SPI serial clock pin or general-purpose bidirectional I/O pin
- Two operational modes: Master and slave
- Eight programmable baud rates
 - Maximum baud rate in master mode: 2.5M bps at 5 MHz SYSCLK

$$\text{SPI BAUD RATE} = \frac{\text{SYSCLK}}{2 \times 2^b}$$

where b=bit rate in SPICCR.5-3 (range 0–7)

- Maximum baud rate in slave mode: 625K bps at 5 MHz SYSCLK

$$\text{SPI BAUD RATE} < \text{SYSCLK}/8$$

- Data word format: one to eight data bits
- Simultaneous receiver and transmitter operations (transmit function can be disabled in software)

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serial peripheral interface (continued)

- Transmitter and receiver operations occur through interrupt-driven or polled algorithms.
- Seven SPI module control registers located in control register frame beginning at address P030h

The SPI module control registers are listed in Table 15.

Table 15. SPI Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/ SLAVE	TALK	SPI INT ENA	SPICTL
P032 to P036	Reserved								
P037	RCVD7	RCVD6	RCVD5	RCVD4	RCVD3	RCVD2	RCVD1	RCVD0	SPIBUF
P038	Reserved								
P039	SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0	SPIDAT
P03A to P03C	Reserved								
P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
P03F	SPI STEST	SPI PRIORITY	SPI ESPEN	—	—	—	—	—	SPIPRI

The SPI block diagram is listed in Figure 12.

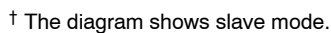


Figure 12. SPI Block Diagram

The TMS370x2x devices include a serial communications interface 1 (SCI1) module. The SCI1 module supports digital communications between the TMS370 devices and other asynchronous peripherals, and uses the standard non-return-to-zero (NRZ) format. The SCI1's receiver and transmitter are double buffered, and each has separate enable and interrupt bits. Both can operate independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI1 checks received data for break detection, parity, overrun, and framing errors. The bit rate (baud) is programmable to over 65,000 speeds through a 16-bit baud-select register.

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serial communications interface 1 (SCI1) (continued)

Features of the SCI1 module include:

- Three external pins:
 - SCITXD: SCI transmit output pin or general purpose bidirectional I/O pin
 - SCIRXD: SCI receive input pin or general purpose bidirectional I/O pin
 - SCICLK: SCI bidirectional serial clock pin, or general purpose bidirectional I/O pin
- Two communications modes: asynchronous and isosynchronous[†]
- Baud rate: 64K programmable rates
 - Asynchronous mode: 3 bps to 156K bps at 5 MHz SYSCLK

$$\text{ASYNCHRONOUS BAUD} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 32}$$

- Isosynchronous mode: 39 bps to 2.5M bps at 5 MHz SYSCLK

$$\text{ISOSYNCHRONOUS BAUD} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 2}$$

- Data word format
 - One start bit
 - Data word length programmable from 1 to 8 bits
 - Optional even/odd/no parity bit
 - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: Idle-line and address bit
- Half or full-duplex operation
- Double-buffered receive and transmit functions
- Interrupt driven or polled algorithms with status flags control transmitter (TX) and receiver (RX) operations.
 - Transmitter: TXRDY flag (transmitter buffer register is ready to receive another character) and TX EMPTY flag (transmitter shift register is empty)
 - Receiver: RXRDY flag (receive buffer register ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR monitoring four interrupt conditions
 - Separate enable bits for transmitter and receiver interrupts
 - NRZ (non-return-to-zero) format
- Eleven SCI1 module control registers are located in control register frame beginning at address P050h.

[†] Isosynchronous = Isochronous

serial communications interface 1 (SCI1) (continued)

The SCI1 module control registers are listed in Table 16.

Table 16. Peripheral File Frame 5: SCI1 Module Control Registers†

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNC/ ISOSYNC	ADDRESS IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	Bit 15 Baud Rate Select Register MSB Bit 8								BAUD MSB
P053	Bit 7 Baud Rate Select Register LSB Bit 0								BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	Receive Data Buffer Register								RXBUF
P058	Reserved								
P059	Transmit Data Buffer Register								TXBUF
P05A	Reserved								
P05B									
P05C									
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCI TXD DATA IN	SCI TXD DATA OUT	SCI TXD FUNCTION	SCI TXD DATA DIR	SCI RXD DATA IN	SCI RXD DATA OUT	SCI RXD FUNCTION	SCI RXD DATA DIR	SCIPC2
P05F	SCI STEST	SCI TX PRIORITY	SCI RX PRIORITY	SCI ESPEN	—	—	—	—	SCIPRI

† Privileged bits are shown in bold typeface.

The SCI1 module block diagram is illustrated in Figure 13.



Table 17 provides an opcode-to-instruction cross reference of all 73 instructions and 274 opcodes of the '370Cx2x instruction set. The numbers at the top of this table represent the most significant nibble (MSN) of the opcode while the numbers at the left side of the table represent the least significant nibble (LSN). The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

Table 17. TMS370 Family Opcode/Instruction Map[†]

		MSN															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8				CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
1	JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7	
2	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7	
3	JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8	
4	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes	
5	JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14		
6	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6	
7	JNC ra 2/5	BTJZ Rs,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10	
8	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7	
9	JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9	
A	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12	
B	JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A, *lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8	

[†] All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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Table 17. TMS370 Family Opcode/Instruction Map[†] (Continued)

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L S N	C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
	D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
	E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
	F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7
Second byte of two-byte instructions (F4xx):														F4	8	MOVW *n[Rn] 4/15	DIV Rn,A 3/14-63
														F4	9	JMPL *n[Rn] 4/16	
														F4	A	MOV *n[Rn],A 4/17	
														F4	B	MOV A,*n[Rn] 4/16	
														F4	C	BR *n[Rn] 4/16	
														F4	D	CMP *n[Rn],A 4/18	
														F4	E	CALL *n[Rn] 4/20	
														F4	F	CALLR *n[Rn] 4/22	

Legend:

- * = Indirect addressing operand prefix
- & = Direct addressing operand prefix
- # = immediate operand
- #16 = immediate 16-bit number
- lab = 16-label
- n = immediate 8-bit number
- Pd = Peripheral register containing destination type
- Pn = Peripheral register
- Ps = Peripheral register containing source byte
- ra = Relative address
- Rd = Register containing destination type
- Rn = **Register file**
- Rp = Register pair
- Rpd = Destination register pair
- Rps = Source Register pair
- Rs = Register containing source byte

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

development system support

The TMS370 family development support tools include an assembler, a C compiler, a linker, an in-circuit emulator XDS/22, CDT, and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
 - Includes extensive macro capability
 - Provides high-speed operation
 - Includes format conversion utilities for popular formats
- ANSI C Compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, Sun-3™ or Sun-4™)
 - Generates assembly code for the TMS370 that can be inspected easily
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables direct reference the TMS370's port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (Compact Development Tool) real-time in-circuit emulation
 - Base (Part Number EDSCDT370 – for PC, requires cable)
 - Cable for 40-pin DIP (Part No. EDSTRG40DILX)
 - Cable for 44-pin PLCC (Part No. EDSTRG44PLCCX)
 - Cable for 40-pin SDIP (Part No. EDSTRG40SDILX)
 - EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Includes compatibility to upload/download program and data memory
 - Executes programs and software routines
 - Includes 1024 samples trace buffer
 - Includes single-step executable instructions
 - Uses software breakpoints to halt program execution at selected address
- XDS/22 in-circuit emulator
 - Base (Part Number TMDS3762210 for PC, requires cable)
 - Cable for 40-pin DIP/SDIP, 44-pin PLCC (Part No. TMDS3788844)
 - Contains all of the features of the CDT370 described previously but does not have the capability to program the data EEPROM and program EPROM
 - Contains sophisticated breakpoint trace and timing hardware that provides up to 2047 qualified trace samples with symbolic disassembly
 - Allows qualification of breakpoints by address and/or data on any type of memory acquisition. Up to four levels of events can be combined to cause a breakpoint.

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development system support (continued)

- Provides timers for analyzing total and average time in routines
- Contains an eight-line logic probe for adding visibility of external signals to the breakpoint qualifier and to trace display
- Microcontroller programmer
 - Base (Part No. TMDS3760500A – for PC, requires programmer head)
 - Single unit head for 44-pin PLCC (Part No. TMDS3780510A)
 - Single unit head for 40-pin DIP/SDIP (Part No. TMDS3780511A)
 - PC-based, window/function-key-oriented user interface for ease of use and rapid learning environment
- Starter Kit (Part No. TMDX37000 – for PC)
 - Includes TMS370 Assembler diskette and documentation
 - Includes TMS370 Simulator
 - Includes programming adapter board and programming software
 - Does not include (to be supplied by the user)
 - + 5 V power supply
 - ZIF sockets
 - Nine-pin RS232 cable



device numbering conventions

Figure 14 illustrates the numbering and symbol nomenclature for the TMS370Cx2x family.

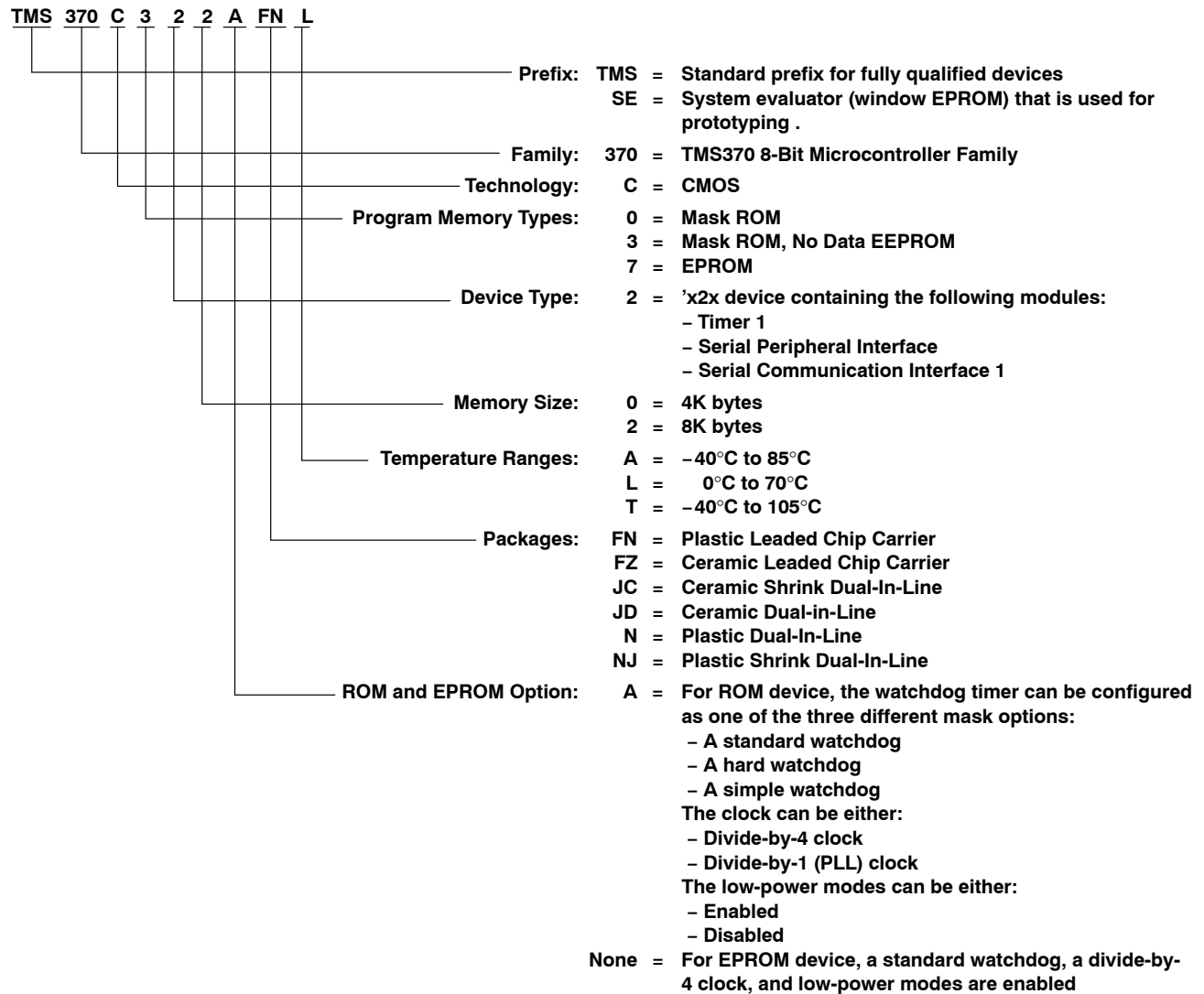


Figure 14. TMS370Cx2x Family Nomenclature

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device part numbers

Table 18 lists all of the 'x2x devices available. The device part number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog timer options desired. Each device can have only one of the three possible watchdog timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 18. Device Part Numbers

DEVICE PART NUMBERS FOR 44 PINS (LCC)	DEVICE PART NUMBERS FOR 40 PINS (DIP)	DEVICE PART NUMBERS FOR 40 PINS (SDIP)
TMS370C020AFNA TMS370C020AFNL TMS370C020AFNT	TMS370C020ANA TMS370C020ANL TMS370C020ANT	TMS370C020ANJA† TMS370C020ANJL† TMS370C020ANJT†
TMS370C022AFNA TMS370C022AFNL TMS370C022AFNT	TMS370C022ANA TMS370C022ANL TMS370C022ANT	TMS370C022ANJA† TMS370C022ANJL† TMS370C022ANJT†
TMS370C320AFNA TMS370C320AFNL TMS370C320AFNT	TMS370C320ANA TMS370C320ANL TMS370C320ANT	TMS370C320ANJA† TMS370C320ANJL† TMS370C320ANJT†
TMS370C322AFNA TMS370C322AFNL TMS370C322AFNT	TMS370C322ANA TMS370C322ANL TMS370C322ANT	TMS370C322ANJA† TMS370C322ANJL† TMS370C322ANJT†
TMS370C722FNT	TMS370C722NT	TMS370C722NJT†
SE370C722FZT‡	SE370C722JDT‡	SE370C722JCT‡

† The NJ designator for the 40-pin plastic shrink DIP package was formerly known as N2. The mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

‡ System evaluators are for use only in prototype environment, and their reliability has not been characterized.



new code release form

Figure 15 shows a sample of the new code release form.

NEW CODE RELEASE FORM TEXAS INSTRUMENTS TMS370 MICROCONTROLLER PRODUCTS		DATE: _____	
To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information:			
1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media) 2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.			
Company Name: _____ Street Address: _____ Street Address: _____ City: _____ State _____ Zip _____ Customer Part Number: _____ Customer Application: _____		Contact Mr./Ms.: _____ Phone: (_____) _____ Ext.: _____ Customer Purchase Order Number: _____ Customer Print Number *Yes: _____ # _____ No: _____ (Std. spec to be followed) *If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.	
TMS370 Device: _____ TI Customer ROM Number: _____ (provided by Texas Instruments)			
OSCILLATOR FREQUENCY			
	MIN	TYP	MAX
☐ External Drive (CLKIN)	_____	_____	_____
☐ Crystal	_____	_____	_____
☐ Ceramic Resonator	_____	_____	_____
☐ Supply Voltage MIN: _____ MAX: _____ (std range: 4.5V to 5.5V)			
TEMPERATURE RANGE			
☐ 'L':	0° to 70°C (standard)		
☐ 'A':	-40° to 85°C		
☐ 'T':	-40° to 105°C		
SYMBOLIZATION			
☐ TI standard symbolization ☐ TI standard w/customer part number ☐ Customer symbolization (per attached spec, subject to approval)			
NON-STANDARD SPECIFICATIONS: ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.			
RELEASE AUTHORIZATION: This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cycletime commences when this document is signed off and the verification code is approved by the customer.			
1. Customer: _____ Date: _____		2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____	

CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS

Low Power Modes ☐ Enabled ☐ Disabled	Watchdog counter ☐ Standard ☐ Hard Enabled ☐ Simple Counter	Clock Type ☐ Standard (/4) ☐ PLL (/1)

NOTE:
 Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B).

PACKAGE TYPE

☐ 'N' 28-pin PDIP ☐ "FN" 28-pin PLCC ☐ "N" 40-pin PDIP ☐ "NJ" 40-pin PSDIP (formerly known as N2)	☐ "FN" 44-pin PLCC ☐ "FN" 68-pin PLCC ☐ "NM" 64-pin PSDIP

BUS EXPANSION

☐ YES
 ☐ NO

Figure 15. Sample New Code Release Form

TMS370Cx2x 8-BIT MICROCONTROLLER

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Table 19 is a collection of all the peripheral file frames used in the 'Cx2x (provided for a quick reference).

Table 19. Peripheral File Frame Compilation

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	System Configuration Registers								
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTO WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT / STANDBY	PWRDWN / IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D P01E P01F	Reserved								
	Digital Port Control Registers								
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	Port B Control Register 2 (must be 0)								BPORT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPORT1
P029	—	—	—	—	—	—	—	Port C Control Register 2 (must be 0)	CPORT2
P02A	—	—	—	—	—	—	—	Port C Data	CDATA
P02B	—	—	—	—	—	—	—	Port C Direction	CDIR
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0)†					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.



Table 19. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
SPI Module Control Register Memory Map									
P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/SLAVE	TALK	SPI INT ENA	SPICTL
P032 to P036	Reserved								
P037	RCVD7	RCVD6	RCVD5	RCVD4	RCVD3	RCVD2	RCVD1	RCVD0	SPIBUF
P038	Reserved								
P039	SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0	SPIDAT
P03A to P03C	Reserved								
P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
P03F	SPI STEST	SPI PRIORITY	SPI ESPEN	—	—	—	—	—	SPIPRI
Timer Module Register Memory Map									
Modes: Dual-Compare and Capture/Compare									
P040	Bit 15	T1Counter MSbyte						Bit 8	T1CNTR
P041	Bit 7	T1 Counter LSbyte						Bit 0	
P042	Bit 15	Compare Register MSbyte						Bit 8	T1C
P043	Bit 7	Compare Register LSbyte						Bit 0	
P044	Bit 15	Capture/Compare Register MSbyte						Bit 8	T1CC
P045	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P046	Bit 15	Watchdog Counter MSbyte						Bit 8	WDCNTR
P047	Bit 7	Watchdog Counter LSbyte						Bit 0	
P048	Bit 7	Watchdog Reset Key						Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE=0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

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Table 19. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	Modes: Dual-Compare and Capture/Compare								
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI
	SCI1 Module Control Register Memory Map								
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNC/ ISOSYNC	ADDRESS IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	Bit 15				Baud Rate Select Register MSB				Bit 8 BAUD MSB
P053	Bit 7				Baud Rate Select Register LSB				Bit 0 BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	Receive Data Buffer Register								RXBUF
P058	Reserved								
P059	Transmit Data Buffer Register								TXBUF
P05A	Reserved								
P05B									
P05C									
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCI TXD DATA IN	SCI TXD DATA OUT	SCI TXD FUNCTION	SCI TXD DATA DIR	SCI RXD DATA IN	SCI RXD DATA OUT	SCI RXD FUNCTION	SCI RXD DATA DIR	SCIPC2
P05F	SCI STEST	SCI TX PRIORITY	SCI RX PRIORITY	SCI ESPEN	—	—	—	—	SCIPRI

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC}) (see Note 2)	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	1 W
Operating free-air temperature, T_A : L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS} .

2. Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 3)		3		5.5	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET	2		V_{CC}	V
		XTAL2/CLKIN	0.8 V_{CC}		V_{CC}	
		RESET	0.7 V_{CC}		V_{CC}	
V_{MC}	MC (mode control) voltage	EEPROM write protect override (WPO)	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	
		Microcomputer	V_{SS}		0.3	
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	
		T version	–40		105	

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS} .

3. RESET must be externally activated when V_{CC} or SYSCLK is out of the recommended operating range.

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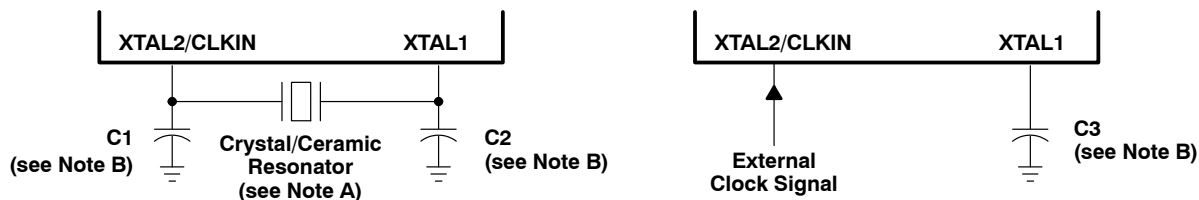
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	$I_{OL} = 1.4 \text{ mA}$			0.4	V
V_{OH}	High-level output voltage	$I_{OH} = -50 \mu\text{A}$	$0.9 V_{CC}$			V
		$I_{OH} = -2 \text{ mA}$	2.4			
I_I	Input current	$0 \text{ V} < V_I \leq 0.3 \text{ V}$			10	μA
		$0.3 \text{ V} < V_I \leq 13 \text{ V}$			650	
		See Note 4 $12 \text{ V} \leq V_I \leq 13 \text{ V}$			50	mA
	I/O pins	$0 \text{ V} \leq V_I \leq V_{CC}$			± 10	μA
I_{OL}	Low-level output current	$V_{OL} = 0.4 \text{ V}$	1.4			mA
I_{OH}	High-level output current	$V_{OH} = 0.9 V_{CC}$	-50			μA
		$V_{OH} = 2.4 \text{ V}$	-2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 7)	See Notes 5 and 6 SYSCLK = 5 MHz		30	45	mA
		See Notes 5 and 6 SYSCLK = 3 MHz		20	30	
		See Notes 5 and 6 SYSCLK = 0.5 MHz		7	11	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 8)	See Notes 5 and 6 SYSCLK = 5 MHz		10	17	mA
		See Notes 5 and 6 SYSCLK = 3 MHz		8	11	
		See Notes 5 and 6 SYSCLK = 0.5 MHz		2	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 9)	See Notes 5 and 6 SYSCLK = 3 MHz		6	8.6	mA
		See Notes 5 and 6 SYSCLK = 0.5 MHz		2	3.0	
	Supply current (HALT mode)	See Note 5 XTAL2/CLKIN < 0.2 V		2	30	μA

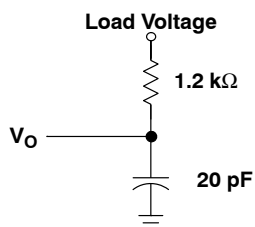
- NOTES: 4. Input current I_{PP} is a maximum of 50 mA only during EPROM programming.
5. Single chip mode, ports configured as inputs or outputs with no load. All inputs $\leq 0.2 \text{ V}$ or $\geq V_{CC} - 0.2 \text{ V}$.
6. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = $0.01 \text{ mA} \times (\text{total load capacitance} + \text{crystal capacitance in pF})$.
7. Maximum operating current = $7.6 (\text{SYSCLK}) + 7 \text{ mA}$.
8. Maximum standby current = $3 (\text{SYSCLK}) + 2 \text{ mA}$ (OSC POWER bit = 0).
9. Maximum standby current = $2.24 (\text{SYSCLK}) + 1.9 \text{ mA}$ (OSC POWER bit = 1, only valid up to 3 MHz SYSCLK).





NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
 B. The values of C1 and C2 are typically 15 pF and C3 value is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 16. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4\text{ V}$; Load Voltage = 0 V

Case 2: $V_O = V_{OL} = 0.4\text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 17. Typical Output Load Circuit (See Note A)

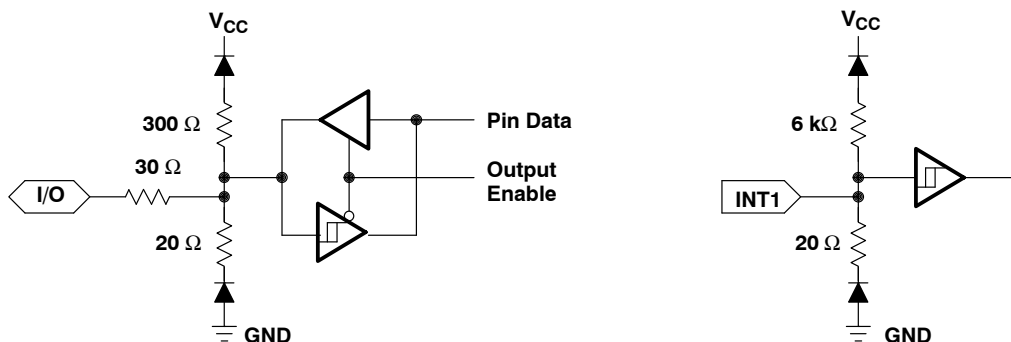


Figure 18. Typical Buffer Circuitry

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PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

AR	Array	S	Slave mode
B	Byte	SC	SYSCLK
CI	XTAL2/CLKIN	SIMO	SPISIMO
D	DATA	SOMI	SPISOMI
M	Master mode	SPC	SPICLK
PGM	Program	TXD	SCITXD
R	READ	W	WRITE
RXD	SCIRXD		

Lowercase subscripts and their meanings are:

c	cycle time (period)	su	setup time
d	delay time	v	valid time
f	fall time	w	pulse duration (width)
r	rise time		

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid

All timings are measured between high and low measurement points as indicated in Figure 19 and Figure 20.

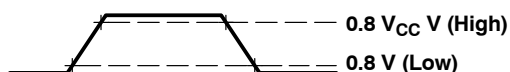


Figure 19. XTAL2/CLKIN Measurement Points

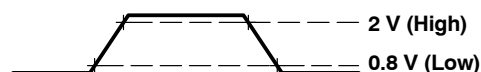


Figure 20. General Measurement Points

external clocking requirements for clock divided by 4 (see Note 10 and Figure 21)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(Cl)}$ Pulse duration, XTAL2/CLKIN (see Note 11)	20		ns
2	$t_{r(Cl)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(ClH-SCL)}$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN Crystal operating frequency	2	20	MHz
	SYSCLK Internal system clock operating frequency [†]	0.5	5	MHz

[†] SYSCLK = CLKIN/4

NOTES: 10. For V_{IL} and V_{IH} , refer to recommended operating conditions.

11. This pulse may be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

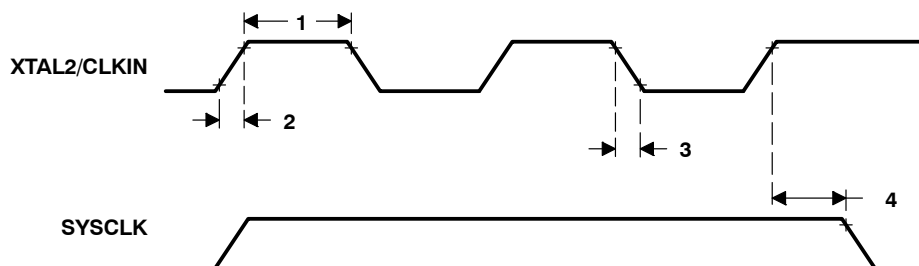


Figure 21. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL) (see Note 10 and Figure 22)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(Cl)}$ Pulse duration, XTAL2/CLKIN (see Note 11)	20		ns
2	$t_{r(Cl)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(ClH-SCH)}$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN Crystal operating frequency	2	5	MHz
	SYSCLK Internal system clock operating frequency [‡]	2	5	MHz

[‡] SYSCLK = CLKIN/1

NOTES: 10. For V_{IL} and V_{IH} , refer to recommended operating conditions.

11. This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

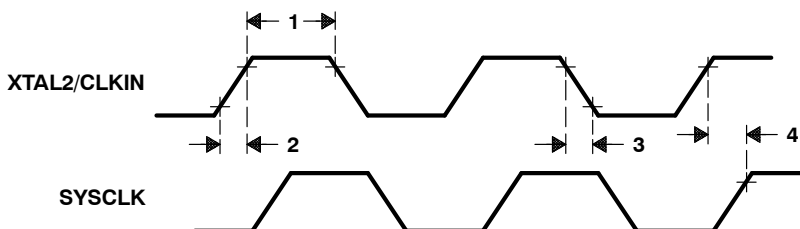


Figure 22. External Clock Timing for Divide-by-1

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switching characteristics and timing requirements (see Note 12 and Figure 23)

NO.	PARAMETER		MIN	MAX	UNIT
5	t_c	Cycle time, SYSCLK (system clock)	200	2000	ns
		Divide-by-4	200	500	
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low	$0.5 t_c - 20$	$0.5 t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high	$0.5 t_c$	$0.5 t_c + 20$	ns

NOTE 12: t_c = system-clock cycle time = $1 / \text{SYSCLK}$

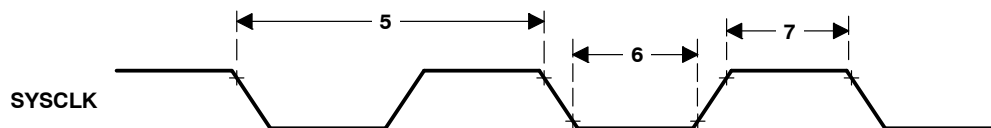


Figure 23. SYSCLK Timing

general purpose output signal switching time requirements (see Figure 24)

	MIN	NOM	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns

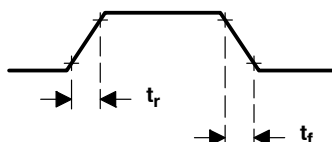


Figure 24. Signal Switching Timing

recommended EEPROM timing requirements for programming

	MIN	NOM	MAX	UNIT
$t_{w(PGM)B}$	10			ms
$t_{w(PGM)AR}$	20			ms

recommended EPROM operating conditions for programming

	MIN	NOM	MAX	UNIT
V_{CC}	4.75	5.5	6	V
V_{PP}	13	13.2	13.5	V
I_{PP}		30	50	mA
SYSCLK	Divide-by-4	0.5	5	MHz
	Divide-by-1	2	5	

recommended EPROM timing requirements for programming

	MIN	NOM	MAX	UNIT
$t_{w(EPGM)}$	0.40	0.50	3	ms

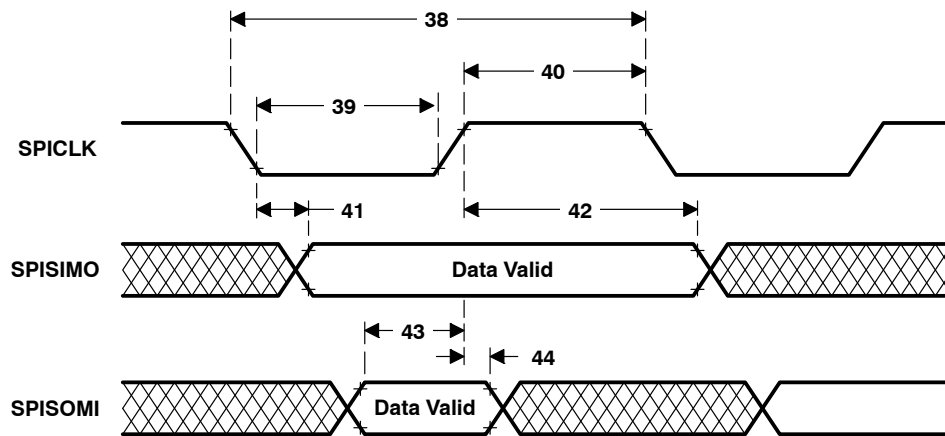
NOTE 13: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.



SPI master mode external timing characteristics and requirements (see Note 12 and Figure 25)

NO.		MIN	MAX	UNIT
38	$t_{c(SPC)M}$ Cycle time, SPICLK	$2t_c$	$256t_c$	ns
39	$t_{w(SPCL)M}$ Pulse duration, SPICLK low	$t_c - 45$	$0.5t_{c(SPC)} + 45$	ns
40	$t_{w(SPCH)M}$ Pulse duration, SPICLK high	$t_c - 55$	$0.5t_{c(SPC)} + 45$	ns
41	$t_{d(SPCL-SIMOV)M}$ Delay time, SPISIMO valid after SPICLK low (polarity = 1)	- 65	50	ns
42	$t_{v(SPCH-SIMO)M}$ Valid time, SPISIMO data valid after SPICLK high (polarity = 1)	$t_{w(SPCH)} - 50$		ns
43	$t_{su(SOMI-SPCH)M}$ Setup time, SPISOMI to SPICLK high (polarity = 1)	$0.25 t_c + 150$		ns
44	$t_{v(SPCH-SOMI)M}$ Valid time, SPISOMI data valid after SPICLK high (polarity = 1)	0		ns

NOTE 12: t_c = system-clock cycle time = $1/\text{SYSCLK}$



NOTE A: The diagram is for polarity = 1. SPICLK is inverted when polarity = 0.

Figure 25. SPI Master External Timing

TMS370Cx2x

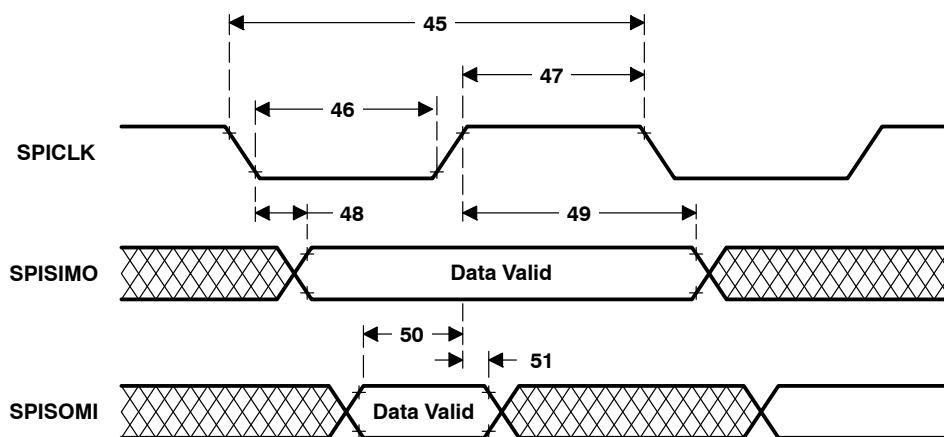
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SPI slave mode external timing characteristics and requirements (see Note 12 and Figure 26)

NO.		MIN	MAX	UNIT
45	$t_{c(SPC)}S$ Cycle time, SPICLK	$8t_c$		ns
46	$t_{w(SPCL)}S$ Pulse duration, SPICLK low	$4t_c - 45$	$0.5t_{c(SPC)}S + 45$	ns
47	$t_{w(SPCH)}S$ Pulse duration, SPICLK high	$4t_c - 45$	$0.5t_{c(SPC)}S + 45$	ns
48	$t_{d(SPCL-SOMI)}S$ Delay time, SPISOMI valid after SPICLK low (polarity = 1)		$3.25t_c + 130$	ns
49	$t_{v(SPCH-SOMI)}S$ Valid time, SPISOMI data valid after SPICLK high (polarity = 1)	$t_{w(SPCH)}S$		ns
50	$t_{su(SIMO-SPCH)}S$ Setup time, SPISIMO to SPICLK high (polarity = 1)	0		ns
51	$t_{v(SPCH-SIMO)}S$ Valid time, SPISIMO data after SPICLK high (polarity = 1)	$3t_c + 100$		ns

NOTE 12: t_c = system-clock cycle time = 1 / SYSCLK



NOTE A: The diagram is for polarity = 1. SPICLK is inverted when polarity = 0.

Figure 26. SPI Slave External Timing

SCI1 isosynchronous[†] mode timing characteristics and requirements for internal clock (see Note 12 and Figure 27)

NO.		MIN	MAX	UNIT
24	$t_c(\text{SCC})$ Cycle time, SCICLK	$2t_c$	$131\,072t_c$	ns
25	$t_w(\text{SCCL})$ Pulse duration, SCICLK low	$t_c - 45$	$0.5t_c(\text{SCC}) + 45$	ns
26	$t_w(\text{SCCH})$ Pulse duration, SCICLK high	$t_c - 45$	$0.5t_c(\text{SCC}) + 45$	ns
27	$t_d(\text{SCCL-TXDV})$ Delay time, SCITXD valid after SCICLK low	- 50	60	ns
28	$t_v(\text{SCCH-TXD})$ Valid time, SCITXD data valid after SCICLK high	$t_w(\text{SCCH}) - 50$		ns
29	$t_{su}(\text{RXD-SCCH})$ Setup time, SCIRXD to SCICLK high	$0.25 t_c + 145$		ns
30	$t_v(\text{SCCH-RXD})$ Valid time, SCIRXD data valid after SCICLK high	0		ns

NOTE 12: t_c = system-clock cycle time = $1/\text{SYSCLK}$

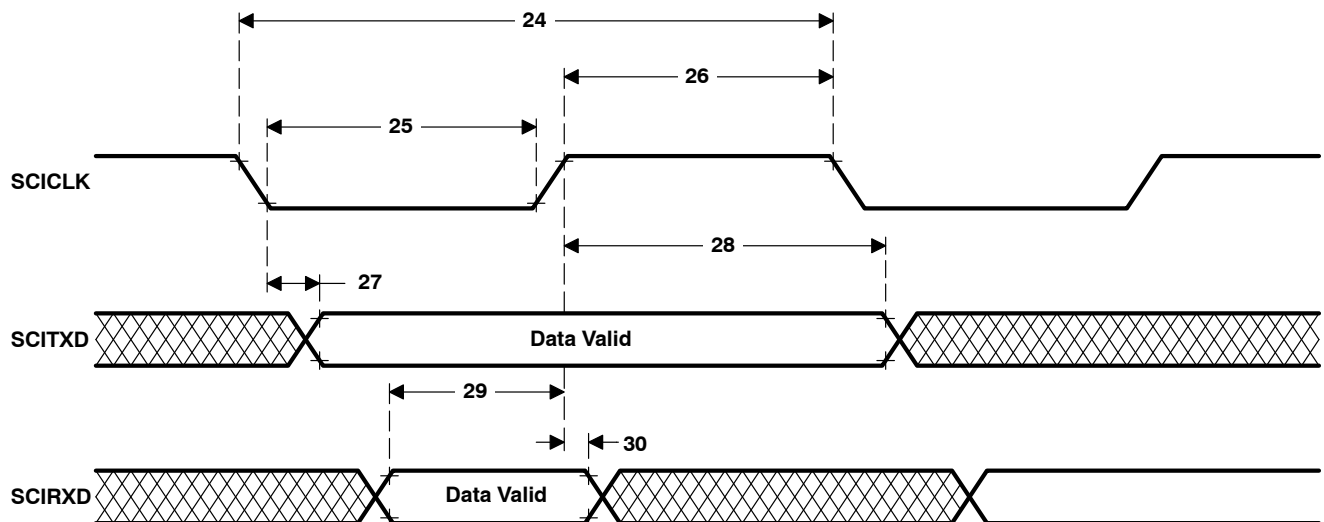


Figure 27. SCI1 Isosynchronous Mode Timing for Internal Clock

[†] Isosynchronous = Isochronous

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SCI1 isosynchronous[†] mode timing characteristics and requirements for external clock (see Note 12 and Figure 28)

NO.		MIN	MAX	UNIT
31	$t_{c(SCC)}$ Cycle time, SCICLK	$10t_c$		ns
32	$t_w(SCCL)$ Pulse duration, SCICLK low	$4.25t_c + 120$		ns
33	$t_w(SCCH)$ Pulse duration, SCICLK high	$t_c + 120$		ns
34	$t_d(SCCL-TXDV)$ Delay time, SCITXD valid after SCICLK low		$4.25t_c + 145$	ns
35	$t_v(SCCH-TXD)$ Valid time, SCITXD data valid after SCICLK high	$t_w(SCCH)$		ns
36	$t_{su}(RXD-SCCH)$ Setup time, SCIRXD to SCICLK high	40		ns
37	$t_v(SCCH-RXD)$ Valid time, SCIRXD data after SCICLK high	$2t_c$		ns

NOTE 12: t_c = system-clock cycle time = 1 / SYSCLK

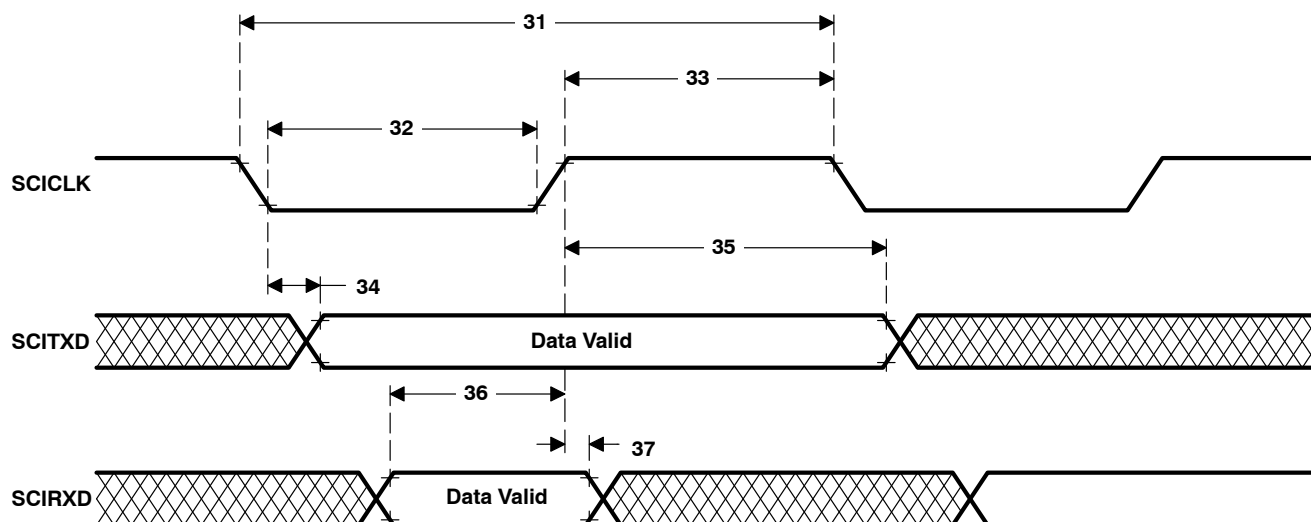


Figure 28. SCI1 Isosynchronous[†] Timing for External Clock

[†] Isosynchronous = Isochronous

Table 20 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

Table 20. TMS370Cx2x Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 44 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C020AFNA TMS370C020AFNL TMS370C020AFNT TMS370C022AFNA TMS370C022AFNL TMS370C022AFNT TMS370C320AFNA TMS370C320AFNL TMS370C320AFNT TMS370C322AFNA TMS370C322AFNL TMS370C322AFNT TMS370C722FNT
FZ – 44 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C722FZT
JD – 40 pin (100-mil pin spacing)	CERAMIC DUAL-IN-LINE PACKAGE (CDIP)	JD(R-CDIP-T**) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE	SE370C722JDT
N – 40 pin (100-mil pin spacing)	PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	N(R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE	TMS370C020ANA TMS370C020ANL TMS370C020ANT TMS370C022ANA TMS370C022ANL TMS370C022ANT TMS370C320ANA TMS370C320ANL TMS370C320ANT TMS370C322ANA TMS370C322ANL TMS370C322ANT TMS370C722NT
JC – 40 pin (70-mil pin spacing)	CERAMIC SHRINK DUAL-IN-LINE PACKAGE (CSDIP)	JC(R-CDIP-T40) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE	SE370C722JCT
NJ – 40 pin (70-mil pin spacing) [†]	PLASTIC SHRINK DUAL-IN-LINE PACKAGE (PSDIP)	NJ(R-PDIP-T**) PLASTIC SHRINK DUAL-IN-LINE PACKAGE	TMS370C020ANJA TMS370C020ANJL TMS370C020ANJT TMS370C022ANJA TMS370C022ANJL TMS370C022ANJT TMS370C320ANJA TMS370C320ANJL TMS370C320ANJT TMS370C322ANJA TMS370C322ANJL TMS370C322ANJT TMS370C722NJT

[†] NJ formerly known as N2; the mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

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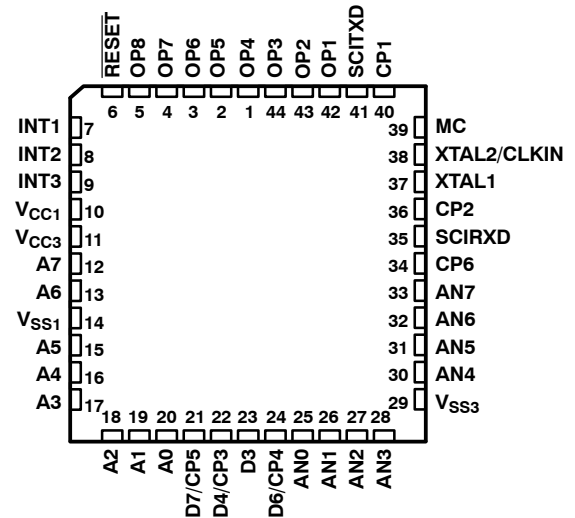
7

TMS3700Cx32 Data Sheet



- **CMOS/EEPROM/EPROM Technologies on a Single Device**
 - Mask-ROM Devices for High-Volume Production
 - One-Time-Programmable (OTP) EPROM Devices for Low-Volume Production
 - Reprogrammable-EPROM Devices for Prototyping Purposes
- **Internal System Memory Configurations**
 - On-Chip Program Memory Versions
 - ROM: 8K Bytes
 - EPROM: 8K Bytes
 - Data EEPROM: 256 Bytes
 - Static RAM: 256 Bytes Usable as Registers
- **Flexible Operating Features**
 - Low-Power Modes: STANDBY and HALT
 - Commercial, Industrial, and Automotive Temperature Ranges
 - Clock Options
 - Divide-by-1 (2 MHz–5 MHz SYSCLK)
 - Phase-Locked Loop (PLL)
 - Divide-by-4 (0.5 MHz–5 MHz SYSCLK)
 - Supply Voltage (V_{CC}) 5 V $\pm$ 10%
- **Programmable Acquisition and Control Timer (PACT) Module**
 - Input Capture on up to Six Pins, Four of Which Can Have a Programmable Prescaler
 - One Input Capture Pin Can Drive an 8-Bit Event Counter
 - Up to Eight Timer-Driven Outputs
 - Interaction Between Event Counter and Timer Activity
 - 18 Independent Interrupt Vectors
 - Watchdog With Selectable Time-Out Period
 - Asynchronous Mini Serial Communication Interface (Mini SCI)
- **Flexible Interrupt Handling**
 - Two Software-Programmable Interrupt Levels
 - Global- and Individual-Interrupt Masking
 - Programmable Rising- or Falling-Edge Detect
 - Individual-Interrupt Vectors

FZ AND FN PACKAGES
(TOP VIEW)



- **Eight-Channel 8-Bit Analog-to-Digital Converter 1 (ADC1)**
- **TMS370 Series Compatibility**
 - Register-to-Register Architecture
 - 256 General-Purpose Registers
 - 14 Powerful Addressing Modes
 - Instructions Upwardly Compatible With All TMS370 Devices
- **CMOS/TTL Compatible I/O Pins/Packages**
 - All Peripheral Function Pins Software Configurable for Digital I/O
 - 14 Bidirectional Pins, Nine Input Pins
 - 44-Pin Plastic and Ceramic Leaded Chip Carrier (LCC) Packages
- **Workstation/PC-Based Development System**
 - C Compiler and C Source Debugger
 - Real-Time In-Circuit Emulation
 - Multi-Window User Interface
 - Microcontroller Programmer
 - Extensive breakpoint/Trace Capability



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
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TMS370Cx32

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Pin Descriptions

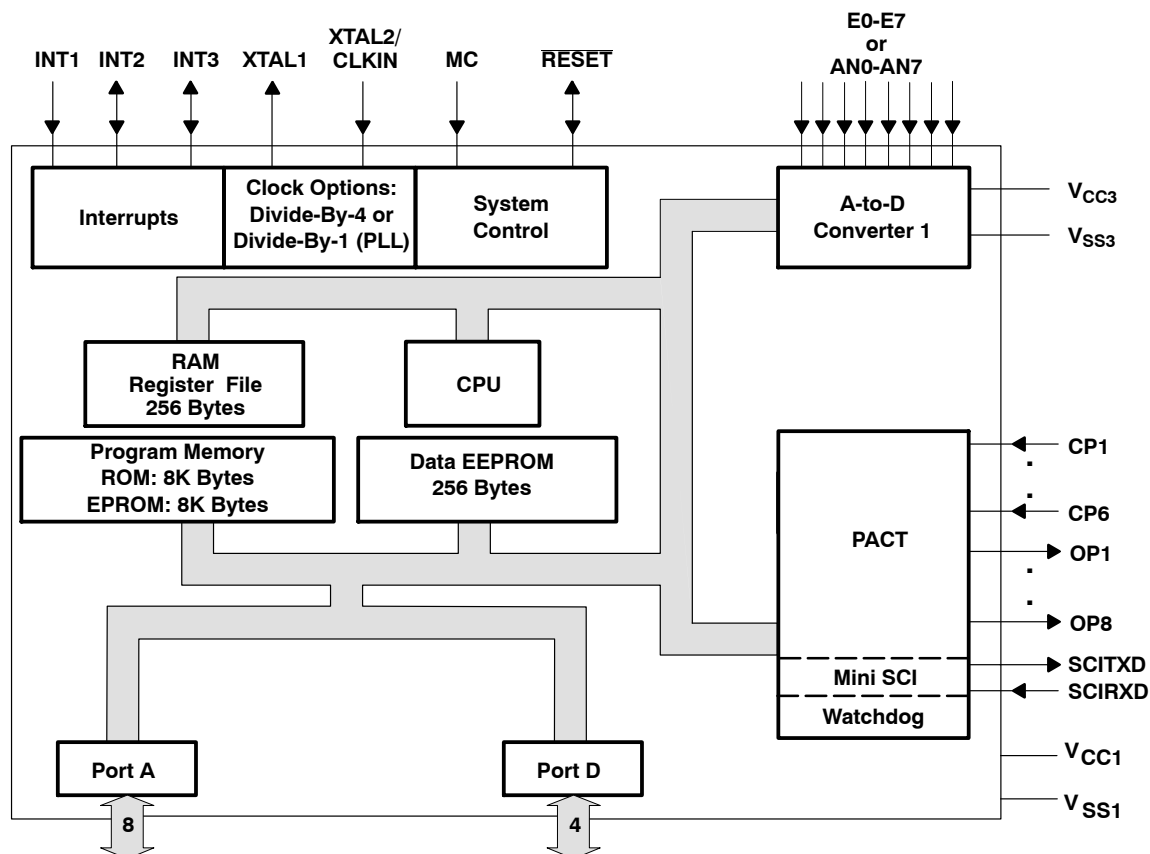
44 PINS		I/O†	DESCRIPTION
NAME	NO.		
A0 A1 A2 A3 A4 A5 A6 A7	20 19 18 17 16 15 13 12	I / O	Port A is a general-purpose bidirectional I/O port.
D3 D4/CP3 D6/CP4 D7/CP5	23 22 24 21	I / O	Port D is a general-purpose bidirectional port. Also configurable as SYSCLK (see Note 1) PACT input capture 3 (see Note 2) PACT input capture 4 (see Note 2) PACT input capture 5 (see Note 2)
CP1 CP2 CP6	40 36 34	I	PACT Input capture pin 1 PACT Input capture pin 2 PACT Input capture pin 3
AN0/E0 AN1/E1 AN2/E2 AN3/E3 AN4/E4 AN5/E5 AN6/E6 AN7/E7	25 26 27 28 30 31 32 33	I	ADC1 analog input pins (AN0 – AN7)/port E digital input pins (E0 – E7) Port E can be programmed individually as a general-purpose digital input pin if it is not used as ADC1 analog input or positive reference input.
INT1 INT2 INT3	7 8 9	I I/O I/O	External interrupt (non-maskable or maskable)/general-purpose input pin External maskable interrupt input/general purpose bidirectional pin External maskable interrupt input/general purpose bidirectional pin
OP1 OP2 OP3 OP4 OP5 OP6 OP7 OP8	42 43 44 1 2 3 4 5	O	PACT output pin 1 PACT output pin 2 PACT output pin 3 PACT output pin 4 PACT output pin 5 PACT output pin 6 PACT output pin 7 PACT output pin 8
SCIRXD SCITXD	35 41	I O	PACT mini SCI data receive input pin PACT mini SCI data transmit output pin
RESET	6	I / O	System reset bidirectional pin; as input pin, $\overline{\text{RESET}}$ initializes the microcontroller; as open-drain output, $\overline{\text{RESET}}$ indicates that an internal failure was detected by watchdog or oscillator fault circuit.
MC	39	I	Mode control input pin; enables EEPROM write protection override (WPO) mode, also EPROM V_{PP}
XTAL2/CLKIN XTAL1	38 37	I O	Internal oscillator crystal input/External clock source input Internal oscillator output for crystal
V_{CC1} V_{SS1} V_{CC3} V_{SS3}	10 14 11 29		Positive supply voltage for digital logic and digital I/O pins Ground reference for digital logic and digital I/O pins ADC1 positive supply voltage and optional positive reference input ADC1 ground supply and low reference input pin

† I = input, O = output

- NOTES:
1. D3 can be configured as SYSCLK by appropriately programming the DPORT1 and DPORT2 registers.
 2. These digital I/O buffers are connected internally to some of the PACT module's input capture pins. This allows the microcontroller to read the level on the input capture pin, or if the port D pin is configured as an output, to generate a capture. Be careful to leave the port D pin configured as an input if the corresponding input capture pin is being driven by external circuitry.



functional block diagram



description

The TMS370C032A, TMS370C332A, TMS370C732A, and SE370C732A devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx32 refers to these devices. The TMS370 family provides cost-effective real-time system control through integration of advanced peripheral-function modules and various on-chip memory configurations.

The TMS370Cx32 family of devices is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technologies. Low-operating power, wide-operating temperature range, and noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx32 devices attractive for system designs for automotive electronics, industrial motors, computer peripheral controls, telecommunications, and consumer applications.

All TMS370Cx32 devices contain the following on-chip peripheral modules:

- Programmable acquisition and control timer (PACT)
 - Asynchronous mini SCI
 - PACT watchdog timer
- Eight channel, 8-bit analog-to-digital converter 1 (ADC1)

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description (continued)

Table 1 provides a memory configuration overview of the TMS370Cx32 devices.

Table 1. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		44 PIN PACKAGES
	ROM	EPROM	RAM	EEPROM	
TMS370C032A	8K	—	256	256	FN – PLCC
TMS370C332A	8k	—	256	—	FN – PLCC
TMS370C732A	—	8K	256	256	FN – PLCC
SE370C732A [†]	—	8K	256	256	FZ – CLCC

[†] System evaluators and development are for use only in prototype environment, and their reliability has not been characterized.

The suffix letter (A) appended to the device names shown in the device column of Table 1 indicates the configuration of the device. ROM or EPROM devices have different configurations as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 2. Suffix Letter Configuration

DEVICE [†]	CLOCK	LOW-POWER MODE
EPROM A	Divide-by-4 (Standard oscillator)	Enabled
ROM A	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled

[†] Refer to the “device numbering conventions” section for device nomenclature and to the “device part numbers” section for ordering.

The 8K bytes of mask-programmable ROM in the associated TMS370Cx32 devices are replaced in the TMS370C732A with 8K bytes of EPROM. All other available memory and on-chip peripherals are identical except for the TMS370C332A which does not have EEPROM memory. The OTP (TMS370C732A) and reprogrammable (SE370C732A) devices are available.

The TMS370C732A OTP device is available in a plastic package. This microcontroller is effective to use for immediate production updates for other members of the TMS370Cx32 family or for low-volume production runs when the mask charge or cycle time for the low-cost mask ROM devices is not practical.

The SE370C732A has a windowed ceramic package to allow reprogramming of the program EPROM memory during the development/prototyping phase of design. The SE370C732A device allows quick updates to breadboards and prototype systems while iterating initial designs.

The TMS370Cx32 family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all CPU activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator, the PACT counter, and PACT's first command/definition entry remain active. This allows the PACT module to bring the device out of STANDBY mode. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx32 features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx32 family is fully instruction-set-compatible, providing easy transition between members of the TMS370 8-bit microcontroller family.

The TMS370Cx32 has a PACT module that acts as a timer coprocessor by gathering timing information on input signals and controlling output signals with little or no intervention by the CPU. The coprocessor nature of this module allows for levels of flexibility and power not found in traditional microcontroller timers.



description (continued)

The TMS370Cx32 family provides the system designer with an economical, efficient solution to real-time control applications. The PACT compact development tool (CDT™) solves the challenge of efficiently developing the software and hardware required to design the TMS370Cx32 into an ever-increasing number of complex applications. The application source code can be written in assembly and C language, and the output code can be generated by the linker. Precise real-time, in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as a reduced time-to-market cycle.

The TMS370Cx32 family together with the TMS370 PACT CDT370, BP programmer, starter kit, software tools, the SE370C732A reprogrammable devices, comprehensive product documentation, and customer support provide a complete solution to the needs of the system designer.

central processing unit (CPU)

The CPU on the TMS370Cx32 device is the high-performance 8-bit TMS370 CPU module. The 'x32 implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'x32 instruction map is shown in Table 15.

The '370Cx32 CPU architecture provides the following components:

CPU registers:

- A stack pointer (SP) that points to the last entry in the memory stack
- A status register (ST) that monitors the operation of the instructions and contains the global interrupt-enable bits
- A program counter (PC) that points to the memory location of the next instruction to be executed

A memory map that includes:

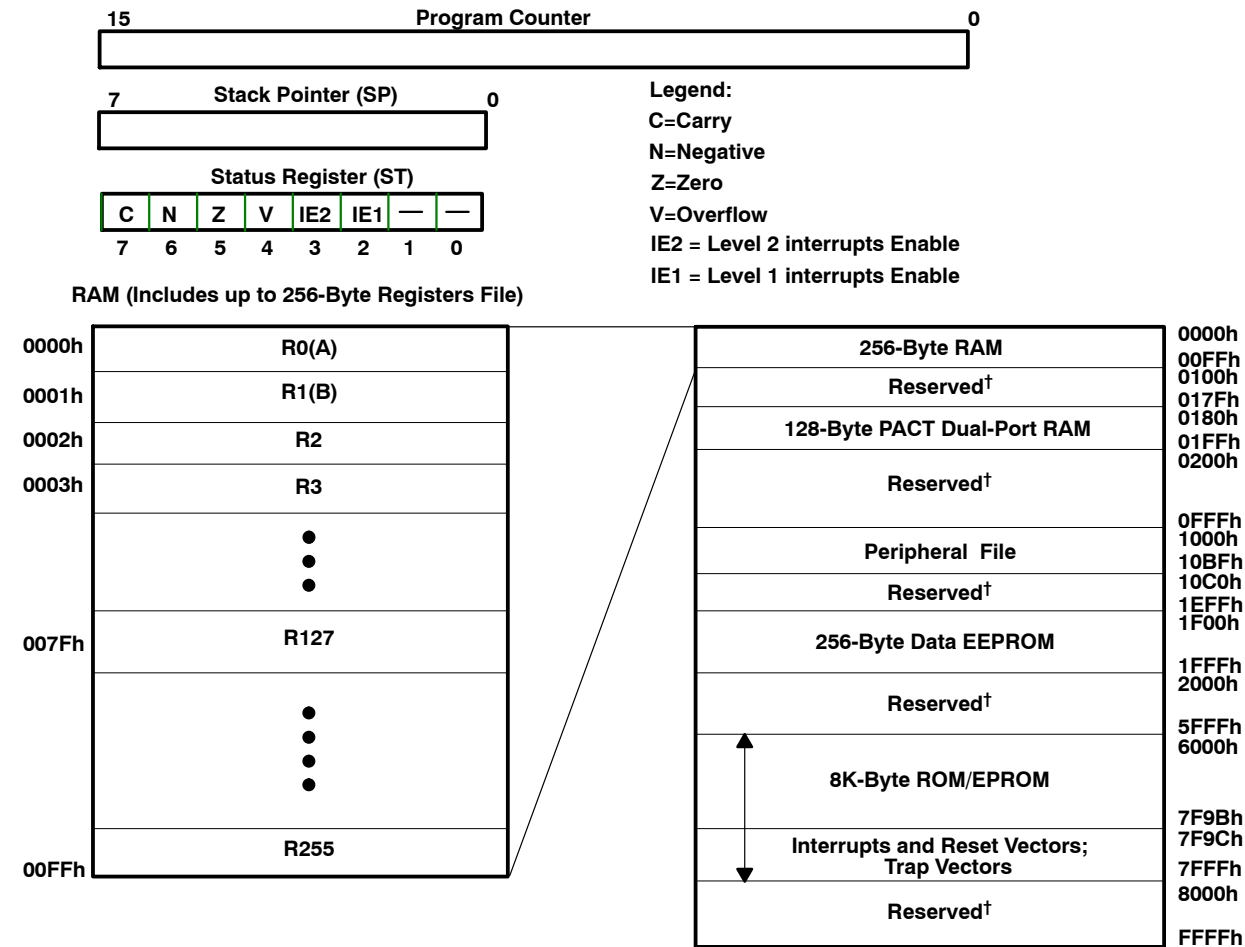
- 256-byte general-purpose RAM that can be used for data memory storage, program instructions, general purpose register, dual-port RAM, or the stack
- The upper 128-bytes of the register file is called dual-port RAM that contains the capture registers, the circular buffer, and a command/definition area.
- A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM/EPROM programming control
- 256-byte EEPROM module that provides in-circuit programmability and data retention in power-off conditions
- 8K-byte ROM or 8K-byte EPROM

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central processing unit (CPU) (continued)

Figure 1 Illustrates the CPU registers and memory blocks.



† Reserved means the address space is reserved for future expansion.

Figure 1. Programmer's Model

stack pointer (SP)

The SP is an 8-bit CPU register. Stack operates as a last-in, first-out, read/write memory. Typically, the stack is used to store the return address on subroutine calls as well as the ST contents during interrupt sequences.

The SP points to the last entry or top of the stack. The SP is incremented automatically before data is pushed onto the stack and decremented after data is popped from the stack. The stack can be placed anywhere in the on-chip RAM.

status register (ST)

The ST monitors the operation of the instructions and contains the global interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits.

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional-jump instructions) use the status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

central processing unit (CPU) (continued)

The ST, status-bit notation, and status-bit definitions are shown in Table 3.

Table 3. Status Registers

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most significant byte (MSbyte) and least significant byte (LSbyte) of a 16-bit address.

During reset, the contents of the reset vector (7FFEh, 7FFFh) are loaded into the PC. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 6000h as the contents of the reset vector.

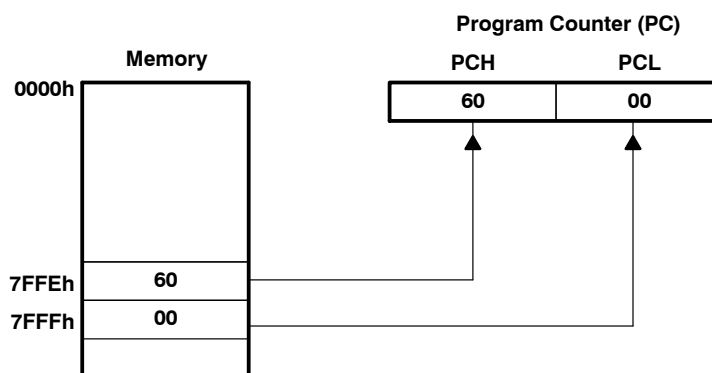


Figure 2. Program Counter After Reset

memory map

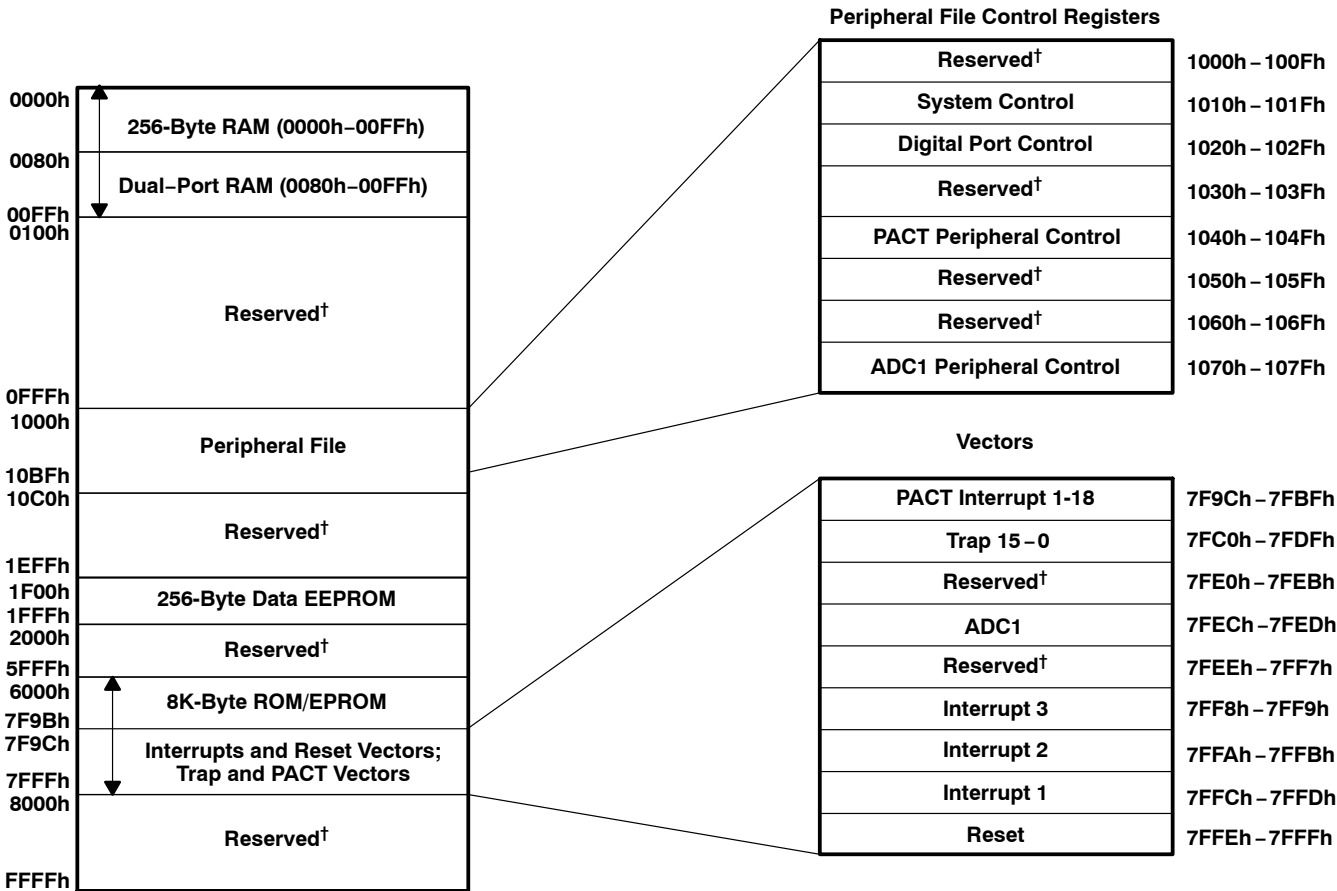
The TMS370Cx32 architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. As shown in Figure 3, the TMS370Cx32 provides memory-mapped RAM, ROM, EPROM, data EEPROM, I/O pins, peripheral functions, and system-interrupt vectors.

The peripheral file contains all I/O port control, peripheral status and control, EEPROM, EPROM, and system-wide control functions. The peripheral file is located between 1000h to 107Fh and is divided logically into eight peripheral file frames of 16 bytes each. The eight PF frames consist of five control frames and three reserved frames. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed.

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central processing unit (CPU) (continued)



† Reserved means that the address space is reserved for future expansion.

Figure 3. TMS370Cx32 Memory Map

RAM/register file (RF)

Locations within the RAM address space can serve as the RF, general-purpose read/write memory, program memory, or the stack instructions. The TMS370Cx32 devices contain 256 bytes of internal RAM, memory-mapped beginning at location 0000h (R0) and continuing through location 00FFh (R255) which is shown in Figure 1.

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

dual-port RAM

The upper 128 bytes of the register files (0080h – 00FFh) can be used by the PACT module to contain commands and definitions as well as timer values. Any RAM not used by PACT can be used as additional CPU register or as general-purpose memory.

peripheral file (PF)

The TMS370Cx32 control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or P for a decimal designator. For example, the system-control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 4 shows the TMS370Cx32 PF address map.

Table 4. TMS370Cx32 Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h – 100Fh	P000 – P00F	Reserved
1010h – 101Fh	P010 – P01F	System and EPROM/EEPROM control registers
1020h – 102Fh	P020 – P02F	Digital I/O port control registers
1030h – 103Fh	P030 – P03F	Reserved
1040h – 104Fh	P040 – P04F	PACT registers
1050h – 106Fh	P050 – P06F	Reserved
1070h – 107Fh	P070 – P07F	Analog-to-digital converter 1 registers
1080h – 10FFh	P080 – P0FF	Reserved

data EEPROM

The TMS370Cx32 devices, containing 256 bytes of data EEPROM, have a memory that is mapped beginning at location 1F00h and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B). The data EEPROM features include the following:

- Programming:
 - Bit-, byte-, and block-write/erase modes
 - Internal charge pump circuitry. No external EEPROM programming voltage supply is needed.
 - Control register: Data EEPROM programming is controlled by the DEECTL located in the PF frame beginning at location P01A. See Table 5.
 - In-circuit programming capability. There is no need to remove the device to program it.
- Write protection. Writes to the data EEPROM are disabled during the following conditions.
 - Reset. All programming of the data EEPROM module is halted.
 - Write protection active. There is one write-protect bit per 32-byte EEPROM block.
 - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 5. Data EEPROM and PROGRAM EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME
P01A	DEECTL	Data EEPROM Control Register
P01B	—	Reserved
P01C	EPCTLL	Program EPROM Control Register – Low Array

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program EPROM[†]

The TMS370C732 device contains 8K bytes of EPROM mapped, beginning at location 6000h and continuing through location 7FFFh as shown in Figure 3. Reading the program EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the EPROM control register (EPCTLL). The program EPROM module features include:

- Programming
 - In-circuit programming capability if V_{PP} is applied to MC
 - Control register: EPROM programming is controlled by the EPROM control register (EPCTLL) located in the peripheral file (PF) frame at location P01C as shown in Table 5.
- Write protection: Writes to the program EPROM are disabled under the following conditions:
 - Reset: All programming to the EPROM module is halted
 - Low-power modes
 - 13 V not applied to MC

program ROM[†]

The program ROM consists of 8K bytes of mask programmable read-only memory. The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication. Refer to Figure 3 for ROM memory map.

system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx32 CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are generated internally, while one (RESET pin) is controlled externally. These actions are as follows:

- PACT watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside of the recommended operating range. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.
- External RESET pin. A low level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.

Once a reset source is activated, the external RESET pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x32 device to reset external system components. Additionally, if a cold start condition (V_{CC} is off for several hundred milliseconds) or oscillator failure occurs or the RESET pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator-fault flag (OSC FLT FLAG, SCCR0.4) and the cold-start flag (COLD START, SCCR0.7) to determine the source of the reset. A reset does not clear these flags. Table 6 depicts the reset sources. If none of the sources indicated in Table 1 caused the reset, then the RESET pin was pulled low by the external hardware or the PACT module's watchdog.

[†] Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments, and 7FECb through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions are located between addresses 7FC0h and 7FDFh. PACT interrupts are located between addresses 7F9Ch and 7FBFh.

system reset (continued)

Table 6. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Registers A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

When an external reset circuit is connected to the $\overline{\text{RESET}}$ pin, the pin must be held low until the clock signal is valid and V_{CC} is within the operating range. Figure 4 shows a typical reset circuit.

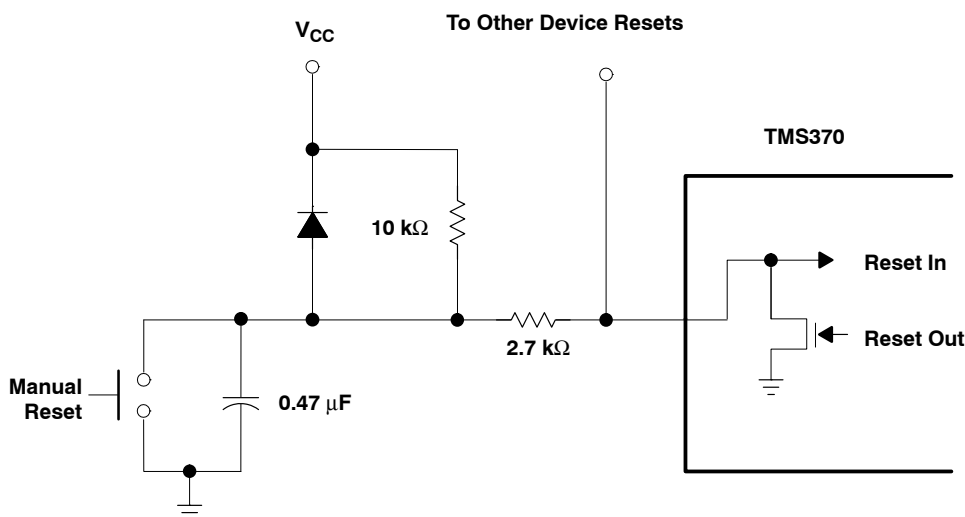


Figure 4. Typical Reset Circuit

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interrupts

The TMS370 family software-programmable interrupt structure permits flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global interrupt mask bits (IE1 and IE2) of the ST.

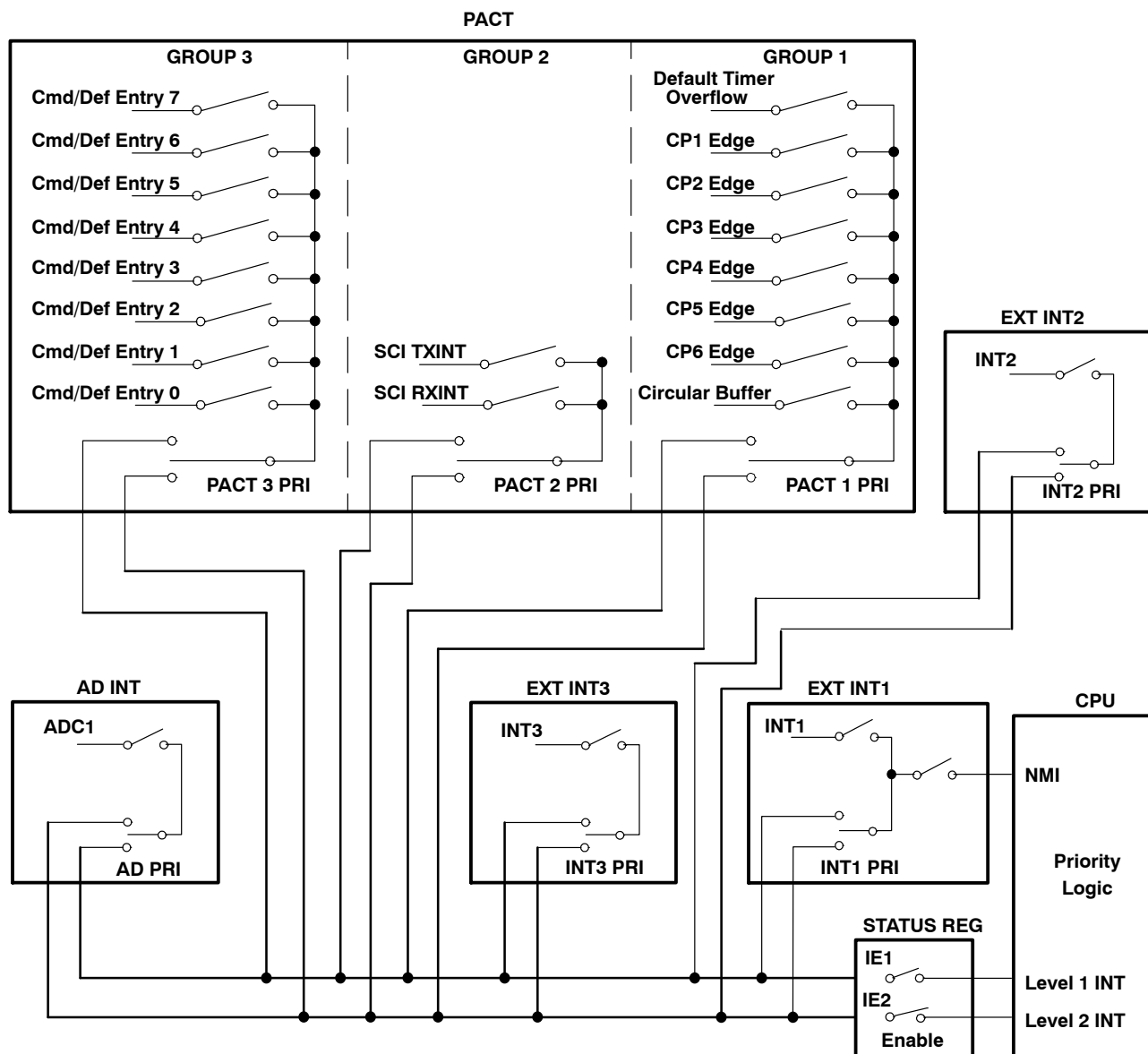


Figure 5. Interrupt Control

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is selectively configured on either the high- or low-priority-interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority

interrupts (continued)

chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx32 has 22 hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 7. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. A system interrupt may have multiple interrupt sources. All the interrupt sources are individually maskable by local interrupt enable control bits in the associated peripheral file. Each interrupt source FLAG bit is individually readable for software polling or for determining which interrupt source generated the associated system interrupt.

Nineteen of the system interrupts are generated by on-chip peripheral functions, and three external interrupts are supported. Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in peripheral file frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual- or global-enable mask bits. The INT1 NMI bit is protected during non-privileged operation and, therefore, should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software configured as general-purpose input/output pins if the interrupt function is not required (INT1 can be similarly configured as an input pin).

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interrupts (continued)

Table 7. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	OSC FLT FLG	SYSTEM INTERRUPT	VECTOR ADDRESS	MODULE PRIORITY [†]	PRIORITY IN GROUP
RESET	External RESET Watchdog Overflow Oscillator Fault	COLD START (No Flag) OSC FLT FLAG	RESET [‡]	7FEEh, 7FFFh	1	1
INT1	External Interrupt 1	INT1 FLAG	INT1 [‡]	7FFCh, 7FFDh	2	1
INT2	External Interrupt 2	INT2 FLAG	INT2 [‡]	7FFAh, 7FFBh	3	1
INT3	External Interrupt 3	INT3 FLAG	INT3 [‡]	7FF8h, 7FF9h	4	1
PACT (Group 1)	PACT Circular Buffer	Buffer Half/Full Interrupt Flag	BUFINT	7FB0h, 7FB1h	5	1
	PACT CP6 Event	CP6 INT FLAG	CP6INT	7FB2h, 7FB3h		2
	PACT CP5 Event	CP5 INT FLAG	CP5INT	7FB4h, 7FB5h		3
	PACT CP4 Event	CP4 INT FLAG	CP4INT	7FB6h, 7FB7h		4
	PACT CP3 Event	CP3 INT FLAG	CP3INT	7FB8h, 7FB9h		5
	PACT CP2 Event	CP2 INT FLAG	CP2INT	7FBAh, 7FBBh		6
	PACT CP1 Event	CP1 INT FLAG	CP1INT	7FBCh, 7FBDh		7
	Default Timer Overflow	DEFTIM OVRFL INT FLAG	POVRL INT	7FBEh, 7FBFh		8
PACT (Group 2)	PACT SCI Rx Int	PACT RX RDY	PRXINT	7F9Eh, 7F9Fh	6	1
	PACT SCI Tx Int	PACT TX RDY	PTXINT	7F9Ch, 7F9Dh		2
PACT (Group 3)	PACT Cmd/Def Entry 0	CMD/DEF INT 0 FLAG	CDINT 0	7FA0h, 7FA1h	7	1
	PACT Cmd/Def Entry 1	CMD/DEF INT 1 FLAG	CDINT 1	7FA2h, 7FA3h		2
	PACT Cmd/Def Entry 2	CMD/DEF INT 2 FLAG	CDINT 2	7FA4h, 7FA5h		3
	PACT Cmd/Def Entry 3	CMD/DEF INT 3 FLAG	CDINT 3	7FA6h, 7FA7h		4
	PACT Cmd/Def Entry 4	CMD/DEF INT 4 FLAG	CDINT 4	7FA8h, 7FA9h		5
	PACT Cmd/Def Entry 5	CMD/DEF INT 5 FLAG	CDINT 5	7FAAh, 7FABh		6
	PACT Cmd/Def Entry 6	CMD/DEF INT 6 FLAG	CDINT 6	7FACH, 7FADh		7
	PACT Cmd/Def Entry 7	CMD/DEF INT 7 FLAG	CDINT 7	7FAEh, 7FAFh		8
ADC1	ADC1 Conversion Complete	AD INT FLAG	ADINT	7FECh, 7FEDh	8	1

[†] Relative priority within an interrupt level

[‡] Release microcontroller from STANDBY and HALT low-power modes

privileged operation and EEPROM write protection override

The TMS370Cx32 family is designed with significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx32 operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) is set to 1 to enter the nonprivileged mode, disabling write operations to specific configuration-control bits within the PF. Table 8 displays the system-configuration bits which are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

privileged operation and EEPROM write protection override (continued)

Table 8. Privilege Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCRO	P010.5 P010.6	PF AUTO WAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
PACTSCR	P040.0 P040.1 P040.2 P040.3 P040.4	PACT PRESCALE SELECT 0 PACT PRESCALE SELECT 1 PACT PRESCALE SELECT 2 PACT PRESCALE SELECT 3 FAST MODE SELECT
PACTPRI	P04F.0 P04F.1 P04F.2 P04F.3 P04F.4 P04F.5 P04F.7	PACT WD PRESCALE SELECT 0 PACT WD PRESCALE SELECT 1 PACT MODE SELECT PACT GROUP 3 PRIORITY PACT GROUP 2 PRIORITY PACT GROUP 1 PRIORITY PACT STEST
ADPRI	P07F.5 P07F.6 P07F.7	AD ESPEN AD PRIORITY AD STEST

† The privilege bits are shown in a bold typeface in the peripheral file frame 1 section.

low-power and IDLE modes

The TMS370Cx32 devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time when the mask is manufactured.

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls the low-power mode selection.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, the PACT counter, and the first PACT command entry remain active in all modules. System processing is suspended until a qualified interrupt (hardware RESET or external interrupt on INT1, INT2, or INT3) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx32 is placed in its lowest power consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware RESET or external interrupt on the INT1, INT2, or INT3) is detected. The power-down mode-selection bits are summarized in Table 9.

low-power and IDLE modes (continued)

Table 9. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X [†]	IDLE

[†] X = don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6-7 bits is ignored. In addition, if an IDLE instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method for always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI is generated always, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (SP, PC, and ST), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the WD timer is inhibited.

clock modules

The 'x32 family provides two clock options that are referred to as divide-by-1 (phase-locked loop) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The 'x32 masked-ROM devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device. The '732A EPROM has only the divide-by-4.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a one-to-one match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency, whereas the divide-by-4 produces a SYSCLK which is one-fourth the frequency of the external resonator. Inside the divide-by-1 module, the frequency of the external resonator is multiplied by four, and the clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. These are formulated as follows:

$$\text{Divide-by-4 option : } \text{SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option : } \text{SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the reduced EMI. The harmonics of low-speed resonators extend through fewer of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 provides the capability of reducing the resonator speed by four times, and this results in a steeper decay of emissions produced by the oscillator.

system configuration registers

Table 10, contains system-configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in a bold typeface and shaded areas.

Table 10. Peripheral File Frame 1: System-Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTO WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D to P01F	Reserved								

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digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 11 shows the specific addresses, registers, and control bits within this peripheral file frame. Table 12 shows the port configuration register setup.

Table 11. Peripheral File Frame 2: Digital Port-Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)	—		Port D Control Register 1 (must be 0)	—	—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0) [†]	—		Port D Control Register 2 (must be 0) [†]	—	—	—	—	DPORT2
P02E	Port D Data	—		Port D Data	—	—	—	—	DDATA
P02F	Port D Direction	—		Port D Direction	—	—	—	—	DDIR

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 12. Port Configuration Register Setup

PORT	PIN	abcd 00q1	abcd 00y0
A	0 – 7	Data out q	Data In y
D	3, 4, 6, 7	Data out q	Data In y
a = Port x Control Register 1 b = Port x Control Register 2 c = Data d = Direction			

programmable acquisition and control timer (PACT) module

Traditionally, timers in microcontrollers provide limited capture and compare functions consuming significant CPU processing power, leading to inaccurate timings due to interrupt latencies. The programmable acquisition and control timer (PACT8) acts as a coprocessor combining configurable capture and compare features, within a flexible dual-port RAM, able to run real-time tasks with little or no CPU intervention. The PACT structure allows concatenation of tasks, thus enabling the CPU to perform data manipulation while the PACT module both captures and outputs real-time-related information. Since all the PACT control information is held within the dual-port RAM, the CPU can access these parameters quickly.

To use the PACT, the user must set up three distinct areas of memory. The first is the dual-port RAM, which contains the capture area, the commands, and the timer definitions. The second is the peripheral frame. The third is an area near the end of the program memory which holds the interrupt vectors of PACT.



programmable acquisition and control timer (PACT) module (continued)

The PACT module features include the following:

- Input-capture functions on up to six input pins (CP1 to CP6), depending on the mode selected:
 - Mode A: CP1–2 are dedicated capture, CP3–6 are circular-buffer capture, and CP6 is an event pin.
 - Mode B: CP1–4 are dedicated capture, CP5–6 are circular-buffer capture, and CP6 is an event pin.
- Multiple timer-driven outputs on eight pins (OP1 to OP8)
 - Standard compare command: sets or clears an output pin whenever the timer/counter is equal to a certain value
 - Virtual timers: Enable variations of the PWM's period and provides periodic interrupts to the processor.
 - Double event-compare command: Comparisons of the 8-bit event counter with two event-compare values and the actions that can be performed are based on each value.
 - Event-compare 1 matching the event counter: sets or resets the selected output pin (OP1–OP8), generates interrupt, and generates a 32-bit capture into the circular buffer.
 - Event-compare 2 matching the event counter: sets or resets the selected output pin (OP1–OP8), generates interrupt, generates a 32-bit capture into the circular buffer, and resets the 20-bit default timer.
 - Offset timer definition-time from last event:
 - Generates an interrupt when the maximum event count is reached
 - Stores the 16-bit virtual timer in the circular buffer on each event
 - Stores the 20-bit default timer and 8-bit event counter in the circular buffer when the maximum event count is reached
 - Resets the 20-bit hardware default timer when the maximum event count is reached
 - Conditional-compare command has a timer-compare value and an event-compare value.
 - Generates an interrupt when the event-compare value equals the event counter and the timer-compare value equals the last defined timer
 - Sets or clears one of the seven output pins (OP1–OP7) when the event compare value equals the event counter and the timer-compare value equals the last defined timer
 - Baud rate timer definition: runs the mini-serial communications port built into the PACT module.
- Configurable timer overflow rates
- One 8-bit event counter driven by CP6
- Up to 20-bit timer capability
- Interaction between event counter and timer activity
- Register-based organization allowing direct access to timer parameters by the CPU
- 18 independent interrupt vectors with two priority levels
- Integrated, configurable watchdog with selectable time-out period

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programmable acquisition and control timer (PACT) module (continued)

- Mini-serial communications interface works as a simplified full duplex universal asynchronous receiver/transmitter (UART) with independent setup of baud rate for receive and transmit lines.

- Asynchronous communications mode

$$\text{Asynchronous Baud} = \frac{1}{(\text{Max Virtual Timer Value}) \times (4) \times (\text{PACT Resolution})} - 2$$

where PACT Resolution = SYSCLK × Prescale Value

PACT block diagram

The PACT module block diagram is illustrated in Figure 6.

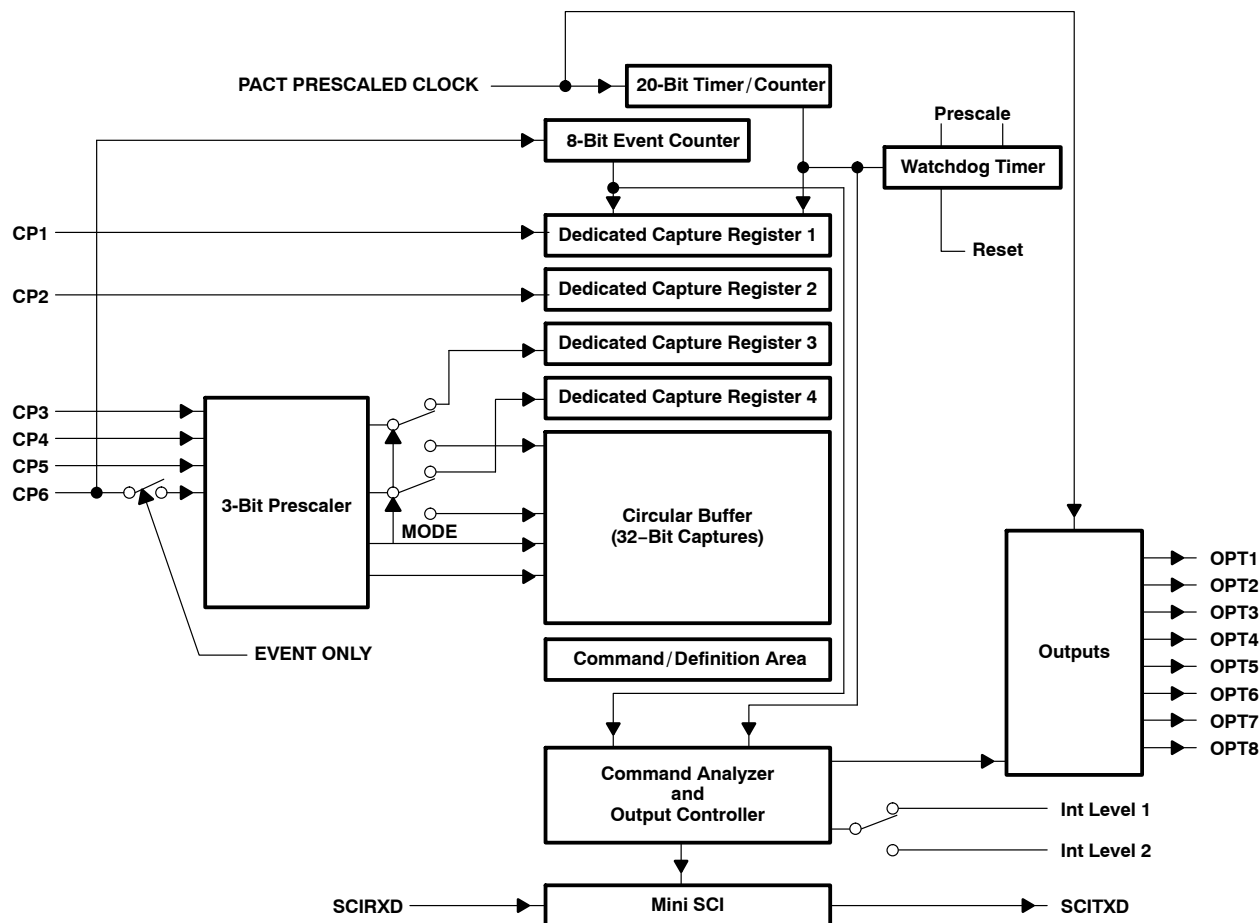


Figure 6. PACT Block diagram

PACT control registers

The PACT module is controlled and accessed through registers in peripheral frame 4. These registers are listed in Table 13. The bits in shaded boxes are privileged mode bits; that is, they can be written to only in the privileged mode.

Table 13. PACT Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P040	DEFTIM OVRFL INT ENA	DEFTIM OVRFL INT FLAG	CMD/DEF AREA ENA	FAST MODE SELECT	PACT PRESCALE SELECT3	PACT PRESCALE SELECT2	PACT PRESCALE SELECT1	PACT PRESCALE SELECT0	PACTSCR
P041	CMD/DEF AREA INT ENA	—	CMD/DEF AREA START BIT 5	CMD/DEF AREA START BIT 4	CMD/DEF AREA START BIT 3	CMD/DEF AREA START BIT 2	—	—	CDSTART
P042	—	CMD/DEF AREA END BIT 6	CMD/DEF AREA END BIT 5	CMD/DEF AREA END BIT 4	CMD/DEF AREA END BIT 3	CMD/DEF AREA END BIT 2	—	—	CDEND
P043	1	1	BUFFER POINTER BIT 5	BUFFER POINTER BIT 4	BUFFER POINTER BIT 3	BUFFER POINTER BIT 2	BUFFER POINTER BIT 1	—	BUFPTR
P044	Reserved								
P045	PACT RXRDY	PACT TXRDY	PACT PARITY	PACT FE	PACT SCI RX INT ENA	PACT SCI TX INT ENA	—	PACT SCI SW RESET	SCICTLP
P046	PACT RXDT7	PACT RXDT6	PACT RXDT5	PACT RXDT4	PACT RXDT3	PACT RXDT2	PACT RXDT1	PACT RXDT0	RXBUFP
P047	PACT TXDT7	PACT TXDT6	PACT TXDT5	PACT TXDT4	PACT TXDT3	PACT TXDT2	PACT TXDT1	PACT TXDT0	TXBUFP
P048	PACT OP8 STATE	PACT OP7 STATE	PACT OP6 STATE	PACT OP5 STATE	PACT OP4 STATE	PACT OP3 STATE	PACT OP2 STATE	PACT OP1 STATE	PSTATE
P049	CMD/DEF INT 7 FLAG	CMD/DEF INT 6 FLAG	CMD/DEF INT 5 FLAG	CMD/DEF INT 4 FLAG	CMD/DEF INT 3 FLAG	CMD/DEF INT 2 FLAG	CMD/DEF INT 1 FLAG	CMD/DEF INT 0 FLAG	CDFLAGS
P04A	CP2 INT ENA	CP2 INT FLAG	CP2 CAPT RISING EDGE	CP2 CAPT FALLING EDGE	CP1 INT ENA	CP1 INT FLAG	CP1 CAPT RISING EDGE	CP1 CAPT FALLING EDGE	CPCTL1
P04B	CP4 INT ENA	CP4 INT FLAG	CP4 CAPT RISING EDGE	CP4 CAPT FALLING EDGE	CP3 INT ENA	CP3 INT FLAG	CP3 CAPT RISING EDGE	CP3 CAPT FALLING EDGE	CPCTL2
P04C	CP6 INT ENA	CP6 INT FLAG	CP6 CAPT RISING EDGE	CP6 CAPT FALLING EDGE	CP5 INT ENA	CP5 INT FLAG	CP5 CAPT RISING EDGE	CP5 CAPT FALLING EDGE	CPCTL3
P04D	BUFFER HALF/FULL INT ENA	BUFFER HALF/FULL INT FLAG	INPUT CAPT PRESCALE SELECT 3	INPUT CAPT PRESCALE SELECT 2	INPUT CAPT PRESCALE SELECT 1	CP6 EVENT ONLY	EVENT COUNTER SW RESET	OP/ SET/CLR SELECT	CPPRE
P04E	WATCHDOG RESET KEY								WDRST
P04F	PACT STEST	PACT SUSPEND	PACT GROUP 1 PRIORITY	PACT GROUP 2 PRIORITY	PACT GROUP 3 PRIORITY	PACT MODE SELECT	PACT WD PRESCALE SELECT 1	PACT WD PRESCALE SELECT 0	PACTPRI

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analog-to-digital converter 1 module

The analog-to-digital converter 1 (ADC1) module is an 8-bit, successive approximation converter with internal sample-and-hold circuitry. The module has four multiplexed analog input channels that allow the processor to convert the voltage levels from up to eight different sources. The ADC1 module features include the following:

- Minimum conversion time: 32.8 μ s at 5 MHz SYSCLK
- Ten external pins:
 - Eight analog-input channels (AN0–AN7), any of which can be software-configured as digital inputs (E0–E7) when not needed as analog channels
 - AN1–AN7 also can be configured as positive-input voltage reference.
 - V_{CC3} : ADC1 module high-voltage reference input
 - V_{SS3} : ADC1 module low-voltage reference input
- The ADDATA register, which contains the digital result of the last ADC1 conversion.
- ADC1 operations can be accomplished through either interrupt-driven or polled algorithms.
- Six ADC1 module control registers located in the control-register frame beginning at address 1070h

The ADC1 module control registers are listed in Table 14.

Table 14. ADC1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A/D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI

analog-to-digital converter 1 module (continued)

The ADC1 module block diagram is illustrated in Figure 7.

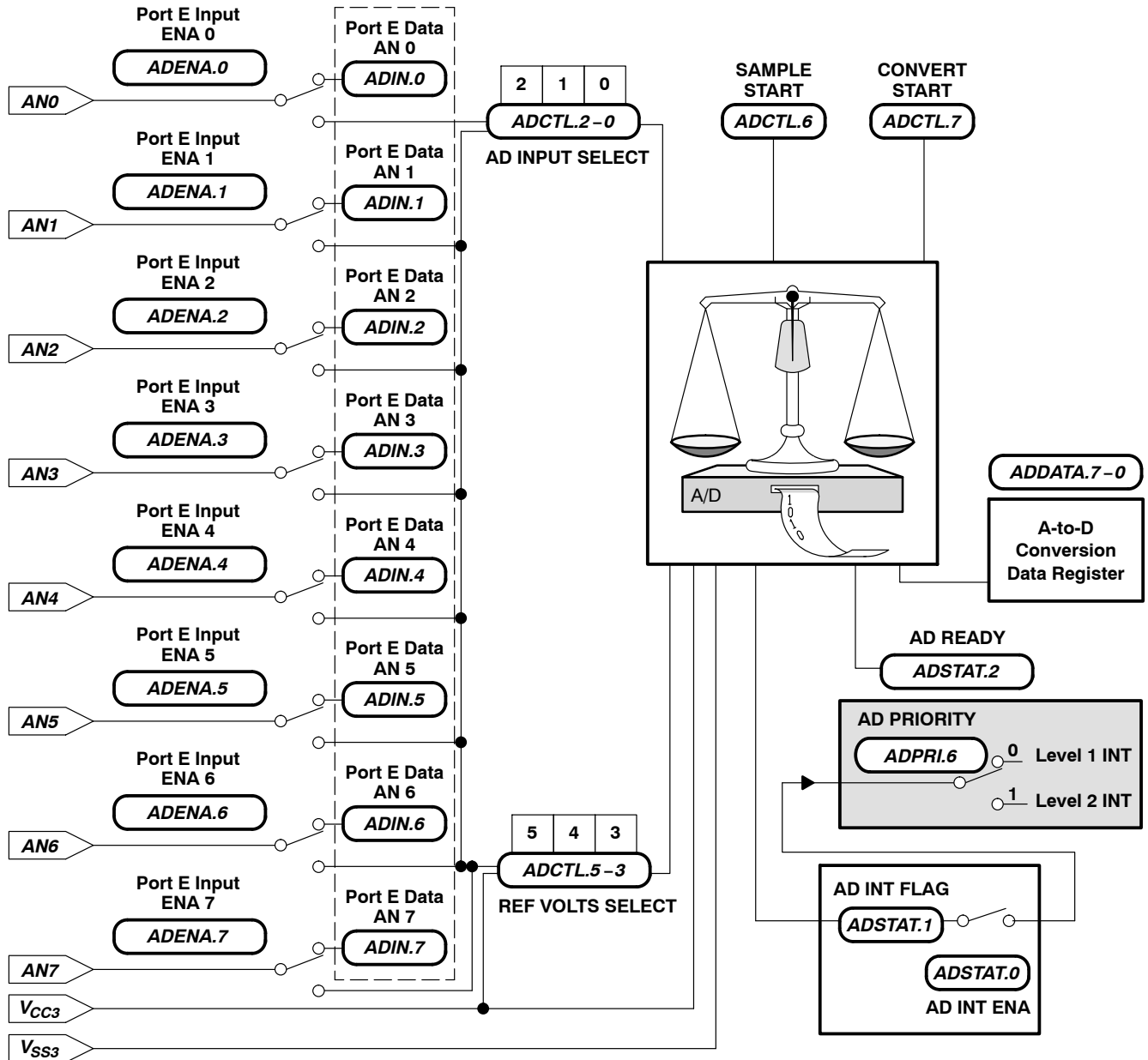


Figure 7. ADC1 Block Diagram

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instruction set overview

Table 15 provides an opcode to instruction cross reference of all 73 instructions and 274 opcodes of the '370Cx32 instruction set. The numbers at the top of this table represent the most significant nibble (MSN) of the opcode while the numbers at the left side of the table represent the least significant nibble (LSN). The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

Table 15. TMS370 Family Opcode/Instruction Map[†]

		MSN															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8				CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
1	JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7	
2	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8				MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7
3	JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8	
4	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes	
5	JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14		
6	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6	
7	JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10	
8	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7	
9	JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9	
A	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12	
B	JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8	

[†] All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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Table 15. TMS370 Family Opcode/Instruction Map[†] (Continued)

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L S N	C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
	D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
	E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
	F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7
Second byte of two-byte instructions (F4xx):														F4	8	MOVW *n[Rn] 4/15	DIV Rn,A 3/14-63
														F4	9	JMPL *n[Rn] 4/16	
														F4	A	MOV *n[Rn],A 4/17	
														F4	B	MOV A,*n[Rn] 4/16	
														F4	C	BR *n[Rn] 4/16	
														F4	D	CMP *n[Rn],A 4/18	
														F4	E	CALL *n[Rn] 4/20	
														F4	F	CALLR *n[Rn] 4/22	

Legend:

- * = Indirect addressing operand prefix
- & = Direct addressing operand prefix
- # = immediate operand
- #16 = immediate 16-bit number
- lab = 16-label
- n = immediate 8-bit number
- Pd = Peripheral register containing destination type
- Pn = Peripheral register
- Ps = Peripheral register containing source byte
- ra = Relative address
- Rd = Register containing destination type
- Rn = **Register file**
- Rp = Register pair
- Rpd = Destination register pair
- Rps = Source Register pair
- Rs = Register containing source byte

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

development system support

The TMS370 family development support tools include an assembler, a C-compiler, a linker, a starter kit, CDT and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
 - Includes extensive macro capability
 - Provides high-speed operation
 - Includes format conversion utilities for popular formats
- ANSI C Compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, SUN-3™ or SUN-4™)
 - Generate assembly code for the TMS370 that can be inspected easily
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables direct reference to the TMS370's port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (Compact Development Tool) PACT real-time in-circuit emulation
 - Base (Part Number EDSCDT37P – for PC, requires cable)
 - Cable for 44-pin PLCC (Part No. EDSTRG44PLCC32)
 - EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Includes compatibility to upload/download program and data memory
 - Execute programs and software routines
 - Includes 1024-sample trace buffer
 - Includes single-step executable instructions
 - Uses software breakpoints to halt program execution at selected address
- Microcontroller programmer
 - Base (Part No. TMDS3760500A – for PC, requires programmer head)
 - Single unit head for 44-pin PLCC (Part No. TMDS3780510A)
 - PC-based, window/function-key-oriented user interface for ease of use and rapid learning environment
- Starter Kit (Part No. TMDX37000 – For PC)
 - Includes TMS370 Assembler diskette and documentation
 - Includes TMS370 Simulator
 - Includes programming adapter board and programming software
 - Does not include – (to be supplied by the user):
 - + 5 V power supply
 - ZIF sockets
 - 9-pin RS-232 cable

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device numbering conventions

Figure 8 illustrates the numbering and symbol nomenclature for the TMS370CX32 family.

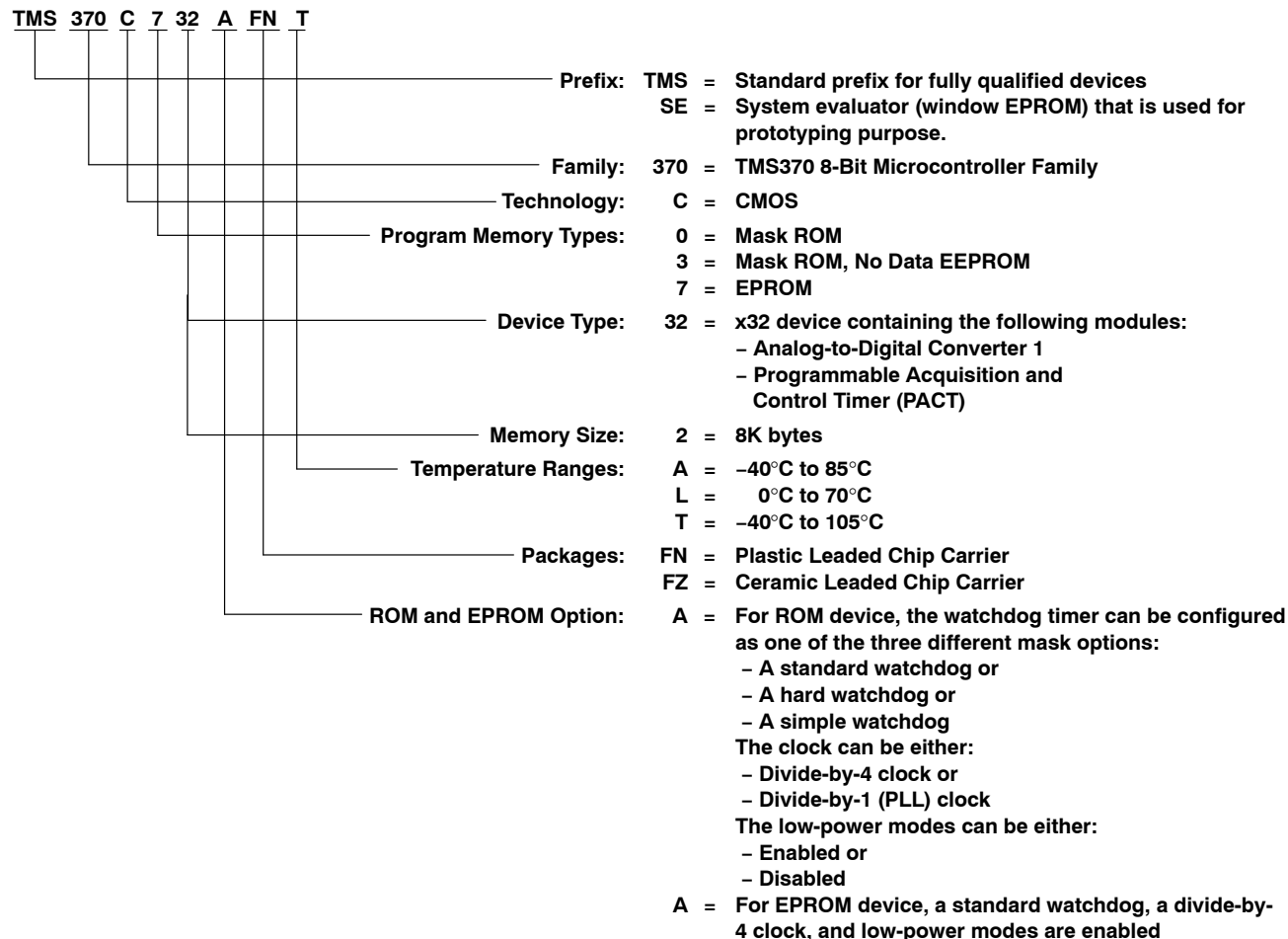


Figure 8. TMS370Cx32 Family Nomenclature

device part numbers

Table 16 lists all the 'x32 devices available. The device part number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog timer options desired. Each device can have only one of the three possible watchdog timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 16. Device Part Numbers

DEVICE PART NUMBERS FOR 44 PINS (LCC)
TMS370C032AFNA TMS370C032AFNL TMS370C032AFNT
TMS370C332AFNA TMS370C332AFNL TMS370C332AFNT
TMS370C732AFNT
SE370C732AFZT [†]

[†] System evaluators are for use in prototype environment, and their reliability has not been characterized.

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new code release form

Figure 9 shows a sample of the new code release form.

NEW CODE RELEASE FORM TEXAS INSTRUMENTS TMS370 MICROCONTROLLER PRODUCTS				DATE: _____																			
To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information: 1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media) 2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.																							
Company Name: _____ Street Address: _____ Street Address: _____ City: _____ State _____ Zip _____		Contact Mr./Ms.: _____ Phone: (_____) _____ Ext.: _____ Customer Purchase Order Number: _____ Customer Print Number *Yes: _____ # _____ No: _____ (Std. spec to be followed) *If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.																					
Customer Part Number: _____ Customer Application: _____																							
TMS370 Device: _____ TI Customer ROM Number: _____ (provided by Texas Instruments)																							
OSCILLATOR FREQUENCY <table border="1" style="width: 100%; border-collapse: collapse;"><thead><tr><th></th><th>MIN</th><th>TYP</th><th>MAX</th></tr></thead><tbody><tr><td>☐ External Drive (CLKIN)</td><td>_____</td><td>_____</td><td>_____</td></tr><tr><td>☐ Crystal</td><td>_____</td><td>_____</td><td>_____</td></tr><tr><td>☐ Ceramic Resonator</td><td>_____</td><td>_____</td><td>_____</td></tr></tbody></table> ☐ Supply Voltage MIN: _____ MAX: _____ (std range: 4.5V to 5.5V) CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS <table style="width: 100%;"><tr><td style="vertical-align: top;">Low Power Modes ☐ Enabled ☐ Disabled</td><td style="vertical-align: top;">Watchdog counter ☐ Standard ☐ Hard Enabled ☐ Simple Counter</td><td style="vertical-align: top;">Clock Type ☐ Standard (/4) ☐ PLL (/1)</td></tr></table> NOTE: Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the <i>TMS370 Family User's Guide</i> (literature number SPNU127) or the <i>TMS370 Family Data Manual</i> (literature number SPNS014B).						MIN	TYP	MAX	☐ External Drive (CLKIN)	_____	_____	_____	☐ Crystal	_____	_____	_____	☐ Ceramic Resonator	_____	_____	_____	Low Power Modes ☐ Enabled ☐ Disabled	Watchdog counter ☐ Standard ☐ Hard Enabled ☐ Simple Counter	Clock Type ☐ Standard (/4) ☐ PLL (/1)
	MIN	TYP	MAX																				
☐ External Drive (CLKIN)	_____	_____	_____																				
☐ Crystal	_____	_____	_____																				
☐ Ceramic Resonator	_____	_____	_____																				
Low Power Modes ☐ Enabled ☐ Disabled	Watchdog counter ☐ Standard ☐ Hard Enabled ☐ Simple Counter	Clock Type ☐ Standard (/4) ☐ PLL (/1)																					
TEMPERATURE RANGE <table style="width: 100%;"><tr><td>☐ 'L': 0° to 70°C (standard)</td><td></td></tr><tr><td>☐ 'A': -40° to 85°C</td><td></td></tr><tr><td>☐ 'T': -40° to 105°C</td><td></td></tr></table>		☐ 'L': 0° to 70°C (standard)		☐ 'A': -40° to 85°C		☐ 'T': -40° to 105°C		PACKAGE TYPE <table style="width: 100%;"><tr><td>☐ 'N' 28-pin PDIP</td><td>☐ "FN" 44-pin PLCC</td></tr><tr><td>☐ "FN" 28-pin PLCC</td><td>☐ "FN" 68-pin PLCC</td></tr><tr><td>☐ "N" 40-pin PDIP</td><td>☐ "NM" 64-pin PSDIP</td></tr><tr><td colspan="2">☐ "NJ" 40-pin PSDIP (formerly known as N2)</td></tr></table>			☐ 'N' 28-pin PDIP	☐ "FN" 44-pin PLCC	☐ "FN" 28-pin PLCC	☐ "FN" 68-pin PLCC	☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP	☐ "NJ" 40-pin PSDIP (formerly known as N2)						
☐ 'L': 0° to 70°C (standard)																							
☐ 'A': -40° to 85°C																							
☐ 'T': -40° to 105°C																							
☐ 'N' 28-pin PDIP	☐ "FN" 44-pin PLCC																						
☐ "FN" 28-pin PLCC	☐ "FN" 68-pin PLCC																						
☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP																						
☐ "NJ" 40-pin PSDIP (formerly known as N2)																							
SYMBOLIZATION ☐ TI standard symbolization ☐ TI standard w/customer part number ☐ Customer symbolization (per attached spec, subject to approval)		BUS EXPANSION ☐ YES ☐ NO																					
NON-STANDARD SPECIFICATIONS: ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.																							
RELEASE AUTHORIZATION: This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cycletime commences when this document is signed off and the verification code is approved by the customer.																							
1. Customer: _____ Date: _____		2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____																					

Figure 9. Sample New Code Release Form



Table 17 is a collection of all the peripheral file frames used in the 'Cx32 (provided for a quick reference).

Table 17. Peripheral File Frame Compilation

System Configuration Registers									
PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTO WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D to P01F	Reserved								
Digital Port Control Registers									
P020	Reserved								APOINT1
P021	Port A Control Register 2 (must be 0)								APOINT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)		—	Port D Control Register 1 (must be 0)		—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0) [†]		—	Port D Control Register 2 (must be 0) [†]		—	—	—	DPORT2
P02E	Port D Data		—	Port D Data		—	—	—	DDATA
P02F	Port D Direction		—	Port D Direction		—	—	—	DDIR
PACT Module Register Memory Map									
P040	DEFTIM OVRFL INT ENA	DEFTIM OVRFL INT FLAG	CMD/DEF AREA ENA	FAST MODE SELECT	PACT PRESCALE SELECT3	PACT PRESCALE SELECT2	PACT PRESCALE SELECT1	PACT PRESCALE SELECT0	PACTSCR
P041	CMD/DEF AREA INT ENA	—	CMD/DEF AREA START BIT 5	CMD/DEF AREA START BIT 4	CMD/DEF AREA START BIT 3	CMD/DEF AREA START BIT 2	—	—	CDSTART

[†] To configure D3 as SYSCLK, set port D register 2 = 08h.

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Table 17. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
PACT Module Register Memory Map									
P042	—	CMD/DEF AREA END BIT 6	CMD/DEF AREA END BIT 5	CMD/DEF AREA END BIT 4	CMD/DEF AREA END BIT 3	CMD/DEF AREA END BIT 2	—	—	CDEND
P043	1	1	BUFFER POINTER BIT 5	BUFFER POINTER BIT 4	BUFFER POINTER BIT 3	BUFFER POINTER BIT 2	BUFFER POINTER BIT 1	—	BUFPTR
P044	Reserved								
P045	PACT RXRDY	PACT TXRDY	PACT PARITY	PACT FE	PACT SCI RX INT ENA	PACT SCI TX INT ENA	—	PACT SCI SW RESET	SCICTLP
P046	PACT RXDT7	PACT RXDT6	PACT RXDT5	PACT RXDT4	PACT RXDT3	PACT RXDT2	PACT RXDT1	PACT RXDT0	RXBUFPP
P047	PACT TXDT7	PACT TXDT6	PACT TXDT5	PACT TXDT4	PACT TXDT3	PACT TXDT2	PACT TXDT1	PACT TXDT0	TXBUFPP
P048	PACT OP8 STATE	PACT OP7 STATE	PACT OP6 STATE	PACT OP5 STATE	PACT OP4 STATE	PACT OP3 STATE	PACT OP2 STATE	PACT OP1 STATE	PSTATE
P049	CMD/DEF INT 7 FLAG	CMD/DEF INT 6 FLAG	CMD/DEF INT 5 FLAG	CMD/DEF INT 4 FLAG	CMD/DEF INT 3 FLAG	CMD/DEF INT 2 FLAG	CMD/DEF INT 1 FLAG	CMD/DEF INT 0 FLAG	CDFLAGS
P04A	CP2 INT ENA	CP2 INT FLAG	CP2 CAPT RISING EDGE	CP2 CAPT FALLING EDGE	CP1 INT ENA	CP1 INT FLAG	CP1 CAPT RISING EDGE	CP1 CAPT FALLING EDGE	CPCTL1
P04B	CP4 INT ENA	CP4 INT FLAG	CP4 CAPT RISING EDGE	CP4 CAPT FALLING EDGE	CP3 INT ENA	CP3 INT FLAG	CP3 CAPT RISING EDGE	CP3 CAPT FALLING EDGE	CPCTL2
P04C	CP6 INT ENA	CP6 INT FLAG	CP6 CAPT RISING EDGE	CP6 CAPT FALLING EDGE	CP5 INT ENA	CP5 INT FLAG	CP5 CAPT RISING EDGE	CP5 CAPT FALLING EDGE	CPCTL3
P04D	BUFFER HALF/FULL INT ENA	BUFFER HALF/FULL INT FLAG	INPUT CAPT PRESCALE SELECT 3	INPUT CAPT PRESCALE SELECT 2	INPUT CAPT PRESCALE SELECT 1	CP6 EVENT ONLY	EVENT COUNTER SW RESET	OP/ SET/CLR SELECT	CPPRE
P04E	WATCHDOG RESET KEY								WDRST
P04F	PACT STEST	PACT SUSPEND	PACT GROUP 1 PRIORITY	PACT GROUP 2 PRIORITY	PACT GROUP 3 PRIORITY	PACT MODE SELECT	PACT WD PRESCALE SELECT 1	PACT WD PRESCALE SELECT 0	PACTPRI
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SE- LECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A/D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC1} (see Note 3)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC1}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC1}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC1}) (see Note 4)	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	800 mW
Operating free-air temperature, T_A : L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 3. Unless otherwise noted, all voltage values are with respect to V_{SS1} .

4. Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage (see Note 3)		4.5	5	5.5	V
	RAM data retention supply voltage (see Note 5)		3		5.5	V
V_{CC3}	Analog supply voltage (see Note 3)		4.5	5	5.5	V
V_{SS3}	Analog supply ground		– 0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS1}		0.8	V
		MC, normal operation	V_{SS1}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET	2		V_{CC1}	V
		XTAL2/CLKIN	0.8 V_{CC1}		V_{CC1}	
		RESET	0.7 V_{CC1}		V_{CC1}	
V_{MC}	MC (mode control) voltage	EEPROM write protect override (WPO)	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	
		Microcomputer	V_{SS1}		0.3	
T_A	Operating free-air temperature	L version	0		70	°C
		A version	– 40		85	
		T version	– 40		105	

NOTES: 3. Unless otherwise noted, all voltage values are with respect to V_{SS1} .

5. RESET must be externally activated when V_{CC1} or SYSCLK is not within the recommended operating range.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

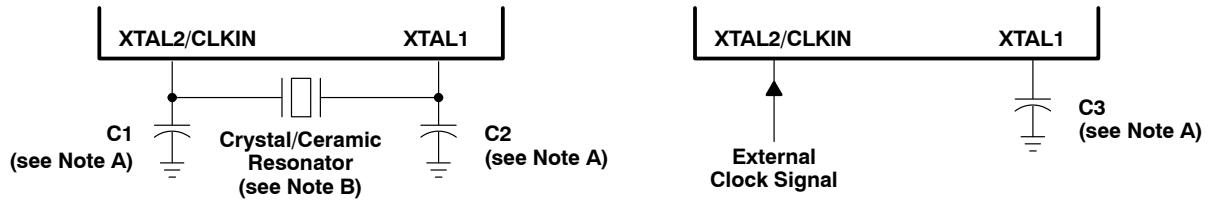
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OL}	Low-level output voltage	I _{OL} = 1.4 mA			0.4	V
V _{OH}	High-level output voltage	I _{OH} = -50 µA	0.9 V _{CC1}			V
		I _{OH} = -2 mA	2.4			
I _I	Input current	MC	0 V ≤ V _I ≤ 0.3 V		10	µA
			0.3 V < V _I ≤ 13 V		650	µA
			12 V ≤ V _I ≤ 13 V [†]		50	mA
	I/O pins		0 V ≤ V _I ≤ V _{CC1}		± 10	µA
I _{OL}	Low-level output current	V _{OL} = 0.4 V	1.4			mA
I _{OH}	High-level output current	V _{OH} = 0.9 V _{CC1}	- 50			µA
		V _{OH} = 2.4 V	- 2			mA
I _{CC1}	Supply current (operating mode) OSC POWER bit = 0	See Notes 6 and 7 SYSCLK = 5 MHz		35	45	mA
		See Notes 6 and 7 SYSCLK = 3 MHz		25	35	
		See Notes 6 and 7 SYSCLK = 0.5 MHz		10	14	
	Supply current (STANDBY mode) OSC POWER bit = 0	See Notes 6 and 7 SYSCLK = 5 MHz		12	17	mA
		See Notes 6 and 7 SYSCLK = 3 MHz		8	13	
		See Notes 6 and 7 SYSCLK = 0.5 MHz		3	4	
	Supply current (STANDBY mode) OSC POWER bit = 1	See Notes 6 and 7 SYSCLK = 3 MHz		6	8.6	mA
		See Notes 6 and 7 SYSCLK = 0.5 MHz		2	3.0	
	Supply current (HALT mode)	See Note 6 XTAL2/CLKIN < 0.2 V		15	40	µA

[†] Input current I_{PP} will be a maximum of 50 mA only when programming EPROM.

NOTES: 6. Single chip mode, ports configured as inputs or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} - 0.2V.

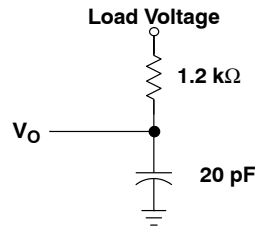
7. XTAL2/CLKIN is driven with an external square-wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = 0.01 mA x (total load capacitance + crystal capacitance in pF).





NOTES: A. The values of C1 and C2 are typically 15 pF and C3 value is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.
B. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.

Figure 10. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4 \text{ V}$; Load Voltage = 0 V
Case 2: $V_O = V_{OL} = 0.4 \text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 11. Typical Output Load Circuit (See Note A)

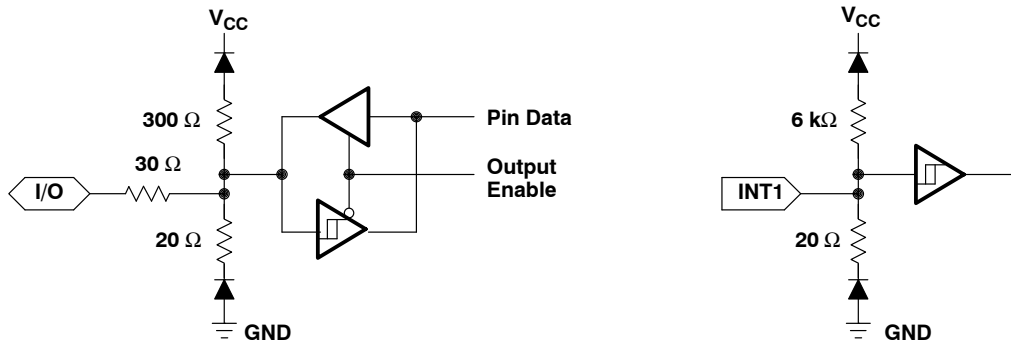


Figure 12. Typical Buffer Circuitry

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PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

AR	Array	PGM	Program
B	Byte	SC	SYSCLK
CI	XTAL2/CLKIN		

Lowercase subscripts and their meanings are:

c	cycle time (period)	su	setup time
d	delay time	v	valid time
f	fall time	w	pulse duration (width)
r	rise time		

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid

All timings are measured between high and low measurement points as indicated in Figure 13 and Figure 14.

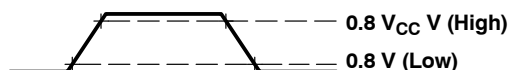


Figure 13. XTAL2/CLKIN Measurement Points

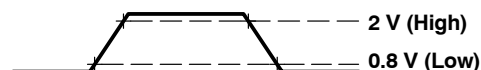


Figure 14. General Measurement Points

external clocking requirements for clock divided by 4 (see Note 8 and Figure 15)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(Cl)}$ Pulse duration, XTAL2/CLKIN (see Note 9)	20		ns
2	$t_{r(Cl)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN Crystal operating frequency	2	20	MHz
	SYSCLK Internal system clock operating frequency [†]	0.5	5	MHz

[†] SYSCLK = CLKIN/4

NOTES: 8. For V_{IL} and V_{IH} , refer to recommended operating conditions.

9. This pulse may be either a high pulse, as illustrated below, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

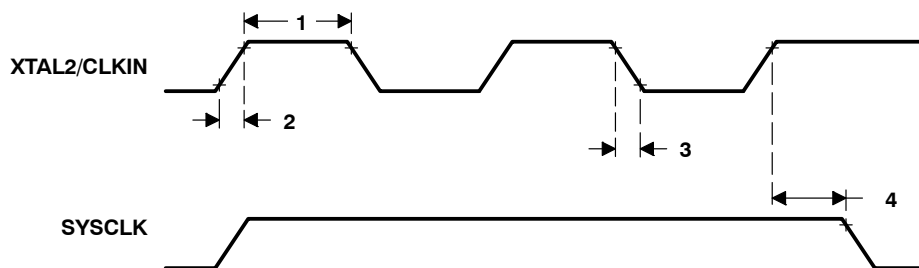


Figure 15. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL) (see Note 8 and Figure 16)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(Cl)}$ Pulse duration, XTAL2/CLKIN (see Note 9)	20		ns
2	$t_{r(Cl)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN Crystal operating frequency	2	5	MHz
	SYSCLK Internal system clock operating frequency [†]	2	5	MHz

[†] SYSCLK = CLKIN/1

NOTES: 8. For V_{IL} and V_{IH} , refer to recommended operating conditions.

9. This pulse can be either a high pulse, as illustrated below, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

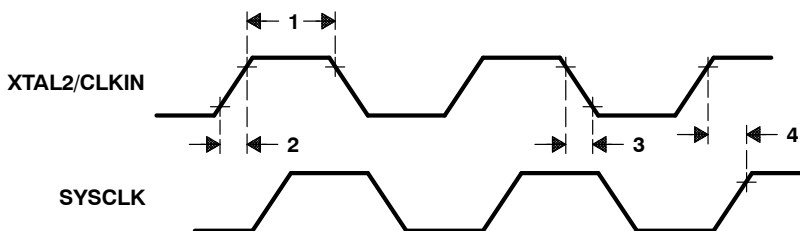


Figure 16. External Clock Timing for Divide-by-1

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switching characteristics and timing requirements (see Note 10 and Figure 17)

NO.	PARAMETER		MIN	MAX	UNIT
5	t_c	Cycle time, SYSCLK (system clock)	200	2000	ns
			200	500	
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low	$0.5 t_c - 20$	$0.5 t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high	$0.5 t_c$	$0.5 t_c + 20$	ns

NOTE 10: t_c = system clock cycle time = $1 / \text{SYSCLK}$

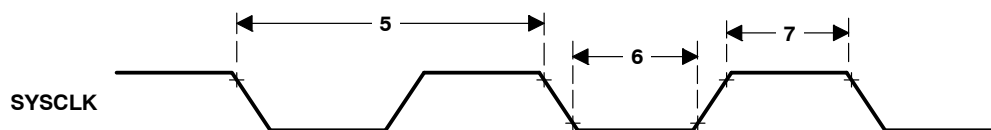


Figure 17. SYSCLK Timing

general purpose output signal switching time requirements (see Figure 18)

	MIN	NOM	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns

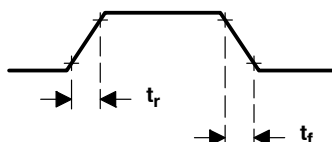


Figure 18. Signal Switching Timing

recommended EEPROM timing requirements for programming

	MIN	MAX	UNIT
$t_{w(PGM)B}$ Pulse duration, programming signal to ensure valid data is stored (byte mode)	10		ms
$t_{w(PGM)AR}$ Pulse duration, programming signal to ensure valid data is stored (array mode)	20		ms

recommended EPROM operating conditions for programming

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5.5	6	V
V_{PP} Supply voltage at MC pin	13	13.2	13.5	V
I_{PP} Supply current at MC pin during programming ($V_{PP} = 13$ V)		30	50	mA
SYSCLK System clock	Divide-by-4	0.5	5	MHz
	Divide-by-1	2	5	

recommended EPROM timing requirements for programming

	MIN	NOM	MAX	UNIT
$t_{w(EPGM)}$ Pulse duration, programming signal (see Note 11)	0.40	0.50	3	ms

NOTE 11: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.



ADC1 converter

The ADC1 converter has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3} . The purpose is to enhance ADC1 performance by preventing digital switching noise of the logic circuitry that can be present on V_{SS1} and V_{CC1} from coupling into the ADC1 analog stage. All ADC1 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution 8-bits (256 values)
 Monotonic Yes
 Output conversion mode 00h to FFh (00 for $V_I \leq V_{SS3}$; FF for $V_I \leq V_{ref}$)
 Conversion time (excluding sample time) $164 t_c$

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC3} Analog supply voltage	4.5	5	5.5	V
	$V_{CC3}-0.3$		$V_{CC3}+0.3$	
V_{SS3} Analog ground	$V_{SS3}-0.3$		$V_{SS3}+0.3$	V
V_{ref} Non- V_{CC3} reference [†]	2.5	V_{CC3}	$V_{CC3} + 0.1$	V
Analog input for conversion	V_{SS3}		V_{ref}	V

[†] V_{ref} must be stable, within $\pm 1/2$ LSB of the required resolution, during the entire conversion time.

operating characteristics over recommended ranges operating conditions

PARAMETER		MIN	MAX	UNIT
Absolute accuracy [†]	$V_{CC3} = 5.5$ V $V_{ref} = 5.1$ V	± 1.5		LSB
Differential/integral linearity error ^{†‡}	$V_{CC3} = 5.5$ V $V_{ref} = 5.1$ V	± 0.9		LSB
I_{CC3} Analog supply current	Converting	2		mA
	Nonconverting	5		μ A
I_I Input current, AN0 – AN7	$0 \text{ V} \leq V_I \leq 5.5 \text{ V}$	2		μ A
I_{ref} Input charge current		1		mA
Z_{ref} Source impedance of V_{ref}	$\text{SYSCLK} \leq 3 \text{ MHz}$	24		k Ω
	$3 \text{ MHz} < \text{SYSCLK} \leq 5 \text{ MHz}$	10		k Ω

[†] Absolute resolution = 20 mV. At $V_{ref} = 5$ V, this is one LSB. As V_{ref} decreases, LSB size decreases; therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

[‡] Excluding quantization error of $1/2$ LSB

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ADC1 converter (continued)

The ADC1 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined so that the high-impedance can be accommodated without penalty to the low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC1 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter will reset the SAMPLE START and CONVERT START bits, signaling that a conversion has started and that the analog signal can be removed.

analog timing requirements (see Figure 19)

	MIN	MAX	UNIT
$t_{su(S)}$ Setup time, analog to sample command	0		ns
$t_{h(AN)}$ Hold time, analog input from start of conversion	$18t_c$		ns
$t_w(S)$ Pulse duration, sample time per kilo- Ω of source impedance [†]	1		$\mu s/k\Omega$

[†] The value given is valid for a signal with a source impedance > 1 k Ω . If the source impedance is < 1 k Ω , use a minimum sampling time of 1 μs .

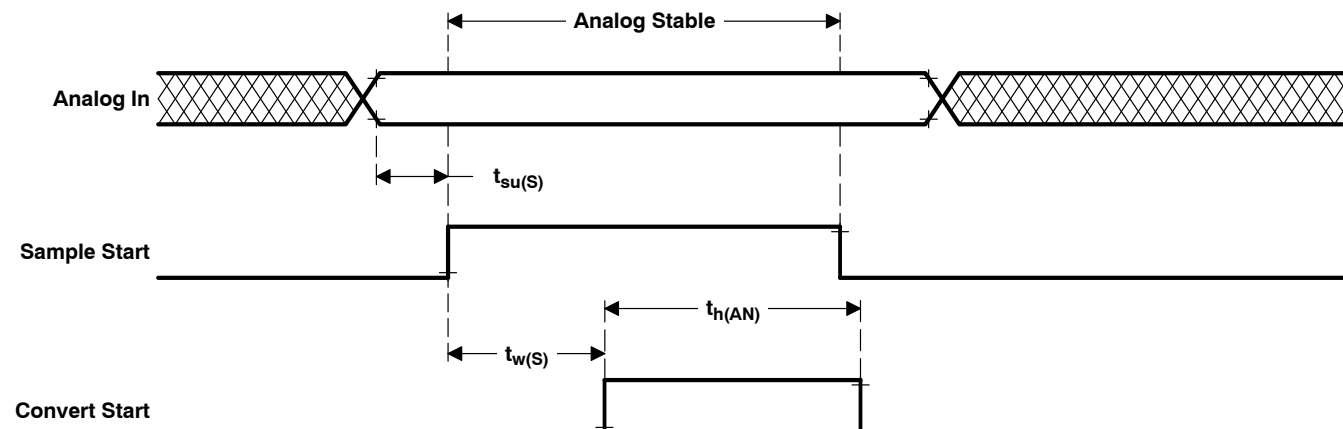


Figure 19. Analog Timing

Table 18 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

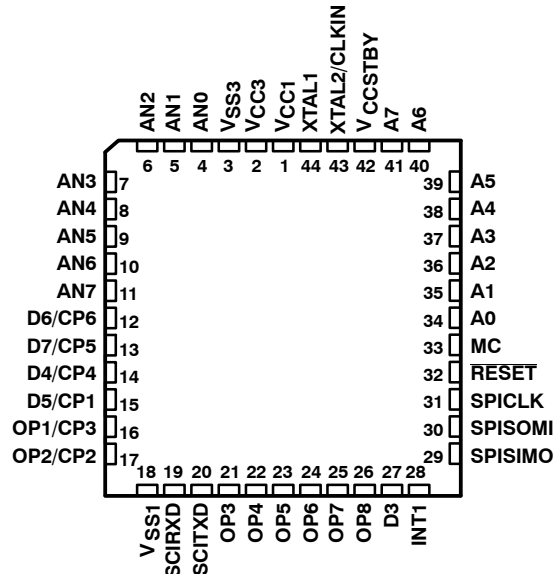
Table 18. TMS370Cx32 Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 44 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C032AFNA TMS370C032AFNL TMS370C032AFNT TMS370C332AFNA TMS370C332AFNL TMS370C332AFNT TMS370C732AFNT
FZ – 44 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C732AFZT

General Information	1
Selection Guide/Tools	2
Ops Cond/Timing/Glossary	3
TMS370Cx0x Data Sheet	4
TMS370Cx1x Data Sheet	5
TMS370Cx2x Data Sheet	6
TMS370Cx32 Data Sheet	7
TMS370Cx36 Data Sheet	8
TMS370Cx4x Data Sheet	9
TMS370Cx5x Data Sheet	10
TMS370Cx6x Data Sheet	11
TMS370Cx7x Data Sheet	12
TMS370Cx8x Data Sheet	13
TMS370Cx9x Data Sheet	14
TMS370CxAx Data Sheet	15
TMS370CxBx Data Sheet	16
TMS370CxCx Data Sheet	17
Mechanical Data	18
Quality and Reliability	19
Electrostatic Discharge Guidelines	20

- **CMOS/EEPROM/EPROM Technologies on a Single Device**
 - Mask-ROM Devices for High-Volume Production
 - One-Time-Programmable (OTP) EPROM Devices for Low-Volume Production
 - Reprogrammable-EPROM Devices for Prototyping Purposes
- **Internal System Memory Configurations**
 - On-Chip Program Memory Versions
 - ROM: 16K Bytes
 - EPROM: 16K Bytes
 - Data EEPROM: 256 Bytes
 - Static RAM: 256 Bytes Usable as Registers
 - Standby RAM With Separate Power Supply Pin: 256 Bytes
- **Flexible Operating Features**
 - Low-Power Modes: STANDBY and HALT
 - Commercial, Industrial, and Automotive Temperature Ranges
 - Clock Options
 - Divide-by-1 (2 MHz–5 MHz SYSCLK) Phase-Locked Loop (PLL)
 - Divide-by-4 (0.5 MHz–5 MHz SYSCLK)
 - Supply Voltage (V_{CC}) 5 V $\pm$ 10%
- **Programmable Acquisition and Control Timer (PACT) Module**
 - Input Capture on up to Six Pins, Four of Which Can Have a Programmable Prescaler
 - One Input Capture Pin Can Drive an 8-Bit Event Counter
 - Up to Eight Timer-Driven Outputs
 - Interaction Between Event Counter and Timer Activity
 - 18 Independent Interrupt Vectors
 - Watchdog With Selectable Time-Out Period
 - Asynchronous Mini Serial Communication Interface (Mini SCI)
- **Flexible Interrupt Handling**
 - Two Software-Programmable Interrupt Levels
 - Global- and Individual-Interrupt Masking
 - Programmable Rising- or Falling-Edge Detect
 - Individual-Interrupt Vectors

FZ AND FN PACKAGES
(TOP VIEW)



- **Serial Peripheral Interface (SPI)**
 - Variable-Length High-Speed Shift Register
 - Synchronous Master/Slave Operation
- **Eight Channel 8-Bit Analog-to-Digital Converter 1 (ADC1)**
- **TMS370 Series Compatibility**
 - Register-to-Register Architecture
 - 256 General-Purpose Registers
 - 14 Powerful Addressing Modes
 - Instructions Upwardly Compatible With All TMS370 Devices
- **CMOS/TTL Compatible I/O Pins/Packages**
 - All Peripheral Function Pins Software Configurable for Digital I/O
 - 16 Bidirectional Pins, Nine Input Pins
 - 44-Pin Plastic and Ceramic Leaded Chip Carrier (LCC) Packages
- **Workstation/PC-Based Development System**
 - C Compiler and C Source Debugger
 - Real-Time In-Circuit Emulation
 - Multi-Window User Interface
 - Microcontroller Programmer



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 **TEXAS
INSTRUMENTS**

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TMS370Cx36

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Pin Descriptions

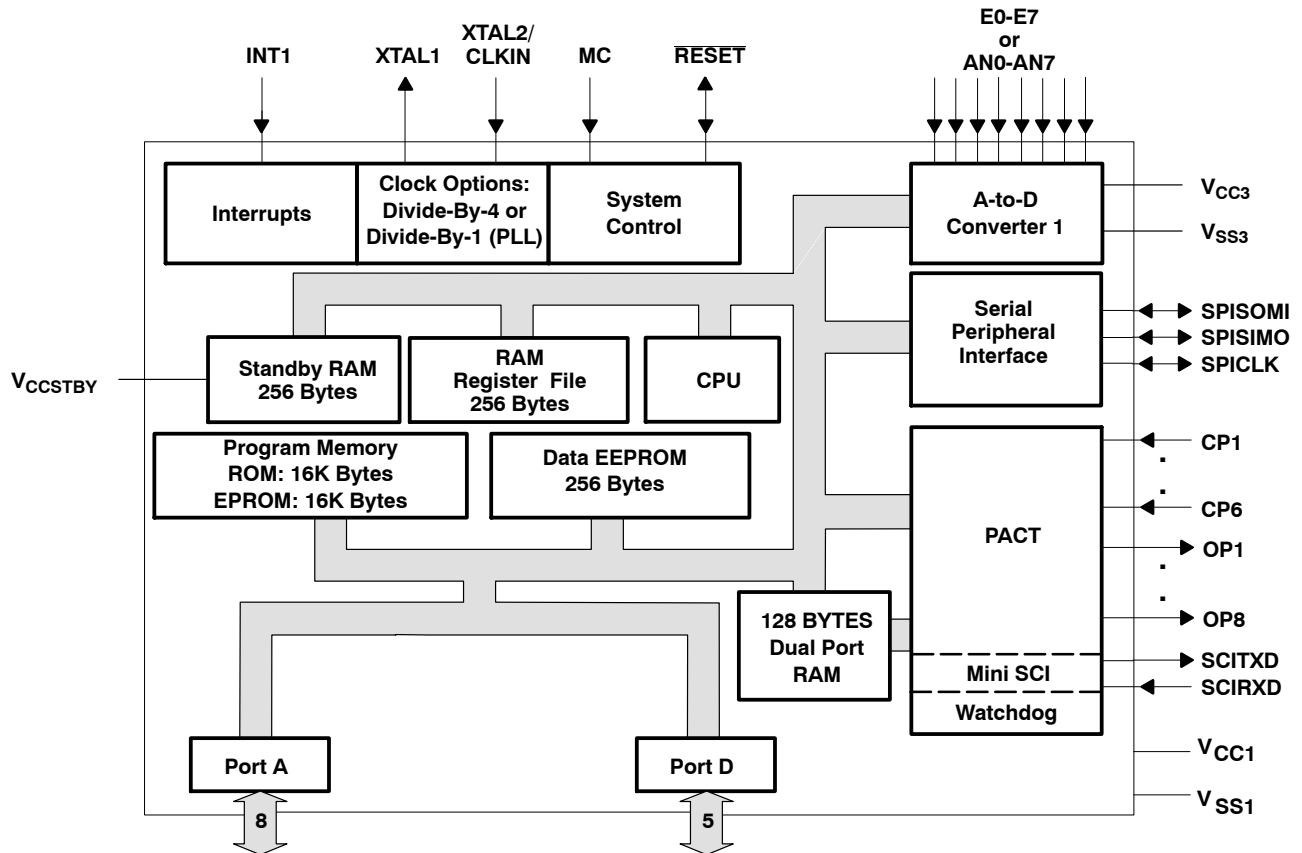
44 PINS		I/O†	DESCRIPTION
NAME	NO.		
A0 A1 A2 A3 A4 A5 A6 A7	34 35 36 37 38 39 40 41	I / O	Port A is a general-purpose bidirectional I/O port.
D3 D4/CP4 D5/CP1 D6/CP6 D7/CP5	27 14 15 12 13	I / O	Port D is a general-purpose bidirectional port. Also configurable as SYSCCLK (see Note 1) PACT input capture 4 (see Note 2) PACT input capture 1 (see Note 2) PACT input capture 6 (see Note 2) PACT input capture 5 (see Note 2)
AN0/E0 AN1/E1 AN2/E2 AN3/E3 AN4/E4 AN5/E5 AN6/E6 AN7/E7	4 5 6 7 8 9 10 11	I	ADC1 analog input pins (AN0 – AN7) / port E digital input pins (E0 – E7) Port E can be programmed individually as a general-purpose digital input pin if it is not used as ADC1 analog input or positive reference input.
INT1	28	I	External interrupt (non-maskable or maskable) / general-purpose input pin
OP1/CP3 OP2/CP2 OP3 OP4 OP5 OP6 OP7 OP8	16 17 21 22 23 24 25 26	O	PACT PWM output 1/input capture 3 (see Note 3) PACT output pin 2/input capture 2 (see Note 3) PACT PWM output 3 PACT PWM output 4 PACT PWM output 5 PACT PWM output 6 PACT PWM output 7 PACT PWM output 8
SCIRXD SCITXD	19 20	I O	PACT mini SCI data receive input pin PACT mini SCI data transmit output pin
SPISOMI SPISIMO SPICLK	30 29 31	I / O	SPI slave output pin, master input pin / general-purpose bidirectional pin SPI slave input pin, master output pin / general-purpose bidirectional pin SPI bidirectional serial clock pin / general-purpose bidirectional pin
RESET	32	I / O	System reset bidirectional pin; as input pin, RESET initializes the microcontroller; as open-drain output, RESET indicates that an internal failure was detected by watchdog or oscillator fault circuit.
MC	33	I	Mode control input pin; enables EEPROM write protection override (WPO) mode, also EPROM V _{PP}
XTAL2/CLKIN XTAL1	43 44	I O	Internal oscillator crystal input / External clock source input Internal oscillator output for crystal
V _{CC1} V _{SS1} V _{CC3} V _{SS3} V _{CCSTBY}	1 18 2 3 42		Positive supply voltage for digital logic and digital I/O pins Ground reference for digital logic and digital I/O pins ADC1 positive supply voltage and optional positive reference input ADC1 ground supply and low reference input pin Positive supply voltage pin for standby RAM

† I = input, O = output

- NOTES:
- D3 can be configured as SYSCCLK by appropriately programming the DPORT1 and DPORT2 registers.
 - These digital I/O buffers are connected internally to some of the PACT module's input capture pins. This allows the microcontroller to read the level on the input capture pin, or if the port D pin is configured as an output, to generate a capture. Be careful to leave the port D pin configured as an input if the corresponding input capture pin is being driven by external circuitry.
 - CP2 and CP3 are connected internally to OP2 and OP1. CP2 and CP3 can be used only to capture OP2 and OP1, respectively and not as external capture inputs.



functional block diagram



description

The TMS370C036, TMS370C736, and SE370C736 devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx36 refers to these devices. The TMS370 family provides cost-effective real-time system control through advanced peripheral-function modules and various on-chip memory configurations.

The TMS370Cx36 family of devices uses high-performance silicon-gate CMOS EPROM and EEPROM technologies. Low operating power, wide operating temperature range, and noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx36 devices attractive for system designs for automotive electronics, industrial motors, computer peripheral controls, telecommunications, and consumer applications.

All TMS370Cx36 devices contain the following on-chip peripheral modules:

- Programmable acquisition and control timer (PACT)
 - Asynchronous mini SCI
 - PACT watchdog timer
- Serial peripheral interface (SPI)
- Eight channel, 8-bit analog-to-digital converter 1 (ADC1)

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description (continued)

Table 1 provides a memory configuration overview of the TMS370Cx36 devices.

Table 1. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		44 PIN PACKAGES
	ROM	EPROM	RAM	EEPROM	
TMS370C036A	16K	—	512	256	FN – PLCC
TMS370C736A	—	16K	512	256	FN – PLCC
SE370C736A [†]	—	16K	512	256	FZ – CLCC

[†] System evaluators and development are for use only in prototype environment, and their reliability has not been characterized.

The suffix letter A appended to the device names in Table 1 indicates the configuration of the devices. ROM or EPROM devices have different configurations as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 2. Suffix Letter Configuration

DEVICE [†]	CLOCK	LOW-POWER MODE
EPROM A	Divide-by-4 (Standard oscillator)	Enabled
ROM A	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled

[†] Refer to the “device numbering conventions” section for device nomenclature and to the “device part numbers” section for ordering.

The 16K bytes of mask-programmable ROM in the associated TMS370Cx36 devices are replaced in the TMS370C736 with 16K bytes of EPROM. All other available memory and on-chip peripherals are identical. The OTP (TMS370C736) and reprogrammable (SE370C736) devices are available.

The TMS370C736 OTP device is available in a plastic package. This microcontroller is effective to use for immediate production updates for other members of the TMS370Cx36 family or for low-volume production runs when the mask charge or cycle time for the low-cost mask ROM devices is not practical.

The SE370C736 has a windowed ceramic package to allow reprogramming of the program EPROM memory during the development/prototyping phase of design. The SE370C736 device allows quick updates to breadboards and prototype systems while iterating initial designs.

The TMS370Cx36 family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all CPU activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator, the PACT counter, and PACT's first command/definition entry remain active. This allows the PACT module to bring the device out of STANDBY mode. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx36 features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx36 family is fully instruction-set-compatible, providing easy transition between members of the family.

The TMS370Cx36 has a PACT module that acts as a timer coprocessor by gathering timing information on input signals and controlling output signals with little or no intervention by the CPU. The coprocessor nature of this module allows for levels of flexibility and power not found in traditional microcontroller timers.



description (continued)

The TMS370Cx36 family provides the system designer with an economical, efficient solution to real-time control applications. The PACT compact development tool (CDT™) meets the challenge of efficiently developing the software and hardware required to design the TMS370Cx36 into an ever-increasing number of complex applications. The application source code can be written in assembly and C language, and the output code can be generated by the linker. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as a reduced time-to-market cycle.

The TMS370Cx36 family together with the TMS370 PACT CDT370, BP programmer, software tools, SE370C736 reprogrammable devices, comprehensive product documentation, and customer support provides a complete solution to the needs of the system designer.

central processing unit (CPU)

The CPU on the TMS370Cx36 device is the high-performance 8-bit TMS370 CPU module. The 'x36 implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'x36 instruction map is shown in Table 16.

The '370Cx36 CPU architecture provides the following components:

CPU registers:

- A stack pointer (SP) that points to the last entry in the memory stack
- A status register (ST) that monitors the operation of the instructions and contains the global interrupt-enable bits
- A program counter (PC) that points to the memory location of the next instruction to be executed

A memory map that includes:

- 256-byte general-purpose RAM that can be used for data memory storage, program instructions, general purpose register, or the stack
- 256-byte general-purpose standby RAM, which is powered through a separate V_{CCSTBY} pin to protect the memory against power failures on the main V_{CC1} pins
- 128-byte dual-port RAM that contains the capture registers, the circular buffer, and a command/definition area
- A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM/EPROM programming control
- 256-byte EEPROM module, that provides in-circuit programmability and data retention in power-off conditions
- 16K-byte ROM or 16K-byte EPROM

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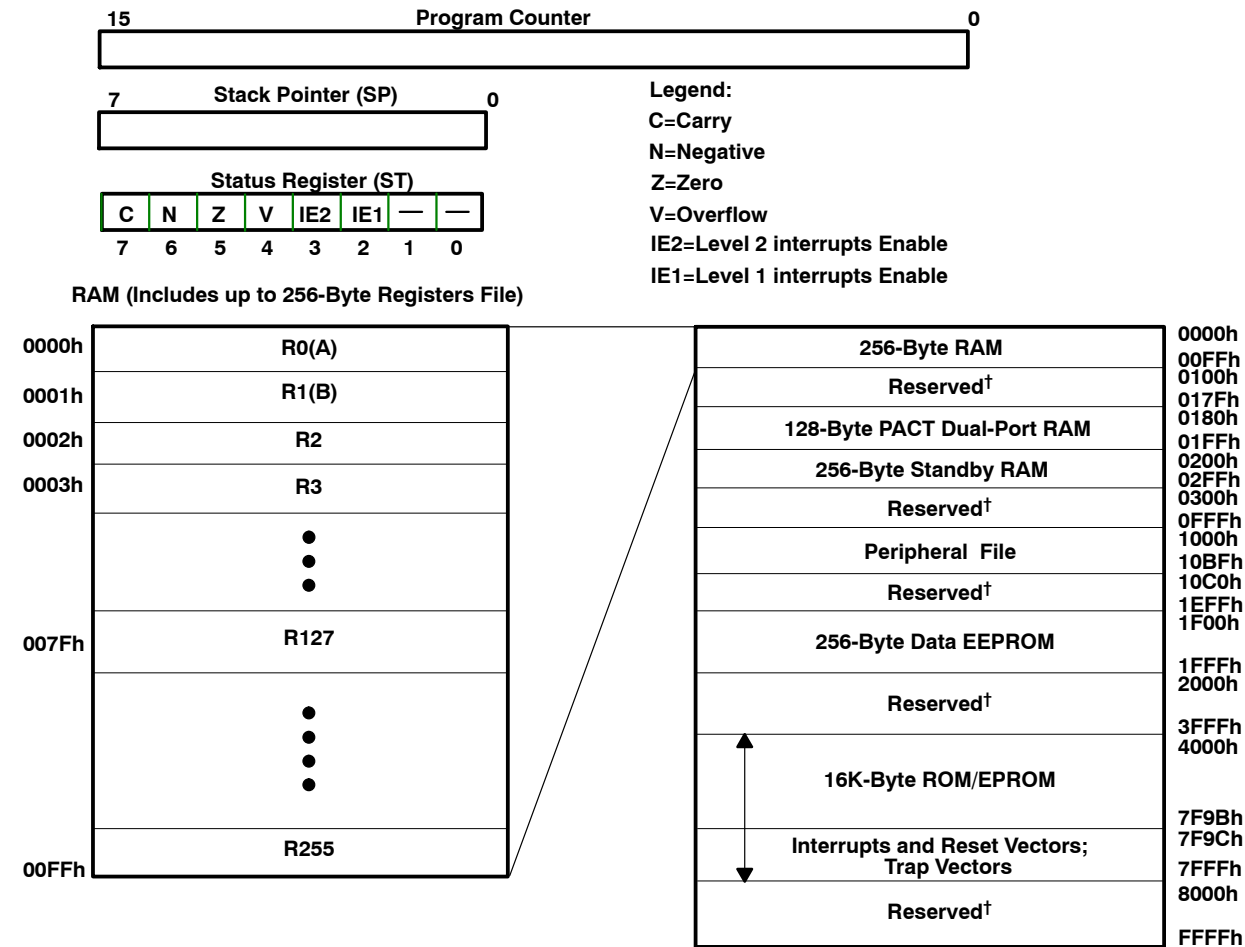


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central processing unit (CPU) (continued)

Figure 1 Illustrates the CPU registers and memory blocks.



† Reserved means the address space is reserved for future expansion.

Figure 1. Programmer's Model

stack pointer (SP)

The SP is an 8-bit CPU register. Stack operates as a last-in, first-out, read/write memory. Typically, the stack is used to store the return address on subroutine calls as well as the ST contents during interrupt sequences.

The SP points to the last entry or top of the stack. The SP is incremented automatically before data is pushed onto the stack and decremented after data is popped from the stack. The stack can be placed anywhere in the on-chip RAM.

status register (ST)

The ST monitors the operation of the instructions and contains the global interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits.

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional-jump instructions) use the status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

central processing unit (CPU) (continued)

The ST, status-bit notation, and status-bit definitions are shown in Table 3.

Table 3. Status Registers

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most significant byte (MSbyte) and least significant byte (LSbyte) of a 16-bit address.

During reset, the contents of the reset vector (7FFEh, 7FFFh) are loaded into the PC. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 4000h as the contents of the reset vector.

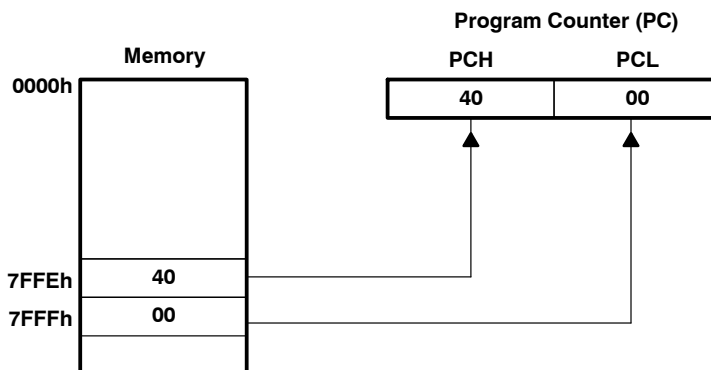


Figure 2. Program Counter After Reset

memory map

The TMS370Cx36 architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. As shown in Figure 3, the TMS370Cx36 provides memory-mapped RAM, ROM, EPROM, data EEPROM, I/O pins, peripheral functions, and system-interrupt vectors.

The peripheral file contains all I/O port control, peripheral status and control, EEPROM, EPROM, and system-wide control functions. The peripheral file is located between 1000h to 107Fh and is divided logically into eight peripheral file frames of 16 bytes each. The eight PF frames consist of five control frames and three reserved frames. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information are passed.

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central processing unit (CPU) (continued)

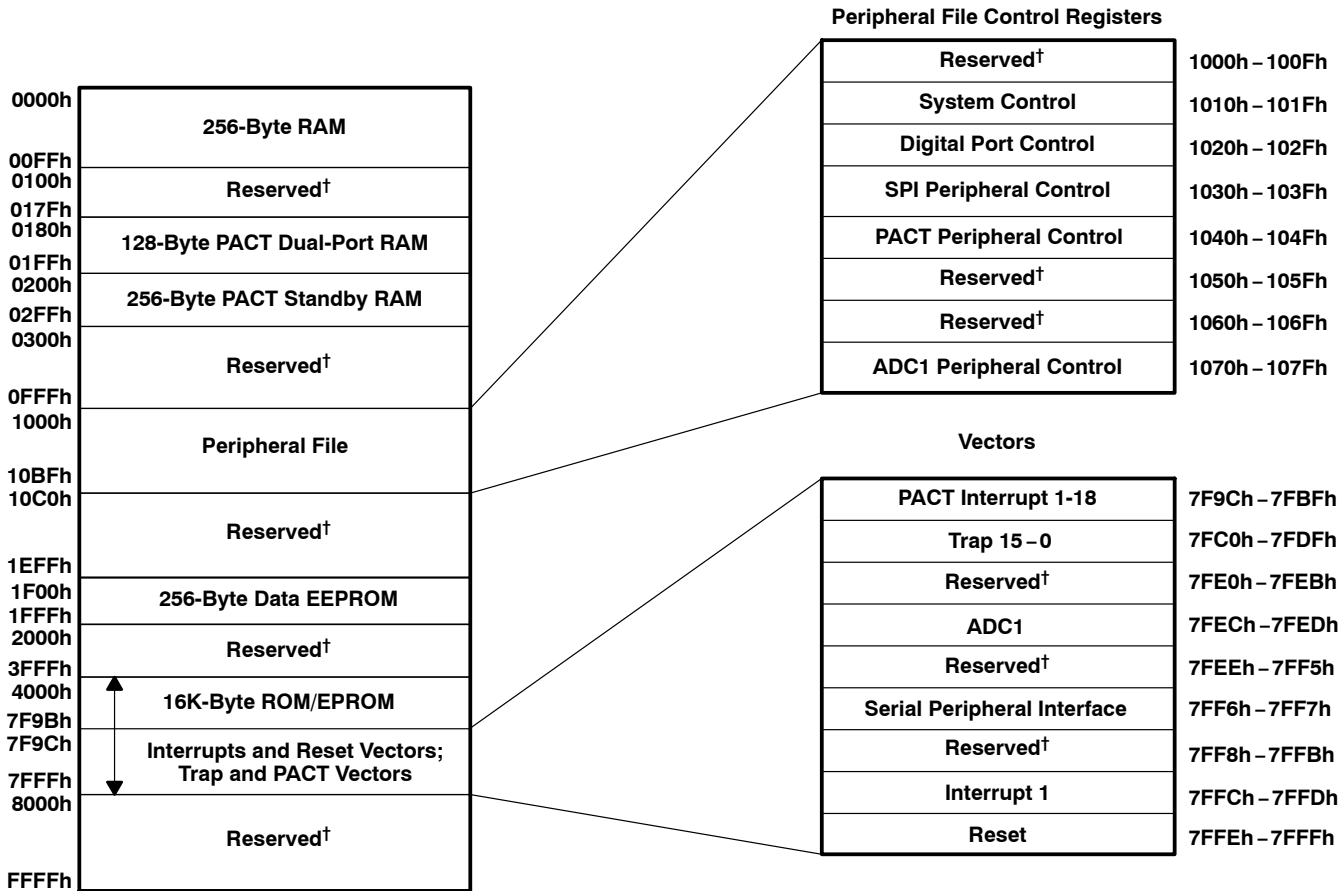


Figure 3. TMS370Cx36 Memory Map

RAM/register file (RF)

Locations within the RAM address space can serve as the RF, general-purpose read/write memory, program memory, or the stack instructions. The TMS370Cx36 devices contain 256 bytes of internal RAM, memory-mapped beginning at location 0000h (R0) and continuing through location 00FFh (R255) which is shown in Figure 1.

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

dual-port RAM

The upper 128 bytes of the register files can be used by the PACT module to contain commands and definitions as well as timer values. Any RAM not used by PACT can be used as an additional CPU register or as general-purpose memory.

standby RAM module

The 256 byte standby RAM is general-purpose and powered through a separate V_{CCSTBY} pin. The data stored in this memory is protected against power failures on the main V_{CC1} pins.

The standby RAM data is saved if the power failure on the main V_{CC1} pins is detected externally and an external reset is generated when V_{CC1} falls below 4.3 V (see Figure 4). The external reset must remain low during the entire power failures. The falling edge of the reset signal is internally detected to set the standby RAM in low-power HALT mode. After the next power up, the $\overline{RESET}$ pin must be pulled high to get out of the HALT mode of the standby RAM. In halt mode, the standby RAM consumes only leakage current.

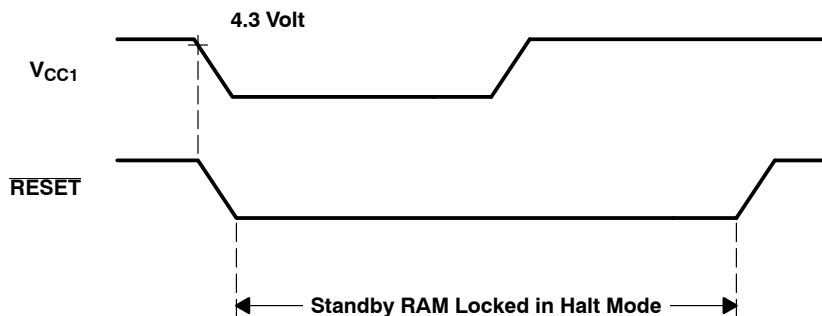


Figure 4. Standby RAM Locked in Halt Mode

peripheral file (PF)

The TMS370Cx36 control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or P for a decimal designator. For example, the system-control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 4 lists the TMS370Cx36 PF address map.

Table 4. TMS370Cx36 Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h – 100Fh	P000 – P00F	Reserved
1010h – 101Fh	P010 – P01F	System and EPROM/EEPROM control registers
1020h – 102Fh	P020 – P02F	Digital I/O port control registers
1030h – 103Fh	P030 – P03F	SPI registers
1040h – 104Fh	P040 – P04F	PACT registers
1050h – 106Fh	P050 – P06F	Reserved
1070h – 107Fh	P070 – P07F	Analog-to-digital converter 1 registers
1080h – 10FFh	P080 – P0FF	Reserved

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data EEPROM

The TMS370Cx36 devices, containing 256 bytes of data EEPROM, have a memory mapped beginning at location 1F00h and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B). The data EEPROM features include the following:

- Programming:
 - Bit-, byte-, and block-write/erase modes.
 - Internal charge pump circuitry. No external EEPROM programming voltage supply is needed.
 - Control register: Data EEPROM programming is controlled by the DEECTL located in the PF frame beginning at location P01A. See Table 5.
 - In-circuit programming capability. There is no need to remove the device to program.
- Write protection. Writes to the data EEPROM are disabled during the following conditions.
 - Reset. All programming of the data EEPROM module is halted.
 - Write protection active. There is one write-protect bit per 32-byte EEPROM block.
 - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 5. Data EEPROM and PROGRAM EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME
P01A	DEECTL	Data EEPROM Control Register
P01B	—	Reserved
P01C	EPCTLL	Program EPROM Control Register – Low Array

program EPROM[†]

The TMS370Cx36 device contains 16K bytes of EPROM mapped, beginning at location 4000h and continuing through location 7FFFh as shown in Figure 3. Reading the program EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the EPROM control register (EPCTLL). The program EPROM module features include:

- Programming
 - In-circuit programming capability if V_{PP} is applied to MC
 - Control register: EPROM programming is controlled by the EPROM control register (EPCTLL) located in the peripheral file (PF) frame at location P01C as shown in Table 5.
- Write protection: Writes to the program EPROM are disabled under the following conditions:
 - Reset: All programming to the EPROM module is halted
 - Low-power modes
 - 13 V not applied to MC

[†] Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments (TI[™]), and addresses 7FECb through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh.

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program ROM[†]

The program ROM consists of 16K bytes of mask programmable read-only memory. The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication. Refer to Figure 3 for ROM memory map.

system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx36 CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are generated internally, while one ($\overline{\text{RESET}}$ pin) is controlled externally. These actions are as follows:

- PACT watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 User's Guide* (literature number SPNU127) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside of the recommended operating range. See the *TMS370 User's Guide* (literature number SPNU127) for more information.
- External $\overline{\text{RESET}}$ pin. A low level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 User's Guide* (literature number SPNU127) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x36 device to reset external system components. Additionally, if a cold start (V_{CC} is off for several hundred milliseconds) condition or oscillator failure occurs or the $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator-fault flag (OSC FLT FLAG, SCCR0.4) and the cold-start flag (COLD START, SCCR0.7) to determine the source of the reset. A reset does not clear these flags. Table 6 lists the reset sources. If none of the sources indicated in Table 6 caused the reset, then the $\overline{\text{RESET}}$ pin was pulled low by the external hardware or the PACT module's watchdog.

Table 6. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Registers A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

When an external reset circuit is connected to the $\overline{\text{RESET}}$ pin, the pin must be held low until the clock signal is valid and V_{CC} is within the operating range. Figure 5 shows a typical reset circuit.

[†] Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments, and addresses 7FECb through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh.

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system reset (continued)

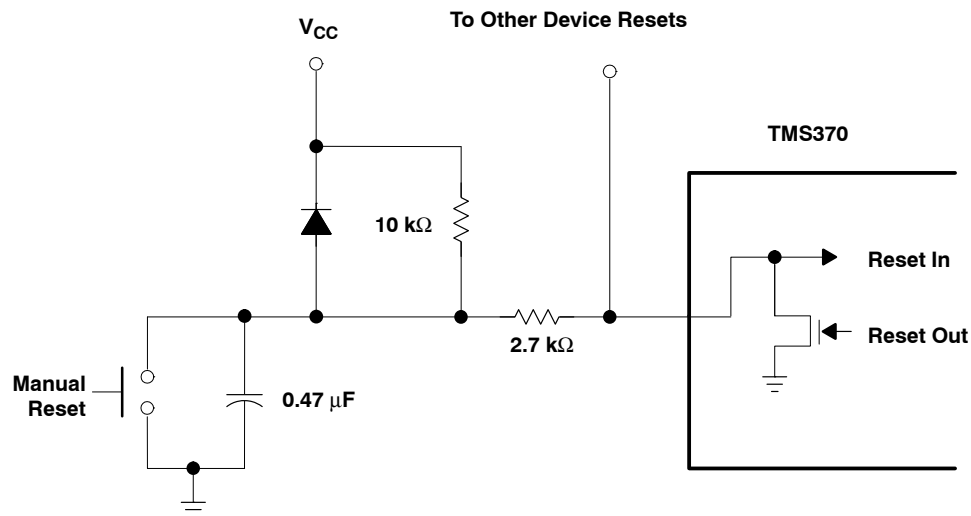


Figure 5. Typical Reset Circuit

interrupts

The TMS370 family software-programmable interrupt structure permits flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 6. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global interrupt mask bits (IE1 and IE2) of the ST.

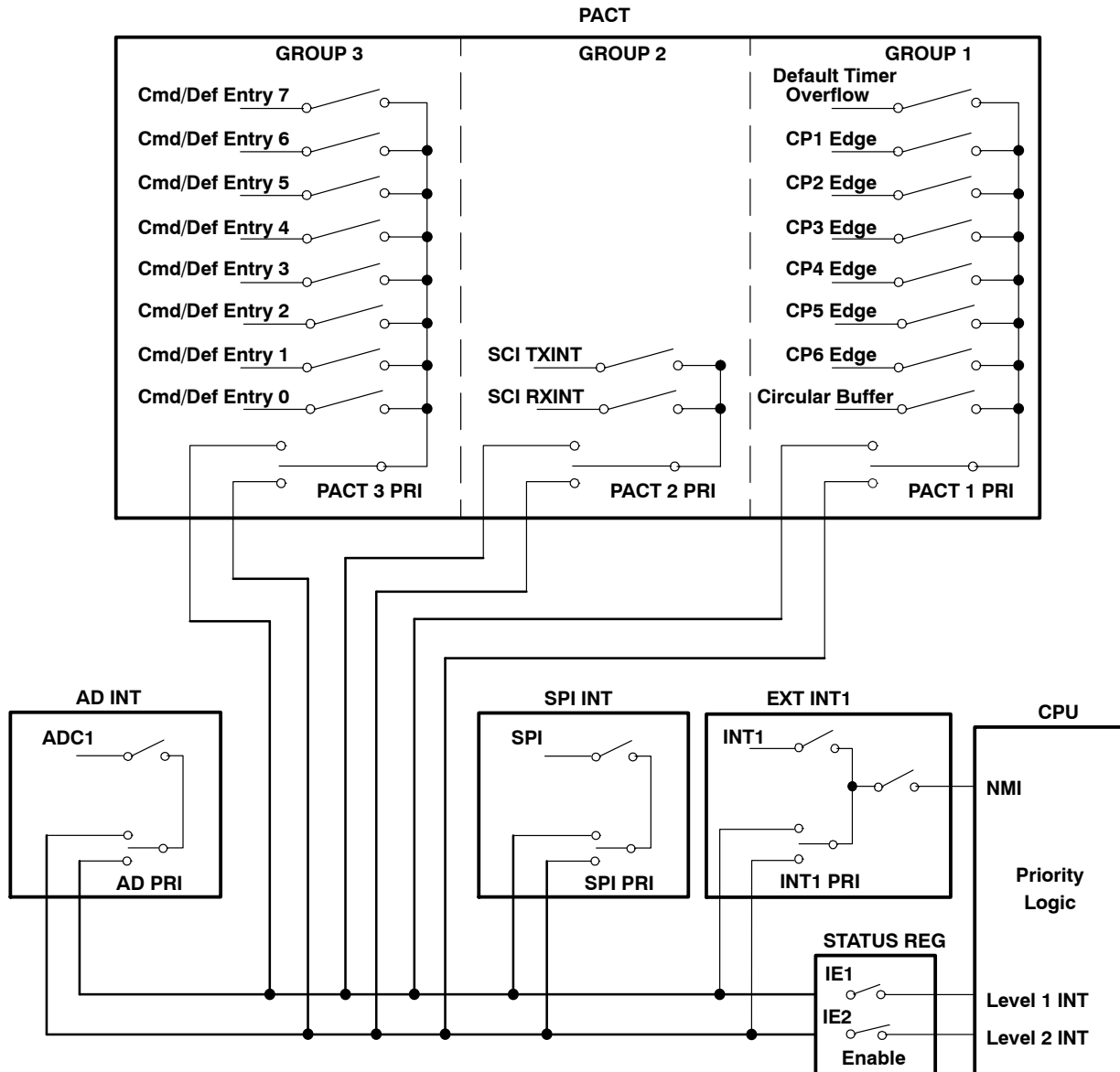


Figure 6. Interrupt Control

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is selectively configured on either the high- or low-priority-interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority

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interrupts (continued)

chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx36 has 21 hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 7. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. A system interrupt may have multiple interrupt sources. All of the interrupt sources are individually maskable by local interrupt enable control bits in the associated peripheral file. Each interrupt source FLAG bit is individually readable for software polling or for determining which interrupt source generated the associated system interrupt.

Twenty of the system interrupts are generated by on-chip peripheral functions, and one external interrupt is supported. Software configuration of the external interrupts is performed through the INT1 control register in peripheral file frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual- or global-enable mask bits. The INT1 NMI bit is protected during non-privileged operation and, therefore, should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupt INT1 can be software configured as a general-purpose input pin if the interrupt function is not required.



interrupts (continued)

Table 7. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	OSC FLT FLG	SYSTEM INTERRUPT	VECTOR ADDRESS	MODULE PRIORITY [†]	PRIORITY IN GROUP
RESET	External RESET Watchdog Overflow Oscillator Fault	COLD START (No Flag) OSC FLT FLAG	RESET [†]	7FFEh, 7FFFh	1	
INT1	External Interrupt 1	INT1 FLAG	INT1 [‡]	7FFCh, 7FFDh	2	
SPI	SPI RX/TX Complete	SPI INT FLAG	SPIINT	7FF6h, 7FF7h	3	
PACT (Group 1)	PACT Circular Buffer	Buffer Half/Full Interrupt Flag	BUFINT	7FB0h, 7FB1h	4	1
	PACT CP6 Event	CP6 INT FLAG	CP6INT	7FB2h, 7FB3h		2
	PACT CP5 Event	CP5 INT FLAG	CP5INT	7FB4h, 7FB5h		3
	PACT CP4 Event	CP4 INT FLAG	CP4INT	7FB6h, 7FB7h		4
	PACT CP3 Event	CP3 INT FLAG	CP3INT	7FB8h, 7FB9h		5
	PACT CP2 Event	CP2 INT FLAG	CP2INT	7FBAh, 7FBBh		6
	PACT CP1 Event	CP1 INT FLAG	CP1INT	7FBCh, 7FBDh		7
	Default Timer Overflow	DEFTIM OVRFL INT FLAG	POVRL INT	7FBEh, 7FBFh		8
PACT (Group 2)	PACT SCI Rx Int	PACT RX RDY	PRXINT	7F9Eh, 7F9Fh	5	1
	PACT SCI Tx Int	PACT TX RDY	PTXINT	7F9Ch, 7F9Dh		2
PACT (Group 3)	PACT Cmd/Def Entry 0	CMD/DEF INT 0 FLAG	CDINT 0	7FA0h, 7FA1h	6	1
	PACT Cmd/Def Entry 1	CMD/DEF INT 1 FLAG	CDINT 1	7FA2h, 7FA3h		2
	PACT Cmd/Def Entry 2	CMD/DEF INT 2 FLAG	CDINT 2	7FA4h, 7FA5h		3
	PACT Cmd/Def Entry 3	CMD/DEF INT 3 FLAG	CDINT 3	7FA6h, 7FA7h		4
	PACT Cmd/Def Entry 4	CMD/DEF INT 4 FLAG	CDINT 4	7FA8h, 7FA9h		5
	PACT Cmd/Def Entry 5	CMD/DEF INT 5 FLAG	CDINT 5	7FAAh, 7FABh		6
	PACT Cmd/Def Entry 6	CMD/DEF INT 6 FLAG	CDINT 6	7FACh, 7FADh		7
	PACT Cmd/Def Entry 7	CMD/DEF INT 7 FLAG	CDINT 7	7FAEh, 7FAFh		8
ADC1	ADC1 Conversion Complete	AD INT FLAG	ADINT	7FECh, 7FEDh	7	

[†] Relative priority within an interrupt level

[‡] Release microcontroller from STANDBY and HALT low-power modes

privileged operation and EEPROM write protection override

The TMS370Cx36 family is designed with significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx36 operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) is set to 1 to enter the nonprivileged mode, disabling write operations to specific configuration-control bits within the PF. Table 8 lists the control bits shown in the table which are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

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privileged operation and EEPROM write protection override (continued)

Table 8. Privilege Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCRO	P010.5 P010.6	PF AUTO WAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
SPIPRI	P03F.5 P03F.6 P03F.7	SPI ESPEN SPI PRIORITY SPI STEST
PACTSCR	P040.0 P040.1 P040.2 P040.3 P040.4	PACT PRESCALE SELECT 0 PACT PRESCALE SELECT 1 PACT PRESCALE SELECT 2 PACT PRESCALE SELECT 3 FAST MODE SELECT
PACTPRI	P04F.0 P04F.1 P04F.2 P04F.3 P04F.4 P04F.5 P04F.7	PACT WD PRESCALE SELECT 0 PACT WD PRESCALE SELECT 1 PACT MODE SELECT PACT GROUP 3 PRIORITY PACT GROUP 2 PRIORITY PACT GROUP 1 PRIORITY PACT STEST
ADPRI	P07F.5 P07F.6 P07F.7	AD ESPEN AD PRIORITY AD STEST

† The privilege bits are shown in a bold typeface and shaded areas in the system configuration registers section of Table 10.

low-power and IDLE modes

The TMS370Cx36 devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact when the mask is manufactured.

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls the low-power mode selection.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, the PACT counter, and the first PACT command entry remain active in all modules. System processing is suspended until a qualified interrupt (hardware RESET or external interrupt on INT1) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx36 is placed in its lowest power consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware RESET or external interrupt on the INT1) is detected. The power-down mode-selection bits are summarized in Table 9.



low-power and IDLE modes (continued)

Table 9. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X [†]	IDLE

[†] X = Don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6-7 bits is ignored. In addition, if an IDLE instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method for always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI is generated always, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (SP, PC, and ST), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the WD timer is inhibited.

clock modules

The 'x36 family provides two clock options that are referred to as divide-by-1 (phase-locked loop) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The 'x36 masked-ROM devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device. The '736A EPROM has only the divide-by-4.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a one-to-one match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency, whereas the divide-by-4 produces a SYSCLK which is one-fourth the frequency of the external resonator. Inside of the divide-by-1 module, the frequency of the external resonator is multiplied by four, and the clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. These are formulated as follows:

$$\text{Divide-by-4 option : } \text{SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option : } \text{SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the reduced EMI. The harmonics of low-speed resonators extend through fewer of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 provides the capability of reducing the resonator speed by four times, and this results in a steeper decay of emissions produced by the oscillator.

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system configuration registers

Table 10 contains system-configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in a bold typeface and shaded areas.

Table 10. Peripheral File Frame 1: System-Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTO WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	Reserved								
P019	Reserved								
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D to P01F	Reserved								

digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 11 shows the specific addresses, registers, and control bits within this peripheral file frame. Table 12 shows the port configuration register setup.

Table 11. Peripheral File Frame 2: Digital Port-Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
P020	Reserved								APOINT1
P021	Port A Control Register 2 (must be 0)								APOINT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPOINT1
P02D	Port D Control Register 2 (must be 0) [†]					—	—	—	DPOINT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 12. Port Configuration Register Setup

PORT	PIN	abcd 00q1	abcd 00y0
A	0 – 7	Data out q	Data In y
D	3 – 7	Data out q	Data In y
a = Port x Control Register 1 b = Port x Control Register 2 c = Data d = Direction			

serial peripheral interface

The SPI is a high-speed synchronous serial I/O port that allows a serial bit stream of programmed length (one to eight bits) to be shifted into and out of the device at a programmable bit transfer rate. The SPI normally is used for communications between the microcontroller and external peripherals or another microcontroller. Typical applications include external I/O or peripheral expansion by way of devices such as shift registers, display drivers, and A/D converters. Multi-device communications are supported by the master/slave operation of the SPI. The SPI module features include the following:

- Three external pins
 - SPISOMI: SPI slave output/master input pin or general-purpose bidirectional I/O pin
 - SPISIMO: SPI slave input/master output pin or general-purpose bidirectional I/O pin
 - SPICLK: SPI serial clock pin or general-purpose bidirectional I/O pin
- Two operational modes: Master and slave

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serial peripheral interface (continued)

- Baud rate: Eight different programmable rates
 - Maximum baud rate in master mode: 2.5M bps at 5-MHz SYSCLK

$$\text{SPI BAUD RATE} = \frac{\text{SYSCLK}}{2 \times 2^b}$$

where b=bit rate in SPICCR.5-3 (range 0–7)

- Maximum baud rate in slave mode: 625K bps at 5-MHz SYSCLK
for maximum slave SPI BAUD RATE < SYSCLK/8
- Data word format: one to eight data bits
- Simultaneous receiver and transmitter operations (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Seven SPI module control registers located in control register frame beginning at address P030h

The SPI module-control registers are listed in Table 13.

Table 13. SPI Module-Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/SLAVE	TALK	SPI INT ENA	SPICTL
P032 to P036	Reserved								
P037	RCVD7	RCVD6	RCVD5	RCVD4	RCVD3	RCVD2	RCVD1	RCVD0	SPIBUF
P038	RESERVED								
P039	SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0	SPIDAT
P03A to P03C	Reserved								
P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
P03F	SPI STEST	SPI PRIORITY	SPI ESPEN	—	—	—	—	—	SPIPRI



The SPI block diagram is illustrated in Figure 7.

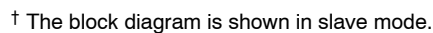


Figure 7. SPI Block Diagram

Traditionally, timers in microcontrollers provide limited capture and compare functions consuming significant CPU processing power and leading to inaccurate timings due to interrupt latencies. The programmable acquisition and control timer (PACT) acts as a coprocessor combining configurable capture and compare features, within a flexible dual-port RAM, able to run real-time tasks with little or no CPU intervention. The PACT structure allows concatenation of tasks, thus enabling the CPU to perform data manipulation while the PACT module both captures and outputs real-time-related information. Since all the PACT control information is held within the dual-port Ram, the CPU can access these parameters quickly.

To use the PACT, the user must set up three distinct areas of memory. The first is the dual-port RAM, which contains the capture area, the commands, and the timer definitions. The second is the peripheral frame. The third is an area near the end of the program memory which holds the interrupt vectors of PACT.

programmable acquisition and control timer (PACT) module (continued)

The PACT module features include the following:

- Input-capture functions on up to six input pins (CP1 to CP6), depending on the mode selected:
 - Mode A: CP1–2 are dedicated capture, CP3–6 are circular buffer capture, and CP6 is also an event pin.
 - Mode B: CP1–4 are dedicated capture, CP5–6 are circular buffer capture, and CP6 is also an event pin.
- Multiple timer-driven outputs on eight pins (OP1 to OP8)
 - Standard compare command: set or clear an output pin whenever the timer/counter is equal to a certain value
 - Virtual timers: enable variations of the PWM's period and provides periodic interrupts to the processor.
 - Double event-compare command: comparisons of the 8-bit event counter with two event-compare values and the actions that can be performed are based on each value:
 - Event-compare 1 matching the event counter: sets or resets the selected output pin (OP1–OP8), generates interrupt, and generates a 32-bit capture into the circular buffer.
 - Event-compare 2 matching the event counter: sets or resets the selected output pin (OP1–OP8), generates interrupt, generates a 32-bit capture into the circular buffer, and resets the 20-bit default timer.
 - Offset timer definition-time from last event:
 - Generates an interrupt when the maximum event count is reached
 - Stores the 16-bit virtual timer in the circular buffer on each event
 - Stores the 20-bit default timer and 8-bit event counter in the circular buffer when the maximum event count is reached
 - Resets the 20-bit hardware default timer when the maximum event count is reached.
 - Conditional-compare command has a timer-compare value and an event-compare value.
 - Generates an interrupt when the event-compare value equals the event counter and the timer-compare value equals the last defined timer
 - Sets or clears one of the seven output pins (OP1–OP7) when the event compare value equals the event counter and the timer-compare value equals the last defined timer
 - Baud rate timer definition: runs the mini-serial communications port built into the PACT module.
- Configurable timer overflow rates
- One 8-bit event counter driven by CP6
- Up to 20-bit timer capability
- Interaction between event counter and timer activity
- Register-based organization allowing direct access to timer parameters by the CPU
- 18 independent interrupt vectors with two priority levels
- Integrated, configurable watchdog with selectable time-out period

programmable acquisition and control timer (PACT) module (continued)

- Mini-serial communications interface works as a simplified full duplex universal asynchronous receiver/transmitter (UART) with independent setup of baud rate for receive and transmit lines.
 - Asynchronous communications mode

$$\text{Asynchronous Baud} = \frac{1}{(\text{Max Virtual Timer Value}) \times (4) \times (\text{PACT Resolution})} \times 10^6$$

where PACT Resolution = SYSCLK × Prescale Value

PACT block diagram

The PACT module block diagram is illustrated in Figure 8.

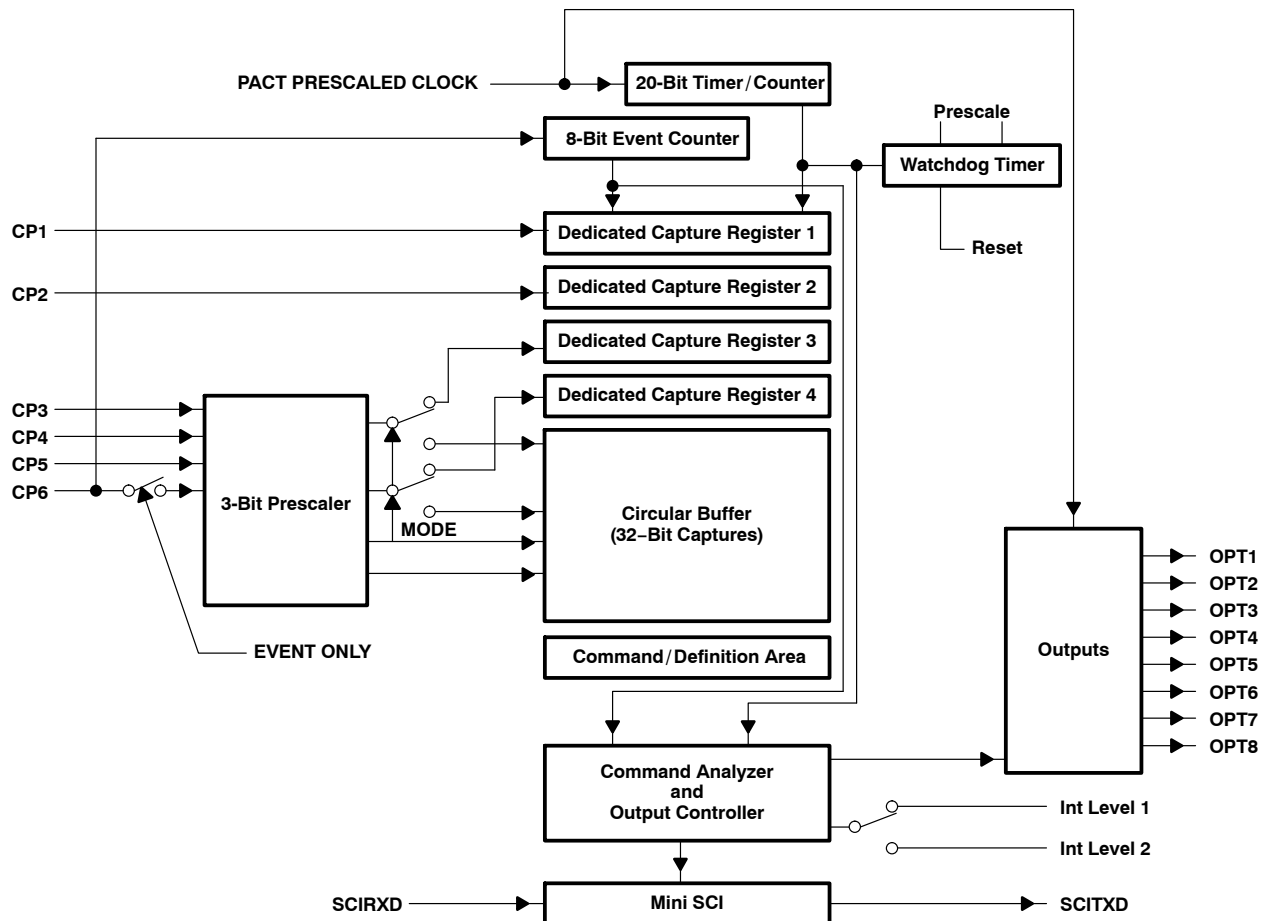


Figure 8. PACT Block diagram

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PACT control registers

The PACT module is controlled and accessed through registers in peripheral frame 4. These registers are listed in Table 14. The bits in shaded boxes are privileged mode bits; that is, they can be written to only in the privileged mode.

Table 14. PACT Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P040	DEFTIM OVRFL INT ENA	DEFTIM OVRFL INT FLAG	CMD/DEF AREA ENA	FAST MODE SELECT	PACT PRESCALE SELECT3	PACT PRESCALE SELECT2	PACT PRESCALE SELECT1	PACT PRESCALE SELECT0	PACTSCR
P041	CMD/DEF AREA INT ENA	—	CMD/DEF AREA START BIT 5	CMD/DEF AREA START BIT 4	CMD/DEF AREA START BIT 3	CMD/DEF AREA START BIT 2	—	—	CDSTART
P042	—	CMD/DEF AREA END BIT 6	CMD/DEF AREA END BIT 5	CMD/DEF AREA END BIT 4	CMD/DEF AREA END BIT 3	CMD/DEF AREA END BIT 2	—	—	CDEND
P043	1	1	BUFFER POINTER BIT 5	BUFFER POINTER BIT 4	BUFFER POINTER BIT 3	BUFFER POINTER BIT 2	BUFFER POINTER BIT 1	—	BUFPTR
P044	Reserved								
P045	PACT RXRDY	PACT TXRDY	PACT PARITY	PACT FE	PACT SCI RX INT ENA	PACT SCI TX INT ENA	—	PACT SCI SW RESET	SCICTLP
P046	PACT RXDT7	PACT RXDT6	PACT RXDT5	PACT RXDT4	PACT RXDT3	PACT RXDT2	PACT RXDT1	PACT RXDT0	RXBUFP
P047	PACT TXDT7	PACT TXDT6	PACT TXDT5	PACT TXDT4	PACT TXDT3	PACT TXDT2	PACT TXDT1	PACT TXDT0	TXBUFP
P048	PACT OP8 STATE	PACT OP7 STATE	PACT OP6 STATE	PACT OP5 STATE	PACT OP4 STATE	PACT OP3 STATE	PACT OP2 STATE	PACT OP1 STATE	PSTATE
P049	CMD/DEF INT 7 FLAG	CMD/DEF INT 6 FLAG	CMD/DEF INT 5 FLAG	CMD/DEF INT 4 FLAG	CMD/DEF INT 3 FLAG	CMD/DEF INT 2 FLAG	CMD/DEF INT 1 FLAG	CMD/DEF INT 0 FLAG	CDFLAGS
P04A	CP2 INT ENA	CP2 INT FLAG	CP2 CAPT RISING EDGE	CP2 CAPT FALLING EDGE	CP1 INT ENA	CP1 INT FLAG	CP1 CAPT RISING EDGE	CP1 CAPT FALLING EDGE	CPCTL1
P04B	CP4 INT ENA	CP4 INT FLAG	CP4 CAPT RISING EDGE	CP4 CAPT FALLING EDGE	CP3 INT ENA	CP3 INT FLAG	CP3 CAPT RISING EDGE	CP3 CAPT FALLING EDGE	CPCTL2
P04C	CP6 INT ENA	CP6 INT FLAG	CP6 CAPT RISING EDGE	CP6 CAPT FALLING EDGE	CP5 INT ENA	CP5 INT FLAG	CP5 CAPT RISING EDGE	CP5 CAPT FALLING EDGE	CPCTL3
P04D	BUFFER HALF/FULL INT ENA	BUFFER HALF/FULL INT FLAG	INPUT CAPT PRESCALE SELECT 3	INPUT CAPT PRESCALE SELECT 2	INPUT CAPT PRESCALE SELECT 1	CP6 EVENT ONLY	EVENT COUNTER SW RESET	OP/ SET/CLR SELECT	CPPRE
P04E	WATCHDOG REST KEY								WDRST
P04F	PACT STEST	PACT SUSPEND	PACT GROUP 1 PRIORITY	PACT GROUP 2 PRIORITY	PACT GROUP 3 PRIORITY	PACT MODE SELECT	PACT WD PRESCALE SELECT 1	PACT WD PRESCALE SELECT 0	PACTPRI

analog-to-digital converter 1 module

The analog-to-digital converter 1 (ADC1) module is an 8-bit, successive approximation converter with internal sample-and-hold circuitry. The module has four multiplexed analog input channels that allow the processor to convert the voltage levels from up to eight different sources. The ADC1 module features include the following:

- Minimum conversion time: 32.8 μ s at 5-MHz SYSCLK
- Ten external pins:
 - Eight analog-input channels (AN0–AN7), any of which can be software-configured as digital inputs (E0–E7) when not needed as analog channels
 - AN1–AN7 also can be configured as positive-input voltage reference.
 - V_{CC3}: ADC1 module high-voltage reference input
 - V_{SS3}: ADC1 module low-voltage reference input
- The ADDATA register, which contains the digital result of the last ADC1 conversion.
- ADC1 operations can be accomplished through either interrupt-driven or polled algorithms.
- Six ADC1 module control registers located in the control-register frame beginning at address 1070h

The ADC1 module control registers are listed in Table 15.

Table 15. ADC1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A/D Conversion Data Register								ADDATA
P073 to P07C	RESERVED								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI

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analog-to-digital converter 1 module (continued)

The ADC1 module block diagram is illustrated in Figure 9.

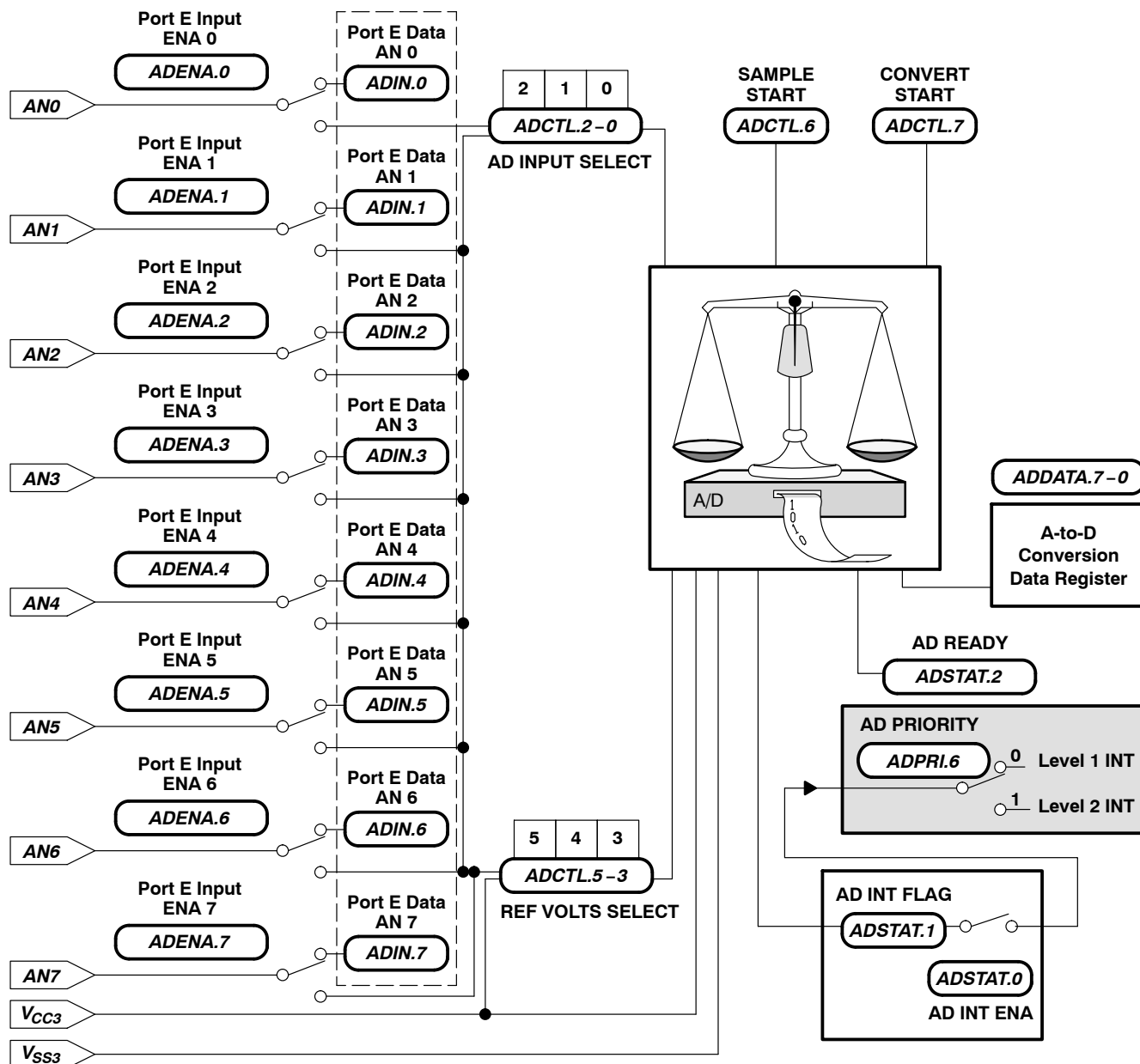


Figure 9. ADC1 Block Diagram

instruction set overview

Table 16 provides an opcode to instruction cross reference of all 73 instructions and 274 opcodes of the '370Cx36 instruction set. The numbers at the top of this table represent the most significant nibble (MSN) of the opcode while the numbers at the left side of the table represent the least significant nibble (LSN). The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.



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Table 16. TMS370 Family Opcode/Instruction Map[†]

		MSN																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0		JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8				CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
1		JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7	
2		JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7	
3		JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8	
4		JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes	
5		JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14		
6		JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6	
7		JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10	
8		JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7	
9		JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9	
A		JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12	
B		JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8	

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

Table 16. TMS370 Family Opcode/Instruction Map[†] (Continued)

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L S N	C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
	D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
	E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
	F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):

F4	8	MOVW *n[Rn] 4/15	DIV Rn,A 3/14-63
F4	9	JMPL *n[Rn] 4/16	
F4	A	MOV *n[Rn],A 4/17	
F4	B	MOV A,*n[Rn] 4/16	
F4	C	BR *n[Rn] 4/16	
F4	D	CMP *n[Rn],A 4/18	
F4	E	CALL *n[Rn] 4/20	
F4	F	CALLR *n[Rn] 4/22	

Legend:

- * = Indirect addressing operand prefix
- & = Direct addressing operand prefix
- # = immediate operand
- #16 = immediate 16-bit number
- lab = 16-label
- n = immediate 8-bit number
- Pd = Peripheral register containing destination type
- Pn = Peripheral register
- Ps = Peripheral register containing source byte
- ra = Relative address
- Rd = Register containing destination type
- Rn = Register file
- Rp = Register pair
- Rpd = Destination register pair
- Rps = Source Register pair
- Rs = Register containing source byte

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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development system support

The TMS370 family development support tools include an assembler, a C-compiler, a linker, CDT and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850-02 for PC)
 - Includes extensive macro capability
 - Provides high-speed operation
 - Includes format conversion utilities for popular formats
- ANSI C Compiler (Part No. TMDS3740855-02 for PC, Part No. TMDS3740555-09 for HP700™, SUN-3™ or SUN-4™)
 - Generate assembly code for the TMS370 that can be inspected easily
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables direct reference the TMS370's port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (Compact Development Tool) PACT real-time in-circuit emulation
 - Base (Part Number EDSCDT37P – for PC, requires cable)
 - Cable for 44-pin PLCC (Part No. EDSTRG44PLCC36)
 - EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Includes compatibility to upload/download program and data memory
 - Execute programs and software routines
 - Includes 1024-sample trace buffer
 - Includes single-step executable instructions
 - Uses software breakpoints to halt program execution at selected address
- Microcontroller programmer
 - Base (Part No. TMDS3760500A – for PC, requires programmer head)
 - Single unit head for 44-pin PLCC (Part No. TMDS3780512A)
 - PC-based, window/function-key-oriented user interface for ease of use and rapid learning environment

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device numbering conventions

Figure 10 illustrates the numbering and symbol nomenclature for the TMS370Cx36 family.

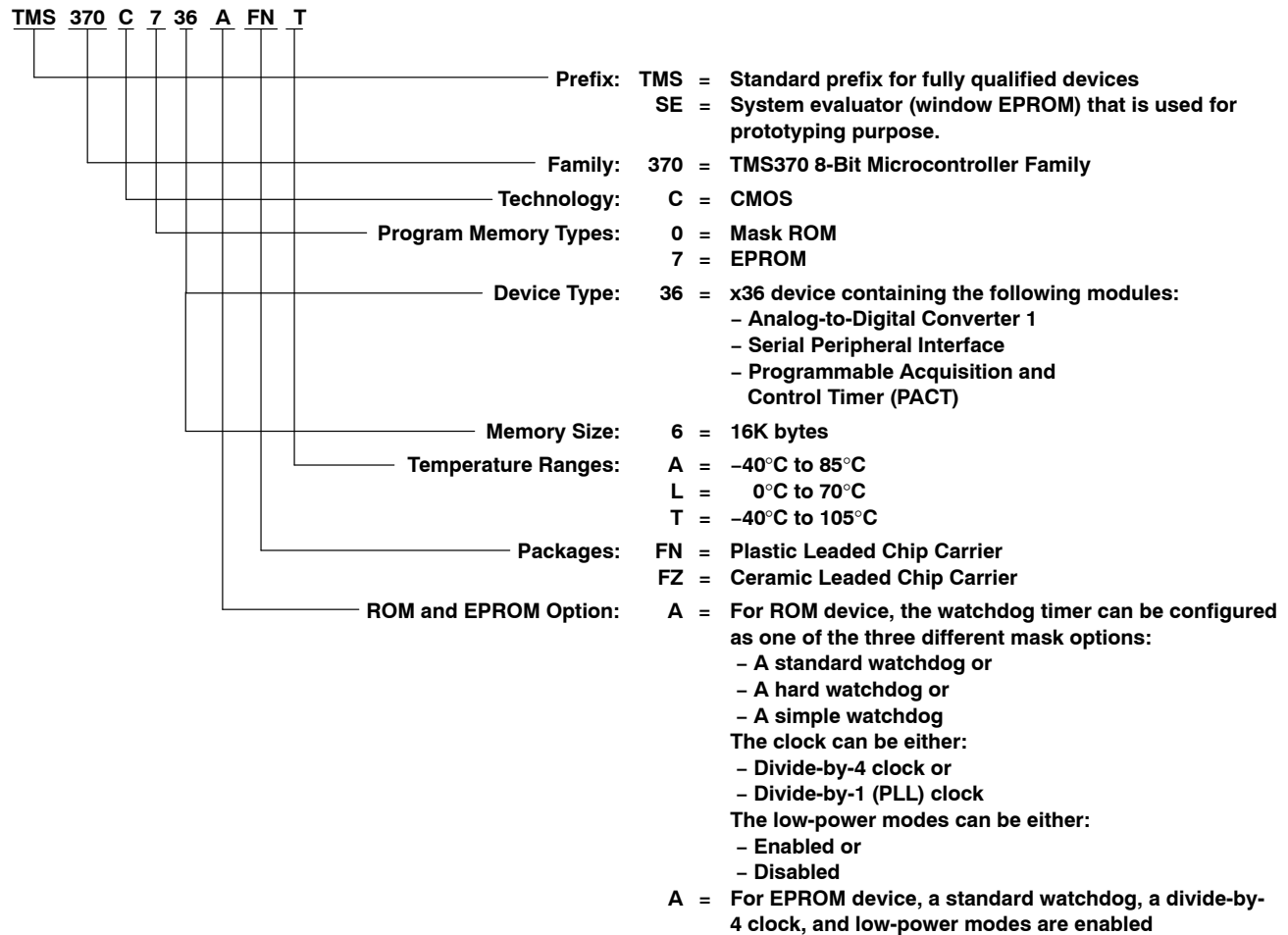


Figure 10. TMS370Cx36 Family Nomenclature

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device part numbers

Table 17 provides a listing of all the 'x36 devices available. The device part number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog timer options desired. Each device can have only one of the three possible watchdog timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 17. Device Part Numbers

DEVICE PART NUMBERS FOR 44 PINS (LCC)
TMS370C036AFNA TMS370C036AFNL TMS370C036AFNT
TMS370C736AFNT
SE370C736AFZT [†]

[†] System evaluators are for use in prototype environment, and their reliability has not been characterized.

new code release form

Figure 11 shows a sample of the new code release form.

NEW CODE RELEASE FORM TEXAS INSTRUMENTS TMS370 MICROCONTROLLER PRODUCTS		DATE: _____																											
To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information:																													
1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media) 2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.																													
Company Name: _____ Street Address: _____ Street Address: _____ City: _____ State _____ Zip _____ Customer Part Number: _____ Customer Application: _____		Contact Mr./Ms.: _____ Phone: (_____) _____ Ext.: _____ Customer Purchase Order Number: _____ Customer Print Number *Yes: _____ # _____ No: _____ (Std. spec to be followed) *If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.																											
TMS370 Device: _____ TI Customer ROM Number: _____ (provided by Texas Instruments) OSCILLATOR FREQUENCY <table border="0" style="width: 100%;"> <tr> <td></td> <td style="text-align: center;">MIN</td> <td style="text-align: center;">TYP</td> <td style="text-align: center;">MAX</td> </tr> <tr> <td>☐ External Drive (CLKIN)</td> <td>_____</td> <td>_____</td> <td>_____</td> </tr> <tr> <td>☐ Crystal</td> <td>_____</td> <td>_____</td> <td>_____</td> </tr> <tr> <td>☐ Ceramic Resonator</td> <td>_____</td> <td>_____</td> <td>_____</td> </tr> </table> ☐ Supply Voltage MIN: _____ MAX: _____ (std range: 4.5V to 5.5V)			MIN	TYP	MAX	☐ External Drive (CLKIN)	_____	_____	_____	☐ Crystal	_____	_____	_____	☐ Ceramic Resonator	_____	_____	_____	CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS <table border="0" style="width: 100%; font-size: small;"> <tr> <td style="vertical-align: top;"> Low Power Modes ☐ Enabled ☐ Disabled </td> <td style="vertical-align: top;"> Watchdog counter ☐ Standard ☐ Hard Enabled ☐ Simple Counter </td> <td style="vertical-align: top;"> Clock Type ☐ Standard (/4) ☐ PLL (/1) </td> </tr> </table> NOTE: Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the <i>TMS370 Family User's Guide</i> (literature number SPNU127) or the <i>TMS370 Family Data Manual</i> (literature number SPNS014B). PACKAGE TYPE <table border="0" style="width: 100%;"> <tr> <td>☐ 'N' 28-pin PDIP</td> <td>☐ "FN" 44-pin PLCC</td> </tr> <tr> <td>☐ "FN" 28-pin PLCC</td> <td>☐ "FN" 68-pin PLCC</td> </tr> <tr> <td>☐ "N" 40-pin PDIP</td> <td>☐ "NM" 64-pin PSDIP</td> </tr> <tr> <td colspan="2">☐ "NJ" 40-pin PSDIP (formerly known as N2)</td> </tr> </table> BUS EXPANSION ☐ YES ☐ NO	Low Power Modes ☐ Enabled ☐ Disabled	Watchdog counter ☐ Standard ☐ Hard Enabled ☐ Simple Counter	Clock Type ☐ Standard (/4) ☐ PLL (/1)	☐ 'N' 28-pin PDIP	☐ "FN" 44-pin PLCC	☐ "FN" 28-pin PLCC	☐ "FN" 68-pin PLCC	☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP	☐ "NJ" 40-pin PSDIP (formerly known as N2)	
	MIN	TYP	MAX																										
☐ External Drive (CLKIN)	_____	_____	_____																										
☐ Crystal	_____	_____	_____																										
☐ Ceramic Resonator	_____	_____	_____																										
Low Power Modes ☐ Enabled ☐ Disabled	Watchdog counter ☐ Standard ☐ Hard Enabled ☐ Simple Counter	Clock Type ☐ Standard (/4) ☐ PLL (/1)																											
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☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP																												
☐ "NJ" 40-pin PSDIP (formerly known as N2)																													
SYMBOLIZATION ☐ TI standard symbolization ☐ TI standard w/customer part number ☐ Customer symbolization (per attached spec, subject to approval)																													
NON-STANDARD SPECIFICATIONS: ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.																													
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Figure 11. Sample New Code Release Form

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Table 18. Peripheral File Frame Compilation

Table 18 is a collection of all the peripheral file frames used in the 'Cx36 (provided for a quick reference).

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	System Configuration Registers								
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTO WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT / STANDBY	PWRDWN / IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	Reserved								
P019	Reserved								
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D	Reserved								
P01E	Reserved								
P01F	Reserved								
	Digital Port Control Registers								
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0) [†]					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR
	SPI Module Control Register Memory Map								
P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/SLAVE	TALK	SPI INT ENA	SPICTL
P032 to P036	Reserved								
P037	RCVD7	RCVD6	RCVD5	RCVD4	RCVD3	RCVD2	RCVD1	RCVD0	SPIBUF
P038	Reserved								
P039	SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0	SPIDAT

[†] To configure D3 as SYSCLK, set port D register 2 = 08h.

Table 18. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P03A to P03C	Reserved								
P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
P03F	SPI STEST	SPI PRIORITY	SPI ESPEN	—	—	—	—	—	SPIPRI
PACT Module Register Memory Map									
P040	DEFTIM OVRFL INT ENA	DEFTIM OVRFL INT FLAG	CMD/DEF AREA ENA	FAST MODE SELECT	PACT PRESCALE SELECT3	PACT PRESCALE SELECT2	PACT PRESCALE SELECT1	PACT PRESCALE SELECT0	PACTSCR
P041	CMD/DEF AREA INT ENA	—	CMD/DEF AREA START BIT 5	CMD/DEF AREA START BIT 4	CMD/DEF AREA START BIT 3	CMD/DEF AREA START BIT 2	—	—	CDSTART
P042	—	CMD/DEF AREA END BIT 6	CMD/DEF AREA END BIT 5	CMD/DEF AREA END BIT 4	CMD/DEF AREA END BIT 3	CMD/DEF AREA END BIT 2	—	—	CDEND
P043	1	1	BUFFER POINTER BIT 5	BUFFER POINTER BIT 4	BUFFER POINTER BIT 3	BUFFER POINTER BIT 2	BUFFER POINTER BIT 1	—	BUFPTR
P044	Reserved								
P045	PACT RXRDY	PACT TXRDY	PACT PARITY	PACT FE	PACT SCI RX INT ENA	PACT SCI TX INT ENA	—	PACT SCI SW RESET	SCICTL
P046	PACT RXDT7	PACT RXDT6	PACT RXDT5	PACT RXDT4	PACT RXDT3	PACT RXDT2	PACT RXDT1	PACT RXDT0	RXBUFP
P047	PACT TXDT7	PACT TXDT6	PACT TXDT5	PACT TXDT4	PACT TXDT3	PACT TXDT2	PACT TXDT1	PACT TXDT0	TXBUFP
P048	PACT OP8 STATE	PACT OP7 STATE	PACT OP6 STATE	PACT OP5 STATE	PACT OP4 STATE	PACT OP3 STATE	PACT OP2 STATE	PACT OP1 STATE	PSTATE
P049	CMD/DEF INT 7 FLAG	CMD/DEF INT 6 FLAG	CMD/DEF INT 5 FLAG	CMD/DEF INT 4 FLAG	CMD/DEF INT 3 FLAG	CMD/DEF INT 2 FLAG	CMD/DEF INT 1 FLAG	CMD/DEF INT 0 FLAG	CDFLAGS
P04A	CP2 INT ENA	CP2 INT FLAG	CP2 CAPT RISING EDGE	CP2 CAPT FALLING EDGE	CP1 INT ENA	CP1 INT FLAG	CP1 CAPT RISING EDGE	CP1 CAPT FALLING EDGE	CPCTL1
P04B	CP4 INT ENA	CP4 INT FLAG	CP4 CAPT RISING EDGE	CP4 CAPT FALLING EDGE	CP3 INT ENA	CP3 INT FLAG	CP3 CAPT RISING EDGE	CP3 CAPT FALLING EDGE	CPCTL2
P04C	CP6 INT ENA	CP6 INT FLAG	CP6 CAPT RISING EDGE	CP6 CAPT FALLING EDGE	CP5 INT ENA	CP5 INT FLAG	CP5 CAPT RISING EDGE	CP5 CAPT FALLING EDGE	CPCTL3
P04D	BUFFER HALF/FULL INT ENA	BUFFER HALF/FULL INT FLAG	INPUT CAPT PRESCALE SELECT 3	INPUT CAPT PRESCALE SELECT 2	INPUT CAPT PRESCALE SELECT 1	CP6 EVENT ONLY	EVENT COUNTER SW RESET	OP/ SET/CLR SELECT	CPPRE

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Table 18. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P04E	WATCHDOG RESET KEY								WDRST
P04F	PACT TEST	PACT SUSPEND	PACT GROUP 1 PRIORITY	PACT GROUP 2 PRIORITY	PACT GROUP 3 PRIORITY	PACT MODE SELECT	PACT WD PRESCALE SELECT 1	PACT WD PRESCALE SELECT 0	PACTPRI
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	ADC1 Conversion Data Register								ADDATA
P073 to P07C	RESERVED								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC1} (see Note 4)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC}) (see Note 5)	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	1 W
Operating free-air temperature, T_A : L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 4. Unless otherwise noted, all voltage values are with respect to V_{SS1} .

5. Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage (see Note 4)	4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 6)	3		5.5	V
V_{CCSTBY}	Standby RAM supply voltage	4.5	5	5.5	V
	Standby RAM data retention supply voltage (see Note 6)	3		5.5	
V_{CC3}	Analog supply voltage (see Note 4)	4.5	5	5.5	V
V_{SS3}	Analog supply ground	– 0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC		0.8	V
		MC, normal operation		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET		V_{CC1}	V
		XTAL2/CLKIN		$0.8 V_{CC1}$	
		RESET		$0.7 V_{CC1}$	
V_{MC}	MC (mode control) voltage	EEPROM write protect override (WPO)		13	V
		EPROM programming voltage (V_{PP})		13.5	
		Microcomputer		0.3	
T_A	Operating free-air temperature	L version		70	°C
		A version		85	
		T version		105	

NOTES: 4. Unless otherwise noted, all voltage values are with respect to V_{SS1} .

6. RESET must be externally activated when V_{CC1} or SYSCLK is not within the recommended operating range.

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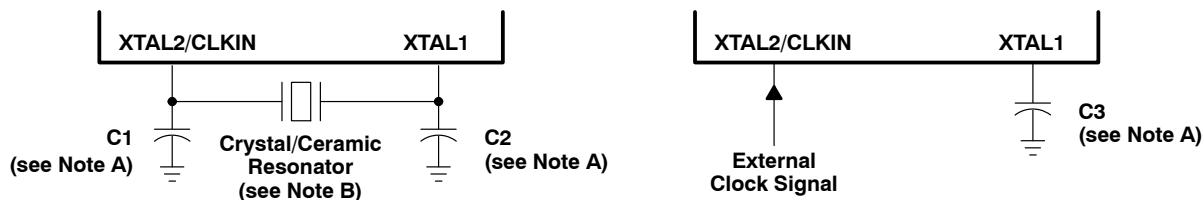
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

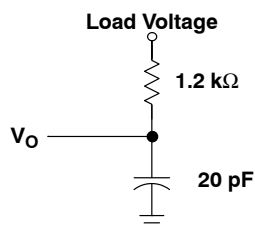
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OL}	Low-level output voltage	All outputs	I _{OL} = 1.4 mA			0.4	V
V _{OH}	High-level output voltage	All outputs except PACT outputs	I _{OH} = − 50 μA		0.9 V _{CC1}		V
		PACT outputs	I _{OH} = − 50 μA		0.7 V _{CC1}		
		All outputs	I _{OH} = − 2 mA		2.4		
I _I	Input current	MC	0 V ≤ V _I ≤ 0.3 V			10	μA
			0.3 V < V _I < V _{CC1} − 0.3 V			50	μA
			V _{CC1} − 0.3 < V _I < V _{CC1} + 0.3 V			10	μA
			V _{CC1} + 0.3 V < V _I < 13 V			650	μA
		I/O pins	0 V < V _I < V _{CC1}			± 10	μA
I _{OL}	Low-level output current	All outputs	V _{OL} = 0.4 V		1.4		mA
I _{OH}	High-level output current	All outputs	V _{OH} = 0.9 V _{CC1}		− 50		μA
			V _{OH} = 2.4 V		− 2		mA
I _{CC1}	Supply current (operating mode) OSC POWER bit = 0		See Notes 7 and 8 SYSCLK = 5 MHz		36	45	mA
	Supply current (STANDBY mode) OSC POWER bit = 0		See Notes 7 and 8 SYSCLK = 5 MHz		7	12	mA
	Supply current (HALT mode)		See Notes 7 and 8 XTAL2/CLKIN < 0.2 V		5	30	μA
I _{CCSTBY}	Standby RAM supply current (operating mode OSC POWER bit = 0)		SYSCLK = 5 MHz V _{CCSTBY} = 4.5 V		1	1.5	mA

- NOTES: 7. Single chip mode, ports configured as inputs or outputs with no load. All inputs $\leq 0.2 \text{ V}$ or $\geq V_{CC1} - 0.2 \text{ V}$.
8. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = $0.01 \text{ mA} \times (\text{total load capacitance} + \text{crystal capacitance in pF})$.



NOTES: A. The values of C1 and C2 are typically 15 pF and C3 value is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.
B. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.

Figure 12. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4 \text{ V}$; Load Voltage = 0 V

Case 2: $V_O = V_{OL} = 0.4 \text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 13. Typical Output Load Circuit (See Note A)

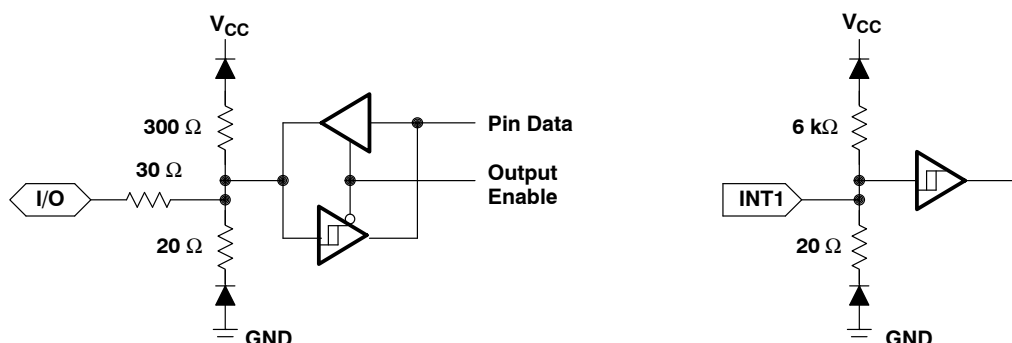


Figure 14. Typical Buffer Circuitry

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PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

AR	Array	SC	SYSCLK
B	Byte	SIMO	SPISIMO
CI	XTAL2/CLKIN	SOMI	SPISOMI
M	Master mode	SPC	SPICLK
S	Slave mode		

Lowercase subscripts and their meanings are:

c	cycle time (period)	su	setup time
d	delay time	v	valid time
f	fall time	w	pulse duration (width)
r	rise time		

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid

All timings are measured between high and low measurement points as indicated in Figure 15 and Figure 16.

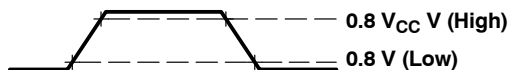


Figure 15. XTAL2/CLKIN Measurement Points

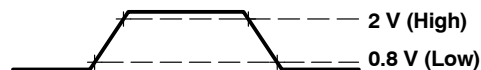


Figure 16. General Measurement Points

external clocking requirements for clock divided by 4 (see Note 9 and Figure 17)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(Cl)}$ Pulse duration, XTAL2/CLKIN (see Note 10)	20		ns
2	$t_{r(Cl)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN Crystal operating frequency	2	20	MHz
	SYSCLK Internal system clock operating frequency [†]	0.5	5	MHz

[†] SYSCLK = CLKIN/4

NOTES: 9. For V_{IL} and V_{IH} , refer to recommended operating conditions.

10. This pulse may be either a high pulse, as illustrated below, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

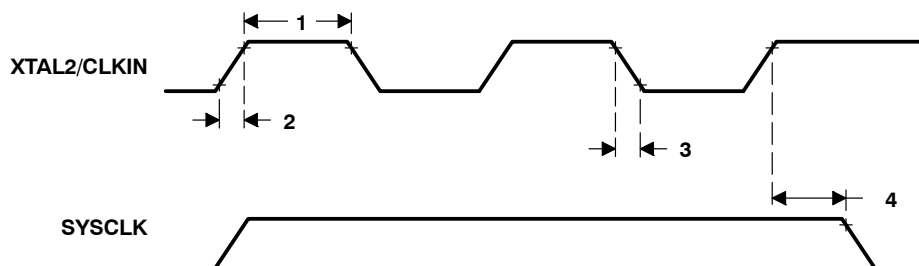


Figure 17. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL) (see Note 9 and Figure 18)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(Cl)}$ Pulse duration, XTAL2/CLKIN (see Note 10)	20		ns
2	$t_{r(Cl)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN Crystal operating frequency	2	5	MHz
	SYSCLK Internal system clock operating frequency [†]	2	5	MHz

[†] SYSCLK = CLKIN/1

NOTES: 9. For V_{IL} and V_{IH} , refer to recommended operating conditions.

10. This pulse can be either a high pulse, as illustrated below, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

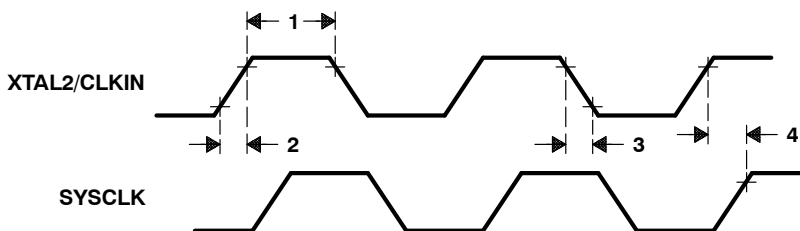


Figure 18. External Clock Timing for Divide-by-1

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switching characteristics and timing requirements (see Note 11 and Figure 19)

NO.	PARAMETER		MIN	MAX	UNIT	
5	t _c	Cycle time, SYSCLK (system clock)	Divide by 4	200	2000	ns
			Divide by 1	200	500	
6	t _{w(SCL)}	Pulse duration, SYSCLK low	0.5 t _c –20	0.5 t _c	ns	
7	t _{w(SCH)}	Pulse duration, SYSCLK high	0.5 t _c	0.5 t _c + 20	ns	

NOTE 11: t_c = system clock cycle time = $1 / \text{SYSCLK}$

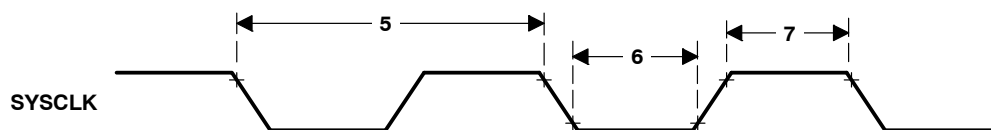


Figure 19. SYSCLK Timing

general purpose output signal switching time requirements (see Figure 20)

	MIN	TYP	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns

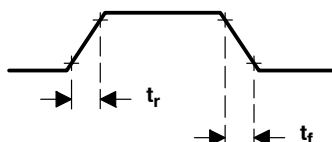


Figure 20. Signal Switching Timing

recommended EEPROM timing requirements for programming

	MIN	MAX	UNIT
$t_{w(PGM)B}$ Pulse duration, programming signal to ensure valid data is stored (byte mode)	10		ms
$t_{w(PGM)AR}$ Pulse duration, programming signal to ensure valid data is stored (array mode)	20		ms

recommended EPROM operating conditions for programming

	MIN	TYP	MAX	UNIT
V_{CC} Supply voltage	4.75	5.5	6	V
V_{PP} Supply voltage at MC pin	13	13.2	13.5	V
I_{PP} Supply current at MC pin during programming ($V_{PP} = 13$ V)		30	50	mA
SYSCLK System clock	Divide by 4	0.5	5	MHz
	Divide by 1	2	5	

recommended EPROM timing requirements for programming

	MIN	TYP	MAX	UNIT
$t_{w(EPGM)}$ Pulse duration, programming signal (see Note 12)	0.40	0.50	3	ms

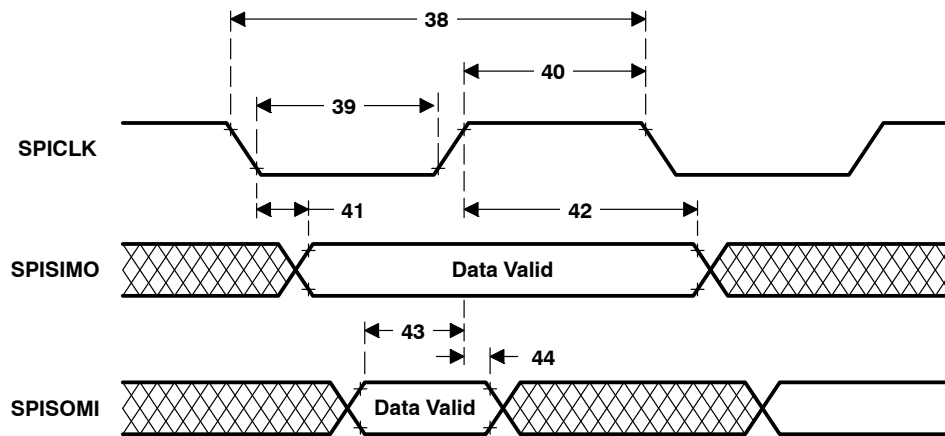
NOTE 12: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.



SPI master mode external timing characteristics and requirements (see Note 11 and Figure 21)

NO.		MIN	MAX	UNIT
38	$t_{c(SPC)M}$ Cycle time, SPICLK	$2t_c$	$256t_c$	ns
39	$t_{w(SPCL)M}$ Pulse duration, SPICLK low	$t_c - 45$	$0.5t_{c(SPC)} + 45$	ns
40	$t_{w(SPCH)M}$ Pulse duration, SPICLK high	$t_c - 55$	$0.5t_{c(SPC)} + 45$	ns
41	$t_{d(SPCL-SIMOV)M}$ Delay time, SPISIMO valid after SPICLK low (polarity = 1)	- 65	50	ns
42	$t_{v(SPCH-SIMO)M}$ Valid time, SPISIMO data valid after SPICLK high (polarity = 1)	$t_{w(SPCH)} - 50$		ns
43	$t_{su(SOMI-SPCH)M}$ Setup time, SPISOMI to SPICLK high (polarity = 1)	$0.25 t_c + 150$		ns
44	$t_{v(SPCH-SOMI)M}$ Valid time, SPISOMI data valid after SPICLK high (polarity = 1)	0		ns

NOTE 11: t_c = system clock cycle time = $1/\text{SYSCLK}$



† The diagram is for polarity = 1. SPICLK is inverted when polarity = 0.

Figure 21. SPI Master External Timing[†]

TMS370Cx36

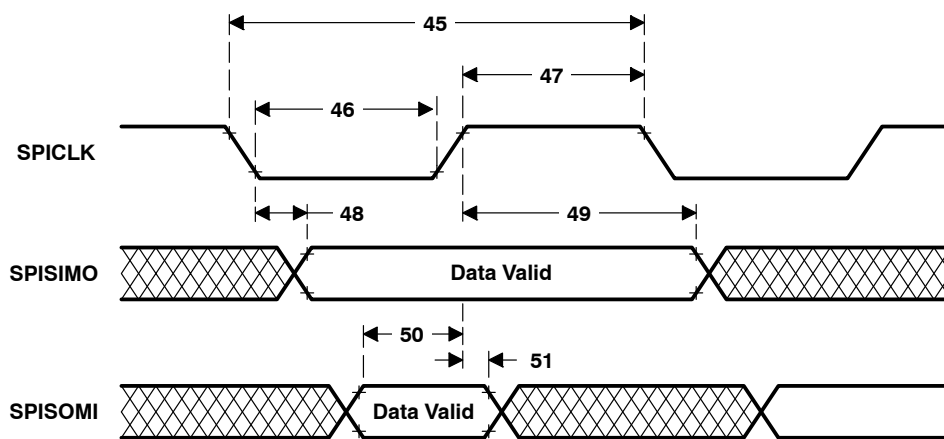
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SPI slave mode external timing characteristics and requirements (see Note 11 and Figure 22)

NO.		MIN	MAX	UNIT
45	$t_{c(SPC)}S$ Cycle time, SPICLK	$8t_c$		ns
46	$t_{w(SPCL)}S$ Pulse duration, SPICLK low	$4t_c - 45$	$0.5t_{c(SPC)}S + 45$	ns
47	$t_{w(SPCH)}S$ Pulse duration, SPICLK high	$4t_c - 45$	$0.5t_{c(SPC)}S + 45$	ns
48	$t_{d(SPCL-SOMI)}S$ Delay time, SPISOMI valid after SPICLK low (polarity = 1)		$3.25t_c + 130$	ns
49	$t_{v(SPCH-SOMI)}S$ Valid time, SPISOMI data valid after SPICLK high (polarity = 1)	$t_{w(SPCH)}S$		ns
50	$t_{su(SIMO-SPCH)}S$ Setup time, SPISIMO to SPICLK high (polarity = 1)	0		ns
51	$t_{v(SPCH-SIMO)}S$ Valid time, SPISIMO data after SPICLK high (polarity = 1)	$3t_c + 100$		ns

NOTE 11: t_c = system clock cycle time = 1 / SYSCLK



† The diagram is for polarity = 1. SPICLK is inverted when polarity = 0.

Figure 22. SPI Slave External Timing†

ADC1 converter

The ADC1 converter has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3} . The purpose is to enhance ADC1 performance by preventing digital switching noise of the logic circuitry that can be present on V_{SS1} and V_{CC1} from coupling into the ADC1 analog stage. All ADC1 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution 8-bits (256 values)
 Monotonic Yes
 Output conversion mode 00h to FFh (00 for $V_I \leq V_{SS3}$; FF for $V_I \leq V_{ref}$)
 Conversion time (excluding sample time) $164 t_c$

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC3} Analog supply voltage	4.5	5	5.5	V
	$V_{CC3}-0.3$		$V_{CC3}+0.3$	
V_{SS3} Analog ground	$V_{SS3}-0.3$		$V_{SS3}+0.3$	V
V_{ref} Non- V_{CC3} reference [†]	2.5	V_{CC3}	$V_{CC3} + 0.1$	V
Analog input for conversion	V_{SS3}		V_{ref}	V

[†] V_{ref} must be stable, within $\pm 1/2$ LSB of the required resolution, during the entire conversion time.

operating characteristics over recommended ranges operating conditions

PARAMETER			MIN	MAX	UNIT
Absolute accuracy†		V _{CC3} = 5.5 V V _{ref} = 5.1 V	± 1.5		LSB
Differential/integral linearity error†‡		V _{CC3} = 5.5 V V _{ref} = 5.1 V	± 0.9		LSB
I _{CC3}	Analog supply current	Converting	2		mA
		Nonconverting	5		μA
I _I	Input current, AN0 – AN7	0 V ≤ V _I ≤ 5.5 V	2		μA
I _{ref}	Input charge current		1		mA
Z _{ref}	Source impedance of V _{ref}	SYSCLK ≤ 3 MHz	24		kΩ
		3 MHz < SYSCLK ≤ 5 MHz	10		kΩ

[†] Absolute resolution = 20 mV. At $V_{ref} = 5 \text{ V}$, this is one LSB. As V_{ref} decreases, LSB size decreases; therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

[‡] Excluding quantization error of $1/2$ LSB

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ADC1 converter (continued)

The ADC1 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined so that the high-impedance can be accommodated without penalty to the low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC1 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter will reset the SAMPLE START and CONVERT START bits, signaling that a conversion has started and that the analog signal can be removed.

analog timing requirements (see Figure 23)

	MIN	MAX	UNIT
$t_{su(S)}$ Setup time, analog to sample command	0		ns
$t_{h(AN)}$ Hold time, analog input from start of conversion	$18t_c$		ns
$t_w(S)$ Pulse duration, sample time per kilo- Ω of source impedance [†]	1		$\mu s/k\Omega$

[†] The value given is valid for a signal with a source impedance > 1 k Ω . If the source impedance is < 1 k Ω , use a minimum sampling time of 1 μs .

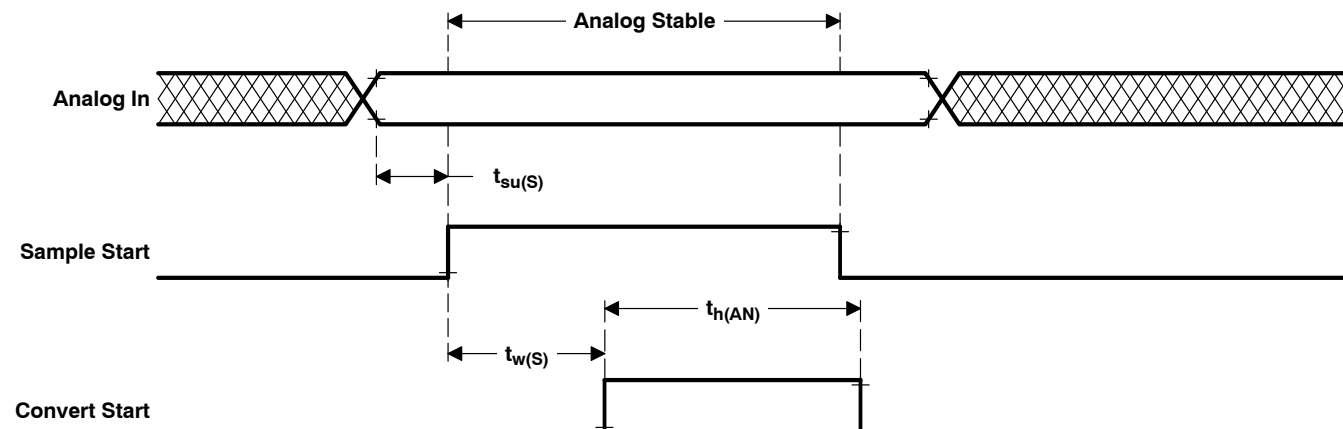


Figure 23. Analog Timing

Table 19 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

Table 19. TMS370Cx36 Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 44 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C036AFNA TMS370C036AFNL TMS370C036AFNT TMS370C736AFNT
FZ – 44 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C736AFZT [†]

General Information	1
Selection Guide/Tools	2
Ops Cond/Timing/Glossary	3
TMS370Cx0x Data Sheet	4
TMS370Cx1x Data Sheet	5
TMS370Cx2x Data Sheet	6
TMS370Cx32 Data Sheet	7
TMS370Cx36 Data Sheet	8
TMS370Cx4x Data Sheet	9
TMS370Cx5x Data Sheet	10
TMS370Cx6x Data Sheet	11
TMS370Cx7x Data Sheet	12
TMS370Cx8x Data Sheet	13
TMS370Cx9x Data Sheet	14
TMS370CxAx Data Sheet	15
TMS370CxBx Data Sheet	16
TMS370CxCx Data Sheet	17
Mechanical Data	18
Quality and Reliability	19
Electrostatic Discharge Guidelines	20

9

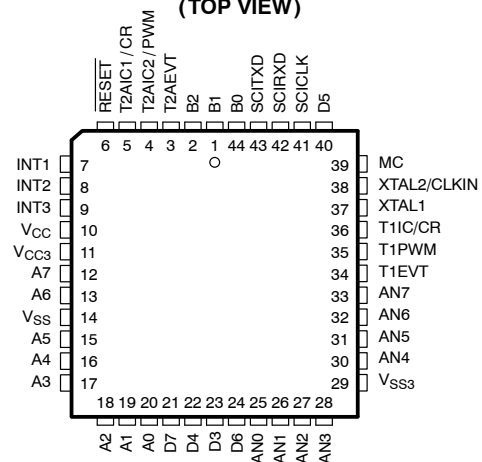
TMS370Cx4x Data Sheet



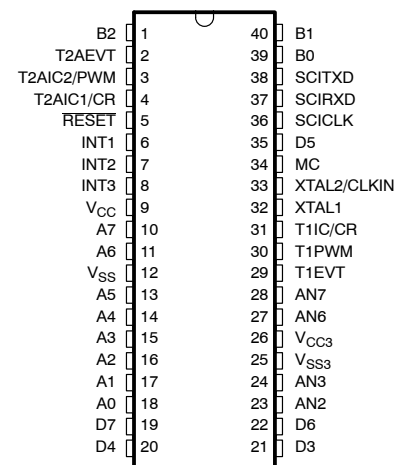
- **CMOS/EEPROM/EPROM Technologies on a Single Device**
 - Mask-ROM Devices for High Volume Production
 - One-Time-Programmable (OTP) Devices for Low-Volume Production
 - Reprogrammable EPROM Devices for Prototyping Purposes
- **Flexible Operating Features**
 - Low-Power Modes: STANDBY and HALT
 - Commercial, Industrial, and Automotive Temperature Ranges
 - Clock Options:
 - Divide-by-1 (2 MHz–5 MHz SYSCLK)
 - Phase-Locked Loop (PLL)
 - Divide-by-4 (0.5 MHz–5 MHz SYSCLK)
 - Voltage (V_{CC}) 5 V $\pm$ 10%
- **Internal System Memory Configurations**
 - On-Chip Program Memory Versions
 - ROM: 4K Bytes or 8K Bytes
 - EPROM: 8K Bytes
 - Data EEPROM: 256 Bytes
 - Static RAM: 256 Bytes Usable as Registers
- **Two 16-Bit General-Purpose Timers**
 - Software Configurable as
 - Two 16-Bit Event Counters, or
 - Two 16-Bit Pulse Accumulators, or
 - Three 16-Bit Input Capture Functions, or
 - Four Compare Registers, or
 - Two Self-Contained Pulse-Width-Modulation (PWM) Functions
- **Serial Communications Interface 1 (SCI1)**
 - Asynchronous and Isosynchronous[†] Modes
 - Full Duplex, Double Buffered RX and TX
 - Two Multiprocessor Communications Formats
- **CMOS/Package/TTL Compatible I/O Pins**
 - All Peripheral Function Pins Software Configurable for Digital I/O
 - 40-Pin Plastic and Ceramic Dual-In-Line Packages/27 Bidirectional, 5 Input Pins
 - 44-Pin Plastic and Ceramic Leaded Chip Carrier Packages/27 Bidirectional, 9 Input Pins
- **On-Chip 24-Bit Watchdog Timer**

- **Eight-Bit ADC1**
 - Four Channels in 40-Pin Packages
 - Eight Channels in 44-Pin Packages
- **Flexible Interrupt Handling**
- **TMS370 Series Compatibility**
- **Workstation/PC-Based Development System**
 - C Compiler Support
 - Real-Time In-Circuit Emulation
 - C Source Debug
 - Extensive Breakpoint/Trace Capability
 - Software Performance Analysis
 - Multi-Window User Interface
 - EEPROM/EPROM Programming

**FN AND FZ PACKAGES
(TOP VIEW)**



**JC, JD, N, AND NJ PACKAGES
(TOP VIEW)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[†] Isosynchronous = Isochronous

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TMS370Cx4x 8-BIT MICROCONTROLLERS

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Pin Descriptions

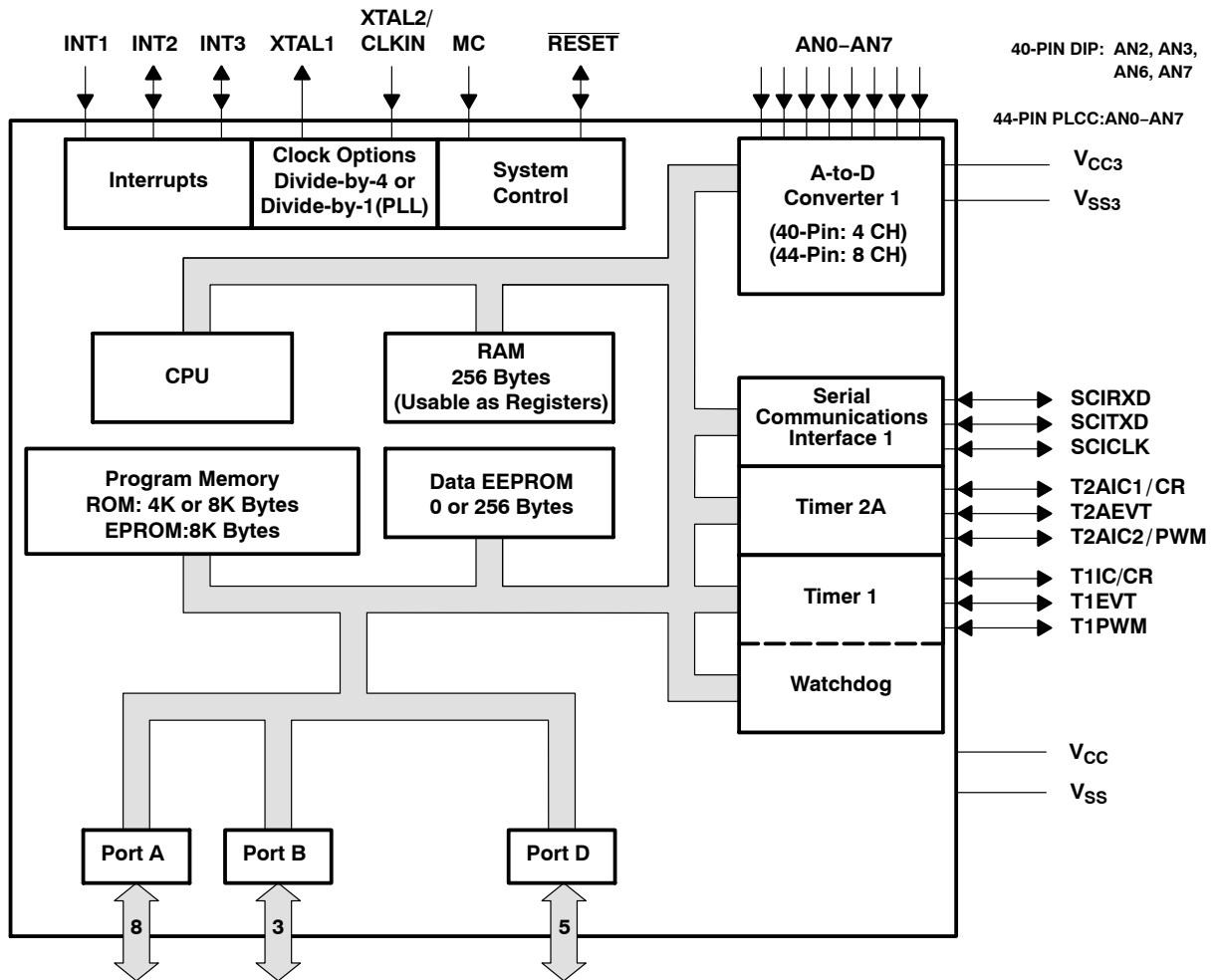
PIN			TYPE†	DESCRIPTION
	NO.			
	DIP (40)	LCC (44)		
A0 A1 A2 A3 A4 A5 A6 A7	18 17 16 15 14 13 11 10	20 19 18 17 16 15 13 12	I/O	Port A pins are general-purpose bidirectional I/O ports.
B0 B1 B2	39 40 1	44 1 2	I/O	Port B pins are general-purpose bidirectional I/O ports.
D3 D4 D5 D6 D7	21 20 35 22 19	23 22 40 24 21	I/O	Port D pins are general-purpose bidirectional I/O ports. D3 is also configurable as SYSCLK.
AN0/E0 AN1/E1 AN2/E2 AN3/E3 AN4/E4 AN5/E5 AN6/E6 AN7/E7	— — 23 24 — — 27 28	25 26 27 28 30 31 32 33	I	Analog-to-digital converter 1 (ADC1) analog input channels or positive reference pins; any ADC1 channel can be programmed as general-purpose input pin (E port) if not used as an analog input or reference channel.
V _{CC3} V _{SS3}	26 25	11 29		ADC1 converter positive supply voltage and optional positive reference input pin ADC1 converter ground supply and low reference input pin
INT1 INT2 INT3	6 7 8	7 8 9	I I/O I/O	External (non-maskable or maskable) interrupt/general-purpose input pin External maskable interrupt input/general-purpose bidirectional pin External maskable interrupt input/general-purpose bidirectional pin
T1IC/CR T1PWM T1EVT	31 30 29	36 35 34	I/O	Timer 1 input capture/counter reset input pin/general-purpose bidirectional pin Timer 1 pulse-width-modulation output pin/general-purpose bidirectional pin Timer 1 external event input pin/general-purpose bidirectional pin
T2AIC1/CR T2AIC2/PWM T2AEVT	4 3 2	5 4 3	I/O	Timer 2A input capture/counter reset input pin/general-purpose bidirectional pin Timer 2A input capture 2/PWM output pin/general-purpose bidirectional pin Timer 2A external event input pin/general-purpose bidirectional pin
SCITXD SCIRXD SCICLK	38 37 36	43 42 41	I/O	SCI transmit data output pin/general-purpose bidirectional pin ‡ SCI receive data input pin/general-purpose bidirectional pin SCI bidirectional serial clock pin/general-purpose bidirectional pin
RESET	5	6	I/O	System reset bidirectional pin. As input, RESET initializes microcontroller; as open-drain output, RESET indicates detection of an internal fault by the watchdog or oscillator fault circuit.
MC	34	39	I	Mode control input pin; enables the EEPROM write-protection-override (WPO) mode, also EPROM V _{PP} .
XTAL1 XTAL2/CLKIN	32 33	37 38	I O	Internal-oscillator output for crystal Internal-oscillator crystal input/external clock source input
V _{CC} V _{SS}	9 12	10 14		Positive supply voltage Ground reference

† I = input, O = output

‡ The three-pin configuration SCI is referred to as SCI1.



functional block diagram



description

The TMS370C040A, TMS370C042A, TMS370C340A, TMS370C342A, TMS370C742A, and SE370C742A devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx4x refers to these devices. TMS370 family provides cost-effective real-time system control through integration of advanced peripheral function modules and various on-chip memory configurations.

The TMS370Cx4x family is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technology. The low-operating power, wide-operating temperature range, and noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx4x devices attractive in system designs for automotive electronics, industrial motor, computer peripheral control, telecommunications, and consumer applications.

The TMS370Cx4x devices contain the following on-chip peripheral modules:

- Eight-channel (for 44 pin device) or four-channel (for 40-pin device) 8-bit analog-to-digital converter 1 (ADC1)
- Serial communications interface 1 (SCI1)
- Two 16-bit general-purpose timers (one with an 8-bit prescaler)

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description (continued)

- One 24-bit general-purpose watchdog timer

Table 1 provides an overview of the various memory configurations of the TMS370Cx4x devices.

Table 1. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		PACKAGES 44 PIN/PLCC/CLCC OR 40 PIN PDIP/CDIP/PSDIP/CSDIP
	ROM	EPROM	RAM	EEPROM	
TMS370C040A	4K	—	256	256	FN-PLCC N-PDIP NJ-PSDIP†
TMS370C042A	8K	—	256	256	FN-PLCC N-PDIP NJ-PSDIP†
TMS370C340A	4K	—	256	—	FN-PLCC N-PDIP NJ-PSDIP†
TMS370C342A	8K	—	256	—	FN-PLCC N-PDIP NJ-PSDIP†
TMS370C742A	—	8K	256	256	FN-PLCC N-PDIP NJ-PSDIP†
SE370C742A‡	—	8K	256	256	FZ-CLCC JD-CDIP JC-CSDIP

† The NJ designator for the 40-pin plastic shrink DIP package was known formerly as the N2. The mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

‡ System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.

The suffix letter (A) appended to the device name (shown in the first column of Table 1) indicates the configuration of the device. ROM and EPROM devices have different configurations as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 2. Suffix Letter Configuration

DEVICE	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM A	Standard	Divide-by-4 (standard oscillator)	Enabled
ROM A	Standard	Divide-by-4 (standard oscillator) or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

The 4K bytes and 8K bytes of mask-programmable ROM in the TMS370C040A, TMS370C042A, TMS370C340A and TMS370C342A are replaced in the TMS370C742 with 8K bytes of EPROM while all other available memory and on-chip peripherals are identical, with the exception of no data EEPROM on the TMS370C340A and TMS370C342A devices. The OTP (TMS370C742A) device and the reprogrammable device (SE370C742A) are available.

TMS370C742A (OTP) devices are available in plastic packages. This microcontroller is effective to use for immediate production updates for other members of the TMS370Cx4x family or for low-volume production runs when the mask charge or cycle time for the low-cost mask ROM devices is not practical.



description (continued)

The SE370C742A has a windowed ceramic package to allow reprogramming of the program EPROM memory during the development/prototyping phase of design. The SE370C742A device allows quick updates to breadboards and prototype systems while iterating initial designs.

The TMS370Cx4x family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all central processing unit (CPU) activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx4x features advanced register-to-register architecture that allows arithmetic and logical operations without requiring an accumulator (e.g., ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx4x family is fully instruction-set-compatible, allowing easy transition between members of the TMS370 8-bit microcontroller family.

The TMS370Cx4x family offers an 8-channel ADC1 with 8-bit accuracy for the 44-pin PLCC packages and also offers a 4-channel ADC1 for the 40-pin DIP packages. The 33- μ s conversion time at 5-MHz SYSCLK and the variable sample period, combined with selectable positive reference voltage sources, turn analog signals into digital data.

The serial communications interface 1 (SCI1) module is a built-in serial interface that can be programmed to be asynchronous or isosynchronous to give two methods of serial communications. The SCI allows standard RS-232-C communications with other common data transmission equipment. The CPU takes no part in serial communications except to write data to be transmitted to a register and to read data received from a register.

The TMS370Cx4x family provides the system designer with very economical, efficient solutions to real-time control applications. The TMS370 family extended development system (XDS™) and compact development tool (CDT™) solve the challenge of efficiently developing the software and hardware required to design the TMS370Cx4x into an ever-increasing number of complex applications. The application source code can be written in assembly and C languages, and the output code can be generated by the linker. The TMS370 family XDS communicates through a standard RS-232-C interface with a personal computer, allowing use of the personal computer editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes ease-of-use through extensive use of menus and screen windowing so that a system designer with minimal training can begin developing software. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation, as well as reduced time-to-market cycle.

The TMS370Cx4x family together with the TMS370 family XDS, CDT370, starter kit, software tools, the SE370C742A reprogrammable devices, comprehensive product documentation, and customer support provide a complete solution for the needs of the system designer.

TMS370Cx4x

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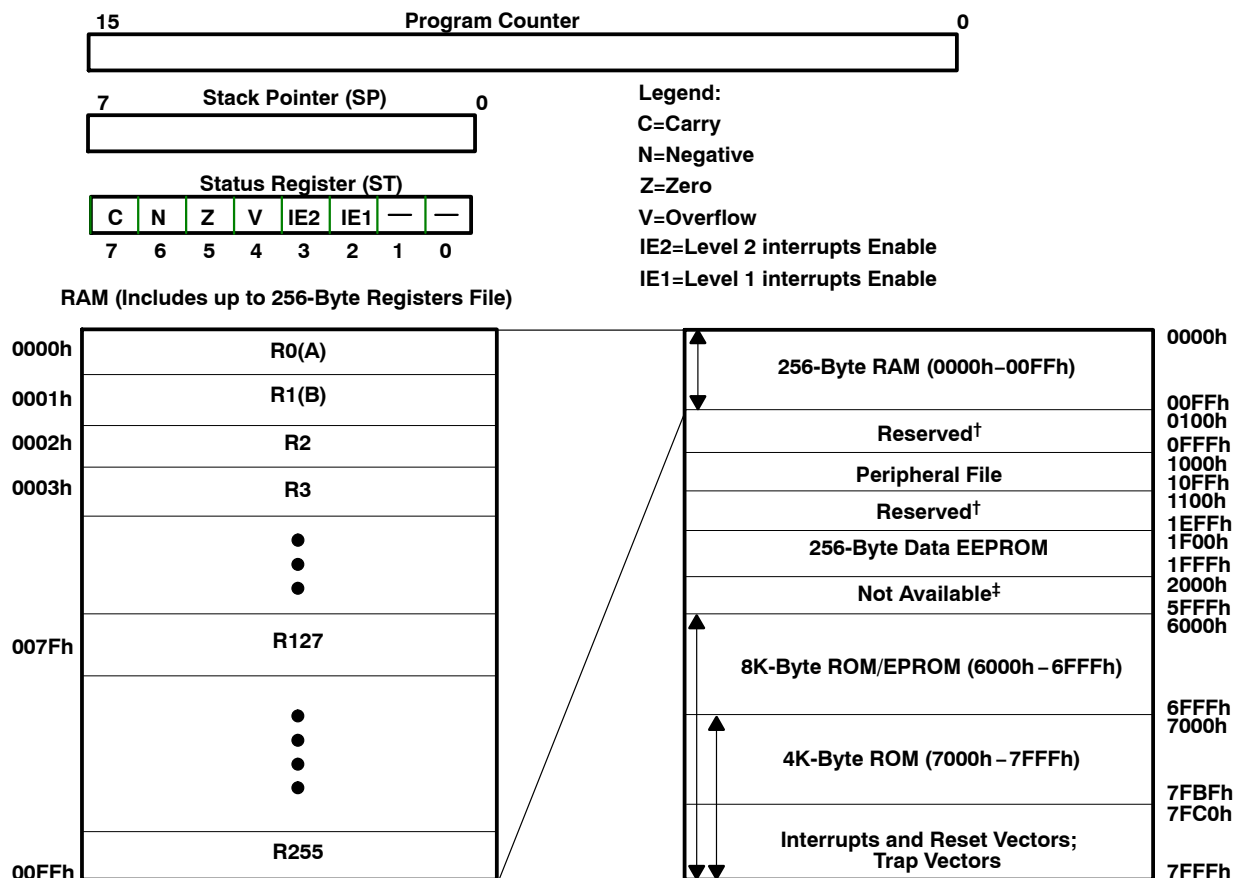
central processing unit (CPU)

The CPU used on the TMS370Cx4x device is the high-performance 8-bit TMS370 CPU module. The 'x4x' implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'x4x' instruction map is shown in Table 17 in the TMS370Cx4x instruction set overview section.

The '370Cx4x CPU architecture provides the following components:

- CPU registers:
 - A stack pointer (SP) that points to the last entry in the memory stack
 - A status register (ST) that monitors the operation of the instructions and contains the global-interrupt-enable bits
 - A program counter (PC) that points to the memory location of the next instruction to be executed

Figure 1 illustrates the CPU registers and memory blocks.



[†] Reserved means the address space is reserved for future expansion.

‡ Not available means the address space is not accessible.

Figure 1. Programmer's Model

central processing unit (CPU) (continued)

- A memory map that includes:
 - 256-byte general-purpose RAM that can be used for data memory storage, program instructions, general-purpose registers, or the stack
 - A peripheral file that provides access to all internal peripheral modules, system-wide control functions and EEPROM/EPROM programming control
 - 256-byte EEPROM module that provides in-circuit programmability and data retention in power-off conditions
 - 4K- or 8K-byte ROM or 8K-byte EPROM program memory

stack pointer (SP)

The SP is an 8-bit CPU register. The stack operates as a last-in, first-out, read/write memory. The stack is used typically to store the return address on subroutine calls as well as the status-register contents during interrupt sequences.

The SP points to the last entry or top of the stack. The SP is incremented automatically before data is pushed onto the stack and decremented after data is popped from the stack. The stack can be placed anywhere in the on-chip RAM memory.

status register (ST)

The ST monitors the operation of the instructions and contains the global interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits:

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional jump instructions) use the status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

The ST register, status-bit notation, and status-bit definitions are shown in Table 3.

Table 3. Status Registers

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most significant byte (MSbyte) and least significant byte (LSbyte) of a 16-bit address.

The contents of the reset vector (7FFEh, 7FFFh) are loaded into the program counter during reset. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 6000h as the contents of memory locations 7FFEh and 7FFFh (reset vector).

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program counter (PC) (continued)

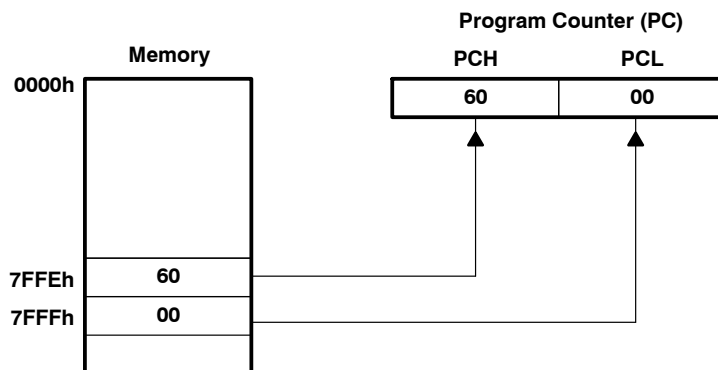


Figure 2. Program Counter After Reset

memory map

The TMS370Cx4x family architecture is based on the Von Neumann architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. As shown in Figure 3, the TMS370Cx4x family provides memory-mapped RAM, ROM, data EEPROM, EPROM, input/output pins, peripheral functions, and system interrupt vectors.

The peripheral file contains all input/output port control, peripheral status and control, EPROM and EEPROM memory programming, and system-wide control functions. The peripheral file is located between 1010h and 107Fh and is logically divided into seven peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed.

memory map (continued)

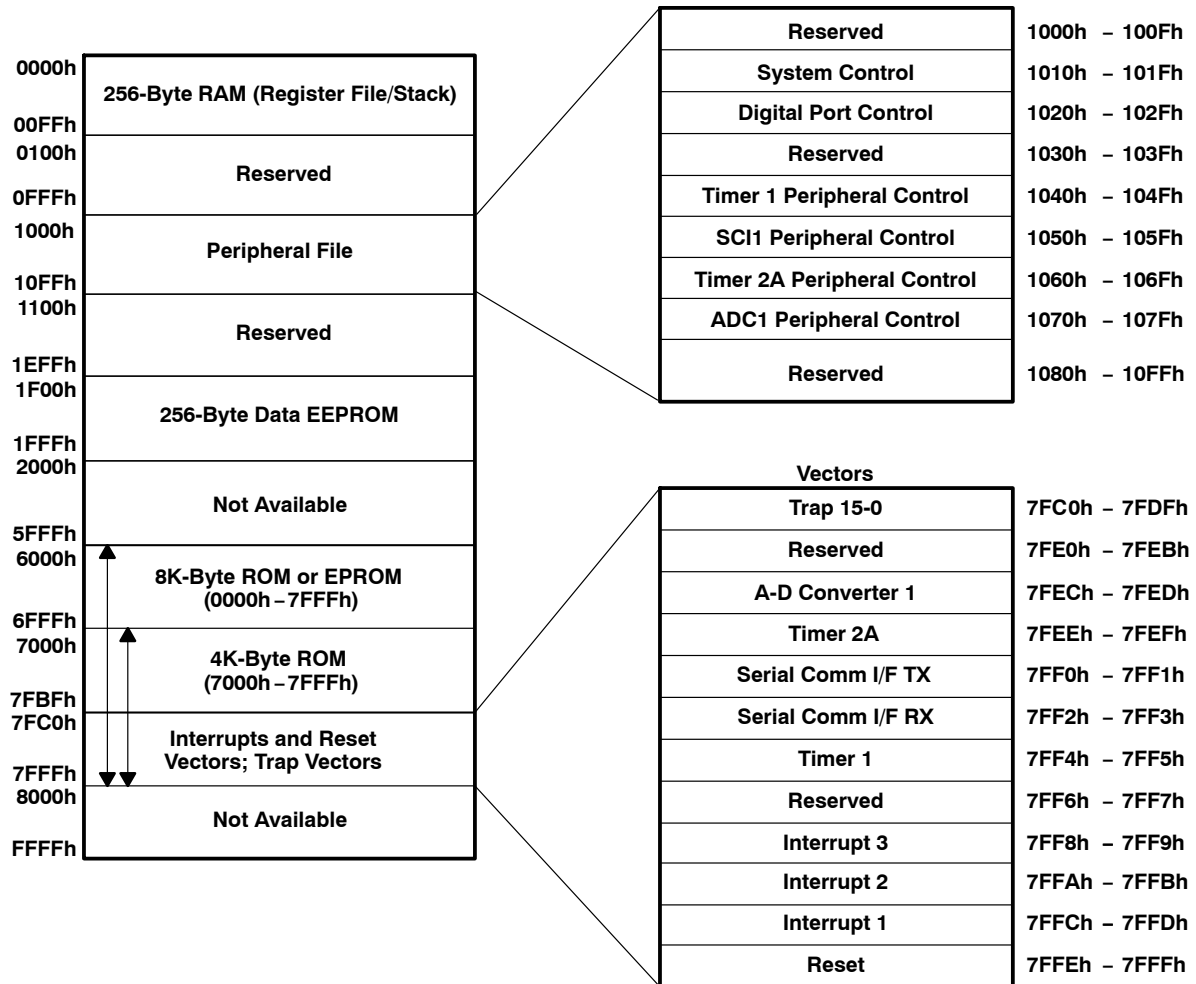


Figure 3. TMS370Cx4x Memory Map

RAM/register file (RF)

Locations within the RAM address space can serve as the RF, general-purpose read/write memory, program memory, or the stack instructions. The TMS370Cx4x devices contain 256 bytes of internal RAM memory mapped beginning at location 0000h (R0) and continuing through location 00FFh (R255).

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370Cx4x control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or P for a decimal designator. For example, the system control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 4 shows the TMS370Cx4x PF address map.

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peripheral file (PF) (continued)

Table 4. TMS370Cx4x Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h–100Fh	P000–P00F	Reserved for factory test
1010h–101Fh	P010–P01F	System and EPROM/EEPROM control registers
1020h–102Fh	P020–P02F	Digital I/O port control registers
1030h–103Fh	P030–P03F	Reserved
1040h–104Fh	P040–P04F	Timer 1 registers
1050h–105Fh	P050–P05F	Serial communications interface 1 registers
1060h–106Fh	P060–P06F	Timer 2A registers
1070h–107Fh	P070–P07F	Analog-to-digital converter 1 registers
1080h–10FFh	P080–P0FF	Reserved

data EEPROM

The TMS370Cx4x devices, containing 256 bytes of data EEPROM, have memory mapped beginning at location 1F00h and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B). The data EEPROM features include the following:

- Programming:
 - Bit-, byte-, and block-write/erase modes
 - Internal charge pump circuitry. No external EEPROM programming voltage supply is needed.
 - Control register: Data EEPROM programming is controlled by the DEECTL located in the PF frame beginning at location P01A (see Table 5).
 - In-circuit programming capability. There is no need to remove the device to program it.
- Write protection. Writes to the data EEPROM are disabled during the following conditions.
 - Reset. All programming of the data EEPROM module is halted.
 - Write protection active. There is one write-protect bit per 32-byte EEPROM block.
 - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 5. Data EEPROM and PROGRAM EPROM Control Register Memory Map

ADDRESS	SYMBOL	NAME
P01A	DEECTL	DATA EEPROM Control Register
P01B	—	Reserved
P01C	EPCTL	Program EPROM Control Register

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program EPROM

The TMS370C742A device contains 8K bytes of EPROM mapped, beginning at location 6000h and continuing through location 7FFFh. Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments (TI™), and memory addresses 7FECb through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh. Reading the program EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the EPROM control register (EPCTL). The program EPROM module features include:

- Programming
 - In-circuit programming capability if V_{PP} is applied to MC
 - Control register: EPROM programming is controlled by the EPROM control register (EPCTL) located in the peripheral file (PF) frame at location P01C as shown in Table 5.
- Write protection: writes to the program EPROM are disabled under the following conditions:
 - Reset: All programming to the EPROM module is halted.
 - Low-power modes
 - 13 V not applied to MC

program ROM

The program ROM consists of 4K or 8K bytes of mask-programmable read-only memory. The program ROM is used for permanent storage of data or instructions. Memory addresses 7FE0h through 7FEBh are reserved for TI, and memory addresses 7FECb through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh. Programming of the mask ROM is performed at the time of device fabrication.

system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx4x CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are generated internally, while one (**RESET** pin) is controlled externally. These actions are as follows:

- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside of the recommended operating range. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.
- External **RESET** pin. A low level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.

Once a reset source is activated, the external **RESET** pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x4x device to reset external system components. Additionally, if a cold start (V_{CC} is off for several hundred milliseconds) condition or oscillator failure occurs or the **RESET** pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator-fault flag (OSC FLT FLAG, SCCR0.4), the cold-start flag (COLD START, SCCR0.7) and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 6 lists the reset sources.

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system reset (continued)

Table 6. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Registers A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

$\overline{\text{RESET}}$ must be held low until the clock signal is valid and V_{CC} is within the operating range, when an external reset circuit is connected to $\overline{\text{RESET}}$. Figure 4 shows a typical reset circuit.

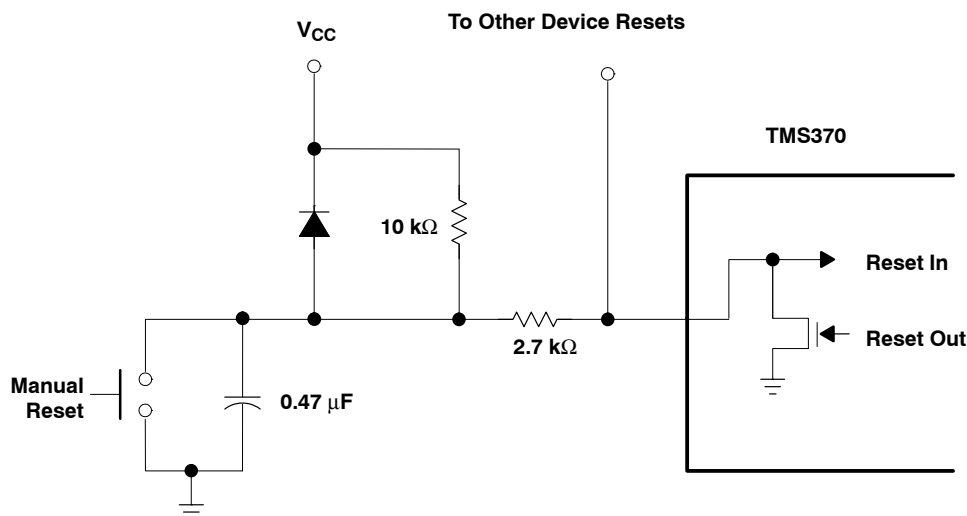


Figure 4. Typical Reset Circuit

interrupts

The TMS370 family software-programmable interrupt structure supports flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be independently enabled by the global-interrupt enable bits (IE1 and IE2) of the status register.

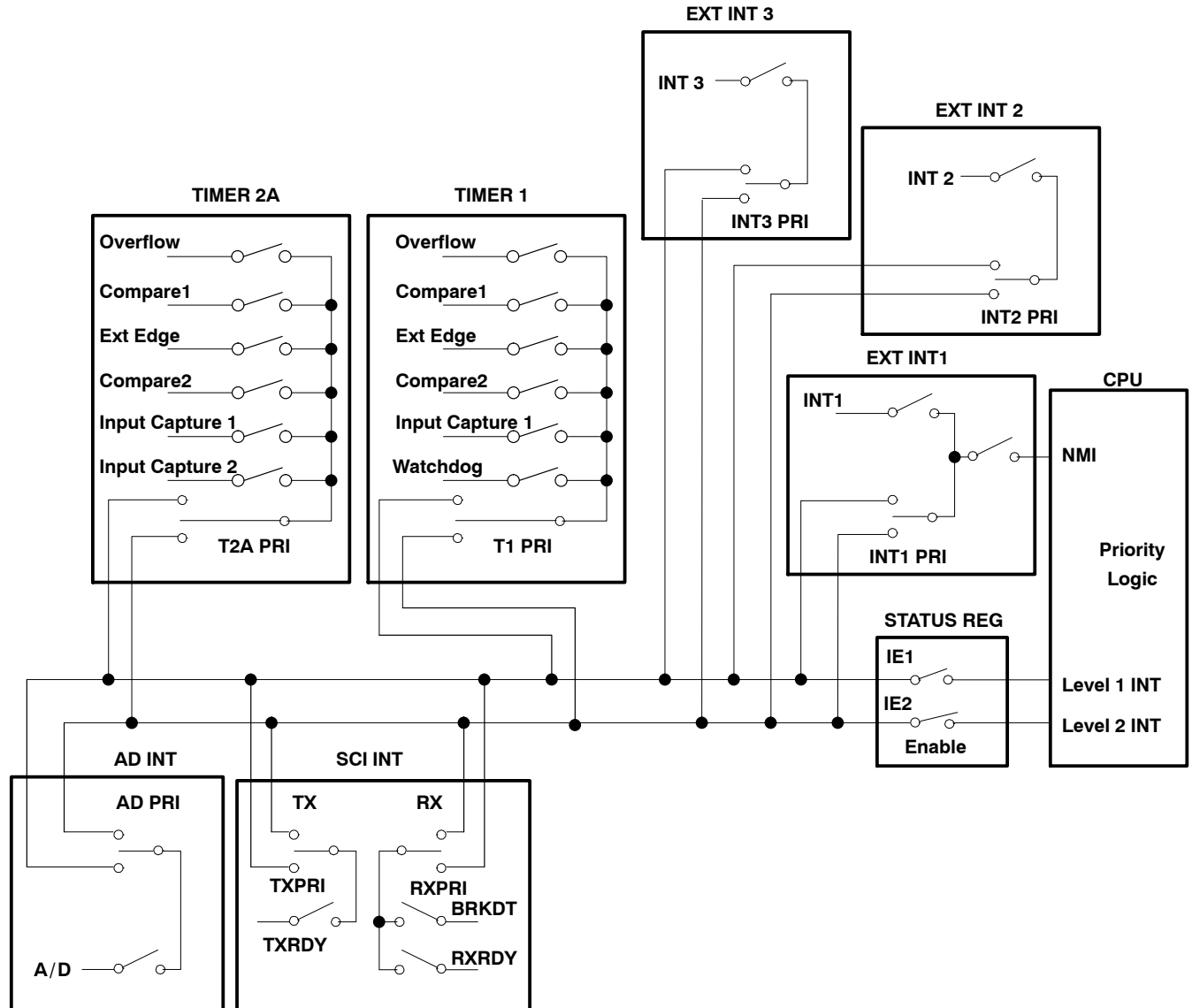


Figure 5. Interrupt Control

Each system interrupt is configured independently on either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is configured selectively on either the high- or low-priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority

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interrupts (continued)

chains is performed within the peripheral modules to support interrupt expansion to future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx4x has eight hardware system interrupts (plus **RESET**) as shown in Table 7. Each system interrupt has a dedicated interrupt vector located in program memory through which control is passed to the interrupt service routines. A system interrupt can have multiple interrupt sources (e.g., SCI RXNT has two interrupt sources). All of the interrupt sources are individually maskable by local interrupt-enable control bits in the associated peripheral file. Each interrupt source FLAG bit is individually readable for software polling or for determining which interrupt source generated the associated system interrupt.

Five of the system interrupts are generated by on-chip peripheral functions, and three external interrupts are supported. Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in peripheral file frame 1. Each external interrupt is individually software-configurable for input polarity (rising or falling) for ease of system interface. External interrupt INT1 is software-configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual- or global-enable mask bits. The INT1 NMI bit is protected during non-privileged operation and, therefore, should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software-configured as general-purpose input/output pins if the interrupt function is not required (INT1 can be configured similarly as an input pin).

Table 7. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY [†]
External RESET Watchdog Overflow Oscillator Fault Detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	RESET [‡]	7FEEh, 7FFFh	1
External INT1	INT1 FLAG	INT1 [‡]	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2 [‡]	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3 [‡]	7FF8h, 7FF9h	4
Timer 1 Overflow Timer 1 Compare 1 Timer 1 Compare 2 Timer 1 External Edge Timer 1 Input Capture Watchdog Overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC INT FLAG WD OVRFL INT FLAG	T1INT [§]	7FF4h, 7FF5h	5
SCI RX Data Register Full SCI RX Break Detect	RXRDY FLAG BRKDT FLAG	RXINT [‡]	7FF2h, 7FF3h	6
SCI TX Data Register Empty	TXRDY FLAG	TXINT	7FF0h, 7FF1h	7
Timer 2A Overflow Timer 2A Compare 1 Timer 2A Compare 2 Timer 2A External Edge Timer 2A Input Capture 1 Timer 2A Input Capture 2	T2A OVRFL INT FLAG T2AC1 INT FLAG T2AC2 INT FLAG T2AEDGE INT FLAG T2AIC1 INT FLAG T2AIC2 INT FLAG	T2AINT	7FEEh, 7FEFh	8
A-D Conversion Complete	AD INT FLAG	ADINT	7FEC h, 7FEDh	9

[†] Relative priority within an interrupt level.

[‡] Releases microcontroller from STANDBY and HALT low-power modes.

[§] Releases microcontroller from STANDBY low-power mode.



privileged operation and EEPROM write-protection override

The TMS370Cx4x family has significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a broad variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once defined for an end application. Following a hardware reset, the TMS370Cx4x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) is set to 1, entering the nonprivileged mode and disabling write operations to specific configuration control bits within the peripheral file. The system-configuration bits listed in Table 8 are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

Table 8. Privilege Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCR0	P010.5 P010.6	PF AUTO WAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
SCIPRI	P05F.4 P05F.5 P05F.6 P05F.7	SCI ESPEN SCI RX PRIORITY SCI TX PRIORITY SCI STEST
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST
T2APRI	P06F.6 P06F.7	T2A PRIORITY T2A STEST
ADPRI	P07F.5 P07F.6 P07F.7	AD ESPEN AD PRIORITY AD STEST

† The privileged bits are shown in a bold typeface in the peripheral file frames of the following sections.

The WPO mode provides an external hardware method for overriding the write protection registers (WPR) of data EEPROM on the TMS370Cx4x. Applying a 12-V input to the MC pin after the RESET pin input goes high causes the device to enter WPO mode. The high voltage on the MC pin during the WPO mode is not the programming voltage for the data EEPROM or program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware system level capability to modify the content of data EEPROM while the device remains in the application but only while requiring a 12-V external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power and IDLE modes

The TMS370Cx4x devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time the mask is manufactured.

low-power and IDLE modes (continued)

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls which low-power mode is entered.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, Timer 1, and the receive start-bit-detection circuit of the SCI1 remain active. System processing is suspended until a qualified interrupt (hardware RESET, external interrupt on INT1, INT2, INT3, Timer 1 interrupt, or a low level on the receive pin of the serial communications interface 1) is detected.

In the HALT mode (HALT/STANDBY=1), the TMS370Cx4x is placed in its lowest power-consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware RESET external interrupt on INT1, INT2, INT3, or low level on the receive pin of the SCI1) is detected. The power-down mode selection bits are summarized in Table 9.

Table 9. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X	IDLE

X = don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6–7 bits is ignored. In addition, if an idle instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method of always exiting low-power modes for mask-ROM devices, INT1 is automatically enabled as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI is always generated, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU-instruction processing is stopped during the STANDBY and HALT modes, the clocking of the WD timer is inhibited.

clock modules

The 'x4x family provides two clock options that are referred to as divide-by-1 (phase-locked loop) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The 'x4x ROM-masked devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device. The '742A EPROM has only the divide-by-4.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 clock module option provides a one-to-one match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency. The divide-by-4 option produces a SYSCLK which is one-fourth of the frequency of the external resonator. Inside of the divide-by-1 module, the frequency of the external resonator is multiplied by four, and the clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency.

clock modules (continued)

These are formulated as follows:

$$\text{Divide-by-4 : SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 : SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the reduction of EMI. The harmonics of low-speed resonators extend through less of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 option provides the capability of reducing the resonator speed by four times, resulting in a steeper decay of emissions produced by the oscillator.

system configuration registers

Table 10 contains system configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in a bold typeface.

Table 10. Peripheral File Frame 1: System Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTOWAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D to P01F	Reserved								

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digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 11 and Table 12 detail the specific addresses, registers, and control bits within the peripheral file frame.

Table 11. Peripheral File Frame 2: Digital Port Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	—	—	—	—	—	Port B Control Register 2 (must be 0)			BPORT2
P026	—	—	—	—	—	Port B Data			BDATA
P027	—	—	—	—	—	Port B Direction			BDIR
P028 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0) [†]					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

[†] To configure pin D3 as SYSCLOCK, set port D control register 2 = 08h.

Table 12. Port Configuration Register Setup

PORT	PIN	abcd 00q1	abcd 00y0
A	0 – 7	Data Out q	Data In y
B	0 – 2	Data Out q	Data In y
D	3 – 7	Data Out q	Data In y
a = Port × Control Register 1 b = Port × Control Register 2 c = Data d = Direction			

timer 1 module

The programmable Timer 1 (T1) module of the TMS370Cx4x provides the designer with the enhanced timer resources required to perform real-time system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers, T1 and WD, allow program selection of input clock sources (real-time, external event, or pulse accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The T1 module includes three external device pins that can be used for multiple counter functions (operation-mode dependent), or used as general-purpose I/O pins. The T1 module block diagram is shown in Figure 6.

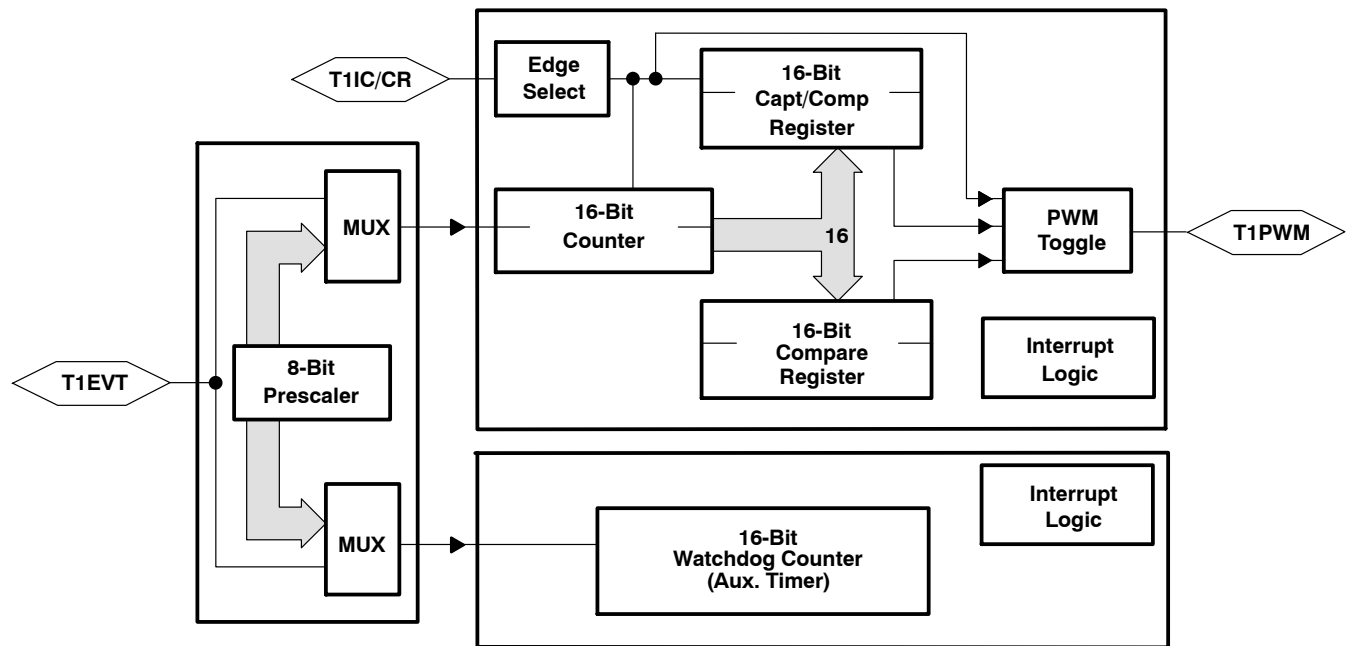


Figure 6. Timer 1 Block Diagram

- Three T1 I/O pins
 - T1IC/CR: T1 input capture / counter-reset input pin, or general-purpose bidirectional I/O pin
 - T1PWM: T1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T1EVT: T1 event input pin, or general-purpose bidirectional I/O pin
- Two operational modes:
 - Dual-compare mode: Provides PWM signal
 - Capture/compare mode: Provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register.
- One 16-bit WD counter can be used as an event counter, a pulse accumulator, or an interval timer if WD feature is not needed.
- Prescaler/clock sources that determine one of eight clock sources for general-purpose timer

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timer 1 module (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR)
- Interrupts that can be generated on the occurrence of:
 - A capture
 - A compare equal
 - A counter overflow
 - An external edge detection
- Sixteen T1 module control registers located in the PF frame, beginning at address P040

The T1 module control registers are illustrated in Table 13.



timer 1 module (continued)

Table 13. Timer 1 Module Registers Memory Map[†]

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Dual-Compare and Capture/Compare									
P040	T1 Counter MSB							Bit 8	T1CNTR
P041	T1 Counter LSB							Bit 0	
P042	Compare Register MSB							Bit 8	T1C
P043	Compare Register LSB							Bit 0	
P044	Capture/Compare Register MSB							Bit 8	T1CC
P045	Capture/Compare Register LSB							Bit 0	
P046	Watchdog Counter MSB							Bit 8	WDCNTR
P047	Watchdog Counter LSB							Bit 0	
P048	Watchdog Reset Key							Bit 0	WDRST
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1INPUT SELECT2	T1INPUT SELECT1	T1INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

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timer 1 module (continued)

Figure 7 shows the T1 dual-compare mode block diagram. The annotations on the diagram identify the register and the bits in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

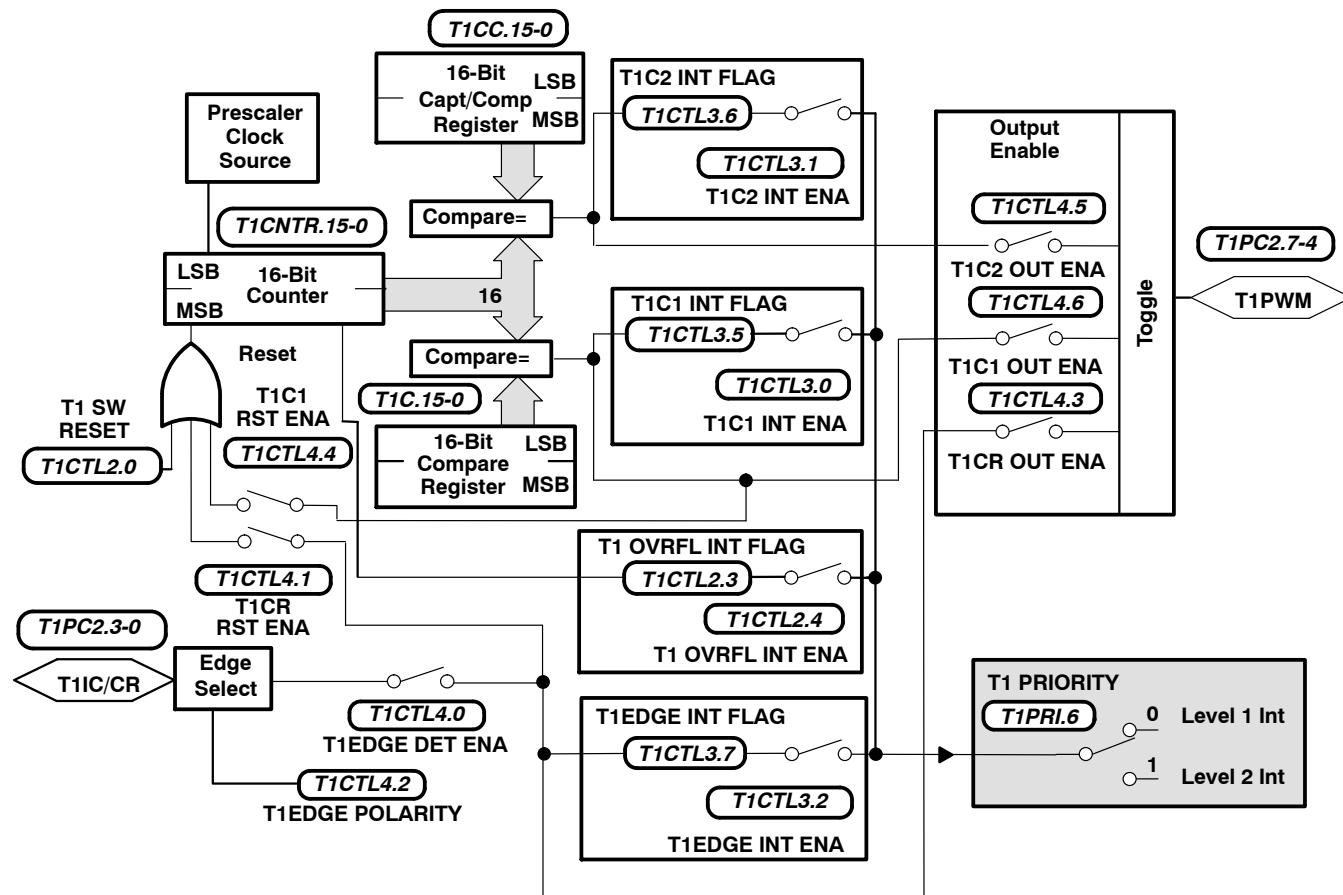


Figure 7. Timer 1: Dual-Compare Mode

timer 1 module (continued)

Figure 8 shows the T1 capture/compare mode block diagram. The annotations on the diagram identify the register and the bits in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

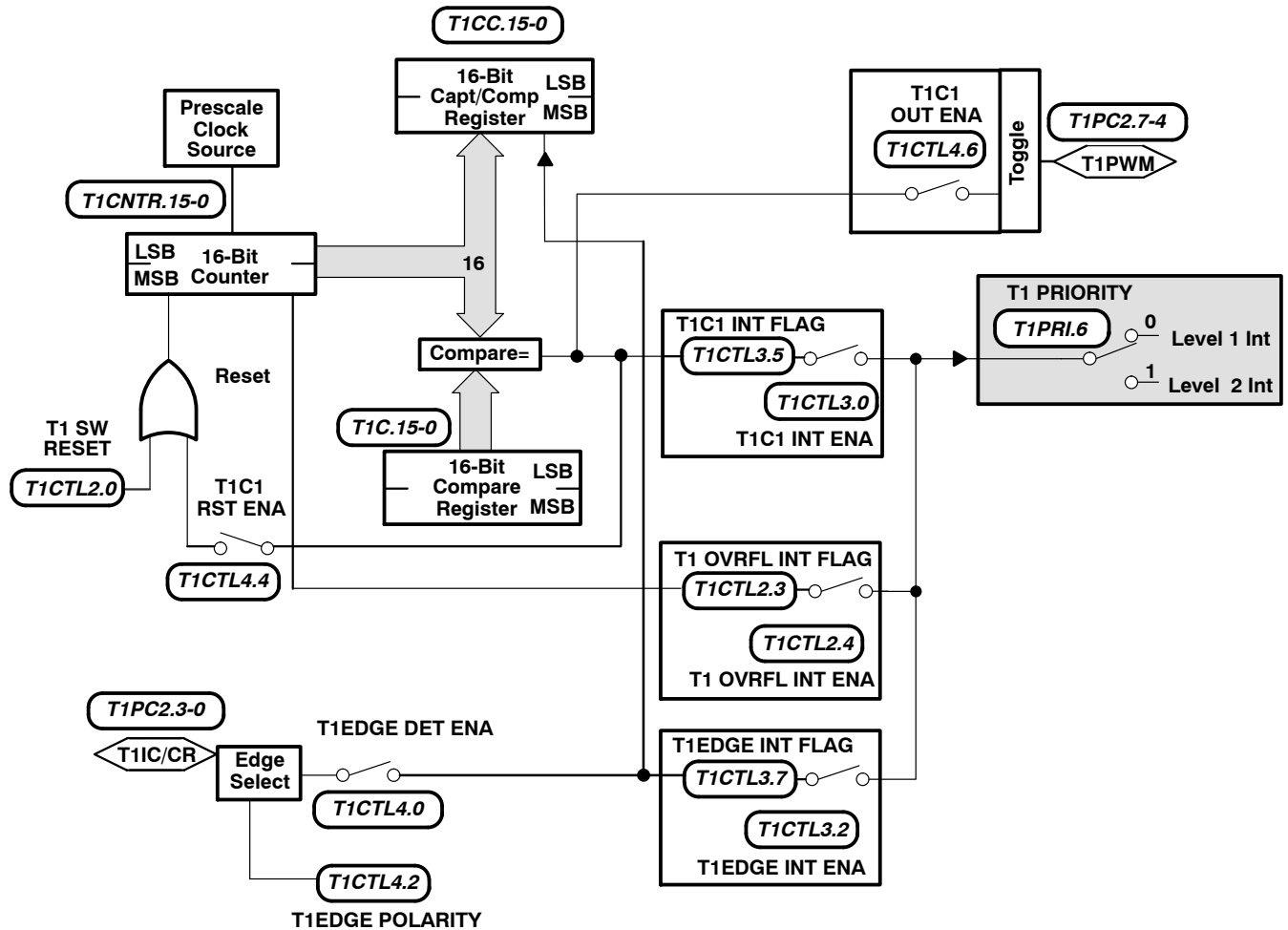


Figure 8. Timer 1: Capture/Compare Mode

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timer 1 module (continued)

The TMS370Cx4x device includes a 24-bit WD timer, contained in the T1 module, which can be programmed as an event counter, pulse accumulator, or interval timer if the WD function is not used. The WD function is to monitor software and hardware operation and to implement a system reset when the WD counter is not properly serviced (WD counter overflow or WD counter is re-initialized by an incorrect value). The WD can be configured as one of three mask options as follows:

- Standard WD configuration (see Figure 9) for 'C742A EPROM and mask-ROM devices:
 - Watchdog mode
 - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written
 - Generates a system reset if an incorrect value is written to the WD reset key or if the counter overflows
 - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
 - Non-watchdog mode
 - Watchdog timer can be configured as an event counter, pulse accumulator, or an interval timer

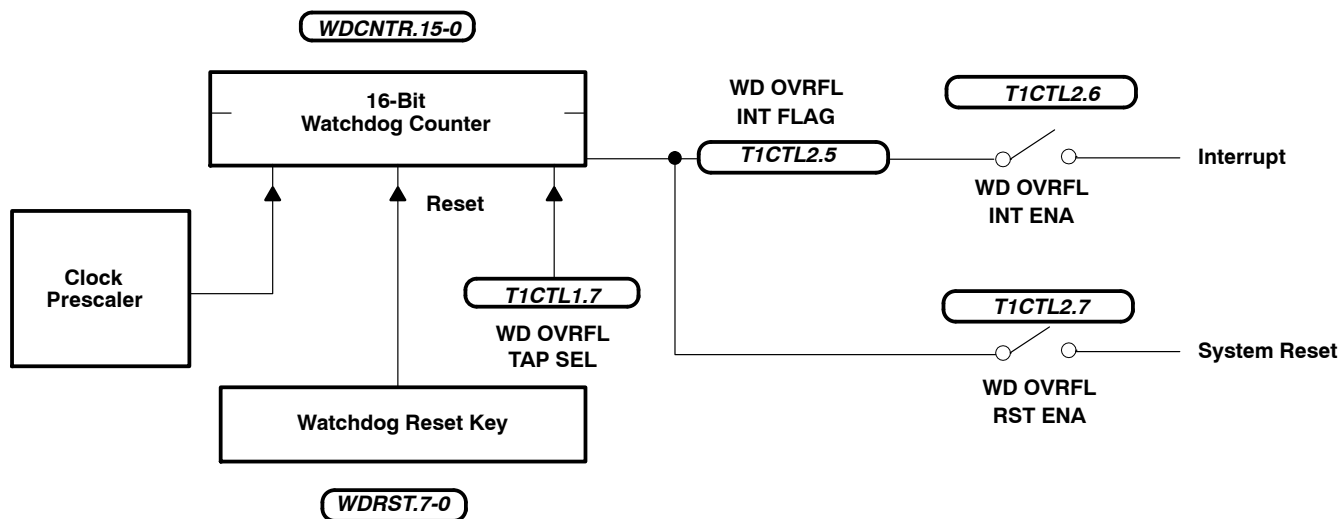


Figure 9. Standard Watchdog

timer 1 module (continued)

- Hard watchdog configuration (see Figure 10) for mask-ROM devices only:
 - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the WDRST or if the counter overflows
 - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
 - Automatic activation of the WD timer upon power-up reset
 - INT1 is enabled as a nonmaskable interrupt during low power modes.

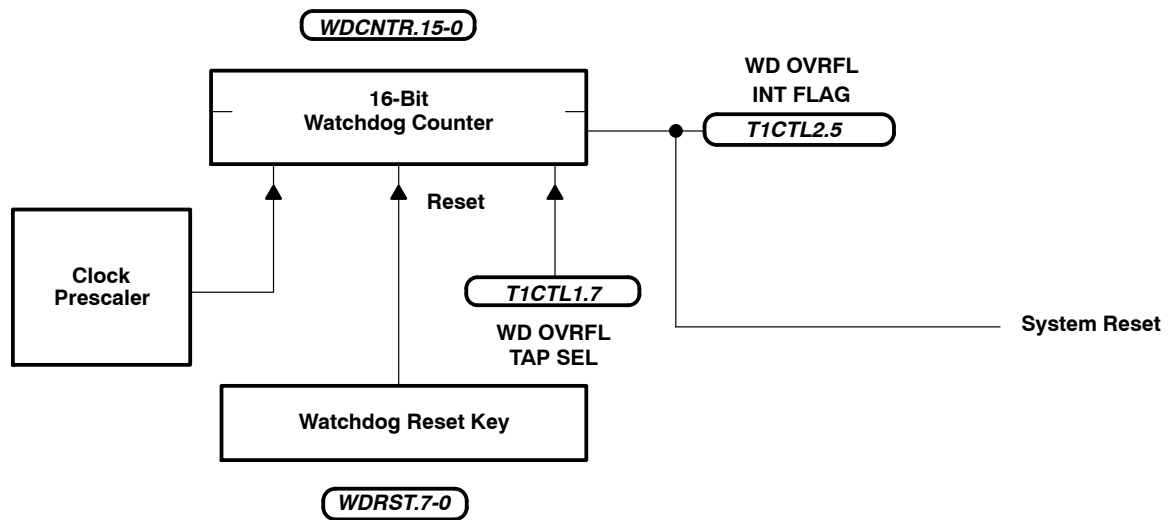


Figure 10. Hard Watchdog

timer 1 module (continued)

- Simple counter configuration (see Figure 11) for mask-ROM devices only
 - Simple counter can be configured as an event counter, pulse accumulator, or an internal timer.

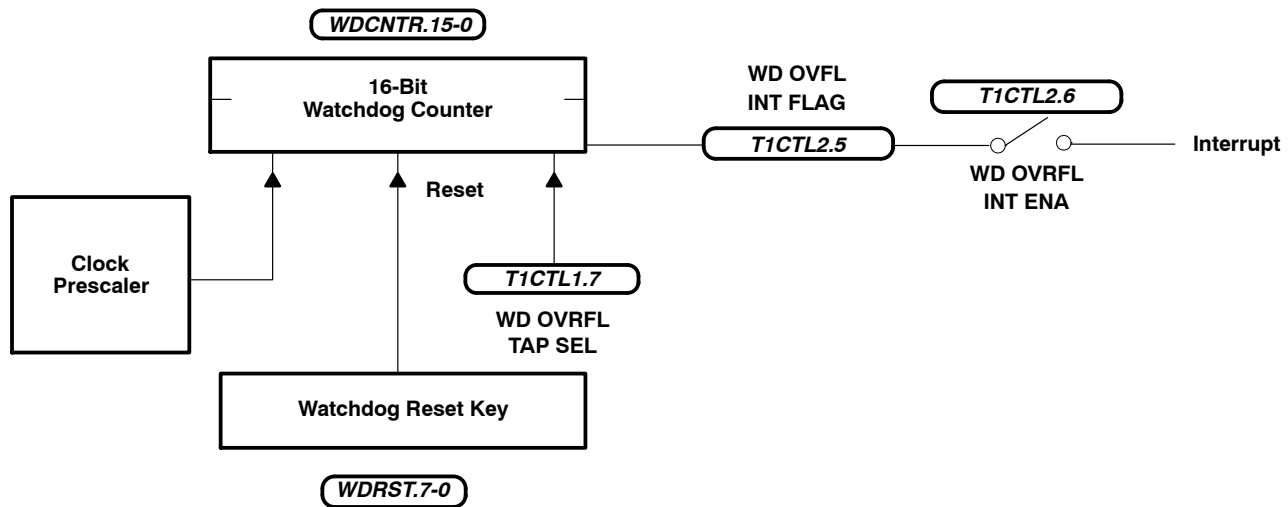


Figure 11. Simple Counter

timer 2A module

The 16-bit general-purpose timer 2A (T2A) module is composed of a 16-bit resettable counter, 16-bit compare register with associated compare logic, 16-bit capture register, and a 16-bit register that functions as a capture register in one mode and as a compare register in the other mode. The T2A module adds an additional timer that provides an event count, input capture, and compare function. The T2A module includes three external device pins that can be dedicated as timer functions or used as general-purpose I/O pins. The T2A module is shown in Figure 12.

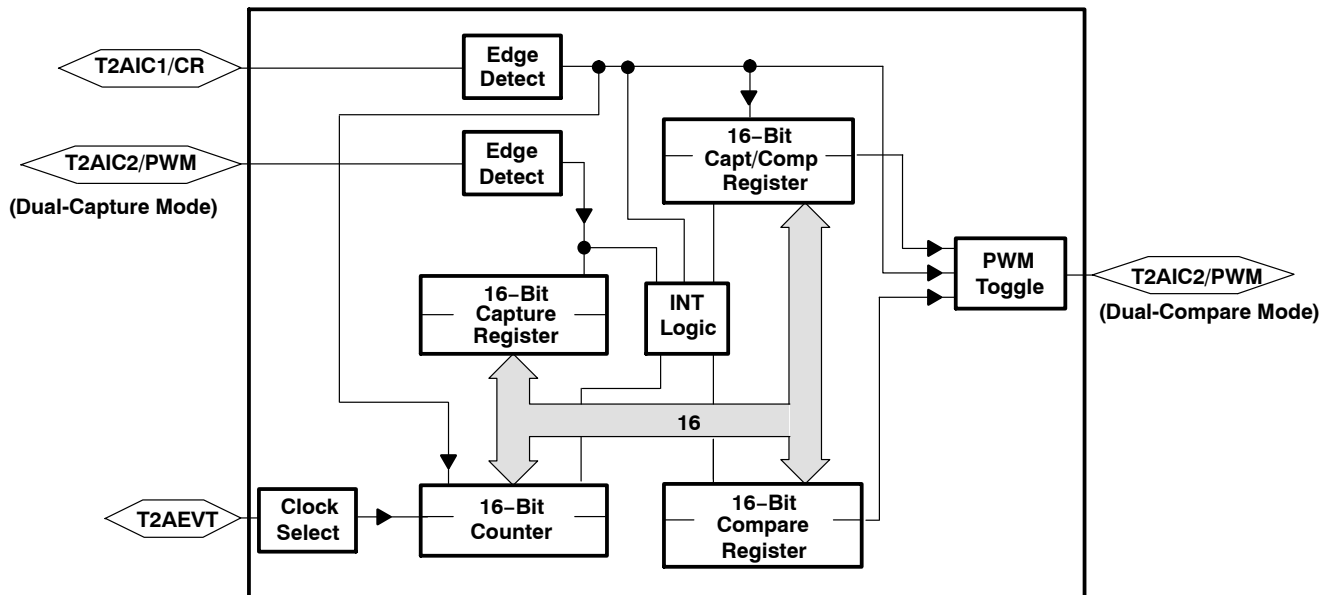


Figure 12. Timer 2A Module Block Diagram

The T2A module features include the following:

- Three T2A I/O pins:
 - T2AIC1/CR: T2A input-capture 1/counter-reset input pin, or general-purpose bidirectional I/O pin
 - T2AIC2/PWM: T2A input-capture 2/pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T2AEVT: Timer 2A event-input pin, or general-purpose bidirectional I/O pin
- Two operational modes:
 - Dual-compare mode: Provides PWM signal
 - Dual-capture mode: Provides input-capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture register with associated capture logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register

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timer 2A module (continued)

- T2A clock sources can be any of the following:
 - System clock
 - No clock (the counter is stopped)
 - External clock synchronized to the system clock (event counter)
 - System clock while external input is high (pulse accumulation)
- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T2AIC1/CR)
- Interrupts that can be generated on the occurrence of:
 - A compare equal to dedicated-compare register
 - A compare equal to capture-compare register
 - A counter overflow
 - An external edge 1 detection
 - An external edge 2 detection
- Fourteen T2A module-control registers: Located in the PF frame beginning at address P060



timer 2A module (continued)

The T2A module-control registers are shown in Table 14.

Table 14. T2A Module Register Memory Map[†]

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Dual-Compare and Dual-Capture									
P060	Bit 15			T2A Counter MSB				Bit 8	T2ACNTR
P061	Bit 7			T2A Counter LSB				Bit 0	
P062	Bit 15			Compare Register MSB				Bit 8	T2AC
P063	Bit 7			Compare Register LSB				Bit 0	
P064	Bit 15			Capture/Compare Register MSB				Bit 8	T2ACC
P065	Bit 7			Capture/Compare Register LSB				Bit 0	
P066	Bit 15			Capture Register 2 MSB				Bit 8	T2AIC
P067	Bit 7			Capture Register 2 LSB				Bit 0	
P068	Reserved								
P069									
P06A	—	—	—	T2A OVRFL INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1
Mode: Dual-Compare									
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC1 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
Mode: Dual-Capture									
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
Modes: Dual-Compare and Dual-Capture									
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2/PWM DATA IN	T2AIC2/PWM DATA OUT	T2AIC2/PWM FUNCTION	T2AIC2/PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC1/CR DATA DIR	T2APC2
P06F	T2A STEST	T2A PRIORITY	—	—	—	—	—	—	T2APRI

[†] Privileged bits are shown in bold typeface.

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timer 2A module (continued)

The T2A dual-compare mode block diagram is illustrated in Figure 13. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2ACTL2.0 is 106Bh, bit 0, in the T2ACTL2 register.

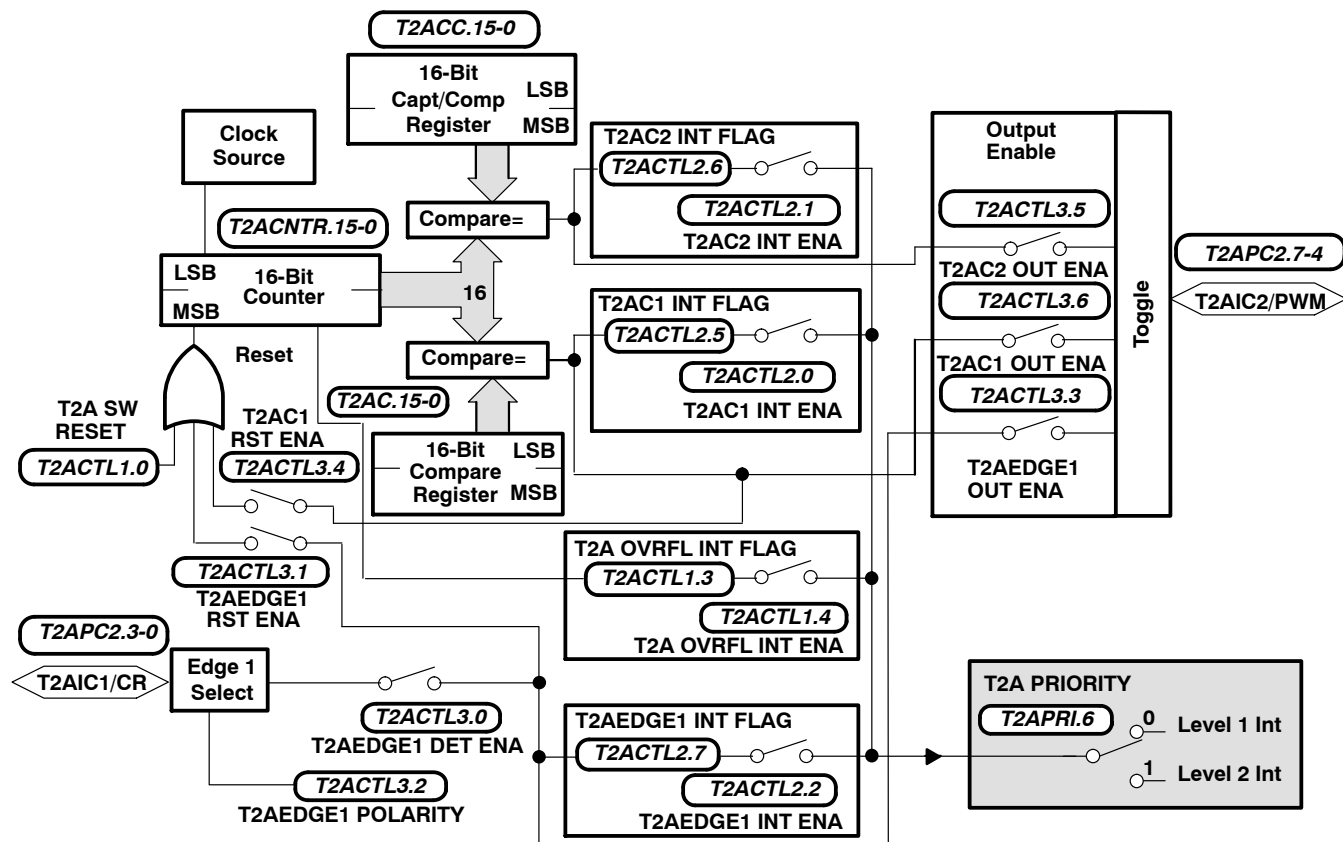


Figure 13. Timer 2A: Dual-Compare Mode

timer 2A module (continued)

The T2A dual-capture mode block diagram is illustrated in Figure 14. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2ACTL2.0 is 106Bh, bit 0, in the T2ACTL2 register.

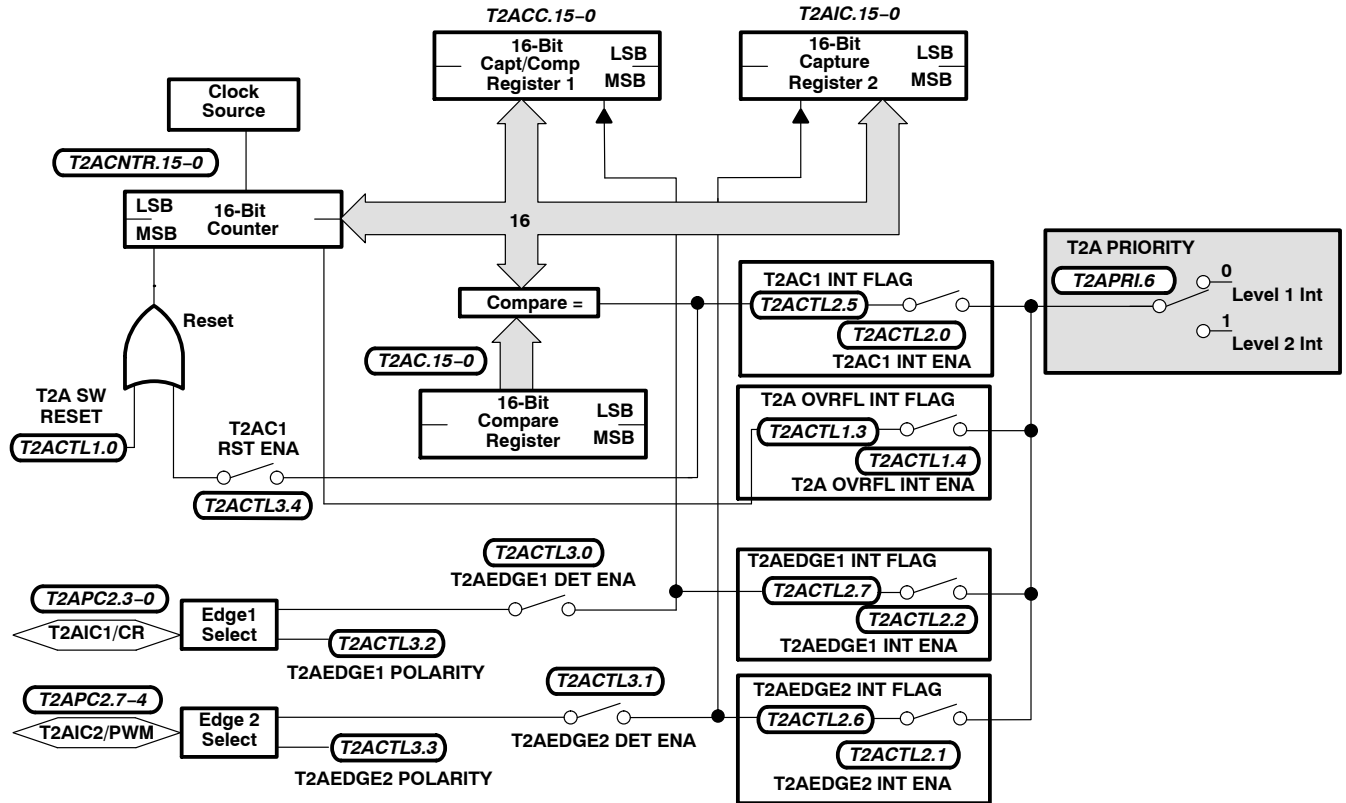


Figure 14. Timer 2A: Dual-Capture Mode

serial communications interface 1 (SCI1)

The TMS370Cx4x devices include a serial communications interface 1 (SCI1) module. The SCI1 module supports digital communications between the TMS370 devices and other asynchronous peripherals and uses the standard non return-to-zero format (NRZ) format. The SCI1's receiver and transmitter are double buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full duplex mode. To ensure data integrity, the SCI1 checks received data for break detection, parity, overrun, and framing errors. The bit rate (baud) is programmable to over 65,000 different rates through a 16-bit baud-select register.

Features of the SCI1 module include:

- Three external pins:
 - SCITXD: SCI transmit-output pin or general purpose bidirectional I/O pin.
 - SCIRXD: SCI receive-input pin or general purpose bidirectional I/O pin.
 - SCICLK: SCI bidirectional serial-clock pin, or general-purpose bidirectional I/O pin.
- Two communications modes: asynchronous and isosynchronous
- Baud rate: 64K different programmable rates
 - Asynchronous mode: 3 bps to 156K bps at 5 MHz SYSCLK

$$\text{Asynchronous Baud} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 32}$$

- Isosynchronous mode: 39 bps to 2.5 Mbps at 5 MHz SYSCLK

$$\text{Isosynchronous Baud} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 2}$$

- Data word format:
 - One start bit
 - Data word length programmable from one to eight bits
 - Optional even/odd/no parity bit
 - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: Idle-line and address bit
- Half or full-duplex operation
- Double-buffered receiver and transmitter operations
- Transmitter and receiver operations can be accomplished through either interrupt-driven or polled-algorithms with status flags:
 - Transmitter: TXRDY flag (transmitter buffer register is ready to receive another character) and TX EMPTY flag (Transmitter shift register is empty)
 - Receiver: RXRDY flag (receive buffer register ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR monitoring four interrupt conditions
 - Separate enable bits for transmitter and receiver interrupts
 - NRZ (non return-to-zero) format
- Eleven SCI1 module control registers, located in control register frame beginning at address P050h

serial communications interface 1 (SCI1) (continued)

Table 15 lists the SCI1 module control registers.

Table 15. SCI1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNCR/ ISOSYNCR	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	RESERVED								
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF
P05A P05B P05C	Reserved								
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	SCI STEST	SCITX PRIORITY	SCIRX PRIORITY	SCI ESPEN	—	—	—	—	SCIPRI

serial communications interface 1 (SCI1) (continued)

Figure 15 shows the SCI1 module block diagram.

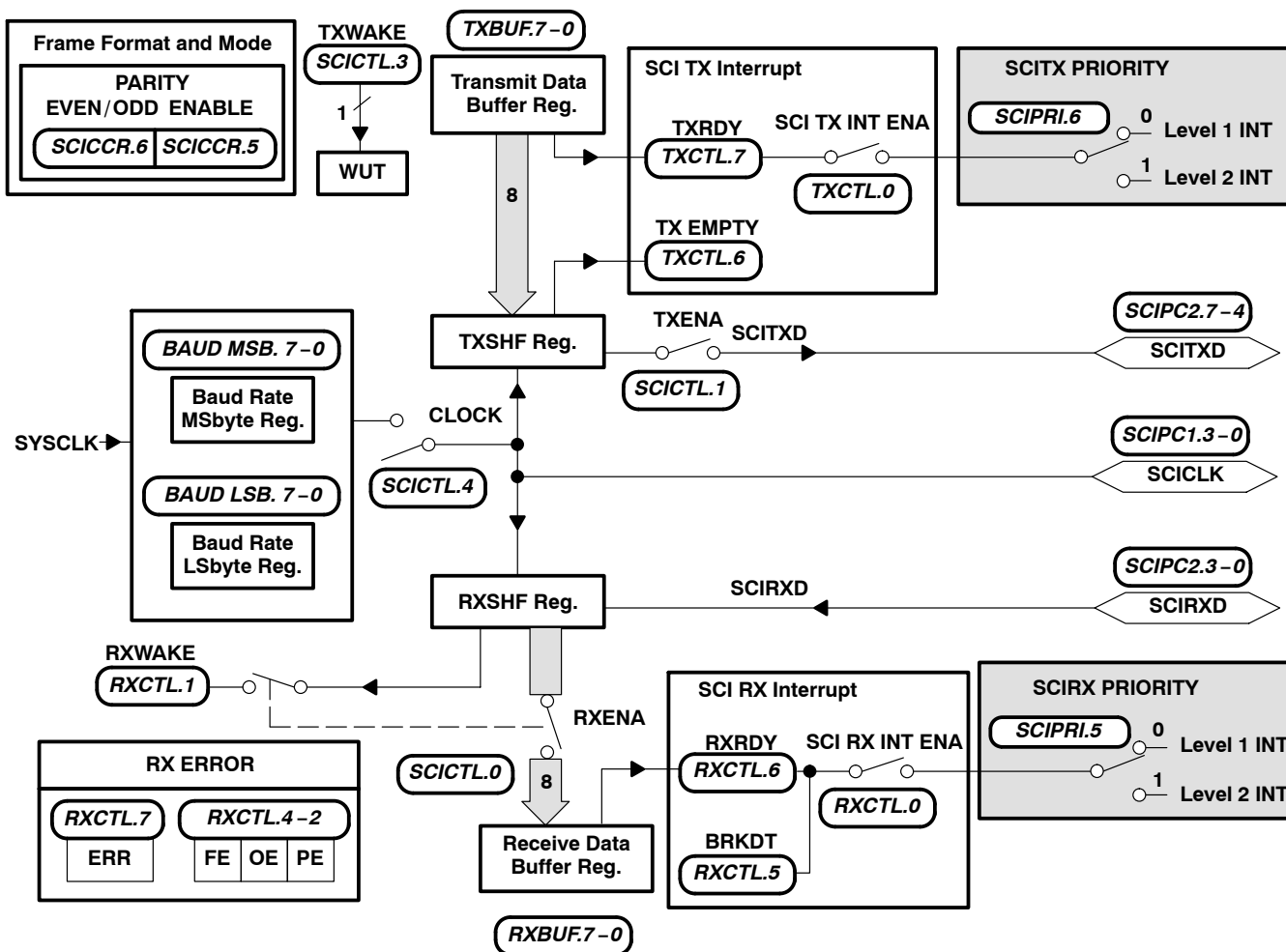


Figure 15. SCI1 Block Diagram

analog-to-digital converter 1 (ADC1) module

The analog-to-digital converter 1 (ADC1) module is an 8-bit, successive approximation converter with internal sample-and-hold circuitry. The module has eight multiplexed analog input channels for the 44-pin device and four multiplexed analog input channels for the 40-pin device that allow the processor to convert the voltage levels from up to eight different sources. The ADC1 module features include the following:

- Minimum conversion time: 32.8 μ s at 5-MHz SYSCLK
- Up to ten external pins:
 - Four (AN2, AN3, AN6, AN7) or eight (AN0-AN7) analog input channels, any of which can be software configured as digital inputs (E2, E3, E6, E7) or (E0–E7), respectively, if not needed as analog channels
 - AN1–AN7 can also be configured as positive-input voltage reference.
 - V_{CC3}: ADC1 module high-voltage reference input
 - V_{SS3}: ADC1 module low-voltage reference input
- The ADDATA register, which contains the digital result of the last A/D conversion
- A/D operations can be accomplished through either interrupt driven or polled algorithms.
- Six ADC1 module control registers are located in the control-register frame beginning at address 1070h.

The ADC1 module control registers are illustrated in Table 16.

Table 16. ADC1 Module Control Register Memory Map[†]

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A-to-D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI

[†] Privileged bits are shown in bold typeface.

analog-to-digital converter 1 (ADC1) module (continued)

The ADC1 module block diagram is illustrated in Figure 16.

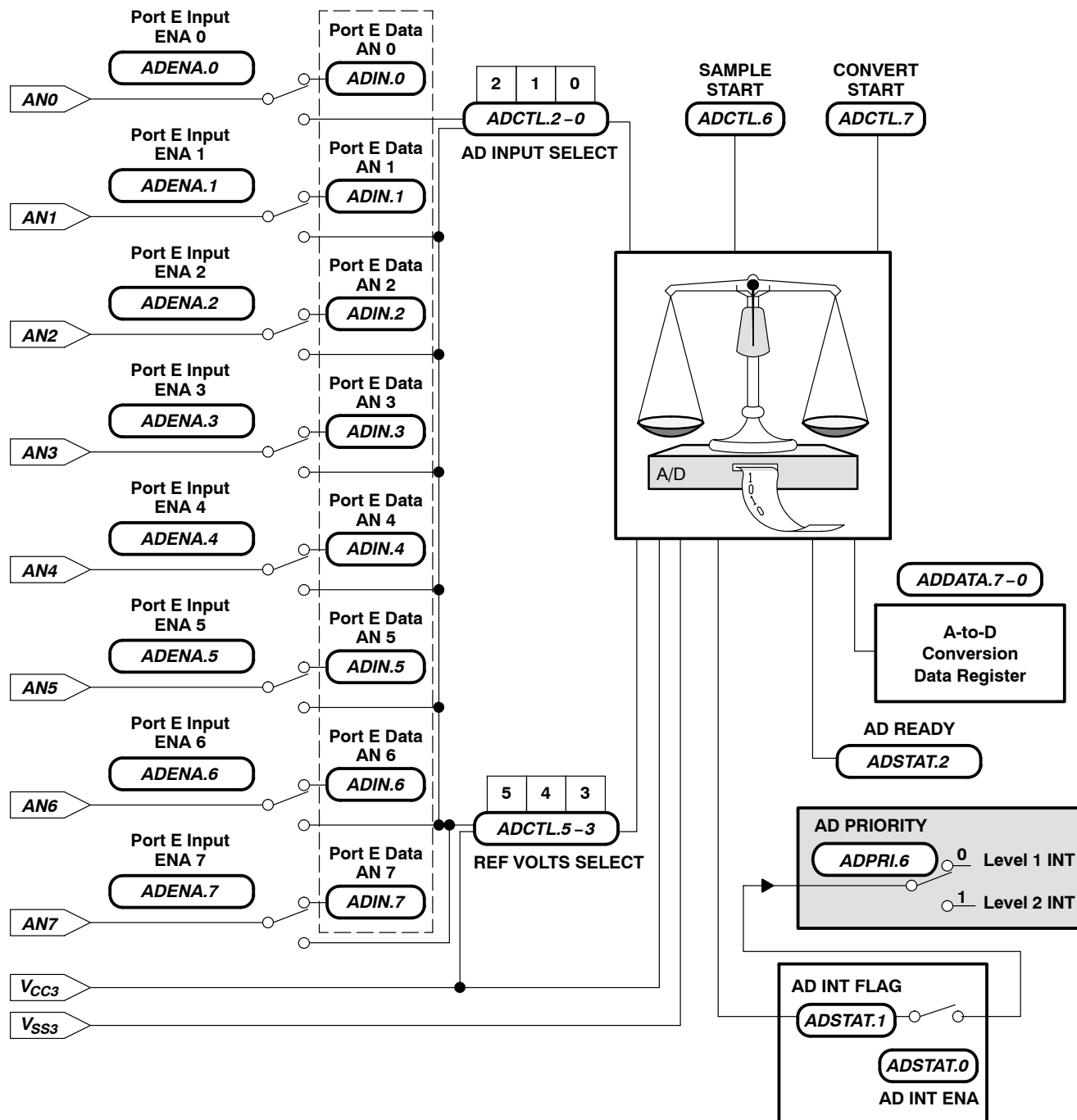


Figure 16. ADC1 Converter Block Diagram

instruction set overview

Table 17 provides an opcode-to-instruction cross-reference of all 73 instructions and 274 opcodes of the '370Cx4x instruction set. The numbers at the top of this table represent the most significant nibble (MSN) of the opcode while the numbers at the left side of the table represent the least significant nibble (LSN). The instructions for these two opcode nibbles contain the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.



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Table 17. TMS370 Family Opcode/Instruction Map[†]

		MSN																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
L S N	0	JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8				CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
	1	JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7	
	2	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7	
	3	JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8	
	4	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes	
	5	JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14		
	6	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6	
	7	JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10	
	8	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7	
	9	JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9	
	A	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12	
	B	JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8	

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

Table 17. TMS370 Family Opcode/Instruction Map[†] (Continued)

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L S N	C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
	D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
	E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
	F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):

F4	8	MOVW *n[Rn] 4/15	DIV Rn,A 3/14-63
F4	9	JMPL *n[Rn] 4/16	
F4	A	MOV *n[Rn],A 4/17	
F4	B	MOV A,*n[Rn] 4/16	
F4	C	BR *n[Rn] 4/16	
F4	D	CMP *n[Rn],A 4/18	
F4	E	CALL *n[Rn] 4/20	
F4	F	CALLR *n[Rn] 4/22	

Legend:

* = Indirect addressing operand prefix
 & = Direct addressing operand prefix
 # = immediate operand
 #16 = immediate 16-bit number
 lab = 16-label
 n = immediate 8-bit number
 Pd = Peripheral register containing destination type
 Pn = Peripheral register
 Ps = Peripheral register containing source byte
 ra = Relative address
 Rd = Register containing destination type
 Rn = Register file
 Rp = Register pair
 Rpd = Destination register pair
 Rps = Source Register pair
 Rs = Register containing source byte

[†] All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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development system support

The TMS370 family development support tools include an assembler, a C compiler, a linker, an in-circuit emulator (XDS/22), compact development tool (CDT) and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850-02 for PC)
 - Includes extensive macro capability
 - Provides high-speed operation
 - Offers format conversion utilities available for popular formats
- ANSI C compiler (Part No. TMDS3740855-02 for PC, Part No. TMDS3740555-09 for HP700™, Sun-3™ or Sun-4™)
 - Generates assembly code of the TMS370 that can be inspected easily
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables the user to directly reference the TMS370's port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (compact development tool) real-time in-circuit emulation
 - Base (Part Number EDSCDT370 – for PC, requires cable)
 - Cable for 44-pin PLCC (Part No. EDSTRG44PLCC)
 - Cable for 40-pin DIP (Part No. EDSTRG40DIL)
 - Cable for 40-pin SDIP (Part No. EDSTRG40SDIL)
 - Provides EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Allows uploading and downloading of program and data memory
 - Provides capability to execute programs and software routines
 - Includes 1 024-sample trace buffer
 - Includes single-step executable instructions
 - Allows uses of software breakpoints to halt program execution at selected address
- XDS/22 (extended development support) in-circuit emulator
 - Base (Part No. TMDS3762210 For PC, requires cable)
 - Cable for 44-pin PLCC, 40-pin DIP, or shrink DIP (Part No. TMDS3788844)
 - Contains all the features of the CDT370 described above but does not have the capability to program the data EEPROM and program EPROM
 - Contains sophisticated breakpoint trace and timing hardware that provides up to 2047 qualified trace samples with symbolic disassembly
 - Allows breakpoints to be qualified by address and/or data on any type of memory acquisition. Up to four levels of events can be combined to cause a breakpoint.

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development system support (continued)

- Provides timers for analyzing total and average time in routines
- Contains an eight-line logic probe for adding external signal visibility to the breakpoint qualifier and to the trace display
- Microcontroller programmer
 - Base (Part No. TMDS3760500A – For PC, requires programming head)
 - Single unit head for 44-pin PLCC (Part No. TMDS3780510A)
 - Single unit head for 40-pin DIP or shrink DIP (Part No. TMDS3780511A)
 - PC-based, window/function-key oriented user interface for ease of use and a rapid learning environment
- Starter kit (Part No. TMDX37000 – For PC)
 - Includes TMS370 Assembler diskette and documentation
 - Includes TMS370 Simulator
 - Includes programming adapter board and programming software
 - Does not include – (to be supplied by the user):
 - + 5 V power supply
 - ZIF sockets
 - 9-pin RS-232 cable

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device numbering conventions

Figure 17 illustrates the numbering and symbol nomenclature for the TMS370Cx4x family.

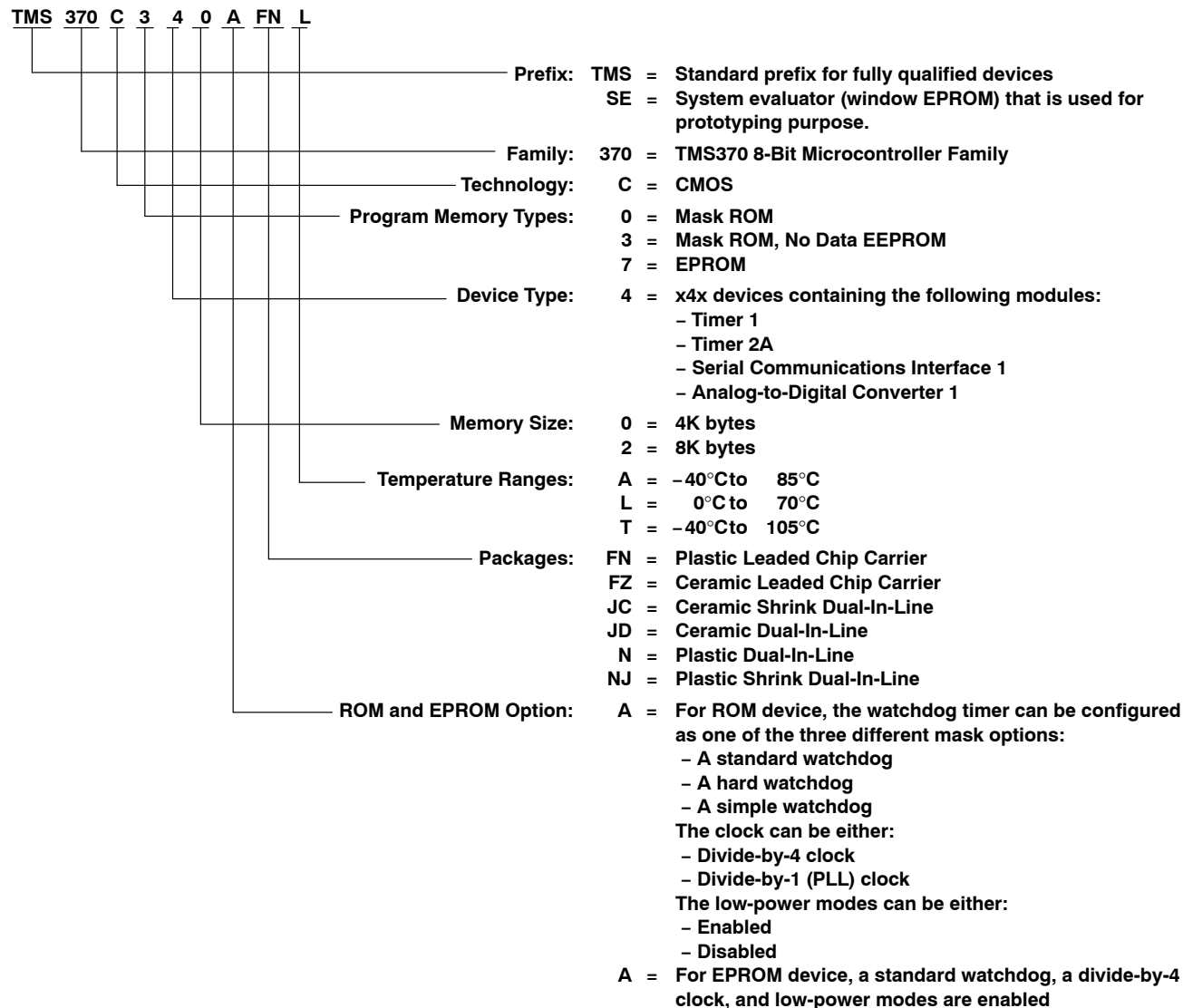


Figure 17. TMS370Cx4x Family Nomenclature

device part numbers

Table 18 lists all the 'x4x devices available at present. The device part-number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog timer options desired. Each device can have only one of the possible three watchdog timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 18. Device Part Numbers

DEVICE PART NUMBERS FOR 44 PINS (LCC)	DEVICE PART NUMBERS FOR 40 PINS (DIP)	DEVICE PART NUMBERS FOR 40 PINS (SDIP)
TMS370C040AFNA TMS370C040AFNL TMS370C040AFNT	TMS370C040ANA TMS370C040ANL TMS370C040ANT	TMS370C040ANJA [†] TMS370C040ANJL [†] TMS370C040ANJT [†]
TMS370C042AFNA TMS370C042AFNL TMS370C042AFNT	TMS370C042ANA TMS370C042ANL TMS370C042ANT	TMS370C042ANJA [†] TMS370C042ANJL [†] TMS370C042ANJT [†]
TMS370C340AFNA TMS370C340AFNL TMS370C340AFNT	TMS370C340ANA TMS370C340ANL TMS370C340ANT	TMS370C340ANJA [†] TMS370C340ANJL [†] TMS370C340ANJT [†]
TMS370C342AFNA TMS370C342AFNL TMS370C342AFNT	TMS370C342ANA TMS370C342ANL TMS370C342ANT	TMS370C342ANJA [†] TMS370C342ANJL [†] TMS370C342ANJT [†]
TMS370C742AFNT	TMS370C742ANT	TMS370C742ANJT [†]
SE370C742AFZT [‡]	SE370C742AJDT [‡]	SE370C742AJCT [‡]

[†] The NJ designator for the 40-pin plastic shrink DIP package was known formerly as the N2. The mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

[‡] System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.

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new code release form

Figure 18 shows a sample of the new code release form.

NEW CODE RELEASE FORM TEXAS INSTRUMENTS TMS370 MICROCONTROLLER PRODUCTS			DATE: _____																
To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information: 1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media) 2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.																			
Company Name: _____ Street Address: _____ Street Address: _____ City: _____ State _____ Zip _____		Contact Mr./Ms.: _____ Phone: (_____) _____ Ext.: _____ Customer Purchase Order Number: _____ Customer Print Number *Yes: _____ # _____ No: _____ (Std. spec to be followed) *If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.																	
Customer Part Number: _____ Customer Application: _____ TMS370 Device: _____ TI Customer ROM Number: _____ (provided by Texas Instruments)		CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS <table style="width: 100%;"><tr><td>Low Power Modes</td><td>Watchdog counter</td><td>Clock Type</td></tr><tr><td>☐ Enabled</td><td>☐ Standard</td><td>☐ Standard (/4)</td></tr><tr><td>☐ Disabled</td><td>☐ Hard Enabled</td><td>☐ PLL (/1)</td></tr><tr><td></td><td>☐ Simple Counter</td><td></td></tr></table> NOTE: Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the <i>TMS370 Family User's Guide</i> (literature number SPNU127) or the <i>TMS370 Family Data Manual</i> (literature number SPNS014B).		Low Power Modes	Watchdog counter	Clock Type	☐ Enabled	☐ Standard	☐ Standard (/4)	☐ Disabled	☐ Hard Enabled	☐ PLL (/1)		☐ Simple Counter					
Low Power Modes	Watchdog counter			Clock Type															
☐ Enabled	☐ Standard			☐ Standard (/4)															
☐ Disabled	☐ Hard Enabled			☐ PLL (/1)															
	☐ Simple Counter																		
OSCILLATOR FREQUENCY <table style="width: 100%;"><thead><tr><th></th><th>MIN</th><th>TYP</th><th>MAX</th></tr></thead><tbody><tr><td>☐ External Drive (CLKIN)</td><td>_____</td><td>_____</td><td>_____</td></tr><tr><td>☐ Crystal</td><td>_____</td><td>_____</td><td>_____</td></tr><tr><td>☐ Ceramic Resonator</td><td>_____</td><td>_____</td><td>_____</td></tr></tbody></table> ☐ Supply Voltage MIN: _____ MAX: _____ (std range: 4.5V to 5.5V)			MIN	TYP	MAX	☐ External Drive (CLKIN)	_____	_____	_____	☐ Crystal	_____	_____	_____	☐ Ceramic Resonator	_____	_____	_____		
	MIN	TYP	MAX																
☐ External Drive (CLKIN)	_____	_____	_____																
☐ Crystal	_____	_____	_____																
☐ Ceramic Resonator	_____	_____	_____																
TEMPERATURE RANGE <table style="width: 100%;"><tbody><tr><td>☐ 'L':</td><td>0° to 70°C (standard)</td></tr><tr><td>☐ 'A':</td><td>-40° to 85°C</td></tr><tr><td>☐ 'T':</td><td>-40° to 105°C</td></tr></tbody></table>		☐ 'L':	0° to 70°C (standard)	☐ 'A':	-40° to 85°C	☐ 'T':	-40° to 105°C												
☐ 'L':	0° to 70°C (standard)																		
☐ 'A':	-40° to 85°C																		
☐ 'T':	-40° to 105°C																		
SYMBOLIZATION ☐ TI standard symbolization ☐ TI standard w/customer part number ☐ Customer symbolization (per attached spec, subject to approval)		PACKAGE TYPE <table style="width: 100%;"><tbody><tr><td>☐ 'N' 28-pin PDIP</td><td>☐ "FN" 44-pin PLCC</td></tr><tr><td>☐ "FN" 28-pin PLCC</td><td>☐ "FN" 68-pin PLCC</td></tr><tr><td>☐ "N" 40-pin PDIP</td><td>☐ "NM" 64-pin PSDIP</td></tr><tr><td>☐ "NJ" 40-pin PSDIP (formerly known as N2)</td><td></td></tr></tbody></table> BUS EXPANSION ☐ YES ☐ NO		☐ 'N' 28-pin PDIP	☐ "FN" 44-pin PLCC	☐ "FN" 28-pin PLCC	☐ "FN" 68-pin PLCC	☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP	☐ "NJ" 40-pin PSDIP (formerly known as N2)									
☐ 'N' 28-pin PDIP	☐ "FN" 44-pin PLCC																		
☐ "FN" 28-pin PLCC	☐ "FN" 68-pin PLCC																		
☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP																		
☐ "NJ" 40-pin PSDIP (formerly known as N2)																			
NON-STANDARD SPECIFICATIONS: ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.																			
RELEASE AUTHORIZATION: This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cycletime commences when this document is signed off and the verification code is approved by the customer.																			
1. Customer: _____ Date: _____		2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____																	

Figure 18. Sample New Code Release Form



Table 19 is a collection of all the peripheral file frames using the 'Cx4x (provided for a quick reference).

Table 19. Peripheral File Frame Compilation

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	SYSTEM CONFIGURATION REGISTERS								
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011		—	—	AUTOWAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D to P01F	Reserved								
	DIGITAL PORT CONTROL REGISTERS								
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	—	—	—	—	—	Port B Control Register 2 (must be 0)			BPORT2
P026	—	—	—	—	—	Port B Data			BDATA
P027	—	—	—	—	—	Port B Direction			BDIR
P028 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0) [†]					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR
	TIMER 1 MODULE REGISTER								
	Modes: Dual-Compare and Capture/Compare								
P040	Bit 15	T1 Counter MSbyte						Bit 8	T1CNTR
P041	Bit 7	T1 Counter LSbyte						Bit 0	
P042	Bit 15	Compare-Register MSbyte						Bit 8	T1C
P043	Bit 7	Compare-Register LSbyte						Bit 0	

[†] To configure pin D3 as CLKOUT, set port D control register 2 = 08h.

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Table 19. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
TIMER 1 MODULE REGISTER (CONTINUED)									
P044	Bit 15 Capture/Compare-Register MSbyte							Bit 8	T1CC
P045	Bit 7 Capture/Compare-Register LSbyte							Bit 0	
P046	Bit 15 Watchdog-Counter MSbyte							Bit 8	WDCNTR
P047	Bit 7 Watchdog-Counter LSbyte							Bit 0	
P048	Bit 7 Watchdog-Reset Key							Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI
SCI1 MODULE CONTROL REGISTER									
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNC/ ISOSYNC	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RE- SET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	Reserved								
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until after a full power-down cycle has been completed.



Table 19. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P05A P05B P05C	Reserved								
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	SCI STEST	SCITX PRIORITY	SCIRX PRIORITY	SCI ESPEN	—	—	—	—	SCIPRI
T2A MODULE REGISTER									
Modes: Dual-Capture and Dual-Compare									
P060	Bit 15 T2A Counter MSbyte Bit 8								T2ACNTR
P061	Bit 7 T2A Counter LSbyte Bit 0								
P062	Bit 15 Compare Register MSbyte Bit 8								T2AC
P063	Bit 7 Compare Register LSbyte Bit 0								
P064	Bit 15 Capture/Compare Register MSbyte Bit 8								T2ACC
P065	Bit 7 Capture/Compare Register LSbyte Bit 0								
P066	Bit 15 Capture Register 2 MSbyte Bit 8								T2AIC
P067	Bit 7 Capture Register 2 LSbyte Bit 0								
P068 P069	Reserved								
P06A	—	—	—	T2A OVRFL- INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1
Mode: Dual-Compare									
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC2 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
Mode: Dual-Capture									
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
Modes: Dual-Capture and Dual-Compare									
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2/PWM DATA IN	T2AIC2/PWM DATA OUT	T2AIC2/PWM FUNCTION	T2AIC2/PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC1/CR DATA DIR	T2APC2
P06F	T2A STEST	T2A PRIORITY	—	—	—	—	—	—	T2APRI
ADC1 MODULE CONTROL REGISTER									
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT

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Table 19. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P072	A-to-D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} , V_{CC3} (see Note 1)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC}) [‡]	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	1 W
Operating free-air temperature, T_A : L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Electrical characteristics are specified with all output buffers loaded with the specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

NOTE 1: Unless otherwise noted, all voltage values are with respect to V_{SS} .

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage (see Note 1)		4.5	5	5.5	V
V _{CC}	RAM data retention supply voltage (see Note 2)		3		5.5	V
V _{CC3}	Analog supply voltage (see Note 1)		4.5	5	5.5	V
V _{SS3}	Analog supply ground		– 0.3	0	0.3	V
V _{IL}	Low-level input voltage	All pins except MC	V _{SS}		0.8	V
		MC, normal operation	V _{SS}		0.3	
V _{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET	2		V _{CC}	V
		XTAL2/CLKIN	0.8 V _{CC}		V _{CC}	
		RESET	0.7 V _{CC}		V _{CC}	
V _{MC}	MC (mode control) voltage	EEPROM write protect override	11.7	12	13	V
		Microcomputer	V _{SS}		0.3	
		EPROM programming voltage (V _{PP})	13	13.2	13.5	
T _A	Operating free-air temperature	L version	0		70	°C
		A version	– 40		85	
		T version	– 40		105	

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS} .

2. RESET must be externally activated when V_{CC} or SYSCLK is out of the recommended operating range.

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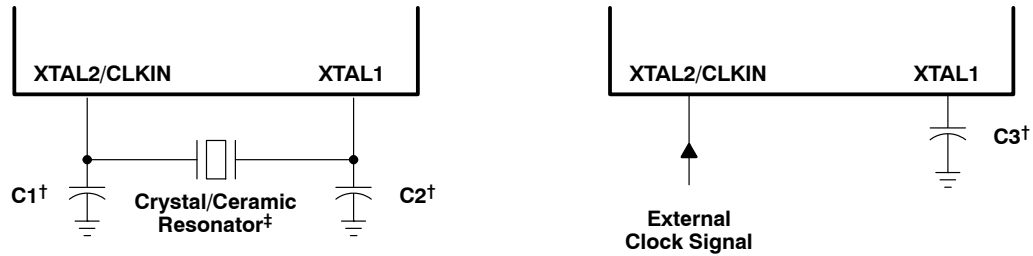
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level digital output voltage	$I_{OL} = 1.4 \text{ mA}$			0.4	V
V_{OH}	High-level output voltage	$I_{OH} = -50 \mu\text{A}$	$0.9 V_{CC}$			V
		$I_{OH} = -2 \text{ mA}$	2.4			
I_I	Input current	MC	$0 \text{ V} < V_I \leq 0.3 \text{ V}$		10	μA
			$0.3 \text{ V} < V_I \leq 13$		650	
			$12 \text{ V} \leq V_I \leq 13 \text{ V}$ (see Note 3)		50	mA
I_I	Input current	I/O pins	$0 \text{ V} \leq V_I \leq V_{CC}$		± 10	μA
I_{OL}	Low-level output current	$V_{OL} = 0.4 \text{ V}$		1.4		mA
I_{OH}	High-level output current	$V_{OH} = 0.9 V_{CC}$		-50		μA
		$V_{OH} = 2.4 \text{ V}$		-2		mA
I_{CC}	Supply current (Operating mode) OSC POWER bit = 0 (see Note 6)	SYSCLK = 5 MHz (see Notes 4 and 5)		30	45	mA
		SYSCLK = 3 MHz (see Notes 4 and 5)		20	30	
		SYSCLK = 0.5 MHz (see Notes 4 and 5)		7	11	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 7)	SYSCLK = 5 MHz (see Notes 4 and 5)		10	17	mA
		SYSCLK = 3 MHz (see Notes 4 and 5)		8	11	
		SYSCLK = 0.5 MHz (see Notes 4 and 5)		2	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 8)	SYSCLK = 3 MHz (see Notes 4 and 5)		6	8.6	mA
		SYSCLK = 0.5 MHz (see Notes 4 and 5)		2	3.0	
	Supply current (HALT mode)	XTALK2/CLKIN < 0.2 V (see Note 4)		2	30	μA

- NOTES: 3. Microcontroller-single chip mode, ports configured as inputs, or outputs with no load. All inputs $\leq 0.2 \text{ V}$ or $\geq V_{CC} - 0.2 \text{ V}$.
4. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK this extra current = $0.01 \text{ mA} \times (\text{total load capacitance} + \text{crystal capacitance in pF})$.
5. Maximum operating current = $7.6 (\text{SYSCLK}) + 7 \text{ mA}$.
6. Maximum standby current = $3 (\text{SYSCLK}) + 2 \text{ mA}$. (Osc power bit = 0.)
7. Maximum standby current = $2.24 (\text{SYSCLK}) + 1.9 \text{ mA}$. (Osc power bit = 1 and valid up to 3-MHz SYSCLK.)
8. Input current I_{pp} is a maximum of 50 mA only when EPROM is being programmed.



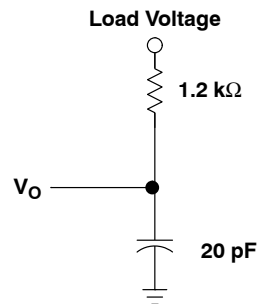
RECOMMENDED CRYSTAL/CLOCK CONNECTIONS



[†] The values of C1 and C2 are typically 15 pF and C3 value is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

[‡] The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.

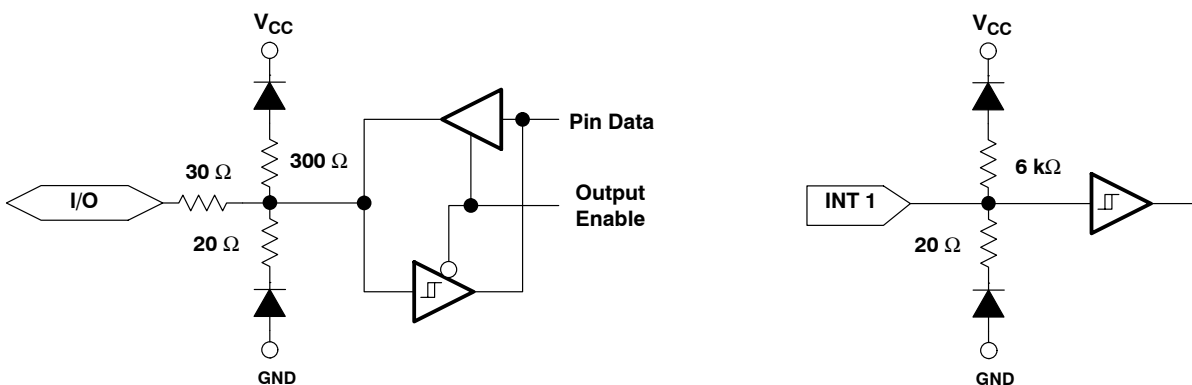
TYPICAL OUTPUT LOAD CIRCUIT[§]



Case 1: V_O = V_{OH} = 2.4 V; Load Voltage = 0 V
 Case 2: V_O = V_{OL} = 0.4 V; Load Voltage = 2.1

[§] All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

TYPICAL INPUT BUFFERS



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PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

A	Address	R	Read
AR	Array	RXD	SCIRXD
B	Byte	SC	SYSCLK
Cl	XTAL2/CLKIN	SCC	SCICLK
D	Data	TXD	SCITXD
PGM	Program	W	Write

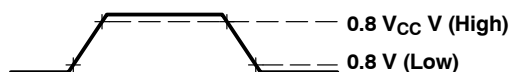
Lowercase subscripts and their meanings are:

c	cycle time (period)	r	rise time
d	delay time	su	setup time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

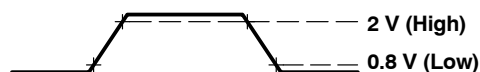
The following additional letters are used with these meanings:

H	High	V	Valid
L	Low	Z	High Impedance

All timings are measured between high and low measurement points as indicated in the figures below.



XTAL2/CLKIN Measurement Points



General Measurement Points

external clocking requirements for clock divided by 4[†]

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 9)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN Crystal operating frequency	2	20	MHz
	SYSCLK System clock [‡]	0.5	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions.

[‡] SYSCLK = CLKIN/4

NOTE 9: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

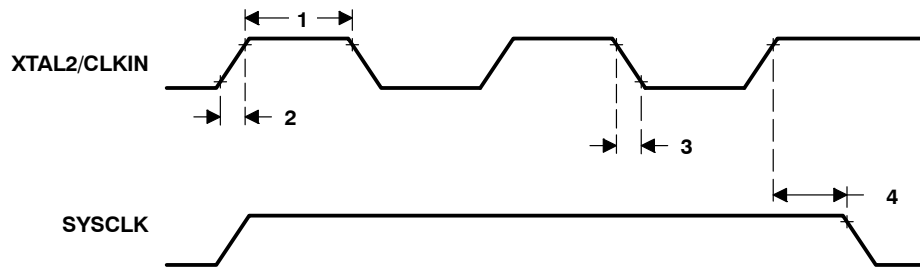


Figure 19. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL)^{†§}

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 9)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN Crystal operating frequency	2	5	MHz
	SYSCLK System clock [§]	2	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions.

[§] SYSCLK = CLKIN/1

NOTE 9: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

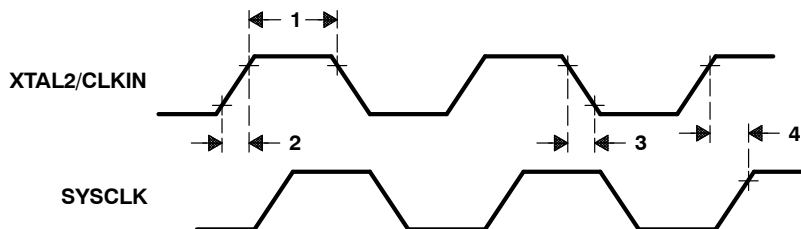


Figure 20. External Clock Timing for Divide-by-1

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switching characteristics and timing requirements (see Note 10 and Figure 21)

NO.	PARAMETER		MIN	MAX	UNIT	
5	t _c	Cycle time, SYSCLK (system clock)	Divide-by-4	200	2000	ns
			Divide-by-1	200	500	ns
6	t _{w(SCL)}	Pulse duration, SYSCLK low	0.5 t _c - 20	0.5 t _c	ns	
7	t _{w(SCH)}	Pulse duration, SYSCLK high	0.5 t _c	0.5 t _c + 20	ns	

NOTE 10: t_c = system-clock cycle time = $1/\text{SYSCLK}$.

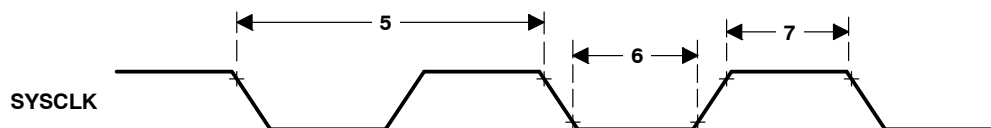
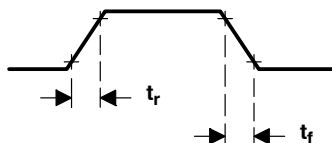


Figure 21. SYSCLK Timing

general-purpose output signal-switching time requirements

	MIN	TYP	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns



recommended EEPROM timing requirements for programming

	MIN	MAX	UNIT
$t_{w(PGM)B}$ Pulse duration, programming signal to be certain valid data is stored (byte mode)	10		ms
$t_{w(PGM)AR}$ Pulse duration, programming signal to be certain valid data is stored (array mode)	20		ms

recommended EPROM operating conditions for programming

	MIN	TYP	MAX	UNIT
V_{CC} Supply voltage	4.75	5.5	6	V
V_{PP} Supply voltage at MC pin	13	13.2	13.5	V
I_{PP} Supply current at MC pin during programming ($V_{PP} = 13$ V)		30	50	mA
SYSCLK System clock	Divide-by-4	0.5	5	MHz
	Divide-by-1	2	5	

recommended EPROM timing requirements for programming

	MIN	TYP	MAX	UNIT
$t_{w(EPGM)}$ Pulse duration, programming signal (see Note 11)	0.40	0.50	3	ms

NOTE 11: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.



SERIAL COMMUNICATIONS INTERFACE 1 (SCI1) INTERNAL CLOCK ISOSYNCHRONOUS MODE I/O TIMING

SCI1 isosynchronous mode timing characteristics and requirements for internal clock (see Note 10 and Figure 22)

NO.	PARAMETER	MIN	MAX	UNIT
24	$t_c(SCC)$ Cycle time, SCICLK	$2t_c$	$131,072t_c$	ns
25	$t_w(SCCL)$ Pulse duration, SCICLK low	$t_c - 45$	$0.5t_c(SCC) + 45$	ns
26	$t_w(SCCH)$ Pulse duration, SCICLK high	$t_c - 45$	$0.5t_c(SCC) + 45$	ns
27	$t_d(SCCL-TXDV)$ Delay time, SCITXD valid after SCICLK low	- 50	60	ns
28	$t_v(SCCH-TXD)$ Valid time, SCITXD data after SCICLK high	$t_w(SCCH) - 50$		ns
29	$t_{su}(RXD-SCCH)$ Setup time, SCIRXD to SCICLK high	$0.25t_c + 145$		ns
30	$t_v(SCCH-RXD)$ Valid time, SCIRXD data after SCICLK high	0		ns

NOTE 10: t_c = system-clock cycle time = $1/SYSCLK$.

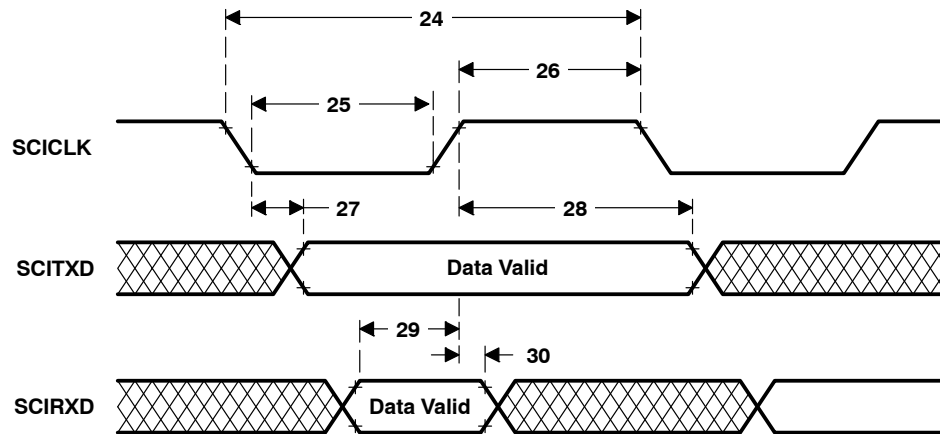


Figure 22. SCI1 Isosynchronous Mode Timing Diagram for Internal Clock

**SERIAL COMMUNICATIONS INTERFACE 1 (SCI1) EXTERNAL CLOCK
ISOSYNCHRONOUS MODE I/O TIMING**

**SCI1 isosynchronous mode timing characteristics and requirements for external clock
(see Note 10 and Figure 23)**

NO.	PARAMETER	MIN	MAX	UNIT
31	$t_c(\text{SCC})$ Cycle time, SCICLK	$10t_c$		ns
32	$t_w(\text{SCCL})$ Pulse duration, SCICLK low	$4.25t_c + 120$		ns
33	$t_w(\text{SCCH})$ Pulse duration, SCICLK high	$t_c + 120$		ns
34	$t_d(\text{SCCL-TXDV})$ Delay time, SCITXD valid after SCICLK low		$4.25t_c + 145$	ns
35	$t_v(\text{SCCH-TXD})$ Valid time, SCITXD data after SCICLK high	$t_w(\text{SCCH})$		ns
36	$t_{su}(\text{RXD-SCCH})$ Setup time, SCIRXD to SCICLK high	40		ns
37	$t_v(\text{SCCH-RXD})$ Valid time, SCIRXD data after SCICLK high	$2t_c$		ns

NOTE 10: t_c = system-clock cycle time = $1/\text{SYSCLK}$.

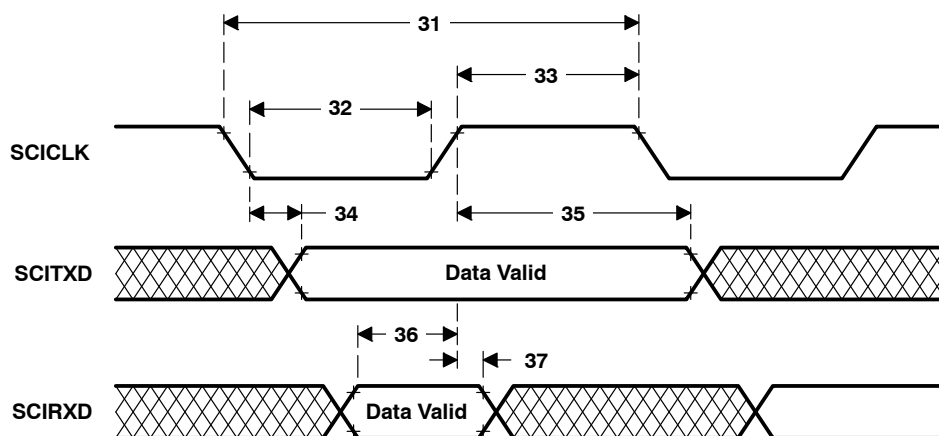


Figure 23. SCI1 Isosynchronous Mode Timing Diagram for External Clock

ADC1

The ADC1 has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3} . Their purpose is to enhance ADC1 performance by preventing digital switching noise on the logic circuitry that could be present on V_{SS} and V_{CC} from coupling into the ADC1 analog stage. All ADC1 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution 8 bits (256 values)
 Monotonic Yes
 Output conversion code 00h to FFh (00h for $V_I \leq V_{SS3}$; FFh for $V_I \geq V_{ref}$)
 Conversion time (excluding sample time) $164t_c$

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC3} Analog supply voltage	4.5	5	5.5	V
	$V_{CC3} - 0.3$		$V_{CC3} + 0.3$	
V_{SS3} Analog ground	$V_{SS3} - 0.3$		$V_{SS3} + 0.3$	V
V_{ref} Non- V_{CC3} reference [†]	2.5	V_{CC3}	$V_{CC3} + 0.1$	V
Analog input for conversion	V_{SS3}		V_{ref}	V

[†] V_{ref} must be stable, within $\pm 1/2$ LSB of the required resolution, during the entire conversion time.

operating characteristics over ranges of recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Absolute accuracy (see Note 12)	$V_{CC3} = 5.5$ V, $V_{ref} = 5.1$ V		+1.5	LSB
Differential/integral linearity error (see Notes 12 and 13)	$V_{CC3} = 5.5$ V, $V_{ref} = 5.1$ V		± 0.9	LSB
I_{CC3} Analog supply current	Converting		2	mA
	Nonconverting		5	μ A
I_I Input current, AN0-AN7	0 V $\leq V_I \leq 5.5$ V		2	μ A
V_{ref} input charge current			1	mA
Z_{ref} Source impedance V_{ref}	$SYSCLK \leq 3$ MHz		24	k Ω
	3 MHz $< SYSCLK \leq 5$ MHz		10	k Ω

NOTES: 12. Absolute resolution = 20 mV. At $V_{ref} = 5$ V, this is 1 LSB. As V_{ref} decreases, LSB size decreases and thus absolute accuracy and differential / integral linearity errors in terms of LSBs increases.

13. Excluding quantization error of $1/2$ LSB.

ADC1 (continued)

The ADC1 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined such that high-impedance sources can be accommodated without penalty to low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC1 control register (ADCTL) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START) of the ADCTL is set to 1. After a hold time, the converter resets the SAMPLE START and CONVERT START bits, signaling that a conversion has started and the analog signal can be removed.

analog timing requirements

	MIN	MAX	UNIT
$t_{su(S)}$ Setup time, analog input to sample command	0		ns
$t_{h(AN)}$ Hold time, analog input from start of conversion	$18t_c$		ns
$t_{w(S)}$ Pulse duration, sample time per kilohm of source impedance (see Note 14)	1		$\mu s/k\Omega$

NOTE 14: The value given is valid for a signal with a source impedance > 1 k Ω . If the source impedance is < 1 k Ω , use a minimum sampling time of 1 μs .

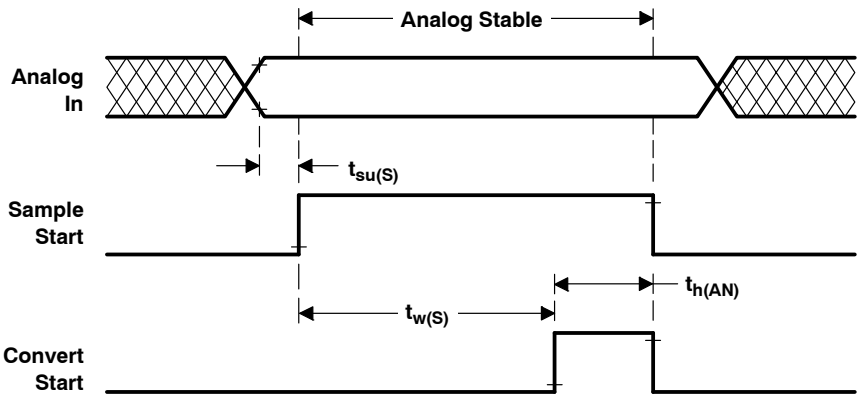


Figure 24. Analog Timing

Table 20 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

Table 20. TMS370Cx4x Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 44 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C040AFNA TMS370C040AFNL TMS370C040AFNT TMS370C042AFNA TMS370C042AFNL TMS370C042AFNT TMS370C340AFNA TMS370C340AFNL TMS370C340AFNT TMS370C342AFNA TMS370C342AFNL TMS370C342AFNT TMS370C742AFNT
FZ – 44 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C742AFZT
JD – 40 pin (100-mil pin spacing)	CERAMIC DUAL-IN-LINE PACKAGE (CDIP)	JD(R-CDIP-T**) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE	SE370C742AJDT
N – 40 pin (100-mil pin spacing)	PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	N(R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE	TMS370C040ANA TMS370C040ANL TMS370C040ANT TMS370C042ANA TMS370C042ANL TMS370C042ANT TMS370C340ANA TMS370C340ANL TMS370C340ANT TMS370C342ANA TMS370C342ANL TMS370C342ANT TMS370C742ANT
JC – 40 pin (70-mil pin spacing)	CERAMIC SHRINK DUAL-IN-LINE PACKAGE (CSDIP)	JC(R-CDIP-T40) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE	SE370C742AJCT
NJ – 40 pin (70-mil pin spacing) [†]	PLASTIC SHRINK DUAL-IN-LINE PACKAGE (PSDIP)	NJ(R-PDIP-T**) PLASTIC SHRINK DUAL-IN-LINE PACKAGE	TMS370C040ANJA TMS370C040ANJL TMS370C040ANJT TMS370C042ANJA TMS370C042ANJL TMS370C042ANJT TMS370C340ANJA TMS370C340ANJL TMS370C340ANJT TMS370C342ANJA TMS370C342ANJL TMS370C342ANJT TMS370C742ANJT

[†] NJ formerly known as N2; the mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

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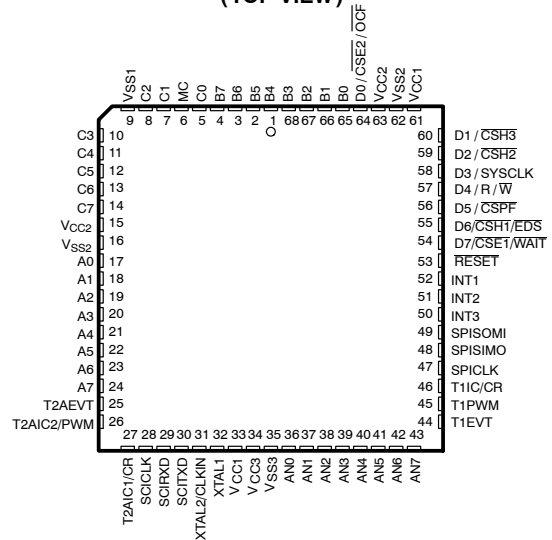
General Information	1
Selection Guide/Tools	2
Ops Cond/Timing/Glossary	3
TMS370Cx0x Data Sheet	4
TMS370Cx1x Data Sheet	5
TMS370Cx2x Data Sheet	6
TMS370Cx32 Data Sheet	7
TMS370Cx36 Data Sheet	8
TMS370Cx4x Data Sheet	9
TMS370Cx5x Data Sheet	10
TMS370Cx6x Data Sheet	11
TMS370Cx7x Data Sheet	12
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TMS370CxCx Data Sheet	17
Mechanical Data	18
Quality and Reliability	19
Electrostatic Discharge Guidelines	20

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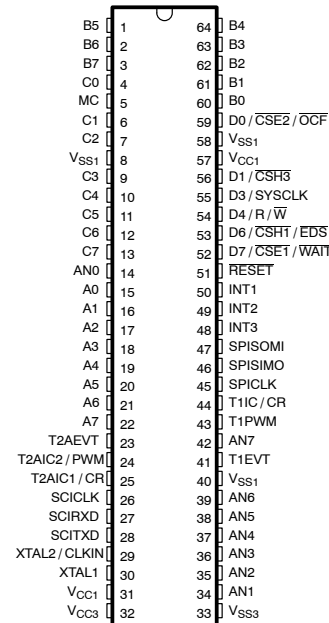
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- **CMOS/EEPROM/EPROM Technologies on a Single Device**
 - Mask-ROM Devices for High-Volume Production
 - One-Time-Programmable (OTP) EPROM Devices for Low-Volume Production
 - Reprogrammable EPROM Devices for Prototyping Purposes
- **Internal System Memory Configurations**
 - On-Chip Program Memory Versions
 - ROM: 4K to 48K Bytes
 - EPROM: 16K to 48K Bytes
 - ROM-less
 - Data EEPROM: 256 or 512 Bytes
 - Static RAM: 256 to 3.5K Bytes
 - External Memory/Peripheral Wait States
 - Precoded External Chip-Select Outputs in Microcomputer Mode
- **Flexible Operating Features**
 - Low-Power Modes: STANDBY and HALT
 - Commercial, Industrial, and Automotive Temperature Ranges
 - Clock Options
 - Divide-by-4 (0.5 MHz – 5 MHz SYSCLK)
 - Divide-by-1 (2 MHz – 5 MHz SYSCLK)
 - Phase-Locked Loop (PLL)
 - Supply Voltage (V_{CC}): 5 V $\pm$ 10%
- **Eight-Channel 8-Bit Analog-to-Digital Converter 1 (ADC1)**
- **Two 16-Bit General-Purpose Timers**
- **On-Chip 24-Bit Watchdog Timer**
- **Two Communication Modules**
 - Serial Communications Interface 1 (SCI1)
 - Serial Peripheral Interface (SPI)
- **Flexible Interrupt Handling**
- **TMS370 Series Compatibility**
- **CMOS/Package/TTL-Compatible I/O Pins**
 - 64-Pin Plastic and Ceramic Shrink Dual-In-Line Packages/44 Bidirectional, 9 Input Pins
 - 68-Pin Plastic and Ceramic Leaded Chip Carrier Packages/46 Bidirectional, 9 Input Pins
 - All Peripheral Function Pins Are Software Configurable for Digital I/O

**FN/FZ PACKAGE
(TOP VIEW)**



**JN/NM PACKAGE
(TOP VIEW)**



- **Workstation/PC-Based Development System**
 - C Compiler and C Source Debugger
 - Real-Time In-Circuit Emulation
 - Extensive Breakpoint/Trace Capability
 - Software Performance Analysis
 - Multi-Window User Interface
 - Microcontroller Programmer



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INSTRUMENTS**

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TMS370Cx5x 8-BIT MICROCONTROLLER

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Pin Descriptions

PIN				I/O†	DESCRIPTION‡
NAME	ALTERNATE FUNCTION	SDIP (64)	LCC (68)		
A0 A1 A2 A3 A4 A5 A6 A7	DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7	15 16 17 18 19 20 21 22	17 18 19 20 21 22 23 24	I/O	Single-chip mode: Port A is a general-purpose bidirectional I/O port. Expansion mode: Port A can be individually programmed as the external bidirectional data bus (DATA0 – DATA7).
B0 B1 B2 B3 B4 B5 B6 B7	ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7	60 61 62 63 64 1 2 3	65 66 67 68 1 2 3 4	I/O	Single-chip mode: Port B is a general-purpose bidirectional I/O port. Expansion mode: Port B can be individually programmed as the low-order address output bus (ADDR0 – ADDR7).
C0 C1 C2 C3 C4 C5 C6 C7	ADDR8 ADDR9 ADDR10 ADDR11 ADDR12 ADDR13 ADDR14 ADDR15	4 6 7 9 10 11 12 13	5 7 8 10 11 12 13 14	I/O	Single-chip mode: Port C is a general-purpose bidirectional I/O port. Expansion mode: Port C can be individually programmed as the high-order address output bus (ADDR8 – ADDR15).
INT1 INT2 INT3	NMI — —	50 49 48	52 51 50	I I/O I/O	External (nonmaskable or maskable) interrupt/general-purpose input pin External maskable interrupt input/general-purpose bidirectional pin External maskable interrupt input/general-purpose bidirectional pin
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	E0 E1 E2 E3 E4 E5 E6 E7	14 34 35 36 37 38 39 42	36 37 38 39 40 41 42 43	I	ADC1 analog input (AN0 – AN7) or positive reference pins (AN1 – AN7) Port E can be individually programmed as general-purpose input pins if not used as ADC1 analog input or positive reference input.
V _{CC3} V _{SS3}		32 33	34 35		ADC1 positive-supply voltage and optional positive-reference input pin ADC1 ground reference pin
RESET		51	53	I/O	System reset bidirectional pin. RESET, as an input, initializes the microcontroller; as open-drain output, RESET indicates an internal failure was detected by the watchdog or oscillator fault circuit.
MC		5	6	I	Mode control (MC) pin. MC enables EEPROM write-protection override (WPO) mode, also EPROM V _{PP} .
XTAL2/CLKIN XTAL1		29 30	31 32	I O	Internal oscillator crystal input/external clock source input Internal oscillator output for crystal
V _{CC1}		31, 57	33, 61		Positive supply voltage
V _{CC2}		—	15, 63		Positive supply voltage

† I = input, O = output

‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Also, port D3 can be configured as SYSCLK.



Pin Descriptions (Continued)

PIN				I/O†	DESCRIPTION‡
NAME	ALTERNATE FUNCTION		SDIP (64)		
V _{SS1}			8, 58, 40	9	Ground reference for digital logic
V _{SS2}			—	16, 62	Ground reference for digital I/O logic
D0 D1 D2 D3 D4 D5 D6 D7	FUNCTION		59 56 — 55 54 — 53 52	64 60 59 58 57 56 55 54	I/O

† I = input, O = output

‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Port D3 also can be configured as SYSCLK.

NOTE 1: The three-pin configuration SCI is referred to as SCI1.

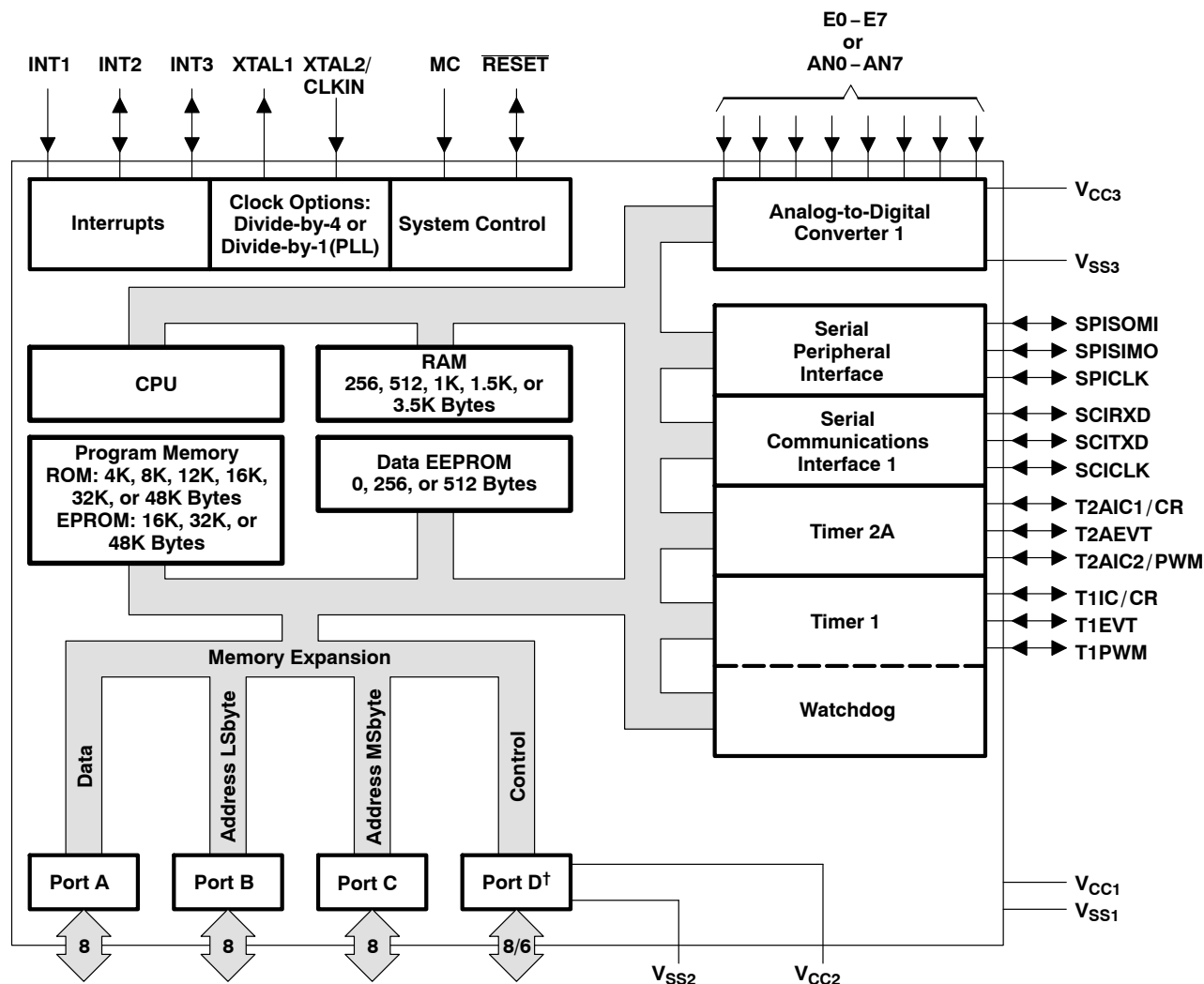
Table 1. Function A: Memory Accesses Locations for 'x5x Devices

FUNCTION A	'X50, 'X52, 'X53, AND 'X56	'X58	'X59
CSE _x	2000h – 3FFFh (8K bytes)	A000h – BFFFh (8K bytes)	E000h – EFFFh (4K bytes)
CSE _x	8000h – FFFFh (32K bytes)	C000h – FFFFh (16K bytes)	F000h – FFFFh (4K bytes)
CSPF	10C0h – 10FFh (64 bytes)	10C0h – 10FFh (64 bytes)	10C0h – 10FFh (64 bytes)

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functional block diagram



† For the 64-pin devices, there are only six pins for port D.

description

The TMS370Cx5x family of single-chip 8-bit microcontrollers provides cost-effective real-time system control through integration of advanced peripheral function modules and various on-chip memory configurations. The TMS370Cx5x family presently consists of twenty-one devices which are grouped into seven main sub-families: the TMS370Cx50, TMS370Cx52, TMS370Cx53, TMS370Cx56, TMS370Cx58, TMS370Cx59, and SE370C75x.

The TMS370Cx5x family of devices is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technologies. The low-operating power, wide-operating temperature range, and noise immunity of CMOS technology, coupled with the high performance and extensive on-chip peripheral functions, make the TMS370Cx5x devices attractive in system designs for automotive electronics, industrial motor control, computer peripheral control, telecommunications, and consumer application. Table 2 provides a memory configuration overview of the TMS370Cx5x devices.

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description (continued)

Table 2. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		OFF-CHIP MEMORY EXP. (BYTES)	DATA MEMORY (BYTES)		OPERATING MODES		PACKAGES 68 PIN PLCC/CLCC, OR 64 PIN PSDIP/CSDIP
	ROM	EPROM		RAM	EEPROM	μC†	μP†	
TMS370Cx50: TMS370C050, TMS370C150, TMS370C250, AND TMS370C350								
TMS370C050A	4K	—	112K	256	256	√	√	FN – PLCC / NM –PSDIP
TMS370C150A	—	—	56K	256	—	—	√	FN – PLCC
TMS370C250A	—	—	56K	256	256	—	√	FN – PLCC
TMS370C350A	4K	—	112K	256	—	√	√	FN – PLCC / NM –PSDIP
TMS370Cx52: TMS370C052, TMS370C352, AND TMS370C452								
TMS370C052A	8K	—	112K	256	256	√	√	FN – PLCC / NM –PSDIP
TMS370C352A	8K	—	112K	256	—	√	√	FN – PLCC / NM –PSDIP
TMS370C452A‡	8K	—	112K	256	256	√	√	FN – PLCC
TMS370Cx53: TMS370C353								
TMS370C353A	12K	—	112K	1.5K	—	√	√	FN – PLCC
TMS370Cx56: TMS370C056, TMS370C156, TMS370C256, TMS370C356, TMS370C456, AND TMS370C756								
TMS370C056A	16K	—	112K	512	512	√	√	FN – PLCC / NM –PSDIP
TMS370C156A	—	—	56K	512	—	—	√	FN – PLCC
TMS370C256A	—	—	56K	512	512	—	√	FN – PLCC
TMS370C356A	16K	—	112K	512	—	√	√	FN – PLCC / NM –PSDIP
TMS370C456A‡	16K	—	112K	512	512	√	√	FN – PLCC
TMS370C756A	—	16K	112K	512	512	√	√	FN – PLCC / NM –PSDIP
TMS370Cx58: TMS370C058, TMS370C358, AND TMS370C758								
TMS370C058A	32K	—	64K	1K	256	√	√	FN – PLCC / NM –PSDIP
TMS370C358A	32K	—	64K	1K	—	√	√	FN – PLCC / NM –PSDIP
TMS370C758A, TMS370C758B	—	32K	64K	1K	256	√	√	FN – PLCC / NM –PSDIP
TMS370Cx59: TMS370C059 AND TMS370C759								
TMS370C059A§	48K	—	20K	3.5K	256	√	√	FN – PLCC
TMS370C759A§	—	48K	20K	3.5K	256	√	√	FN – PLCC
EPROM DEVICE: SE370C756, SE370C758, and SE370C759								
SE370C756A¶	—	16K	112K	512	512	√	√	FZ – CLCC / JN –CSDIP
SE370C758A¶, SE370C758B¶	—	32K	64K	1K	256	√	√	FZ – CLCC / JN –CSDIP
SE370C759A§¶	—	48K	20K	3.5K	256	√	√	FZ – CLCC

[†] μC – Microcomputer mode

μP – Microprocessor mode

[‡] TMS370C45x support ROM memory security. Refer to the program ROM section.

[§] Only operate up to 3 MHz SYSCLK

[¶] System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.



description (continued)

The suffix letter (A or B) appended to the device names shown in the device column of Table 2 indicates the configuration of the device. ROM or an EPROM devices have different configurations as indicated in Table 3. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 3. Suffix Letter Configuration

DEVICE†	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM A	Standard	Divide-by-4 (Standard oscillator)	Enabled
EPROM B	Hard	Divide-by-1 (PLL)	Enabled
ROM A	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		
ROM-less A	Standard	Divide-by-4	Enabled

† Refer to the "device numbering conventions" section for device nomenclature and the "device part numbers" section for ordering.

Unless otherwise noted, the terms TMS370Cx50, TMS370Cx52, TMS370Cx53, TMS370Cx56, TMS370Cx58, TMS370Cx59, and SE370C75x refer to the individual devices listed in Table 2 and described in this data sheet. All TMS370Cx5x devices contain the following on-chip peripheral modules:

- Eight-channel, 8-bit analog-to-digital converter 1 (ADC1)
- Serial communications interface 1 (SCI1)
- Serial peripheral interface (SPI)
- One 24-bit general-purpose watchdog timer
- Two 16-bit general-purpose timers (one with an 8-bit prescaler)

TMS370C756, TMS370C758, and TMS370C759 are one-time programmable (OTP) devices that are available in plastic packages. This microcomputer is effective to use for immediate production updates for other members of the TMS370Cx5x family or for low-volume production runs when the mask charge or cycle time for low-cost mask ROM devices is not practical.

The SE370C756, SE370C758, and SE370C759 have windowed ceramic packages to allow reprogramming of the program EPROM memory during the development/prototyping phase of design. The SE370C75x devices allow quick updates to breadboards and prototype systems while iterating initial designs.

The TMS370Cx5x family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all central processing unit (CPU) activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx5x features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx5x family is fully instruction-set-compatible, allowing easy transition between members of the TMS370 8-bit microcontroller family.

The SPI and the two operational modes of the SCI1 give three methods of serial communications. The SCI1 allows standard RS-232-C communications interface between other common data transmission equipment, while the SPI gives high-speed communications between simpler shift-register type devices, such as display drivers, ADC1 converter, phase-locked loop (PLL), I/O expansion, or other microcontrollers in the system.

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description (continued)

For large memory applications, the TMS370Cx5x family provides an external bus with non-multiplexed address and data. Precoded memory chip-select outputs can be enabled, which allows minimum-chip-count system implementations. Wait-state support facilitates performance matching among the CPU, external memory, and the peripherals. All pins associated with memory expansion interface are individually software configurable for general purpose digital input/output (I/O) pins when operating in the microcomputer mode.

The TMS370Cx5x family provides the system designer with very economical, efficient solution to real-time control applications. The TMS370 family extended development system (XDS™) and compact development tool (CDT™) solve the challenge of efficiently developing the software and hardware required to design the TMS370Cx5x into an ever-increasing number of complex applications. The application source code can be written in assembly and C-language, and the output code can be generated by the linker. The TMS370 family XDS development tools communicate through a standard RS-232-C interface with an existing personal computer. This allows the use of the personal computer editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes ease-of-use through extensive use of menus and screen windowing so that a system designer with minimal training can begin developing software. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as reduced time-to-market cycle.

The TMS370Cx5x family together with the TMS370 family XDS/22, CDT370, design kit, starter kit, software tools, the SE370C75x reprogrammable devices, comprehensive product documentation, and customer support provide a complete solution to the needs of the system designer.

modes

The TMS370Cx5x has four operating modes, two basic modes with each mode having two memory configurations. The basic operating modes are the microcomputer and microprocessor modes, which are selected by the voltage level applied to the dedicated MC pin two cycles before $\overline{\text{RESET}}$ goes inactive. The two memory configurations then are selected through software programming of the internal system configuration registers. The four operating modes are the microcomputer single chip, microcomputer with external expansion, microprocessor without internal program memory, and microprocessor with internal program memory. These modes are described in the following list.

- Microcomputer single chip mode:
 - Operates as a self-contained microcomputer with all memory and peripherals on-chip.
 - Maximizes the general-purpose I/O capability for real-time control applications.
- Microcomputer with external expansion mode:
 - Supports bus expansion to external memory or peripherals, while all on-chip memory (RAM, ROM, EPROM, and data EEPROM) remains active.
 - Configures digital I/O ports (ports A, B, C, and D) through software, under control of the associated port control, to become external memory as follows:
 - Port A: 8-bit data memory
 - Port B and C: 16-bit address memory
 - Port D: 8-bit control memory (pin not used as function A or B can be configured as I/O)
 - Utilizes the pins available (not used for address, data, or control memory) as general-purpose input/output by programming them individually.
 - Lowers the system cost by not requiring an external address/data latch (address memory and data memory are nonmultiplexed).

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modes (continued)

- Reduces external interface decode logic by using the precoded chip select outputs that provide direct memory/peripheral chip select or chip enable functions.
- Function A maps up to 112K bytes of external memory into the address space by using $\overline{\text{CSE1}}$, $\overline{\text{CSE2}}$, $\overline{\text{CSH1}}$, $\overline{\text{CSH2}}$, and $\overline{\text{CSH3}}$ as memory-bank selects under software control.
- Function B maps up to 40K bytes of external memory into the address space by using $\overline{\text{EDS}}$ under software control.
- Microprocessor without internal program memory mode:
 - Ports A, B, C, and D (these ports are not programmable) become the address, data, and control buses for interface to external memory and peripherals.
 - On-chip RAM and data EEPROM remain active, while the on-chip ROM or EPROM is disabled.
 - Program area and the reset, interrupt, and trap vectors are located in off-chip memory locations.
- Microprocessor with internal program memory mode:
 - Configured as the microprocessor without internal program memory mode with respect to the external bus interface.
 - Application program in external memory enables the internal program ROM or EPROM to be active in the system. (Writing a zero to the MEMORY DISABLED control bit (SCCR1.2) of the SCCR1 control register accomplishes this.)

memory/peripheral wait operation

The TMS370Cx5x enhances interface flexibility by providing $\overline{\text{WAIT}}$ -state support, decoupling the cycle time of the CPU from the read/write access of the external memory or peripherals. External devices can extend the read/write accesses indefinitely by placing an active low on the $\overline{\text{WAIT}}$ -input pin. The CPU continues to wait as long as $\overline{\text{WAIT}}$ remains active.

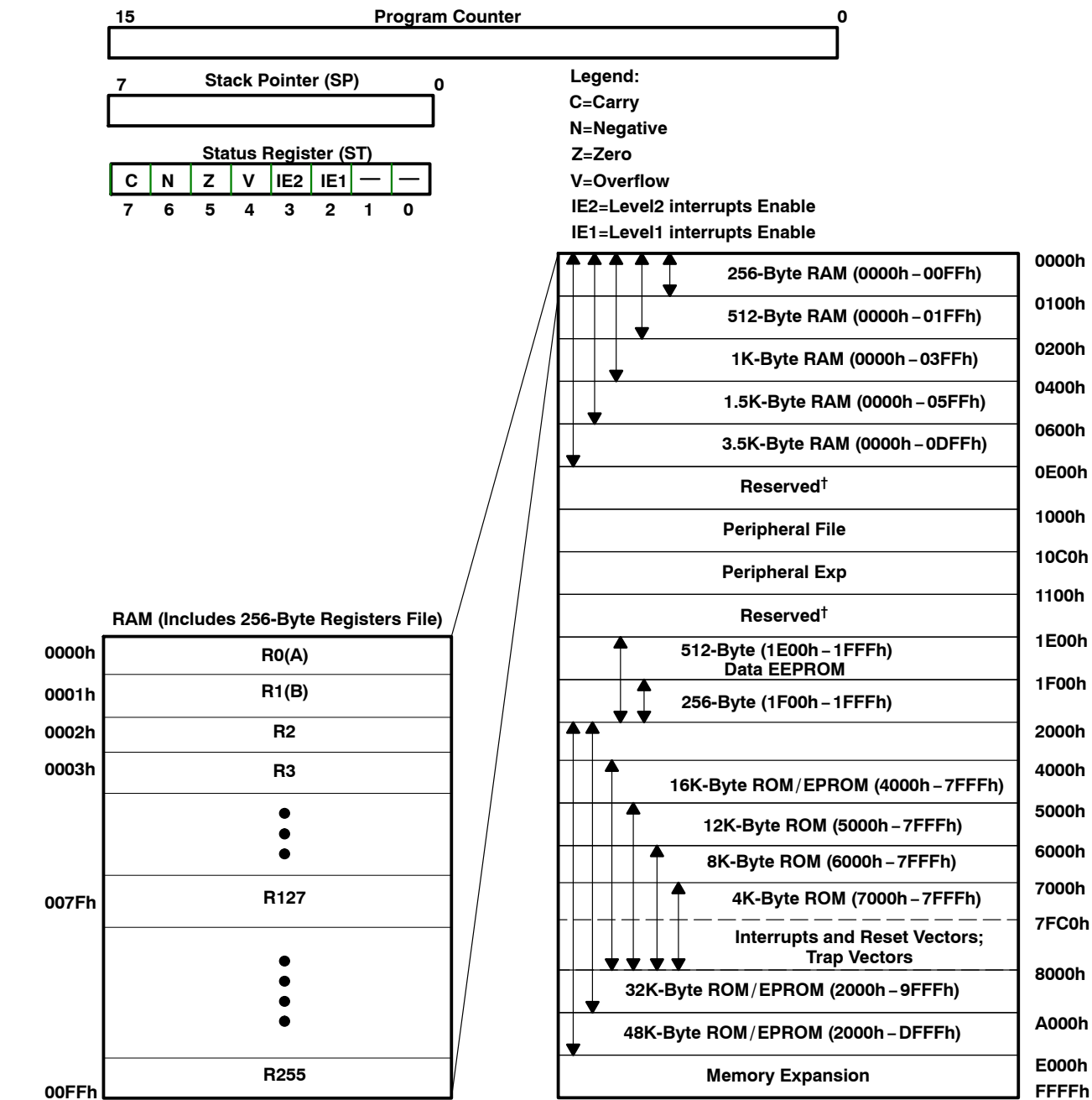
Programmable automatic wait-state generation also is provided by the TMS370Cx5x on-chip bus controller. Following a hardware reset, the TMS370Cx5x is configured to add one wait state to all external bus transactions and memory and peripheral accesses automatically, thus making every external access a minimum of three system-clock cycles. The designer can disable the automatic wait-state generation if the AUTOWAIT DISABLE bit in SCCR1 is set to 1. Also, all accesses to the upper four frames of the peripheral file can be extended independently to four system clock cycles if the PF AUTO WAIT bit in SCCR0 is set to one. Programmable wait states can be used in conjunction with the external $\overline{\text{WAIT}}$ pin. In applications where the external device read/write access can interface with the TMS370Cx5x CPU using one wait state, the automatic wait-state generation can eliminate external $\overline{\text{WAIT}}$ interface logic, lowering system cost.

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CPU

The CPU used on TMS370Cx5x devices is the high-performance 8-bit TMS370 CPU module. The 'x5x implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'x5x instruction set is summarized in Table 23. Figure 1 illustrates the CPU registers and memory blocks.



† Reserved means the address space is reserved for future expansion.

Figure 1. Programmer's Model



CPU (continued)

The 'x5x CPU architecture provides the following components:

- CPU registers:
 - A stack pointer that points to the last entry in the memory stack
 - A status register that monitors the operation of the instructions and contains the global-interrupt-enable bits
 - A program counter (PC) that points to the memory location of the next instruction to be executed
- A memory map that includes :
 - 256-, 512-, 1K-, 1.5K-, or 3.5K-byte general-purpose RAM that can be used for data-memory storage, program instructions, general-purpose register, or the stack (can be located only in the first 256 bytes)
 - A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM/EPROM programming control
 - 256- or 512-byte EEPROM module that provides in-circuit programmability and data retention in power-off conditions
 - 4K-, 8K-, 12K-, 16K-, 32K-, or 48K-byte ROM or 16K-, 32K-, or 48K-byte EPROM program memory

stack pointer (SP)

The SP is an 8-bit CPU register. The stack operates as a last-in, first-out, read/write memory. Typically the stack is used to store the return address on subroutine calls as well as the status-register contents during interrupt sequences.

The SP points to the last entry or to the top of the stack. The SP increments automatically before data is pushed onto the stack and decrements after data is popped from the stack. The stack can be located only in the first 256 bytes of the on-chip RAM memory.

status register (ST)

The ST monitors the operation of the instructions and contains the global-interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits:

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional-jump instructions) use these status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

The ST register, status bit notation, and status bit definitions are shown in Table 4.

Table 4. Status Registers

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

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CPU (continued)

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most-significant byte (MSbyte) and least-significant byte (LSbyte) of a 16-bit address.

The contents of the reset vector (7FFEh, 7FFFh) are loaded into the program counter during reset. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 6000h as the contents of memory locations 7FFEh and 7FFFh (reset vector).

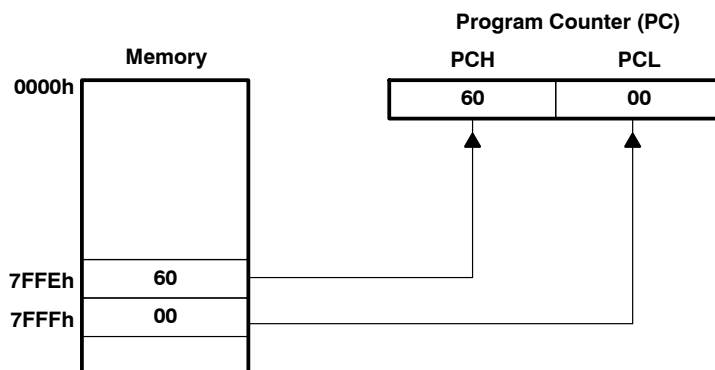


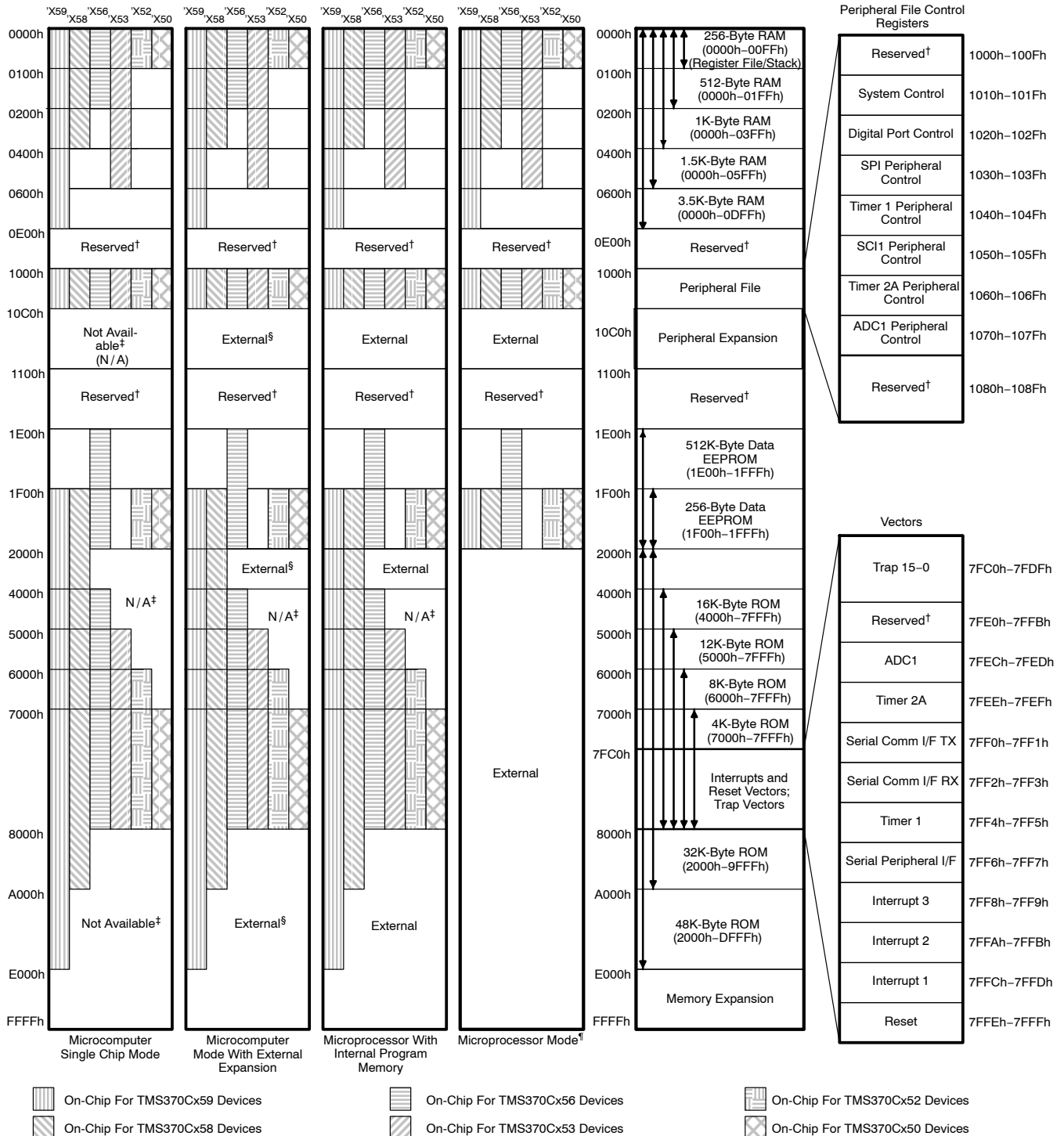
Figure 2. Program Counter After Reset

memory map

The TMS370Cx5x architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. In the expansion mode, external memory peripherals are also memory-mapped into this common address space. As shown in Figure 3, the TMS370Cx5x provides a 16 bit-address range to access internal or external RAM, ROM, data EEPROM, EPROM input/output pins, peripheral functions, and system-interrupt vectors.

The peripheral file contains all input/output port control, on- and off-chip peripheral status and control, EPROM, EEPROM programming, and system-wide control functions. The peripheral file consists of 256 contiguous addresses located from 1000h to 10FFh. The 256 contiguous addresses are divided logically into 16 peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed. The TMS370Cx5x has its on-chip peripherals and system control assigned to peripheral file frames 1 through 7, addresses 1010h through 107Fh.

memory map (continued)



† Reserved = the address space is reserved for future expansion.

‡ Not available (N/A) = address space unavailable in the mode illustrated.

§ Precoded chip select outputs available on external expansion bus.

¶ Microprocessor mode is designed for ROM-less devices ('x50 and 'x56). ROM and EPROM devices can also be used in this mode but all on-chip memory is ignored.

Figure 3. TMS370Cx5x Memory Map

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RAM/register file (RF)

Locations within RAM address space can serve as either register file or general-purpose read/write memory, program memory, or stack instructions. The TMS370Cx50 and TMS370Cx52 devices contain 256 bytes of internal RAM, mapped beginning at location 0000h and continuing through location 00FFh which is shown in Table 5 along with other 'x5x devices.

Table 5. RAM Memory Map

	'x50 and 'x52	'x56	'x58	'x53	'x59
RAM Size	256 Bytes	512 Bytes	1K Bytes	1.5K Bytes	3.5K Bytes
Memory Mapped	0000h – 00FFh	0000h – 01FFh	0000h – 03FFh	0000h – 05FFh	0000h – 0DFFh

The first 256 bytes of RAM (0000h – 00FFh) are register files, R0 through R255 (see Figure 1). The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370Cx5x control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or by P for a decimal designator. For example, the system control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 6 shows the TMS370Cx5x peripheral files.

Table 6. TMS370Cx5x Peripheral File Address map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h–100Fh	P000–P00F	Reserved for factory test
1010h–101Fh	P010–P01F	System and EEPROM/EPROM control registers
1020h–102Fh	P020–P02F	Digital I/O port control registers
1030h–103Fh	P030–P03F	Serial peripheral interface registers
1040h–104Fh	P040–P04F	Timer 1 registers
1050h–105Fh	P050–P05F	Serial communication interface 1 registers
1060h–106Fh	P060–P06F	Timer 2A registers
1070h–107Fh	P070–P07F	Analog-to-digital converter 1 registers
1080h–10BFh	P080–P0BF	Reserved
10C0h–10FFh	P0C0–P0FF	External peripheral control

data EEPROM

The TMS370Cx56 devices contain 512 bytes of data EEPROM, which are memory mapped beginning at location 1E00h and continuing through location 1FFFh as shown in Table 7 along with other 'x5x devices.

Table 7. Data-EEPROM Memory Map

	'x50, 'x52, 'x58, and 'x59	'x56	'X53
Data-EEPROM Size	256 Bytes	512 Bytes	None
Memory Mapped	1F00h–1FFFh	1E00h–1FFFh	None



data EEPROM (continued)

Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B). The data EEPROM features include the following:

- Programming:
 - Bit, byte, and block write/erase modes
 - Internal charge pump circuitry. No external EEPROM programming voltage supply is needed.
 - Control register: Data EEPROM programming is controlled by the data EEPROM control register (DEECTL) located in the PF frame beginning at location P01A.
 - In-circuit programming capability: There is no need to remove the device to program it.
- Write-protection: Writes to the data EEPROM are disabled during the following conditions:
 - Reset: All programming of the data EEPROM module is halted.
 - Write protection active: There is one write-protect bit per 32-byte EEPROM block.
 - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 8 shows the memory map of the control registers.

Table 8. Data EEPROM and Program EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME
P014	EPCTLH	Program EPROM control register – high array
P015 – P016		Reserved
P017	INT1	External interrupt 1 control register
P018	INT2	External interrupt 2 control register
P019	INT3	External interrupt 3 control register
P01A	DEECTL	Data EEPROM control register
P01B		Reserved
P01C	EPCTLM	Program EPROM control register – middle array
P01D		Reserved
P01E	EPCTLL	Program EPROM control register – low array

For the 16K-byte EPROM device, program memory is controlled by P01C; for the 32K-byte EPROM device, the program memory is controlled by P01C and P01E; for the 48K-byte EPROM device, the program memory is controlled by P014, P01C, and P01E.

program EPROM

The '370C756 consists of a 16K-byte array of EPROM at address locations 4000h through 7FFFh. The '370C758 consists of 32K bytes made up of two 16K-byte arrays of EPROM; the first 16K-bytes array is located at address locations 2000h through 5FFFh, and the second 16K byte array is located at address locations 6000h through 9FFFh. The '370C759 consists of 48K bytes that is made up of three 16K byte arrays of EPROM; the first 16K bytes array is located at address locations 2000h through 5FFFh, the second 16K-byte array is located at address locations 6000h through 9FFFh, the third 16K-byte array is located at address locations A000h through DFFFh (see Figure 3).

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program EPROM (continued)

The EPROM memory map in Table 9 expresses the following:

- The programming control register for program EPROM (EPCTLM) for 16K-byte EPROM is located at address 101Ch (P01C).
- For the 32K-byte EPROM, the first 16K-byte array is controlled by EPCTLL, located at 101Eh (P01E); the second 16K-byte array is controlled by EPCTLM, located at 101Ch (P01C).
- For the 48K-byte EPROM, the first 16K-byte array is controlled by EPCTLL, located at 101Eh (P01E); the second 16K-byte array is controlled by EPCTLM, located at 101Ch (P01C); the third 16K-byte array is controlled by EPCTLH, located at 1014h (P014).

Table 9. EPROM Memory Map

	'756	'758		'759		
EPROM size	16K Bytes	32K Bytes		48K Bytes		
Memory Mapped	16K 4000h–7FFFh	First 16K 2000h–5FFFh	Second 16K 6000h–9FFFh	First 16K 2000h–5FFFh	Second 16K 6000h–9FFFh	Third 16K A000h–DFFFh
Control Registers	EPCTLM P01C	EPCTLL P01E	EPCTLM P01C	EPCTLL P01E	EPCTLM P01C	EPCTLH P014

Reading the program-EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the EPCTL. The program EPROM modules' features include:

- Programming
 - In-circuit programming capability if V_{PP} is applied to MC
 - Control register: Program EPROM programming is controlled by the program EPROM control registers (EPCTLL, EPCTLM, and EPCTLH) located in the PF frame as shown in Table 8.
 - Programming one EPROM module while executing the other
- Write protection: Writes to the program EPROM are disabled under the following conditions:
 - Reset: All programming to the EPROM module is halted.
 - Low-power modes
 - 13 V not applied to MC

program ROM

The program ROM consists of 4K to 48K bytes of mask-programmable ROM. The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication. ROM security is a feature of the '45x devices, which inhibits reading of the data using the programmer.

Table 10. ROM Memory Map[†]

	'x50	'x52	'x53	'x56	'x58	'x59
ROM Size	4K Bytes	8K Bytes	12K Bytes	16K Bytes	32K Bytes	48K Bytes
Memory Mapped	7000h – 7FFFh	6000h – 7FFFh	5000h – 7FFFh	4000h – 7FFFh	3000h – 9FFFh	2000h – DFFFh

[†] Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments (TI™), and addresses 7FECb through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions are located between addresses 7FC0h and 7FDFh.

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system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx5x CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are internally generated, while one (**RESET**) is controlled externally. These actions are as follows:

- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside the recommended operating range. See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B) for more information.
- External **RESET** Pin. A low-level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B) for more information.

Once a reset source is activated, the external **RESET** pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x5x device to reset external system components. Additionally, if a cold-start condition (V_{CC} is off for several hundred milliseconds) occurs, oscillator failure occurs, or **RESET** pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator fault flag (OSC FLT FLAG, SCCR0.4), the cold start flag (COLD START, SCCR0.7), and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 11 lists the reset sources.

Table 11. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers initialize: ST = 00h, SP = 01h (reset state).
2. Registers A and B initialize to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to by the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state. During **RESET**, the two basic operating modes which are the microcomputer and microprocessor modes can be selected by applying the desired voltage level to the dedicated MC pin two cycles before **RESET** goes inactive (refer to page 10-10 for operating modes description).

RESET must be held low until the clock signal is valid and V_{CC} is within the operating range, when an external reset circuit is connected to **RESET**. Figure 4 shows a typical reset circuit.

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system reset (continued)

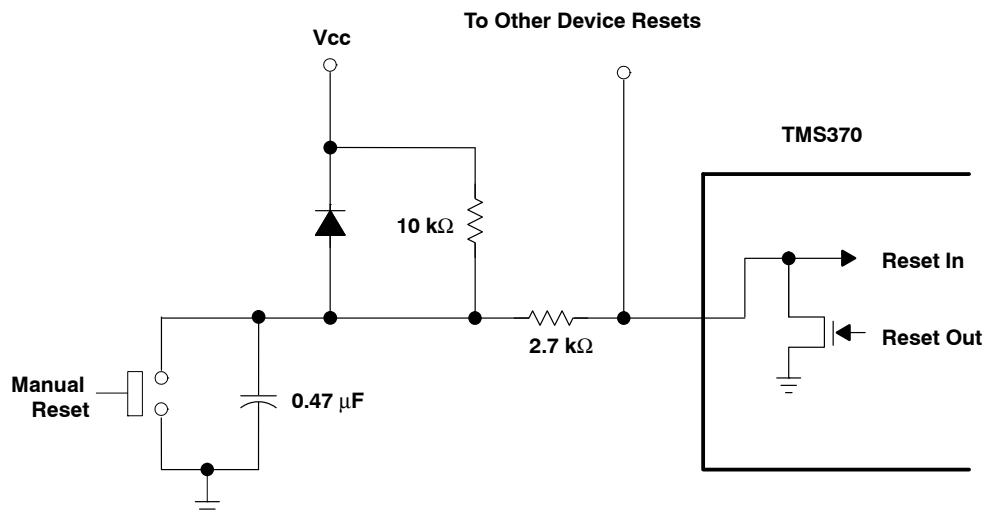


Figure 4. Typical Reset Circuit

interrupts

The TMS370 family software-programmable interrupt structure permits flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global interrupt mask bits (IE1 and IE2) of the status register.

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is configured selectively on either the high- or low-priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx5x has nine hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 12. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. A system interrupt can have multiple interrupt sources (e.g., SCI RXINT has two interrupt sources). All of the interrupt sources are individually maskable by local interrupt-enable control bits in the associated PF. Each interrupt source FLAG bit is individually readable for software polling or determining which interrupt source generated the associated system interrupt. Interrupt control block diagram is illustrated in Figure 5.

interrupts (continued)

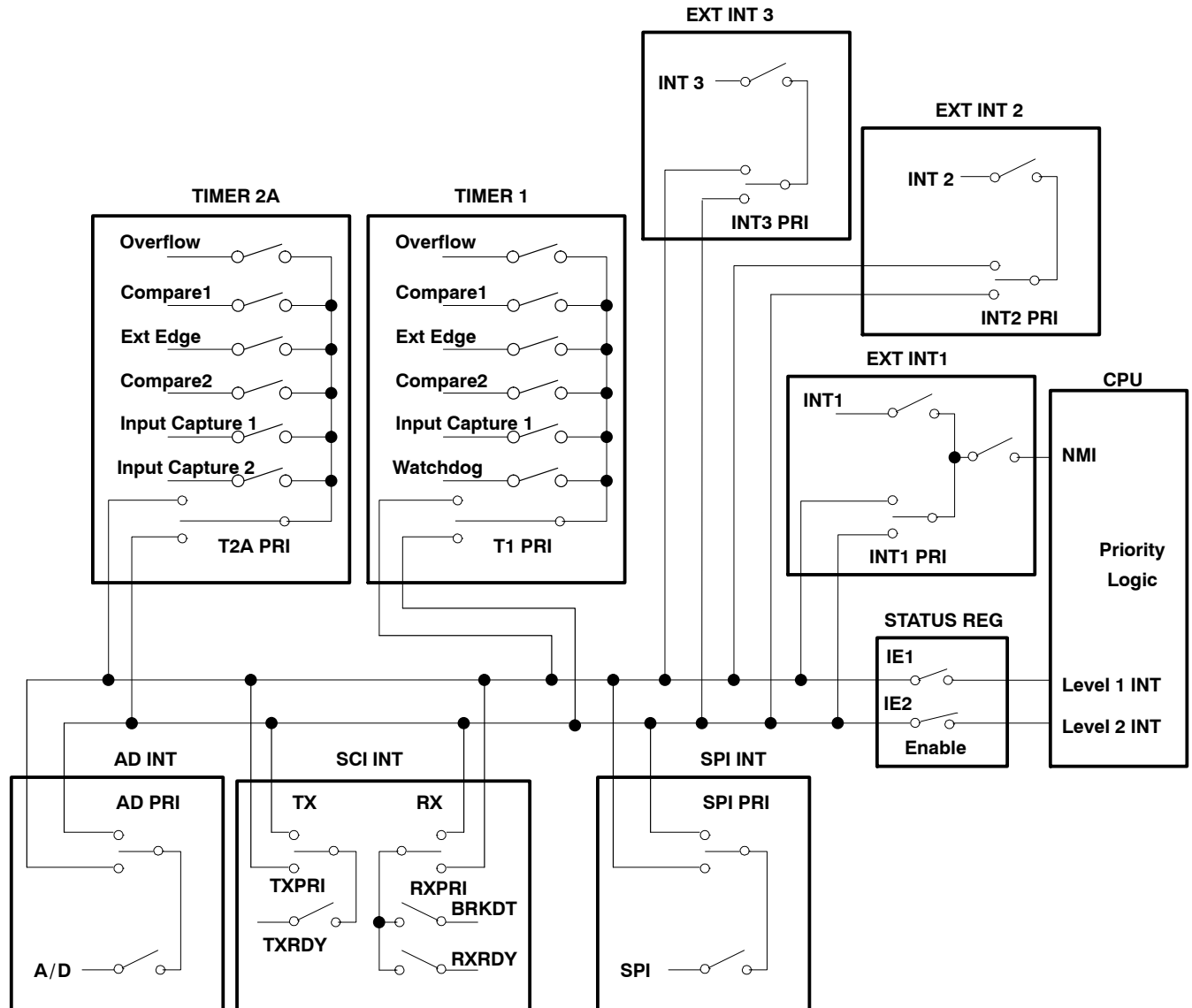


Figure 5. Interrupt Control

On-chip peripheral functions generate six of the system interrupts. Three external interrupts also are supported. Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in PF frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as nonmaskable, it cannot be masked by the individual- or global-enable mask bits. The INT1 NMI bit is protected during non-privileged operation and, therefore, should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software configured as general purpose input/output pins if the interrupt function is not required (INT1 can be similarly configured as an input pin). Table 12 shows the interrupt vector sources, corresponding addresses, and hardware priorities.

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interrupts (continued)

Table 12. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY [†]
External RESET Watchdog overflow Oscillator fault detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	RESET [‡]	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1 [‡]	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2 [‡]	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3 [‡]	7FF8h, 7FF9h	4
SPI RX/TX complete	SPI INT FLAG	SPIINT	7FF6h, 7FF7h	5
Timer 1 overflow Timer 1 compare 1 Timer 1 compare 2 Timer 1 external edge Timer 1 input capture 1 Watchdog overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT [§]	7FF4h, 7FF5h	6
SCI RX data register full SCI RX break detect	RXRDY FLAG BRKDT FLAG	RXINT [‡]	7FF2h, 7FF3h	7
SCI TX data register empty	TXRDY FLAG	TXINT	7FF0h, 7FF1h	8
Timer 2A overflow Timer 2A compare 1 Timer 2A compare 2 Timer 2A external edge Timer 2A input capture 1 Timer 2A input capture 2	T2A OVRFL INT FLAG T2AC1 INT FLAG T2AC2 INT FLAG T2AEDGE INT FLAG T2AIC1 INT FLAG T2AIC2 INT FLAG	T2AINT	7FEEh, 7FEFh	9
A/D conversion complete	AD INT FLAG	ADINT	7FECh, 7FEDh	10

[†] Relative priority within an interrupt level

[‡] Releases microcontroller from STANDBY and HALT low-power modes.

[§] Releases microcontroller from STANDBY low-power mode.

privileged operation and EEPROM write-protection override

The TMS370Cx5x family has significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a broad variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx5x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) should be set to 1 to enter the nonprivileged mode; disabling write operations to specific configuration control bits within the peripheral file. Table 13 displays the system configuration bits that are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

privileged operation and EEPROM write-protection override (continued)

Table 13. Privileged Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCRO	P010.5 P010.6	PF AUTOWAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
SPIPRI	P03F.5 P03F.6 P03F.7	SPI ESPEN SPI PRIORITY SPI STEST
SCIPRI	P05F.4 P05F.5 P05F.6 P05F.7	SCI ESPEN SCIRX PRIORITY SCITX PRIORITY SCI STEST
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST
T2APRI	P06F.6 P06F.7	T2A PRIORITY T2A STEST
ADPRI	P07F.5 P07F.6 P07F.7	AD ESPEN AD PRIORITY AD STEST

† The privileged bits are shown in a bold typeface in Table 15.

The write-protect override (WPO) mode provides an external hardware method for overriding the write-protection registers of data EEPROM on the TMS370Cx5x. The WPO mode is entered by applying a 12-V input to MC after **RESET** input goes high (logic 1). The high voltage on MC during the WPO mode is not the programming voltage for the data EEPROM or Program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware system-level capability to modify the content of the data EEPROM while the device remains in the application, but only while requiring a 12-V external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power and IDLE modes

The TMS370Cx5x devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time when the mask is manufactured.

The STANDBY and HALT low power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls which low-power mode is entered.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, timer 1, and the receive start-bit detection circuit of the serial communications interface remain active. System processing is suspended until a qualified interrupt (hardware **RESET**, external interrupt on INT1, INT2, INT3, timer 1 interrupt, or low level on the receive pin of the serial communications interface 1) is detected.

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low-power and IDLE modes (continued)

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx5x is placed in its lowest power consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware RESET, external interrupt on the INT1, INT2, INT3, or low level on the receive pin of the serial communications interface 1) is detected. The low-power mode selection bits are summarized in Table 14.

Table 14. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X	IDLE

X = don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6–7 bits is ignored. In addition, if an idle instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method of always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI is generated always, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the watchdog timer is inhibited.

clock modules

The 'x5x family provides two clock options which are referred to as divide-by-1 (PLL) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The 'x5x ROM-masked devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device. The '75xA EPROM has only the standard divide-by-4, while the '75xB EPROM has the divide-by-1.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a 1-to-1 match of the external resonator frequency to the internal system clock (SYSCLK) frequency. The divide-by-4 produces a SYSCLK which is one-fourth the frequency of the external resonator. Inside the divide-by-1 module, the frequency of the external resonator is multiplied by four. The clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. The frequencies are formulated as follows

$$\text{Divide-by-4 option : SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option : SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the improved EMI performance. The harmonics of low-speed resonators extend through less of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 provides the capability of reducing the resonator speed by four times, and this results in a steeper decay of emissions produced by the oscillator.



system configuration registers

Table 15 contains system configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in a bold typeface and shaded.

Table 15. Peripheral File Frame 1: System Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTOWAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013	Reserved								
P014	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLH
P015 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLM
P01D	Reserved								
P01E	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLL
P01F	Reserved								



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digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 16 lists the specific addresses, registers, and control bits within this peripheral file frame.

Table 16. Peripheral File Frame 2: Digital Port Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P020	Reserved								APOINT1
P021	Port A Control Register 2								APOINT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPOINT1
P025	Port B Control Register 2								BPOINT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPOINT1
P029	Port C Control Register 2								CPOINT2
P02A	Port C Data								CDATA
P02B	Port C Direction								CDIR
P02C	Port D Control Register 1								DPOINT1
P02D	Port D Control Register 2 [†]								DPOINT2
P02E	Port D Data								DDATA
P02F	Port D Direction								DDIR

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.



digital port control registers (continued)

Table 17. Port Configuration Register Setup

PORT	PIN	INPUT	OUTPUT	FUNCTION A	FUNCTION B (μP MODE)
		XPORT1 = 0 [†] XPORT2 = 0 XDATA = y XDIR = 0	XPORT1 = 0 [†] XPORT2 = 0 XDATA = q XDIR = 1	XPORT1 = 0 [†] XPORT2 = 1 XDATA = x XDIR = x	XPORT1 = 1 [†] XPORT2 = 1 XDATA = x XDIR = x
A	0–7	Data In y	Data Out q	Data Bus	Reserved
B	0–7	Data In y	Data Out q	Low ADDR	Reserved
C	0–7	Data In y	Data Out q	Hi ADDR	Reserved
D	0	Data In y	Data Out q	$\overline{\text{CSE2}}$	$\overline{\text{OCF}}$
	1			$\overline{\text{CSH3}}$	—
	2			$\overline{\text{CSH2}}$	—
	3			SYSCLK	SYSCLK
	4			R/ $\overline{\text{W}}$	R/ $\overline{\text{W}}$
	5			$\overline{\text{CSPF}}$	—
	6			$\overline{\text{CSH1}}$	$\overline{\text{EDS}}$
	7			$\overline{\text{CSE1}}$	WAIT
XPORT1 = 1 XPORT2 = 0 XDATA = x XDIR = x Not defined					

[†] DPORT only

timer 1 module

The programmable timer 1 (T1) module of the TMS370Cx5x provides the designer with the enhanced timer resources required to perform realtime system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers (T1 and WD) allow program selection of input clock sources (real-time, external event, or pulse-accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The T1 module includes three external device pins that can be used for multiple counter functions (operation mode dependent) or used as general-purpose I/O pins. T1 module is shown in Figure 6.

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timer 1 module (continued)

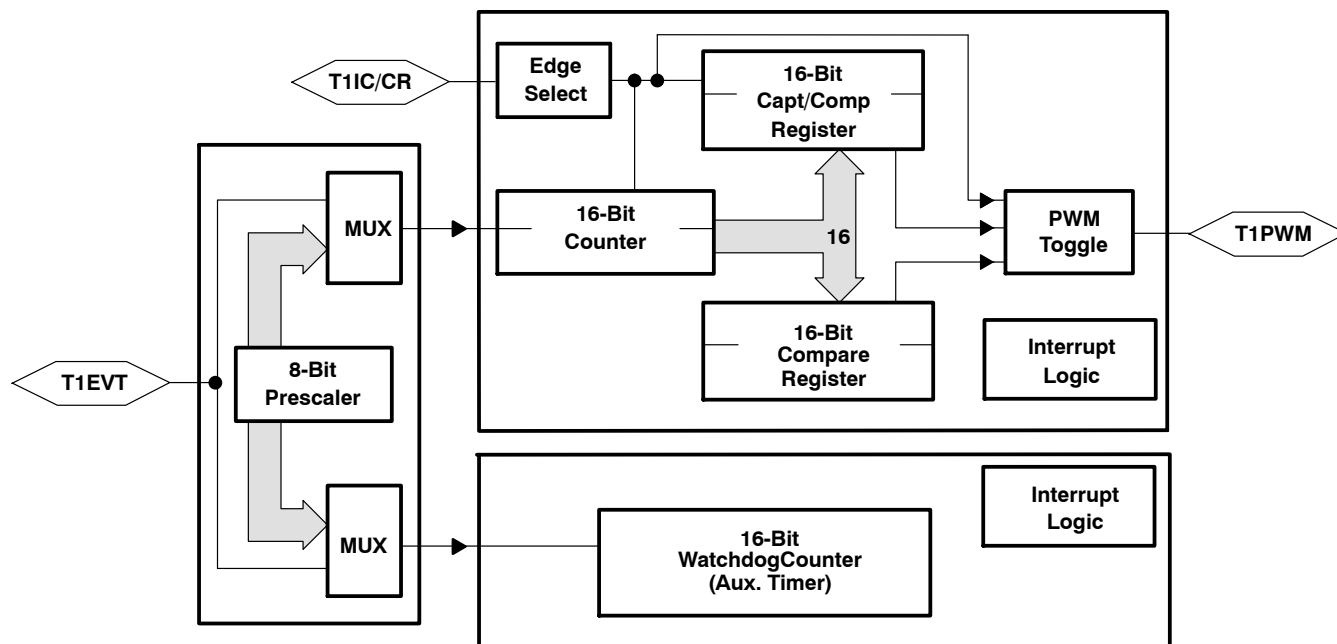


Figure 6. Timer 1 Block Diagram

- Three T1 I/O pins:
 - T1IC/CR: T1 input capture / counter reset input pin, or general-purpose bidirectional I/O pin
 - T1PWM: T1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T1EVT: T1 event input pin, or general-purpose bidirectional I/O pin
- Two operation modes:
 - Dual-compare mode: Provides PWM signal
 - Capture/compare mode: Provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register
- One 16-bit WD counter can be used as an event counter, a pulse accumulator, or an interval timer if watchdog feature is not needed.
- Prescaler/clock sources that determine one of eight clock sources for general-purpose timer
- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR)

timer 1 module (continued)

- Interrupts that can be generated on the occurrence of:
 - A capture
 - A compare equal
 - A counter overflow
 - An external edge detection
- Sixteen T1 module control registers located in the PF frame, beginning at address P040

Table 18 shows the T1 module control register.

Table 18. T1 Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Dual-Compare and Capture/Compare									
P040	Bit 15			T1 Counter MSbyte				Bit 8	T1CNTR
P041	Bit 7			T1 Counter LSbyte				Bit 0	
P042	Bit 15			Compare Register MSbyte				Bit 8	T1C
P043	Bit 7			Compare Register LSbyte				Bit 0	
P044	Bit 15			Capture/Compare Register MSbyte				Bit 8	T1CC
P045	Bit 7			Capture/Compare Register LSbyte				Bit 0	
P046	Bit 15			Watchdog Counter MSbyte				Bit 8	WDCNTR
P047	Bit 7			Watchdog Counter LSbyte				Bit 0	
P048	Bit 15			Watchdog Reset Key				Bit 0	WDRST
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to the simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

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timer 1 module (continued)

The T1 capture/compare mode block diagram is illustrated in Figure 7. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

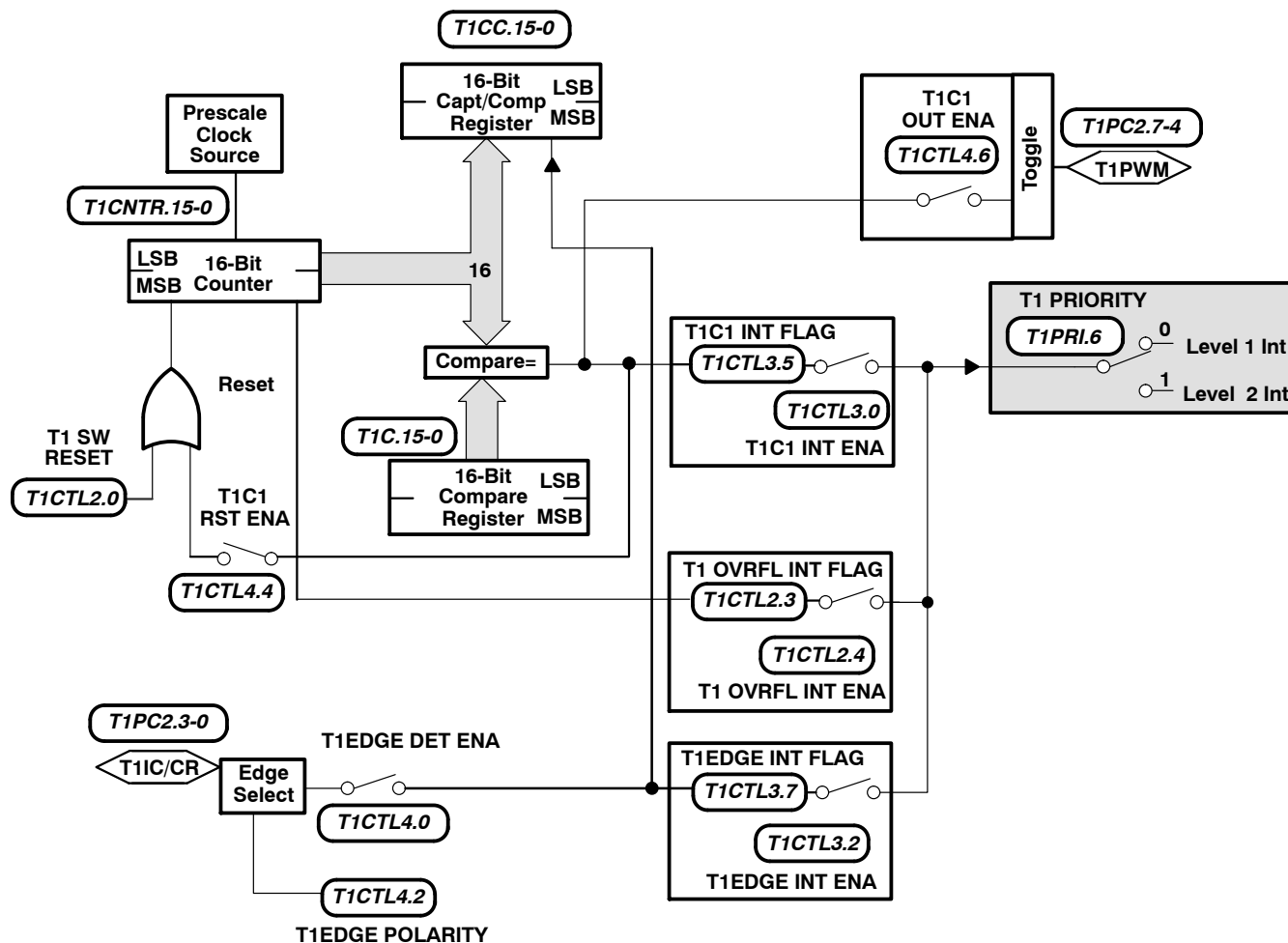


Figure 7. Capture/Compare Mode

timer 1 module (continued)

The T1 dual-compare mode block diagram is illustrated in Figure 8. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

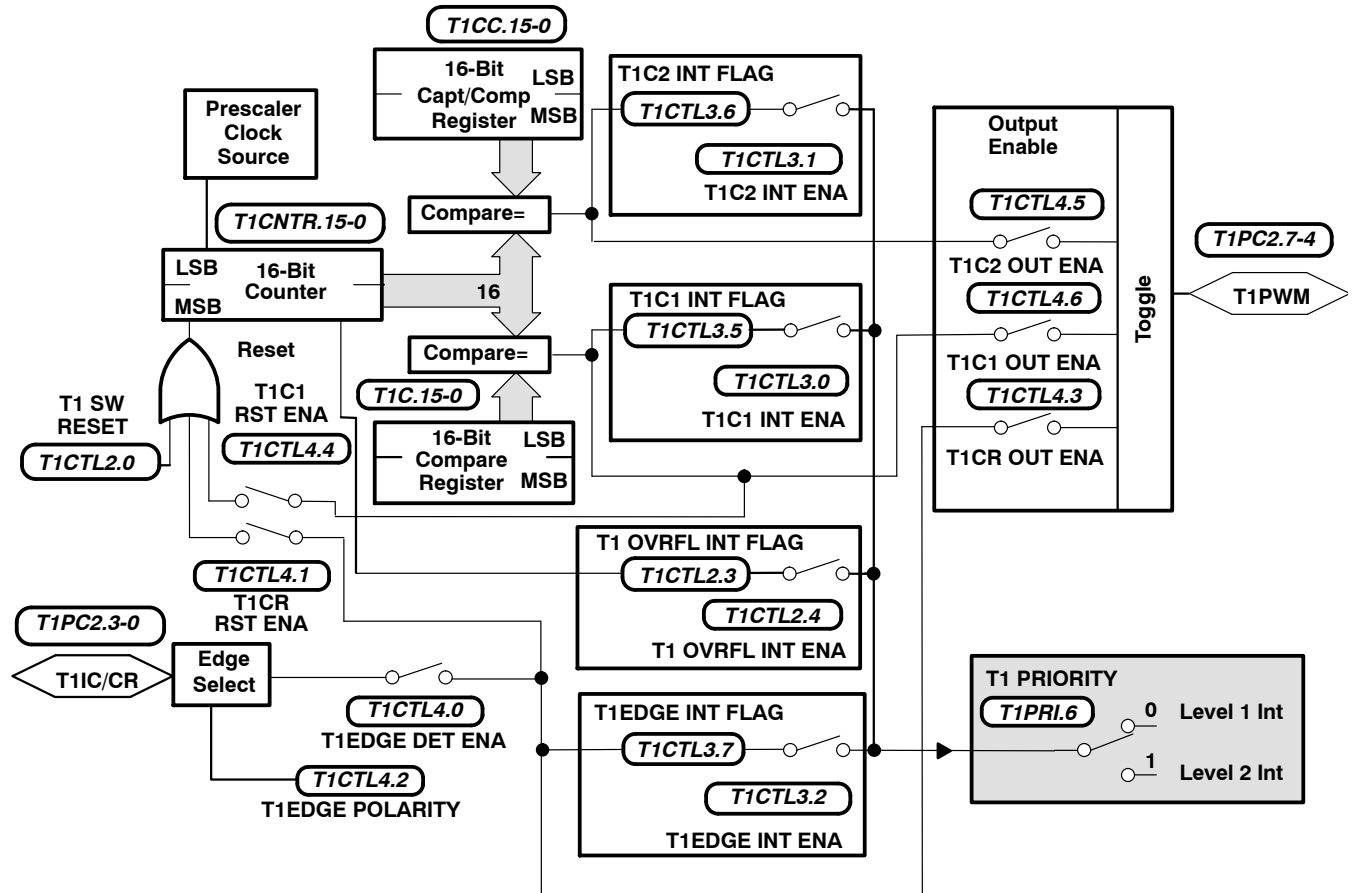


Figure 8. Dual-Compare Mode

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timer 1 module (continued)

The TMS370Cx5x device includes a 24-bit watchdog (WD) timer, contained in the T1 module, which can be software-programmed as an event counter, pulse accumulator, or interval timer if the watchdog function is not desired. The WD function is to monitor software and hardware operation and to implement a system reset when the WD counter is not serviced properly (WD counter overflow or WD counter is reinitialized by an incorrect value). The WD can be configured as one of the three mask options: standard watchdog, hard watchdog, or simple counter.

- Standard watchdog configuration (see Figure 9) – for 'C75xA EPROM and mask-ROM devices
 - Watchdog mode
 - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows
 - A watchdog overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
 - Non-watchdog mode
 - Watchdog timer can be configured as an event counter, pulse accumulator, or an interval timer

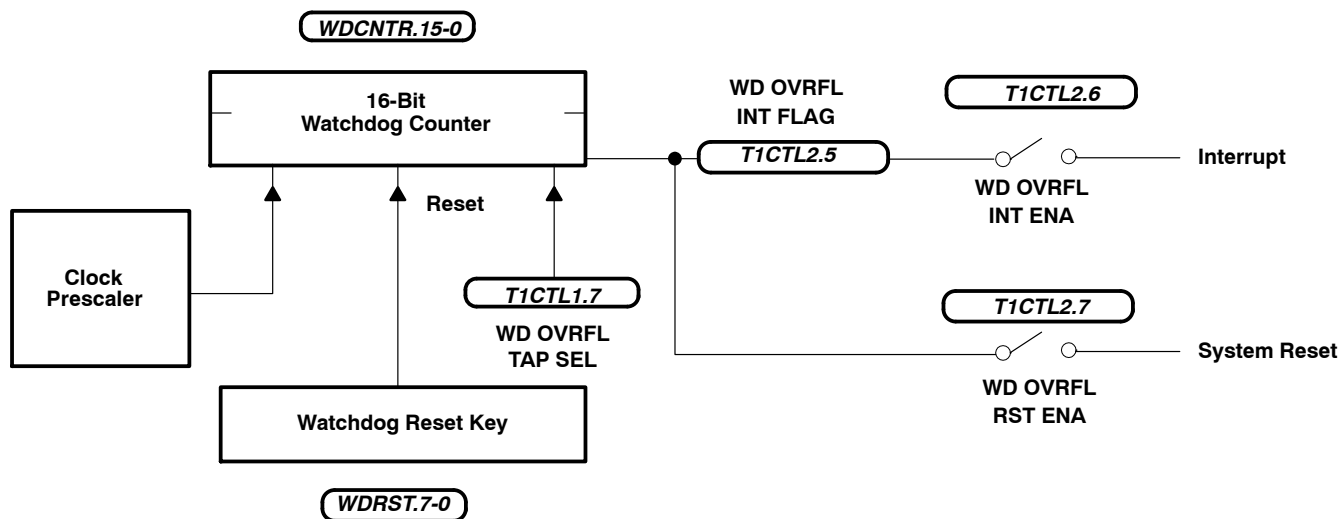


Figure 9. Standard Watchdog

timer 1 module (continued)

- Hard watchdog configuration (see Figure 10) – for 'C75xB EPROM and mask-ROM devices
 - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCLK.
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows
 - Automatic activation of the WD timer upon power-up reset
 - INT1 is enabled as nonmaskable interrupt during low-power modes
 - A watchdog overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset

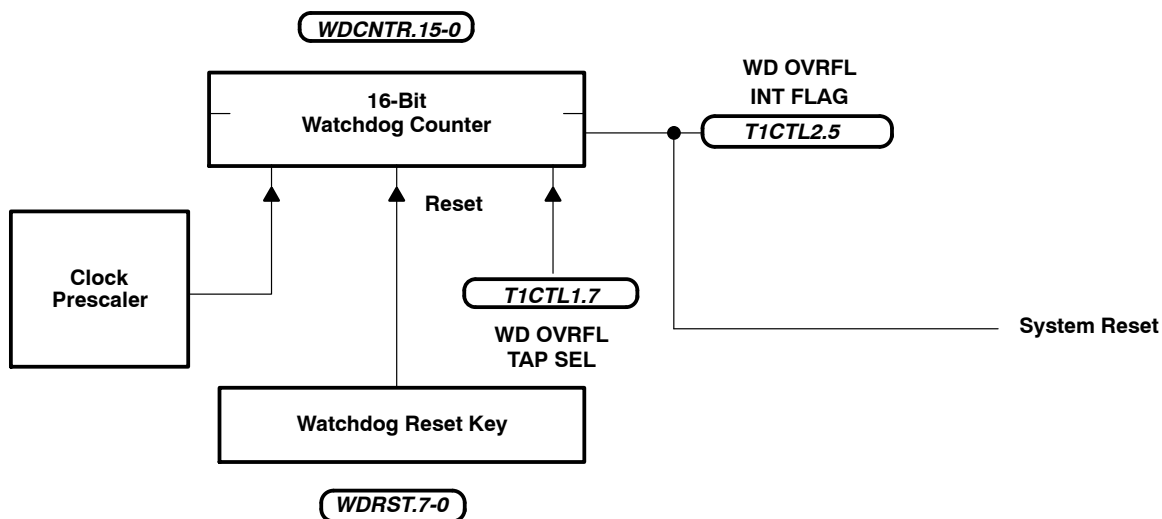


Figure 10. Hard Watchdog

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timer 1 module (continued)

- Simple-counter configuration (see Figure 11) – for mask-ROM devices only
 - The simple counter can be configured as an event counter, pulse accumulator, or an interval timer

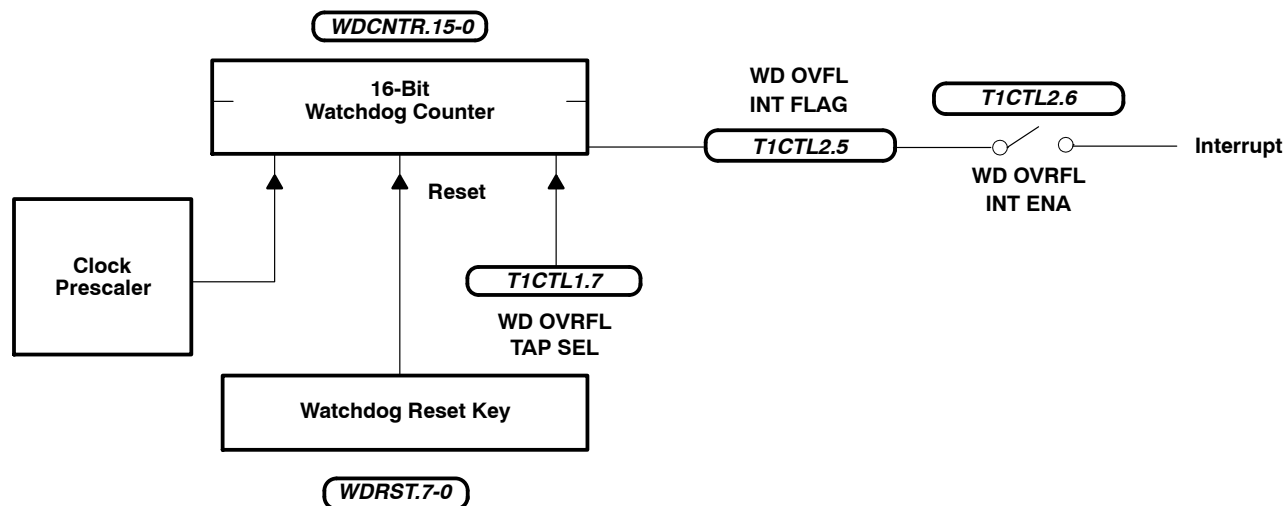


Figure 11. Simple Counter

timer 2A module

The 16-bit general-purpose timer 2A (T2A) module is composed of a 16-bit resettable counter, 16-bit compare register with associated compare logic, 16-bit capture register, and a 16-bit register that functions as a capture register in one mode and as a compare register in the other mode. The T2A module adds an additional timer that provides an event count, input capture, and compare functions. The T2A module includes three external device pins that can be dedicated as timer functions or used as general-purpose I/O pins. The T2A module is shown in Figure 12.

timer 2A module (continued)

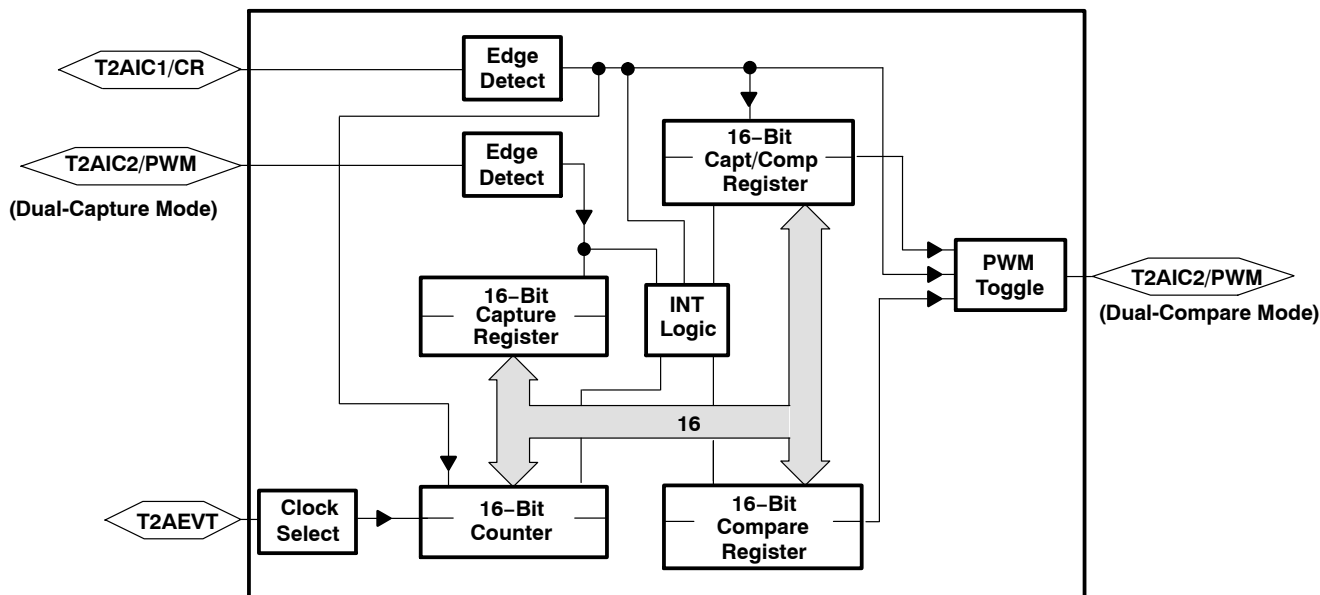


Figure 12. Timer 2A Block Diagram

The T2A module features include the following:

- Three T2A I/O pins:
 - T2AIC1/CR: T2A input-capture 1/counter-reset input pin, or general-purpose bidirectional I/O pin
 - T2AIC2/PWM: T2A input-capture 2/pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T2AEVT: Timer 2A event-input pin, or general-purpose bidirectional I/O pin
- Two operational modes:
 - Dual-compare mode: Provides PWM signal
 - Dual-capture mode: Provides input-capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture register with associated capture logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register
- T2A clock sources can be any of the following:
 - System clock
 - No clock (the counter is stopped)
 - External clock synchronized to the system clock (event counter)
 - System clock while external input is high (pulse accumulation)

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timer 2A module (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T2AIC1/CR)
- Interrupts that can be generated on the occurrence of:
 - A compare equal to dedicated compare register
 - A compare equal to capture-compare register
 - A counter overflow
 - An external edge 1 detection
 - An external edge 2 detection
- Fourteen T2A module-control registers: Located in the PF frame beginning at address P060

The T2A module-control registers are illustrated in Table 19.

Table 19. Timer 2A Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Dual-Compare and Dual-Capture									
P060	T2A Counter MSbyte							Bit 8	T2ACNTR
P061	T2A Counter LSbyte							Bit 0	
P062	Compare Register MSbyte							Bit 8	T2AC
P063	Compare Register LSbyte							Bit 0	
P064	Capture/Compare Register MSbyte							Bit 8	T2ACC
P065	Capture/Compare Register LSbyte							Bit 0	
P066	Capture Register 2 MSbyte							Bit 8	T2AIC
P067	Capture Register 2 LSbyte							Bit 0	
P06A	—	—	—	T2A OVRFL INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1
Mode: Dual-Compare									
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC2 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
Mode: Dual-Capture									
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
Modes: Dual-Compare and Dual-Capture									
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2/PWM DATA IN	T2AIC2/PWM DATA OUT	T2AIC2/PWM FUNCTION	T2AIC2/PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC1/CR DATA DIR	T2APC2
P06F	T2A STEST	T2A PRIORITY	—	—	—	—	—	—	T2APRI

timer 2A module (continued)

The T2A dual-compare mode block diagram is illustrated in Figure 13. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2ACTL2.0 is 106Bh, bit 0, in the T2ACTL2 register.

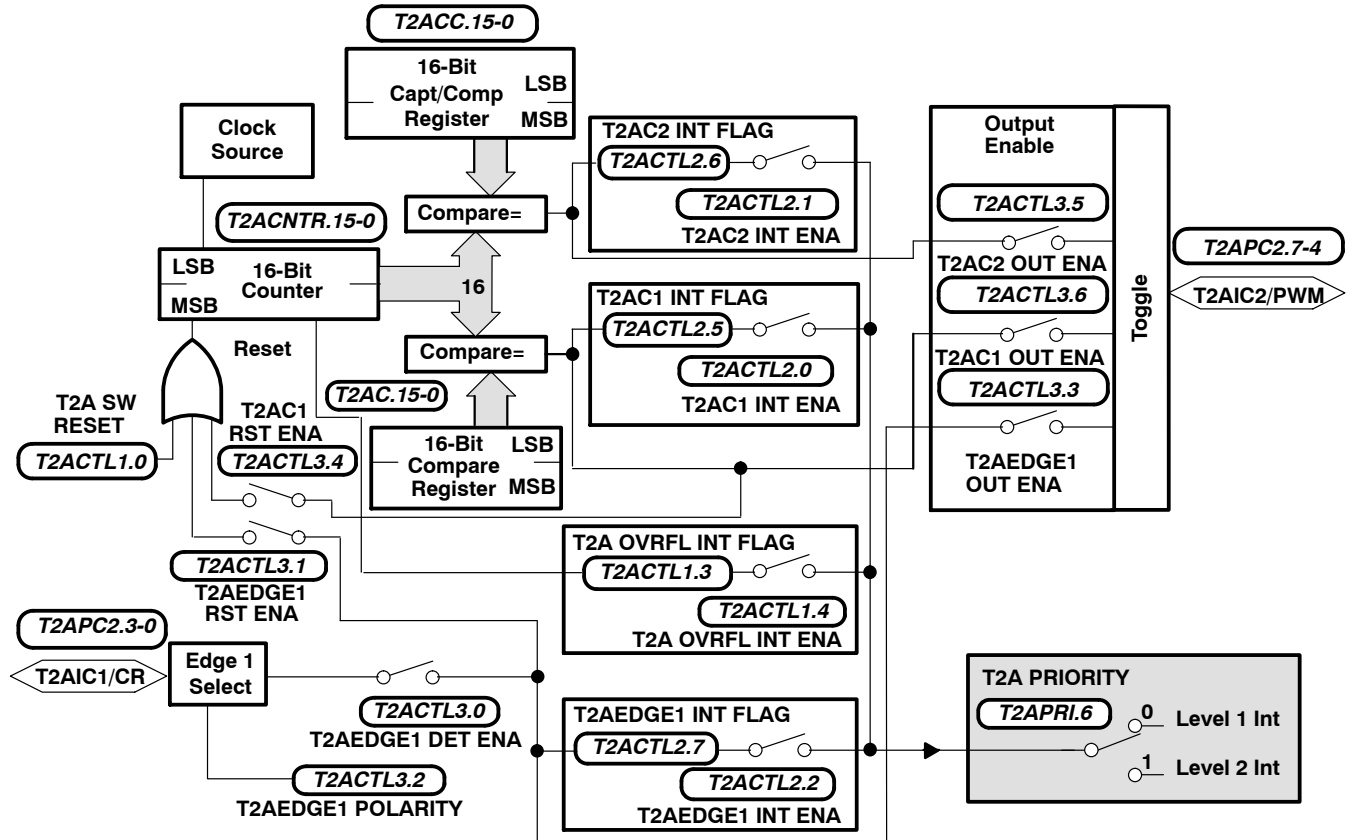


Figure 13. Dual-Compare Mode

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timer 2A module (continued)

The T2A dual-capture mode block diagram is illustrated in Figure 14. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2ACTL2.0 is 106Bh, bit 0, in the T2ACTL2 register.

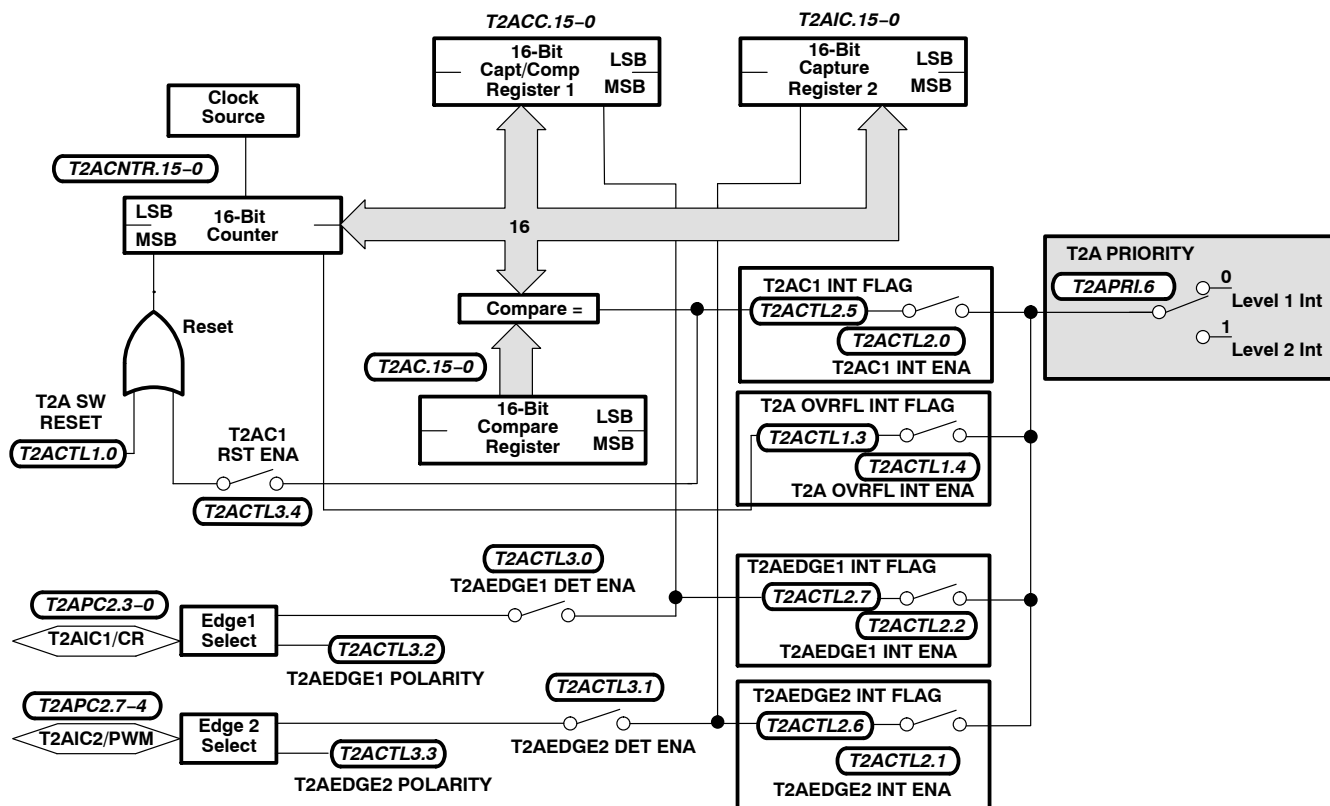


Figure 14. Dual-Capture Mode

serial peripheral interface (SPI) module

The SPI is a high-speed, synchronous, serial I/O port that allows a serial bit stream of programmed length (1 to 8 bits) to be shifted into, and out of, the device at a programmable bit-transfer rate. The SPI is used normally for communications between the microcontroller and external peripherals or another microcontroller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and analog-to-digital converters. The master/slave operation of the SPI supports multi-device communications. The SPI module features include the following:

- Three external pins:
 - SPISOMI: SPI slave output/master input pin or general purpose bidirectional I/O pin
 - SPISIMO: SPI slave input/master output pin or general purpose bidirectional I/O pin
 - SPICLK: SPI serial clock pin or general purpose bidirectional I/O pin
- Two operational modes: master and slave
- Baud rate: Eight different programmable rates
 - Maximum baud rate in master mode: 2.5M bps at 5-MHz SYSCLK

$$\text{SPI BAUD RATE} = \frac{\text{SYSCLK}}{2 \times 2^b}$$

- Maximum baud rate in slave mode: 625K bps at 5-MHz SYSCLK.

For maximum slave SPI BAUD RATE < SYSCLK/8

where b = bit rate in SPICCR.5-3 (range 0–7)

- Data word format: one to eight data bits
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt driven or polled algorithms.
- Seven SPI module control registers located in control register frame beginning at address P030h

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serial peripheral interface (SPI) module (continued)

The SPI module control registers are illustrated in Table 20.

Table 20. SPI Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/SLAVE	TALK	SPI INT ENA	SPICTL
P032 to P036	Reserved								
P037	RCVD7	RCVD6	RCVD5	RCVD4	RCVD3	RCVD2	RCVD1	RCVD0	SPIBUF
P038	Reserved								
P039	SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0	SPIDAT
P03A to P03C	Reserved								
P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
P03F	SPI TEST	SPI PRIORITY	SPI ESPEN	—	—	—	—	—	SPIPRI

The SPI block diagram is illustrated in Figure 15.

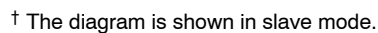


Figure 15. SPI Block Diagram

The TMS370x5x devices include a serial communications interface (SCI1) module. The SCI1 module supports digital communications between the TMS370 devices and other asynchronous peripherals and uses the standard non-return-zero format (NRZ) format. The SCI1's receiver and transmitter are double buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full duplex mode. To ensure data integrity, the SCI1 checks received data for break detection, parity, overrun, and framing errors. The speed of bit rate (baud) is programmable to over 65,000 different speeds through a 16-bit baud-select register.

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serial communications interface 1 (SCI1) module (continued)

Features of the SCI1 module include:

- Three external pins:
 - SCITXD: SCI transmit output pin or general-purpose bidirectional I/O pin
 - SCIRXD: SCI receive input pin or general-purpose bidirectional I/O pin
 - SCICLK: SCI bidirectional serial clock pin, or general-purpose bidirectional I/O pin
- Two communications modes: asynchronous and isosynchronous[†]
- Baud rate: 64K different programmable rates
 - Asynchronous mode: 3 bps to 156K bps at 5-MHz SYSCLK

$$\text{ASYNCHRONOUS BAUD} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 32}$$

- Isosynchronous mode: 39 bps to 2.5M bps at 5-MHz SYSCLK

$$\text{ISOSYNCHRONOUS BAUD} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 2}$$

- Data-word format
 - One start bit
 - Data-word length programmable from 1 to 8 bits
 - Optional even/odd/no parity bit
 - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: Idle-line and address bit
- Half or full-duplex operation
- Double-buffered receive and transmit functions
- Interrupt driven or polled algorithms with status flags accomplish transmitter (TX) and receiver (RX) operations.
 - Transmitter: TXRDY flag (transmitter buffer register is ready to receive another character) and TX EMPTY flag (transmitter shift register is empty)
 - Receiver: RXRDY flag (receive buffer register ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR monitoring four interrupt conditions
 - Separate enable bits for transmitter and receiver interrupts
 - NRZ (non return-to-zero) format
- Eleven SCI1 module control registers are located in control register frame beginning at address P050h.

[†] Isosynchronous = Isochronous

serial communications interface 1 (SCI1) module (continued)

The SCI1 module control registers are illustrated in Table 21.

Table 21. SCI1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNCR/ ISOSYNCR	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	Reserved								
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF
P05A P05B P05C	Reserved								
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	SCI STEST	SCITX PRIORITY	SCIRX PRIORITY	SCI ESPEN	—	—	—	—	SCIPRI

The SCI1 module block diagram is illustrated in Figure 16.

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serial communications interface 1 (SCI1) module (continued)

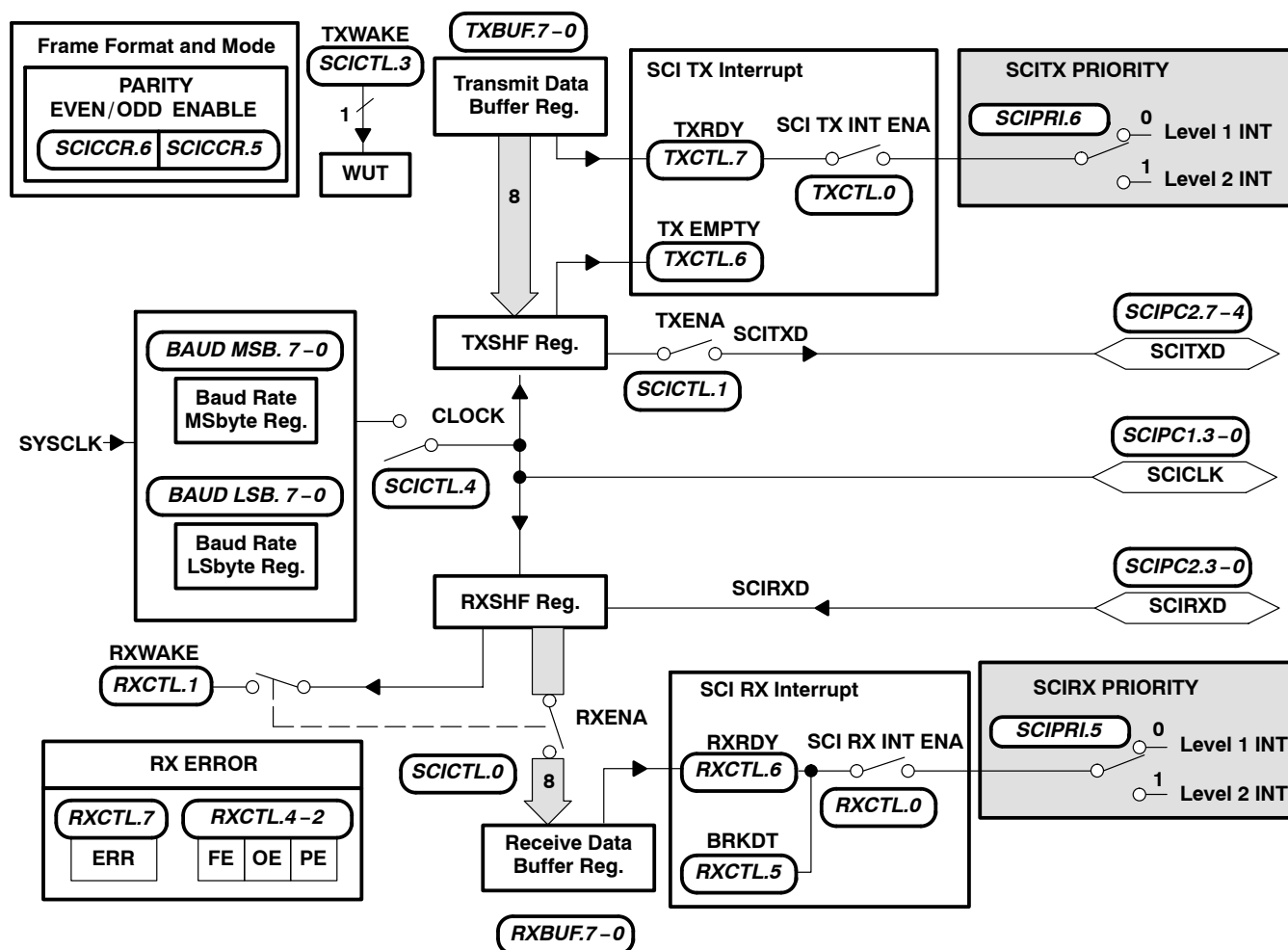


Figure 16. SCI1 Block Diagram

analog-to-digital converter 1 (ADC1) module

The analog-to-digital converter 1 (ADC1) module is an 8-bit, successive approximation converter with internal sample-and-hold circuitry. The module has eight multiplexed analog input channels that allow the processor to convert the voltage levels from up to eight different sources. The ADC1 module features include the following:

- Minimum conversion time: 32.8 μ s at 5-MHz SYSCLK
- Ten external pins:
 - Eight analog input channels (AN0–AN7), any of which can be software configured as digital inputs (E0–E7) if not needed as analog channels
 - AN1–AN7 can also be configured as positive-input voltage reference.
 - V_{CC3}: A/D module high-voltage reference input
 - V_{SS3}: A/D module low-voltage reference input

analog-to-digital converter 1 (ADC1) module (continued)

- The ADDATA register, which contains the digital result of the last ADC1 conversion
- ADC1 operations can be accomplished through either interrupt driven or polled algorithms.
- Six ADC1 module control registers are located in the control-register frame beginning at address 1070h.

The ADC1 module control registers are illustrated in Table 22.

Table 22. ADC1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A-to-D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI

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analog-to-digital converter 1 (ADC1) module (continued)

The ADC1 module block diagram is illustrated in Figure 17.

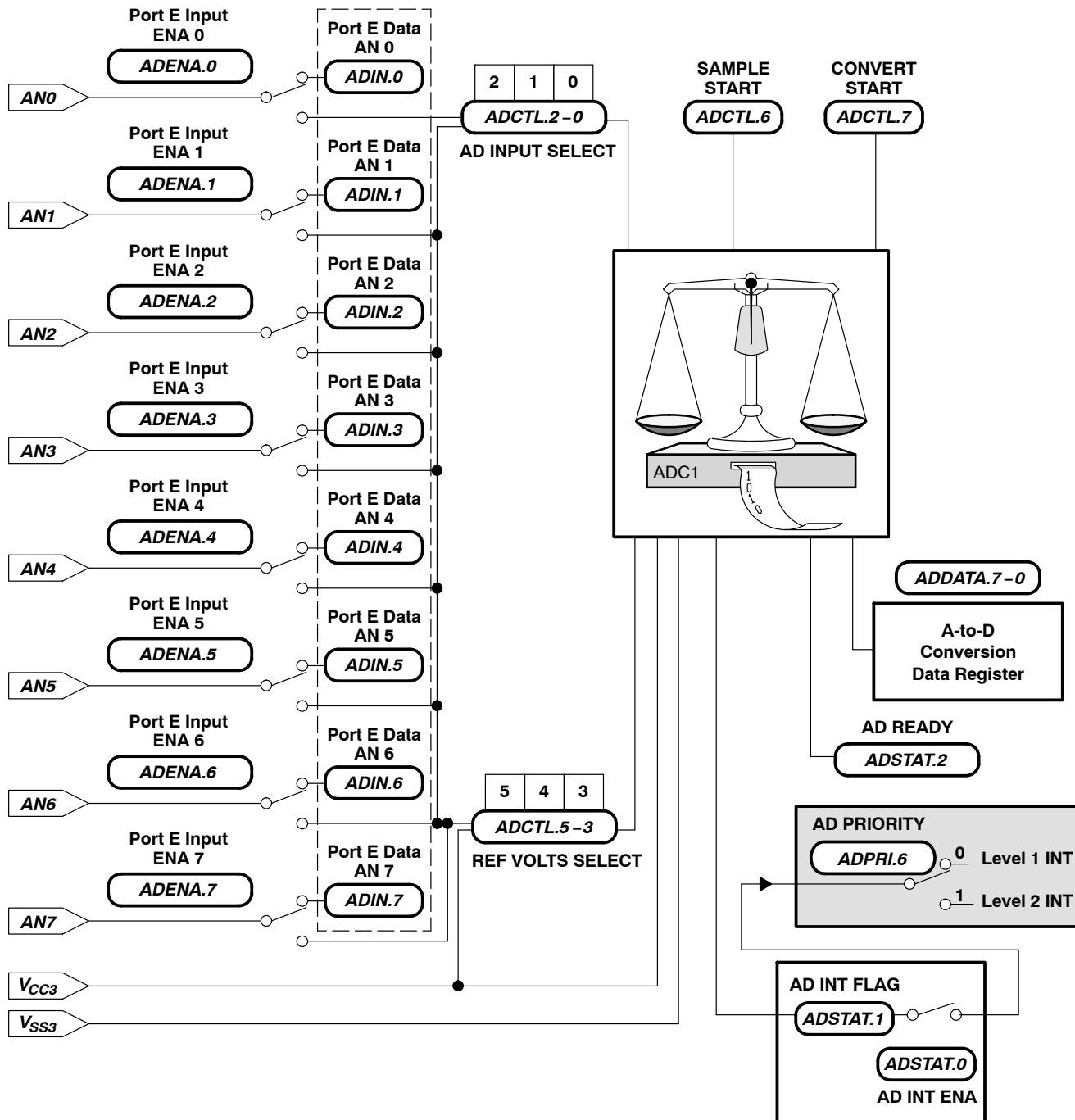


Figure 17. ADC1 Block Diagram

instruction set overview

Table 23 provides an opcode-to-instruction cross-reference of all 73 instructions and 274 opcodes of the '370Cx5x instruction set. The numbers at the top of this table represent the most significant nibble of the opcode while the numbers at the left side of the table represent the least significant nibble. The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.



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Table 23. TMS370 Family Opcode/Instruction Map[†]

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	L	JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8				CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	LDST n 2/6
		JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7
1	S	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7
		JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8
2	N	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes
		JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14	
3	Z	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6
		JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10
4	N	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7
		JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9
5	A	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12
		JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

Table 23. TMS370 Family Opcode/Instruction Map[†] (Continued)

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L S N	C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
	D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
	E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
	F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):

F4	8	MOVW *n[Rn] 4/15	DIV Rn,A 3/14-63
F4	9	JMPL *n[Rn] 4/16	
F4	A	MOV *n[Rn],A 4/17	
F4	B	MOV A,*n[Rn] 4/16	
F4	C	BR *n[Rn] 4/16	
F4	D	CMP *n[Rn],A 4/18	
F4	E	CALL *n[Rn] 4/20	
F4	F	CALLR *n[Rn] 4/22	

Legend:

* = Indirect addressing operand prefix
 & = Direct addressing operand prefix
 # = immediate operand
 #16 = immediate 16-bit number
 lab = 16-label
 n = immediate 8-bit number
 Pd = Peripheral register containing destination type
 Pn = Peripheral register
 Ps = Peripheral register containing source byte
 ra = Relative address
 Rd = Register containing destination type
 Rn = Register file
 Rp = Register pair
 Rpd = Destination register pair
 Rps = Source Register pair
 Rs = Register containing source byte

[†] All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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development system support

The TMS370 family development support tools include an assembler, a C compiler, a linker, an in-circuit emulator (XDS/22), CDT, and an EEPROM/UVEEPROM programmer.

- Assembler/linker (Part No. TMDS3740850-02 for PC)
 - Includes extensive macro capability
 - Features high-speed operation
 - Includes format conversion utilities for popular formats
- ANSI C-Compiler (Part No. TMDS3740855-02 for PC, Part No. TMDS3740555-09 for HP700™, Sun-3™ or Sun-4™)
 - Generates assembly code for the TMS370 that can be inspected easily
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables direct reference of the TMS370's port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (compact development tool) real-time in-circuit emulation
 - Base (Part Number EDSCDT370 – for PC, requires cable)
 - Cable for 68-pin PLCC (Part No. EDSTRG68PLCC)
 - Cable for 64-pin SDIP (Part No. EDSTRG64SDIL)
 - Provides EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Allows uploading/downloading of program and data memory
 - Provides capability to execute programs and software routines
 - Includes 1 024 samples trace buffer
 - Includes single-step executable instructions
 - Allows use of software breakpoints to halt program execution at selected address
- XDS/22 (extended development support) in-circuit emulator
 - Base (Part Number TMDS3762210 for PC, requires cable)
 - Cable for 68-pin PLCC/64-Pin SDIP (Part No. TMDS3788868)
 - Contains all of the features of the CDT370 described above but does not have the capability to program the data EEPROM and program EPROM
 - Contains sophisticated breakpoint trace and timing hardware that provides up to 2047 qualified trace samples with symbolic disassembly
 - Allows breakpoints to be qualified by address and/or data on any type of memory acquisition. Up to four levels of events can be combined to cause a breakpoint
 - Provides timers for analyzing total and average time in routines

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Sun-3 and Sun-4 are trademarks of Sun Microsystems, Inc.



development system support (continued)

- Contains an eight-line logic probe for adding visibility of external signals to the breakpoint qualifier and for tracing display
- Microcontroller programmer
 - Base (Part No. TMDS3760500A – for PC, requires programmer head)
 - Single unit head for 68-pin PLCC (Part No. TMDS3780510A)
 - Single unit head for 64-pin SDIP (Part No. TMDS3780511A)
 - Personal computer-based, window/function-key oriented user interface for ease of use and rapid learning environment
- Design kit (Part No. TMDS3770110 – for PC)
 - Includes TMS370 Application Board and TMS370 Assembler diskette and documentation.
 - Supports quick evaluation of TMS370 functionality
 - Provides capability to upload and download code
 - Provides capability to execute programs and software routines, and to single-step executable instructions
 - Allows software breakpoints to halt program execution at selected addresses
 - Includes wire-wrap prototype area
 - Includes reverse assembler
- Starter Kit (Part No. TMDX37000 – For PC)
 - Includes TMS370 Assembler diskette and documentation
 - Includes TMS370 Simulator
 - Includes programming adapter board and programming software
 - Does not include – (to be supplied by the user):
 - + 5 V power supply
 - ZIF sockets
 - 9-pin RS232 cable

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device numbering conventions

Figure 18 illustrates the numbering and symbol nomenclature for the TMS370Cx5x family.

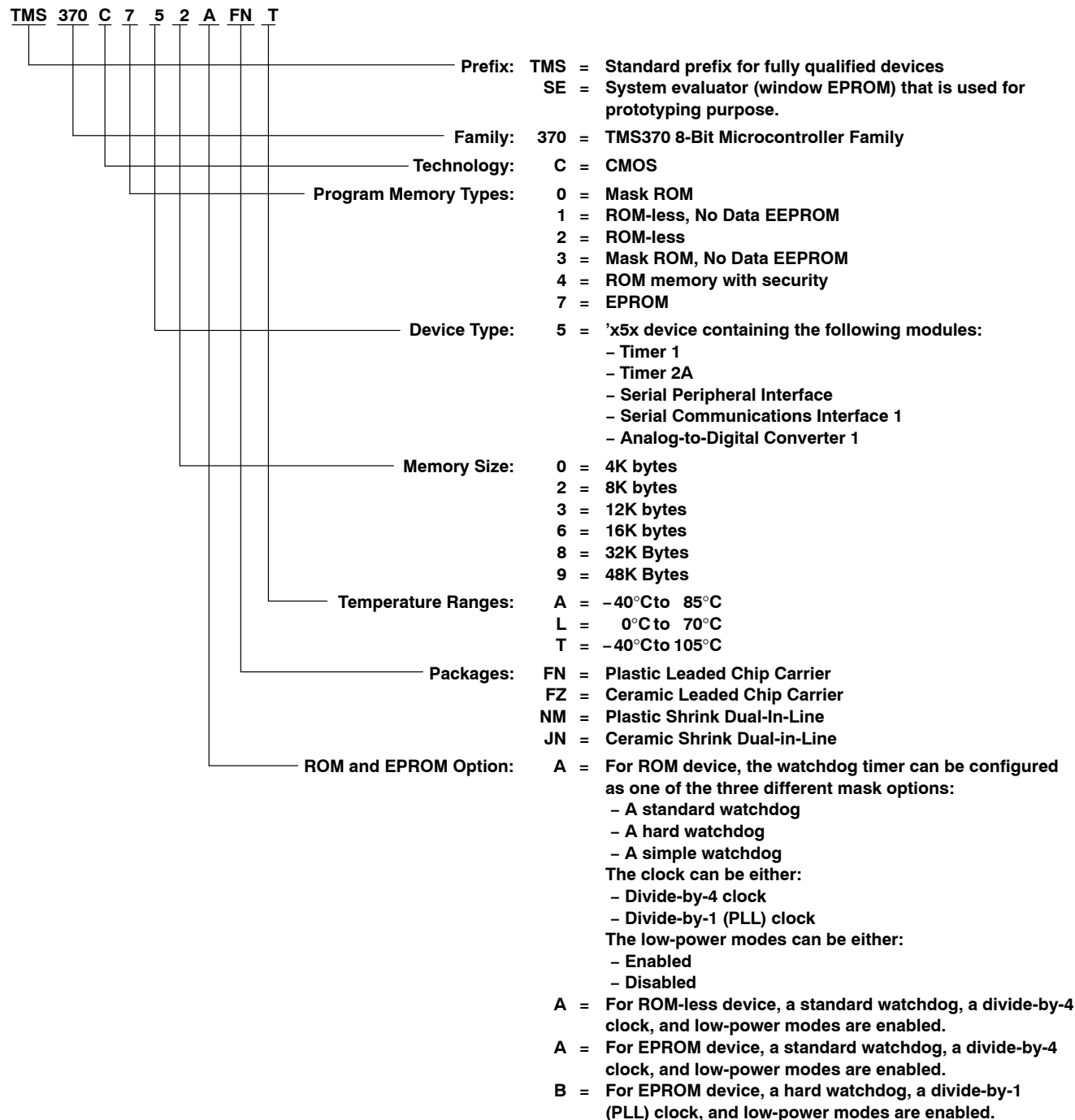


Figure 18. TMS370Cx5x Family Nomenclature

device part numbers

Table 24 provides a list of all the 'x5x devices available. The device part number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number but also the clock and watchdog timer options desired. Remember that each device can have only one of the three possible watchdog timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 24. Device Part Numbers

DEVICE PART NUMBERS FOR 68 PINS	DEVICE PART NUMBERS FOR 64 PINS	DEVICE PART NUMBERS FOR 68 PINS	DEVICE PART NUMBERS FOR 64 PINS
TMS370C050AFNA TMS370C050AFNL TMS370C050AFNT	TMS370C050ANMA TMS370C050ANML TMS370C050ANMT	TMS370C356AFNA TMS370C356AFNL TMS370C356AFNT	TMS370C356ANMA TMS370C356ANML TMS370C356ANMT
TMS370C150AFNT	—	TMS370C456AFNA TMS370C456AFNL TMS370C456AFNT	—
TMS370C250AFNT	—	TMS370C756AFNT	TMS370C756ANMT
TMS370C350AFNA TMS370C350AFNL TMS370C350AFNT	TMS370C350ANMA TMS370C350ANML TMS370C350ANMT	TMS370C058AFNA TMS370C058AFNL TMS370C058AFNT	TMS370C058ANMA TMS370C058ANML TMS370C058ANMT
TMS370C052AFNA TMS370C052AFNL TMS370C052AFNT	TMS370C052ANMA TMS370C052ANML TMS370C052ANMT	TMS370C358AFNA TMS370C358AFNL TMS370C358AFNT	TMS370C358ANMA TMS370C358ANML TMS370C358ANMT
TMS370C352AFNA TMS370C352AFNL TMS370C352AFNT	TMS370C352ANMA TMS370C352ANML TMS370C352ANMT	TMS370C758AFNT	TMS370C758ANMT
TMS370C452AFNA TMS370C452AFNL TMS370C452AFNT	—	TMS370C758BFNT	TMS370C758BNMT
TMS370C353AFNA TMS370C353AFNL TMS370C353AFNT	—	TMS370C059AFNA [†] TMS370C059AFNL [†] TMS370C059AFNT [†]	—
TMS370C056AFNA TMS370C056AFNL TMS370C056AFNT	TMS370C056ANMA TMS370C056ANML TMS370C056ANMT	TMS370C759AFNT [†]	—
TMS370C156AFNT	—	SE370C756AFZT [‡] SE370C758AFZT [‡] SE370C758BFZT [‡] SE370C759AFZT ^{†‡}	SE370C756AJNT [‡] SE370C758AJNT [‡] SE370C758BJNT [‡]
TMS370C256AFNT	—		

[†] Only operate up to 3 MHz SYSCLK

[‡] System evaluators are for use only in prototype environment, and their reliability has not been characterized.

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new code release form

Figure 19 shows a sample of the new code release form.

NEW CODE RELEASE FORM TEXAS INSTRUMENTS TMS370 MICROCONTROLLER PRODUCTS				DATE: _____																
To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information: 1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media) 2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.																				
Company Name: _____ Street Address: _____ Street Address: _____ City: _____ State _____ Zip _____		Contact Mr./Ms.: _____ Phone: (_____) _____ Ext.: _____ Customer Purchase Order Number: _____ Customer Print Number *Yes: _____ # _____ No: _____ (Std. spec to be followed) *If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.																		
Customer Part Number: _____ Customer Application: _____																				
TMS370 Device: _____ TI Customer ROM Number: _____ (provided by Texas Instruments)																				
OSCILLATOR FREQUENCY <table border="1" style="width: 100%; border-collapse: collapse;"><thead><tr><th></th><th style="text-align: center;">MIN</th><th style="text-align: center;">TYP</th><th style="text-align: center;">MAX</th></tr></thead><tbody><tr><td>☐ External Drive (CLKIN)</td><td>_____</td><td>_____</td><td>_____</td></tr><tr><td>☐ Crystal</td><td>_____</td><td>_____</td><td>_____</td></tr><tr><td>☐ Ceramic Resonator</td><td>_____</td><td>_____</td><td>_____</td></tr></tbody></table> ☐ Supply Voltage MIN: _____ MAX: _____ (std range: 4.5V to 5.5V)						MIN	TYP	MAX	☐ External Drive (CLKIN)	_____	_____	_____	☐ Crystal	_____	_____	_____	☐ Ceramic Resonator	_____	_____	_____
	MIN	TYP	MAX																	
☐ External Drive (CLKIN)	_____	_____	_____																	
☐ Crystal	_____	_____	_____																	
☐ Ceramic Resonator	_____	_____	_____																	
CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS <table border="0" style="width: 100%;"><tr><td>Low Power Modes</td><td>Watchdog counter</td><td>Clock Type</td></tr><tr><td>☐ Enabled</td><td>☐ Standard</td><td>☐ Standard (/4)</td></tr><tr><td>☐ Disabled</td><td>☐ Hard Enabled</td><td>☐ PLL (/1)</td></tr><tr><td></td><td>☐ Simple Counter</td><td></td></tr></table> NOTE: Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the <i>TMS370 Family User's Guide</i> (literature number SPNU127) or the <i>TMS370 Family Data Manual</i> (literature number SPNS014B).					Low Power Modes	Watchdog counter	Clock Type	☐ Enabled	☐ Standard	☐ Standard (/4)	☐ Disabled	☐ Hard Enabled	☐ PLL (/1)		☐ Simple Counter					
Low Power Modes	Watchdog counter	Clock Type																		
☐ Enabled	☐ Standard	☐ Standard (/4)																		
☐ Disabled	☐ Hard Enabled	☐ PLL (/1)																		
	☐ Simple Counter																			
TEMPERATURE RANGE <table border="0" style="width: 100%;"><tr><td>☐ 'L': 0° to 70°C (standard)</td><td></td></tr><tr><td>☐ 'A': -40° to 85°C</td><td></td></tr><tr><td>☐ 'T': -40° to 105°C</td><td></td></tr></table>					☐ 'L': 0° to 70°C (standard)		☐ 'A': -40° to 85°C		☐ 'T': -40° to 105°C											
☐ 'L': 0° to 70°C (standard)																				
☐ 'A': -40° to 85°C																				
☐ 'T': -40° to 105°C																				
PACKAGE TYPE <table border="0" style="width: 100%;"><tr><td>☐ 'N' 28-pin PDIP</td><td>☐ "FN" 44-pin PLCC</td></tr><tr><td>☐ "FN" 28-pin PLCC</td><td>☐ "FN" 68-pin PLCC</td></tr><tr><td>☐ "N" 40-pin PDIP</td><td>☐ "NM" 64-pin PSDIP</td></tr><tr><td>☐ "NJ" 40-pin PSDIP (formerly known as N2)</td><td></td></tr></table>					☐ 'N' 28-pin PDIP	☐ "FN" 44-pin PLCC	☐ "FN" 28-pin PLCC	☐ "FN" 68-pin PLCC	☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP	☐ "NJ" 40-pin PSDIP (formerly known as N2)									
☐ 'N' 28-pin PDIP	☐ "FN" 44-pin PLCC																			
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☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP																			
☐ "NJ" 40-pin PSDIP (formerly known as N2)																				
SYMBOLIZATION <table border="0" style="width: 100%;"><tr><td>☐ TI standard symbolization</td><td></td></tr><tr><td>☐ TI standard w/customer part number</td><td></td></tr><tr><td>☐ Customer symbolization</td><td></td></tr><tr><td colspan="2">(per attached spec, subject to approval)</td></tr></table>					☐ TI standard symbolization		☐ TI standard w/customer part number		☐ Customer symbolization		(per attached spec, subject to approval)									
☐ TI standard symbolization																				
☐ TI standard w/customer part number																				
☐ Customer symbolization																				
(per attached spec, subject to approval)																				
BUS EXPANSION <table border="0" style="width: 100%;"><tr><td>☐ YES</td><td>☐ NO</td></tr></table>					☐ YES	☐ NO														
☐ YES	☐ NO																			
NON-STANDARD SPECIFICATIONS: ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.																				
RELEASE AUTHORIZATION: This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cycletime commences when this document is signed off and the verification code is approved by the customer.																				
1. Customer: _____ Date: _____		2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____																		

Figure 19. Sample New Code Release Form



Table 25 is a listing of all the peripheral file frames using the 'Cx5x (provided for a quick reference).

Table 25. Peripheral File Frame Compilation

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
SYSTEM CONFIGURATION REGISTERS									
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011		—	—	AUTOWAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS TEST	CPU TEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013	Reserved								
P014	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLH
P015 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLM
P01D	Reserved								
P01E	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLL
DIGITAL PORT CONTROL REGISTERS									
P01F	Reserved								
P020	Reserved								APORT1
P021	Port A Control Register 2								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	Port B Control Register 2								BPORT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPORT1
P029	Port C Control Register 2								CPORT2
P02A	Port C Data								CDATA
P02B	Port C Direction								CDIR
P02C	Port D Control Register 1								DPORT1
P02D	Port D Control Register 2†								DPORT2
P02E	Port D Data								DDATA
P02F	Port D Direction								DDIR

† To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

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Table 25. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
SPI MODULE CONTROL REGISTER									
P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/SLAVE	TALK	SPI INT ENA	SPICTL
P032 to P036	Reserved								
P037	RCVD7	RCVD6	RCVD5	RCVD4	RCVD3	RCVD2	RCVD1	RCVD0	SPIBUF
P038	Reserved								
P039	SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0	SPIDAT
P03A to P03C	Reserved								
P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
P03F	SPI STEST	SPI PRIORITY	SPI ESPEN	—	—	—	—	—	SPIPRI
TIMER 1 MODULE REGISTER									
Modes: Dual-Compare and Capture/Compare									
P040	Bit 15 T1 Counter MSbyte Bit 8								T1CNTR
P041	Bit 7 T1 Counter LSbyte Bit 0								
P042	Bit 15 Compare Register MSbyte Bit 8								T1C
P043	Bit 7 Compare Register LSbyte Bit 0								
P044	Bit 15 Capture/Compare Register MSbyte Bit 8								T1CC
P045	Bit 7 Capture/Compare Register LSbyte Bit 0								
P046	Bit 15 Watchdog Counter MSbyte Bit 8								WDCNTR
P047	Bit 7 Watchdog Counter LSbyte Bit 0								
P048	Bit 15 Watchdog Reset Key Bit 0								WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to the simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

Table 25. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Mode: Capture/Compare (Continued)									
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI
SCI1 MODULE CONTROL REGISTER									
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNCR/ ISOSYNCR	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	Reserved								
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF
P05A P05B P05C	Reserved								
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	SCI STEST	SCITX PRIORITY	SCIRX PRIORITY	SCI ESPEN	—	—	—	—	SCIPRI
T2A MODULE REGISTER									
Modes: Dual-Compare and Dual-Capture									
P060	Bit 15	T2A Counter MSbyte						Bit 8	T2ACNTR
P061	Bit 7	T2A Counter LSbyte						Bit 0	
P062	Bit 15	Compare Register MSbyte						Bit 8	T2AC
P063	Bit 7	Compare Register LSbyte						Bit 0	
P064	Bit 15	Capture/Compare Register MSbyte						Bit 8	T2ACC
P065	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P066	Bit 15	Capture Register 2 MSbyte						Bit 8	T2AIC
P067	Bit 7	Capture Register 2 LSbyte						Bit 0	

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Table 25. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Dual-Compare and Dual-Capture (Continued)									
P06A	—	—	—	T2A OVRFL- INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1
Mode: Dual-Compare									
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC2 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
Mode: Dual-Capture									
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
Modes: Dual-Compare and Dual-Capture									
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2/PWM DATA IN	T2AIC2/PWM DATA OUT	T2AIC2/PWM FUNCTION	T2AIC2/PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC1/CR DATA DIR	T2APC2
P06F	T2A STEST	T2A PRIORITY	—	—	—	—	—	—	T2APRI
ADC1 MODULE CONTROL REGISTER									
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A-to-D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, $V_{CC1}^{\ddagger}$, V_{CC2} , V_{CC3} (see Note 2)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC1}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC1}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC1}) [§]	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	1 W
Operating free-air temperature range, T_A : L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] $V_{CC1} = V_{CC}$

[§] Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

NOTE 2: Unless otherwise noted, all voltage values are with respect to V_{SS1} .

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage (see Note 2)	4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 3)	3		5.5	
V_{CC2}	Digital I/O supply voltage (see Note 2)	4.5	5	5.5	V
V_{CC3}	Analog supply voltage (see Note 2)	4.5	5	5.5	
V_{SS2}	Digital I/O supply ground	–0.3	0	0.3	V
V_{SS3}	Analog supply ground	–0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC		0.8	V
		MC, normal operation		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET		V_{CC1}	V
		MC (non-WPO mode)		$V_{CC1} - 0.3$ to $V_{CC1} + 0.3$	
		XTAL2/CLKIN		$0.8 V_{CC1}$ to V_{CC1}	
		RESET		$0.7 V_{CC1}$ to V_{CC1}	
V_{MC}	MC (mode control) voltage (see Note 4)	EEPROM write protect override (WPO)		11.7 to 13	V
		EPROM programming voltage (V_{PP})		13 to 13.5	
		Microprocessor		$V_{CC1} - 0.3$ to $V_{CC1} + 0.3$	
		Microcomputer		V_{SS1} to 0.3	
T_A	Operating free-air temperature	L version		0 to 70	°C
		A version		–40 to 85	
		T version		–40 to 105	

NOTES: 2. Unless otherwise noted, all voltage values are with respect to V_{SS1} .

3. RESET must be externally activated when V_{CC1} or SYSCLK is not within the recommended operating range.

4. The basic microcomputer and microprocessor operating modes are selected by the voltage level applied to the dedicated MC pin two system-clock cycles (t_c) before RESET goes inactive (high). The WPO mode can be selected anytime a sufficient voltage is present on MC.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

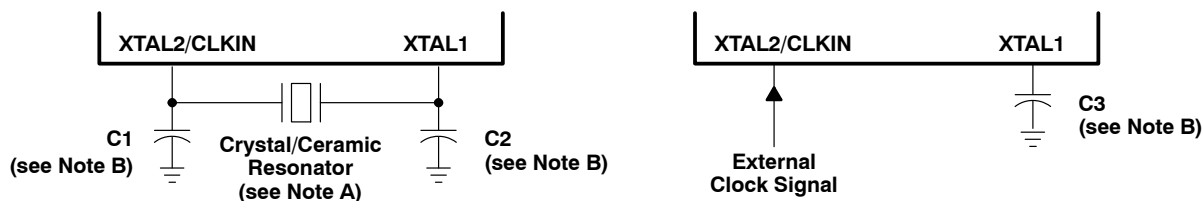
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{OL}	Low-level output voltage (see Note 5)		I _{OL} = 1.4 mA		0.4			V
V _{OH}	High-level output voltage		I _{OH} = − 50 μA		0.9 V _{CC1}			V
			I _{OH} = − 2 mA		2.4			
I _I	Input current	MC	0 V < V _I ≤ 0.3 V		10			μA
			0.3 V < V _I < V _{CC1} − 0.3 V		50			
			V _{CC1} − 0.3 V ≤ V _I ≤ V _{CC1} + 0.3 V		10			
			V _{CC1} + 0.3 V < V _I ≤ 13 V		650			
			12 V ≤ V _I ≤ 13 V See Note 6		50			mA
		I/O pins		0 V ≤ V _I ≤ V _{CC1}		± 10		
I _{OL}	Low-level output current (see Note 5)		V _{OL} = 0.4 V		1.4			mA
I _{OH}	High-level output current		V _{OH} = 0.9 V _{CC1}		− 50			μA
			V _{OH} = 2.4 V		− 2			mA
I _{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 9)	TMS370Cx50A TMS370Cx52A	SYSCLK = 5 MHz	See Notes 7 and 8		30	45	mA
		TMS370Cx53A TMS370Cx56A TMS370Cx58A TMS370Cx58B				35	56	
		TMS370Cx50A TMS370Cx52A	SYSCLK = 3 MHz	See Notes 7 and 8		20	30	
		TMS370Cx53A TMS370Cx56A TMS370Cx58A TMS370Cx58B				25	36	
		TMS370Cx59A†				46	55	
		Supply current (operating mode) OSC POWER bit = 0 (see Note 9)	TMS370Cx50A TMS370Cx52A	SYSCLK = 0.5 MHz	See Notes 7 and 8		5	11
	TMS370Cx53A TMS370Cx56A TMS370Cx58A TMS370Cx58B					13	18	
	TMS370Cx59A†					22	28	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 10)		SYSCLK = 5 MHz, See Notes 7 and 8			12	17	mA
			SYSCLK = 3 MHz, See Notes 7 and 8			8	11	
			SYSCLK = 0.5 MHz, See Notes 7 and 8			2.5	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 11)		SYSCLK = 3 MHz, See Notes 7 and 8			6	8.6	mA
			SYSCLK = 0.5 MHz, See Notes 7 and 8			2	3	
	Supply current (HALT mode)		XTAL2/CLKIN < 0.2 V, See Note 7			2	30	μA

† TMS370Cx59 only operate up to 3 MHz SYSCLK

- NOTES:
- In prior versions of the TMS370 family, the I_{OL} current was equal to 2 mA for ports A, B, C, and D and the RESET pin.
 - Input current I_{pp} is a maximum of 50 mA only when the EPROM is being programmed.
 - Single chip mode, ports configured as inputs or outputs with no load. All inputs $\leq 0.2 \text{ V}$ or $\geq V_{CC} - 0.2 \text{ V}$.
 - XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = $0.01 \text{ mA} \times (\text{total load capacitance} + \text{crystal capacitance in pF})$.
 - Maximum operating current for TMS370Cx50A and TMS370Cx52A = $7.6 (\text{SYSCLK}) + 7 \text{ mA}$. Maximum operating current for TMS370Cx53A, TMS370Cx56A, TMS370Cx58A, and TMS370Cx58B = $10 (\text{SYSCLK}) + 5.8 \text{ mA}$.
 - Maximum standby current for TMS370Cx5xA = $3 (\text{SYSCLK}) + 2 \text{ mA}$. (OSC POWER bit = 0).
 - Maximum standby current for TMS370Cx5xA and TMS370Cx5xB = $2.24 (\text{SYSCLK}) + 1.9 \text{ mA}$. (OSC POWER bit = 1, valid only up to 3 MHz of SYSCLK.)

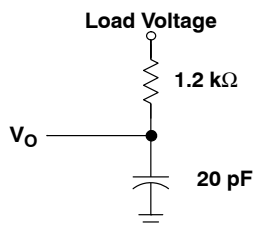


PARAMETER MEASUREMENT INFORMATION



NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
 B. The values of C1 and C2 are typically 15 pF and C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 20. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4 \text{ V}$; Load Voltage = 0 V
 Case 2: $V_O = V_{OL} = 0.4 \text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 21. Typical Output Load Circuit (see Note A)

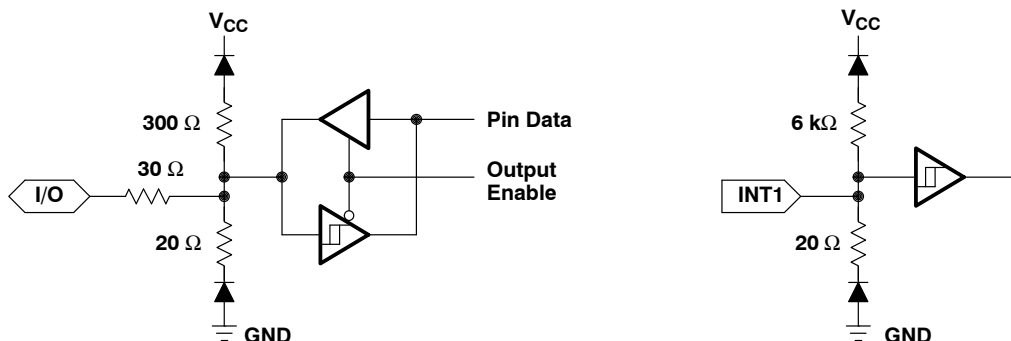


Figure 22. Typical Buffer Circuitry

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PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

A	Address	RXD	SCIRXD
AR	Array	S	Slave mode
B	Byte	SC	SYSCLK
CI	XTAL2/CLKIN	SCC	SCICLK
D	Data	SIMO	SPISIMO
E	$\overline{\text{EDS}}$	SOMI	SPISOMI
FE	Final	SPC	SPICLK
IE	Initial	TXD	SCITXD
M	Master mode	W	Write
PGM	Program	WT	$\overline{\text{WAIT}}$
R	Read		

Lowercase subscripts and their meanings are:

c	cycle time (period)	r	rise time
d	delay time	su	setup time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

The following additional letters are defined as follows:

H	High
L	Low
V	Valid
Z	High impedance

All timings are measured between high and low measurement points as indicated in Figure 23 and Figure 24.

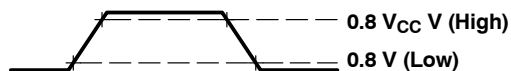


Figure 23. XTAL2/CLKIN Measurement Points

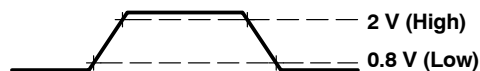


Figure 24. General Measurement Points

external clocking requirements for clock divided by 4[†]

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 12)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN [‡] Crystal operating frequency	2	20	MHz
	SYSCLK [§] System clock	0.5	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions.

[‡] 'x59A operates up to 12 MHz CLKIN

[§] 'x59A operates up to 3 MHz SYSCLK

^{||} SYSCLK = CLKIN/4

NOTE 12: This pulse can be either a high pulse which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

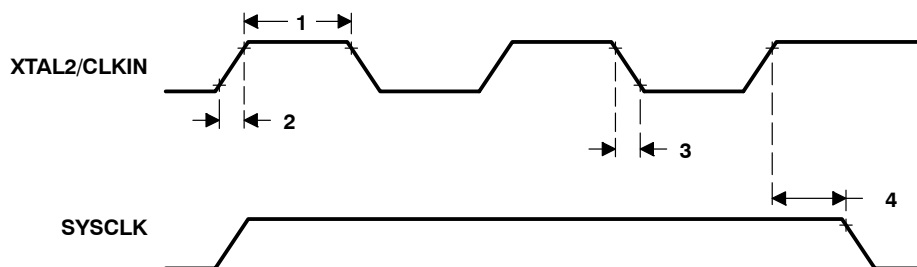


Figure 25. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL)[†]

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 12)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN [#] Crystal operating frequency	2	5	MHz
	SYSCLK [§] System clock	2	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions.

[§] 'x59A operates up to 3 MHz SYSCLK

[#] 'x59A operates up to 3 MHz CLKIN (for divide-by-1 clock option)

^{||} SYSCLK = CLKIN/1

NOTE 12: This pulse can be either a high pulse which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

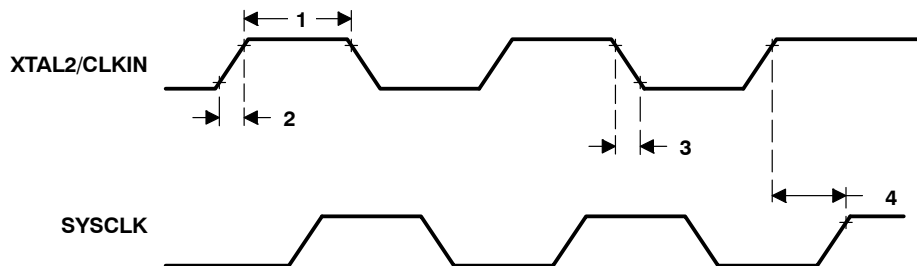


Figure 26. External Clock Timing for Divide-by-1

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general purpose output signal-switching time requirements

	MIN	NOM	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns

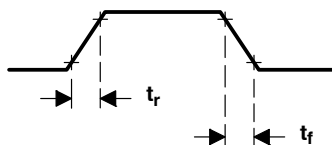


Figure 27. Signal-Switching Timing

recommended EEPROM timing requirements for programming

	MIN	MAX	UNIT
$t_w(\text{PGM})B$ Pulse duration, programming signal to ensure valid data is stored (byte mode)	10		ms
$t_w(\text{PGM})AR$ Pulse duration, programming signal to ensure valid data is stored (array mode)	20		ms

recommended EPROM operating conditions for programming

	MIN	NOM	MAX	UNIT
V_{CC1} Supply voltage	4.75	5.5	6	V
V_{PP} Supply voltage at MC pin	13	13.2	13.5	V
I_{PP} Supply current at MC pin during programming ($V_{PP} = 13$ V)		30	50	mA
SYSCLK System clock	Divide-by-4	0.5	5	MHz
	Divide-by-1	2	5	

recommended EPROM timing requirements for programming

	MIN	NOM	MAX	UNIT
$t_w(\text{EPGM})$ Pulse duration, programming signal (see Note 13)	0.40	0.50	3	ms

NOTE 13: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.

switching characteristics and timing requirements for external read and write (see Figure 28 and Figure 29)[†]

NO.	PARAMETER		MIN	MAX	UNIT
5	t_c	Cycle time, SYSCLK (system clock)	Divide-by-4 clock	200 2000	ns
			Divide-by-1 PLL	200 500	
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low	$0.5t_c-25$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high	$0.5t_c$	$0.5t_c+20$	ns
8	$t_{d(SCL-A)}$	Delay time, SYSCLK low to address $R/\overline{W}$ and $\overline{OCF}$ valid		$0.25t_c+75$	ns
9	$t_{v(A)}$	Valid time, address to $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ low	$0.5t_c-90$		ns
10	$t_{su(D)}$	Setup time, write data time to $\overline{EDS}$ high	$0.75t_c-80^\ddagger$		ns
11	$t_{h(EH-A)}$	Hold time, address, $R/\overline{W}$ and $\overline{OCF}$ from $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ high	$0.5t_c-60$		ns
12	$t_{h(EH-D)W}$	Hold time, write data time from $\overline{EDS}$ high	$0.75t_c+15$		ns
13	$t_{d(DZ-EL)}$	Delay time, data bus high impedance to $\overline{EDS}$ low (read cycle)	$0.25t_c-35$		ns
14	$t_{d(EH-D)}$	Delay time, $\overline{EDS}$ high to data bus enable (read cycle)	$1.25t_c-40$		ns
15	$t_{d(EL-DV)R}$	Delay time, $\overline{EDS}$ low to read data valid		$t_c-95^\ddagger$	ns
16	$t_{h(EH-D)R}$	Hold time, read time from $\overline{EDS}$ high	0		ns
17	$t_{su(WT-SCH)}$	Setup time, $\overline{WAIT}$ time to SYSCLK high	$0.25t_c+70^\S$		ns
18	$t_{h(SCH-WT)}$	Hold time, $\overline{WAIT}$ time from SYSCLK high	0		ns
19	$t_{d(EL-WTV)}$	Delay time, $\overline{EDS}$ low to $\overline{WAIT}$ valid		$0.5t_c-60$	ns
20	t_w	Pulse duration, $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ low	$t_c-80^\ddagger$	$t_c+40^\ddagger$	ns
21	$t_{d(AV-DV)R}$	Delay time, address valid to read data valid		$1.5t_c-115^\ddagger$	ns
22	$t_{d(AV-WTV)}$	Delay time, address valid to $\overline{WAIT}$ valid		t_c-115	ns
23	$t_{d(AV-EH)}$	Delay time, address valid to $\overline{EDS}$ high (end of write)	$1.5t_c-85^\ddagger$		ns

[†] t_c = system-clock cycle time = 1 / SYSCLK

[‡] If wait states, PFWait, or the autowait feature is used, add t_c to this value for each wait state invoked.

[§] If the autowait feature is enabled, the $\overline{WAIT}$ input can assume a "don't care" condition until the third cycle of the access. The $\overline{WAIT}$ signal must be synchronized with the high pulse of the SYSCLK signal while still conforming to the minimum setup time.

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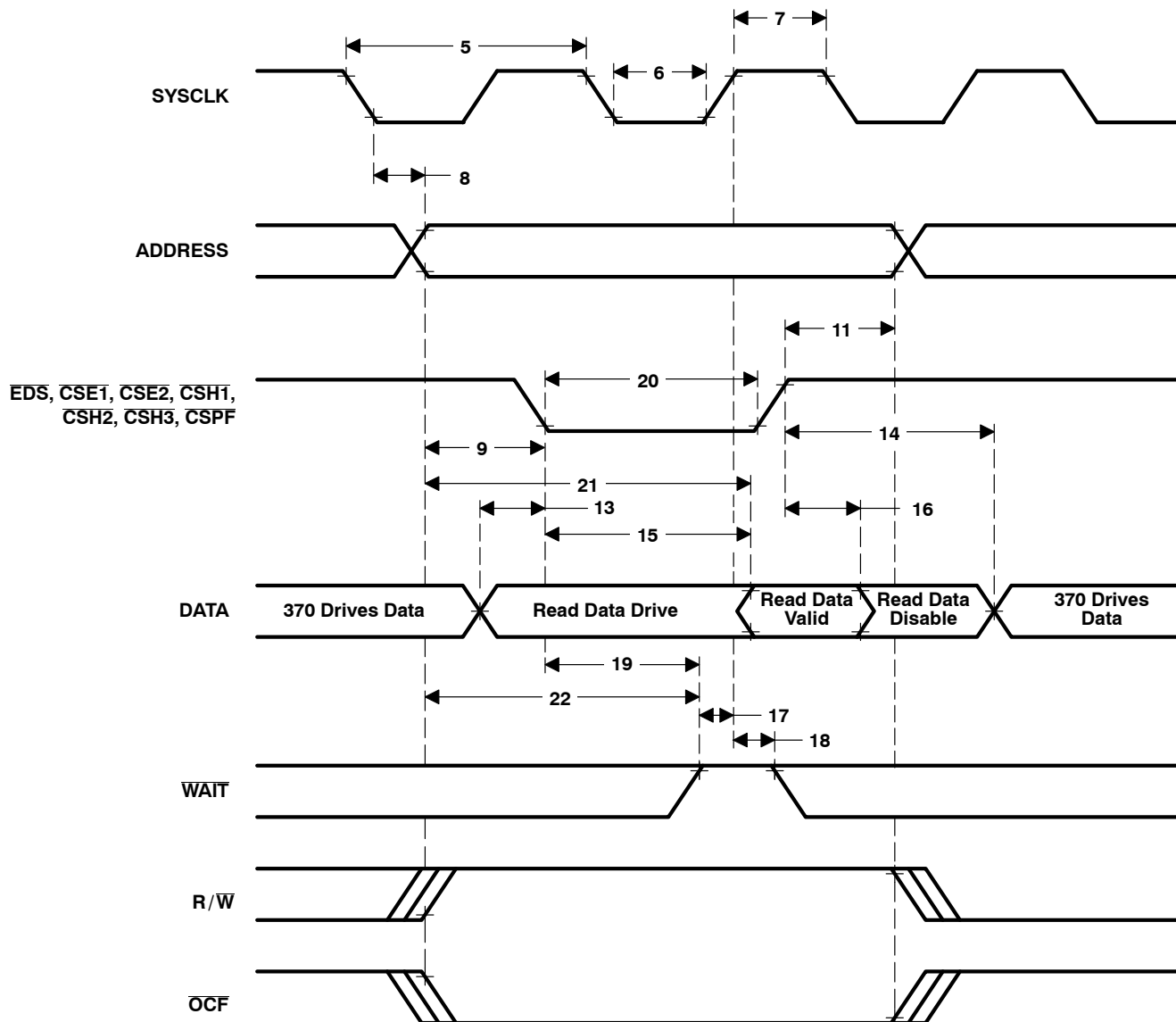


Figure 28. Switching Characteristics and Timing Requirements for External-Read

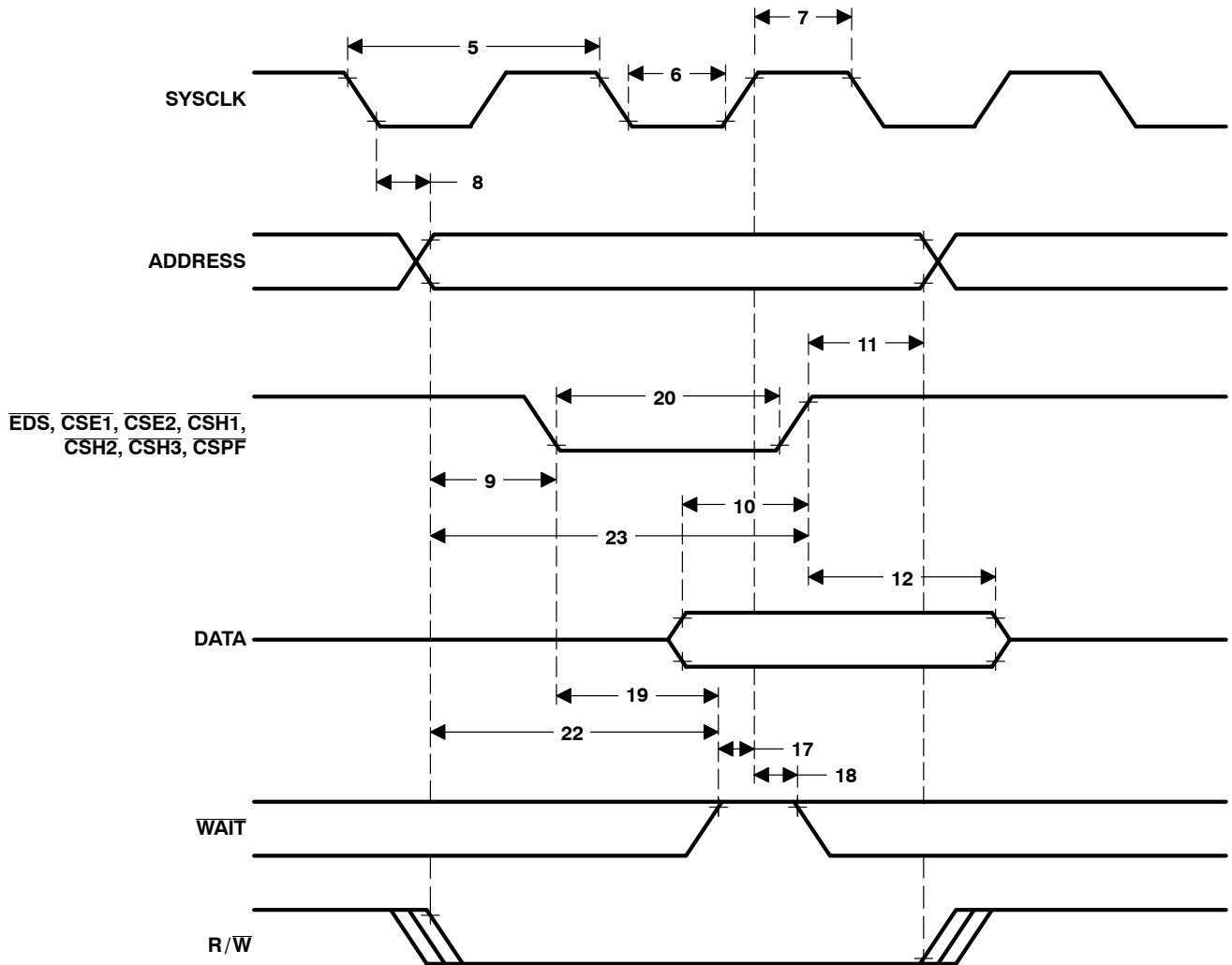


Figure 29. Switching Characteristics and Timing Requirements for External-Write

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SCI1 isosynchronous[†] mode timing characteristics and requirements for internal clock (see Note 14 and Figure 30)

NO.		MIN	MAX	UNIT
24	$t_{c(SCC)}$ Cycle time, SCICLK	$2t_c$	$131\,072t_c$	ns
25	$t_w(SCCL)$ Pulse duration, SCICLK low	$t_c - 45$	$0.5t_{c(SCC)} + 45$	ns
26	$t_w(SCCH)$ Pulse duration, SCICLK high	$t_c - 45$	$0.5t_{c(SCC)} + 45$	ns
27	$t_d(SCCL-TXDV)$ Delay time, SCITXD valid after SCICLK low	- 50	60	ns
28	$t_v(SCCH-TXD)$ Valid time, SCITXD data valid after SCICLK high	$t_w(SCCH) - 50$		ns
29	$t_{su}(RXD-SCCH)$ Setup time, SCIRXD to SCICLK high	$0.25 t_c + 145$		ns
30	$t_v(SCCH-RXD)$ Valid time, SCIRXD data valid after SCICLK high	0		ns

NOTE 14: t_c = system-clock cycle time = 1 / SYSCLK

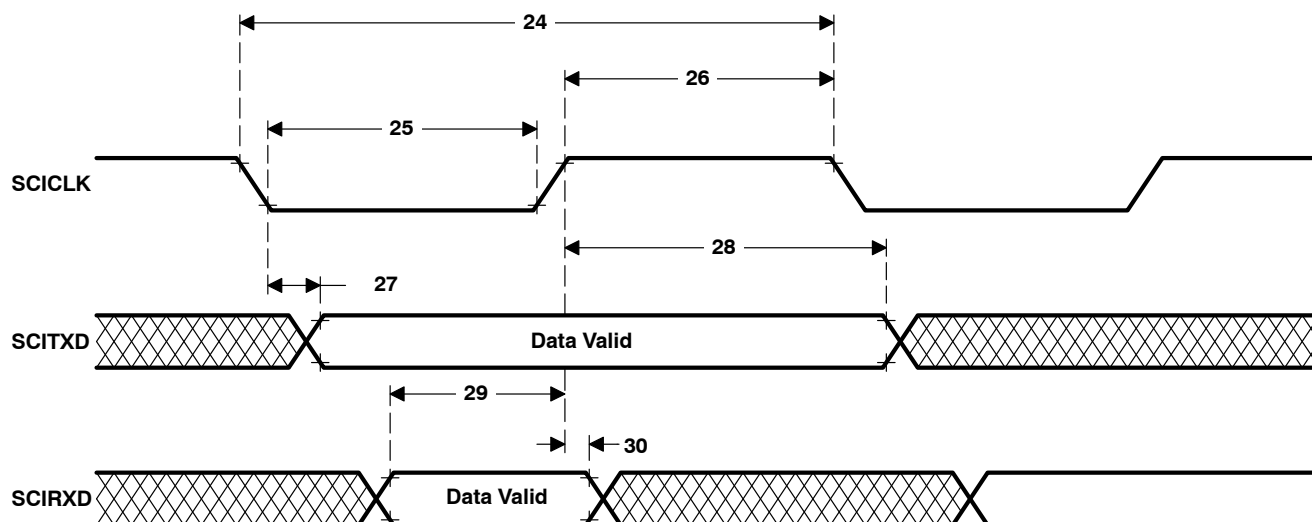


Figure 30. SCI1 Isosynchronous[†] Mode Timing for Internal Clock

[†] Isosynchronous = Isochronous

SCI1 isosynchronous[†] mode timing characteristics and requirements for external clock (see Note 14 and Figure 31)

NO.		MIN	MAX	UNIT
31	$t_c(\text{SCC})$ Cycle time, SCICLK	$10t_c$		ns
32	$t_w(\text{SCCL})$ Pulse duration, SCICLK low	$4.25t_c + 120$		ns
33	$t_w(\text{SCCH})$ Pulse duration, SCICLK high	$t_c + 120$		ns
34	$t_d(\text{SCCL-TXDV})$ Delay time, SCITXD valid after SCICLK low		$4.25t_c + 145$	ns
35	$t_v(\text{SCCH-TXD})$ Valid time, SCITXD data valid after SCICLK high	$t_w(\text{SCCH})$		ns
36	$t_{su}(\text{RXD-SCCH})$ Setup time, SCIRXD to SCICLK high	40		ns
37	$t_v(\text{SCCH-RXD})$ Valid time, SCIRXD data after SCICLK high	$2t_c$		ns

NOTE 14: t_c = system-clock cycle time = $1/\text{SYSCLK}$

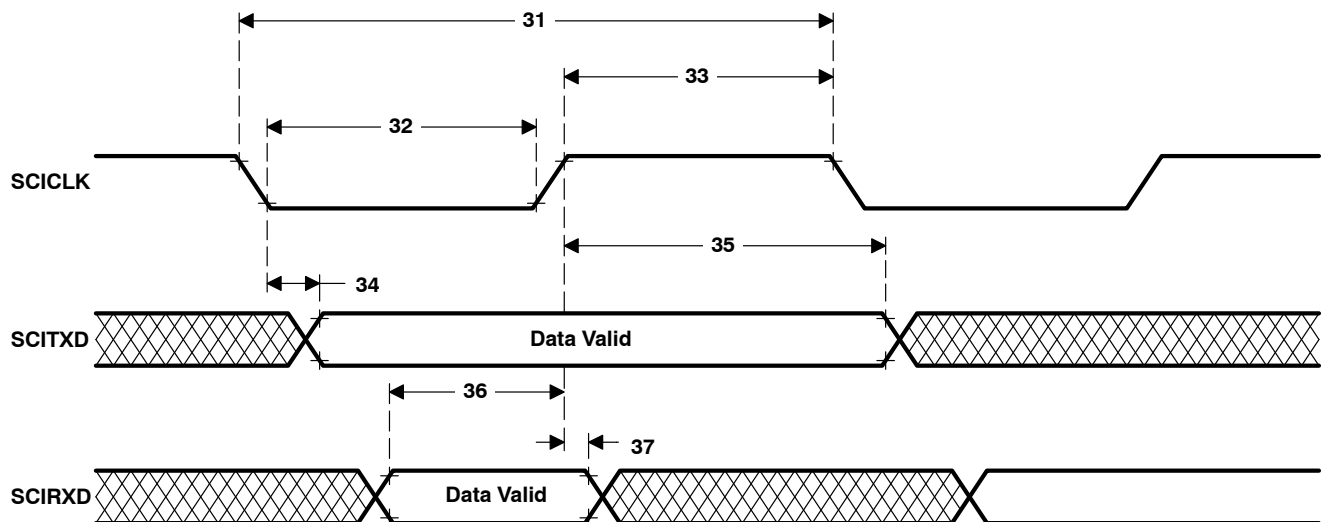


Figure 31. SCI1 Isosynchronous[†] Timing for External Clock

[†] Isosynchronous = Isochronous

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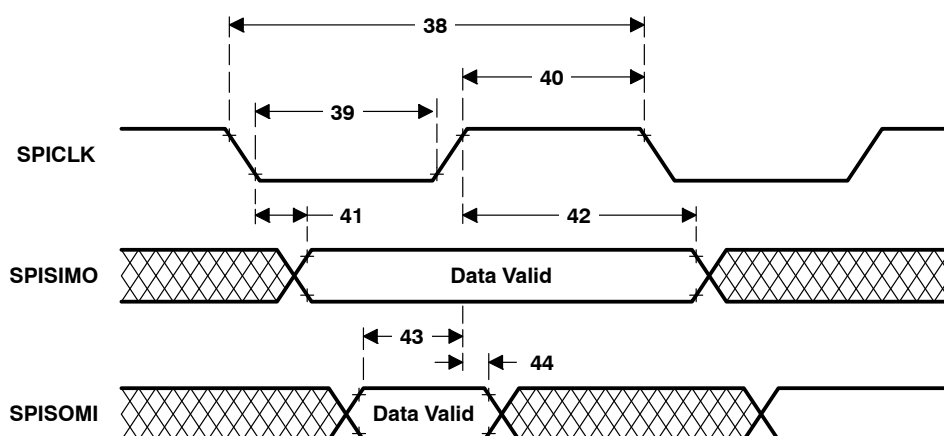
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SPI master mode external timing characteristics and requirements (see Note 14 and Figure 32)

NO.		MIN	MAX	UNIT
38	$t_{c(SPC)}M$ Cycle time, SPICLK	$2t_c$	$256t_c$	ns
39	$t_{w(SPCL)}M$ Pulse duration, SPICLK low	$t_c - 45$	$0.5t_c(SPC)+45$	ns
40	$t_{w(SPCH)}M$ Pulse duration, SPICLK high	$t_c - 55$	$0.5t_c(SPC)+45$	ns
41	$t_{d(SPCL-SIMOV)}M$ Delay time, SPISIMO valid after SPICLK low (polarity = 1)	- 65	50	ns
42	$t_{v(SPCH-SIMO)}M$ Valid time, SPISIMO data valid after SPICLK high (polarity = 1)	$t_{w(SPCH)} - 50$		ns
43	$t_{su(SOMI-SPCH)}M$ Setup time, SPISOMI to SPICLK high (polarity = 1)	$0.25 t_c + 150$		ns
44	$t_{v(SPCH-SOMI)}M$ Valid time, SPISOMI data valid after SPICLK high (polarity = 1)	0		ns

NOTE 14: t_c = system-clock cycle time = 1 / SYSCLK



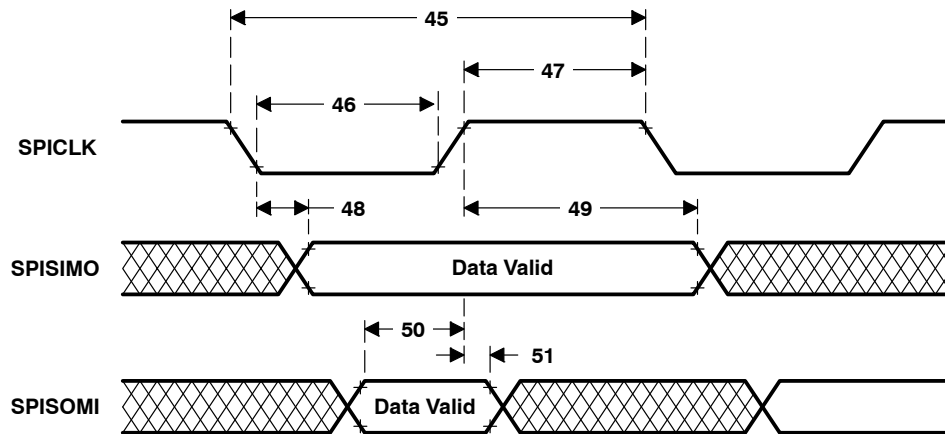
NOTE A: The diagram shows polarity = 1. SPICLK is inverted when polarity = 0.

Figure 32. SPI Master External Timing

SPI slave mode external timing characteristics and requirements (see Note 14 and Figure 33)

NO.		MIN	MAX	UNIT
45	$t_{c(SPC)}S$ Cycle time, SPICLK	$8t_c$		ns
46	$t_{w(SPCL)}S$ Pulse duration, SPICLK low	$4t_c - 45$	$0.5t_{c(SPC)}S + 45$	ns
47	$t_{w(SPCH)}S$ Pulse duration, SPICLK high	$4t_c - 45$	$0.5t_{c(SPC)}S + 45$	ns
48	$t_{d(SPCL-SOMIV)}S$ Delay time, SPISOMI valid after SPICLK low (polarity = 1)		$3.25t_c + 130$	ns
49	$t_{v(SPCH-SOMI)}S$ Valid time, SPISOMI data valid after SPICLK high (polarity = 1)	$t_{w(SPCH)}S$		ns
50	$t_{su(SIMO-SPCH)}S$ Setup time, SPISIMO to SPICLK high (polarity = 1)	0		ns
51	$t_{v(SPCH-SIMO)}S$ Valid time, SPISIMO data after SPICLK high (polarity = 1)	$3t_c + 100$		ns

NOTE 14: t_c = system-clock cycle time = $1/\text{SYSCLK}$



NOTE A: The diagram shows polarity = 1. SPICLK is inverted when polarity = 0.

Figure 33. SPI-Slave External Timing

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The ADC1 has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3} . The purpose is to enhance ADC1 performance by preventing digital switching noise of the logic circuitry that can be present on V_{SS1} and V_{CC1} from coupling into the ADC1 analog stage. All ADC1 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution 8-bits (256 values)
 Monotonic Yes
 Output conversion mode 00h to FFh (00 for $V_I \leq V_{SS3}$; FF for $V_I \leq V_{ref}$)
 Conversion time (excluding sample time) $164 t_c$

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC3} Analog supply voltage	4.5	5	5.5	V
	$V_{CC3}-3$		$V_{CC3}+0.3$	
V_{SS3} Analog ground	$V_{SS3}-3$		$V_{SS3}+0.3$	V
V_{ref} Non- V_{CC3} reference [†]	2.5	V_{CC3}	$V_{CC3}+0.1$	V
Analog input for conversion	V_{SS3}		V_{ref}	V

[†] V_{ref} must be stable, within $\pm 1/2$ LSB of the required resolution, during the entire conversion time.

operating characteristics over recommended ranges operating conditions

PARAMETER			MIN	MAX	UNIT
Absolute accuracy [†]			$V_{CC3} = 5.5 \text{ V}$ $V_{ref} = 5.1 \text{ V}$		± 1.5 LSB
Differential/integral linearity error ^{†‡}			$V_{CC3} = 5.5 \text{ V}$ $V_{ref} = 5.1 \text{ V}$		± 0.9 LSB
I_{CC3} Analog supply current	Converting				2 mA
	Nonconverting				5 μA
I_I	Input current, AN0 – AN7		$0 \text{ V} \leq V_I \leq 5.5 \text{ V}$		2 μA
	I_{ref} input charge current				1 mA
Z_{ref} Source impedance of V_{ref}	$\text{SYSCLK} \leq 3 \text{ MHz}$				24 k Ω
	$3 \text{ MHz} < \text{SYSCLK} \leq 5 \text{ MHz}$				10 k Ω

[†] Absolute resolution = 20 mV. At $V_{ref} = 5 \text{ V}$, this is one LSB. As V_{ref} decreases, LSB size decreases; therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

[‡] Excluding quantization error of $1/2$ LSB



The ADC1 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined so that the high-impedance can be accommodated without penalty to the low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC1 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter will reset the SAMPLE START and CONVERT START bits, signaling that a conversion has started and that the analog signal can be removed.

analog timing requirements

		MIN	MAX	UNIT
$t_{su(S)}$	Setup time, analog to sample command	0		ns
$t_{h(AN)}$	Hold time, analog input from start of conversion	$18t_c$		ns
$t_w(S)$	Pulse duration, sample time per kilohm of source impedance [†]	1		$\mu s/k\Omega$

[†] The value given is valid for a signal with a source impedance > 1 k Ω . If the source impedance is < 1 k Ω , use a minimum sampling time of 1 μs .

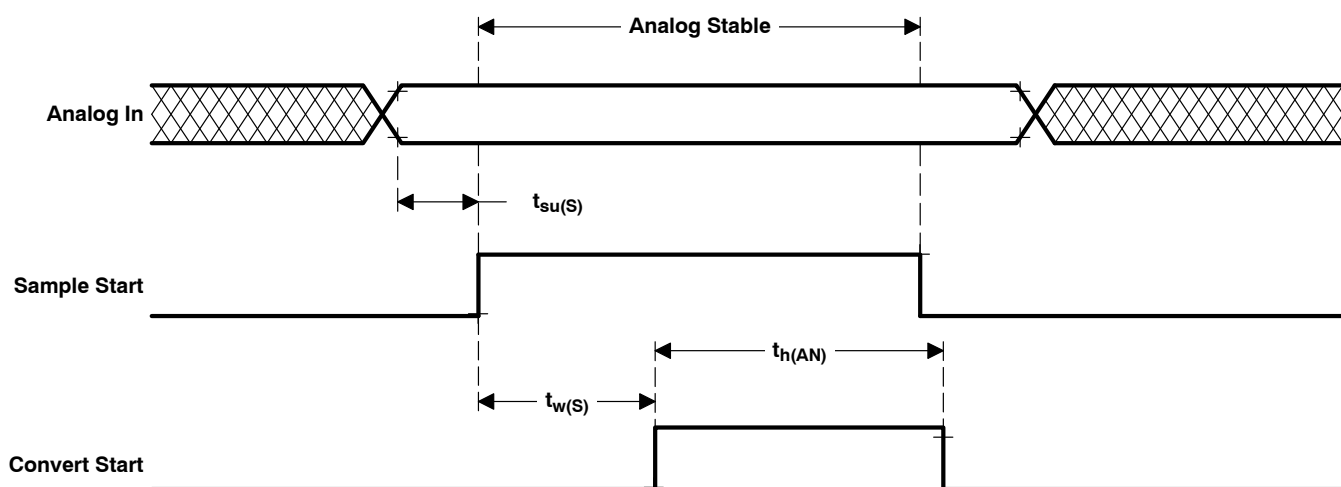


Figure 34. Analog Timing

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Table 26 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

Table 26. TMS370Cx5x Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 68 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C050AFNA TMS370C050AFNL TMS370C050AFNT TMS370C150AFNT TMS370C250AFNT TMS370C350AFNA TMS370C350AFNL TMS370C350AFNT TMS370C052AFNA TMS370C052AFNL TMS370C052AFNT TMS370C352AFNA TMS370C352AFNL TMS370C352AFNT TMS370C452AFNA TMS370C452AFNL TMS370C452AFNT TMS370C353AFNA TMS370C353AFNL TMS370C353AFNT TMS370C056AFNA TMS370C056AFNL TMS370C056AFNT TMS370C156AFNT TMS370C256AFNT TMS370C356AFNA TMS370C356AFNL TMS370C356AFNT TMS370C456AFNA TMS370C456AFNL TMS370C456AFNT TMS370C756AFNT TMS370C058AFNA TMS370C058AFNL TMS370C058AFNT TMS370C358AFNA TMS370C358AFNL TMS370C358AFNT TMS370C758AFNT TMS370C758BFNT TMS370C059AFNA TMS370C059AFNL TMS370C059AFNT TMS370C759AFNT
FZ – 68 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C756AFZT SE370C758AFZT SE370C758BFZT SE370C759AFZT
JN – 64 pin (70-mil pin spacing)	CERAMIC SHRINK DUAL-IN-LINE PACKAGE (CSDIP)	JN(R-CDIP-T64) CERAMIC DUAL-IN-LINE PACKAGE	SE370C756AJNT SE370C758AJNT SE370C758BJNT



Table 26. TMS370Cx5x Family Package Type and Mechanical Cross-Reference (Continued)

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
NM – 64 pin (70-mil pin spacing)	PLASTIC SHRINK DUAL-IN-LINE PACKAGE (PSDIP)	NM(R-PDIP-T64) PLASTIC SHRINK DUAL-IN-LINE PACKAGE	TMS370C050ANMA TMS370C050ANML TMS370C050ANMT TMS370C350ANMA TMS370C350ANML TMS370C350ANMT TMS370C052ANMA TMS370C052ANML TMS370C052ANMT TMS370C352ANMA TMS370C352ANML TMS370C352ANMT TMS370C056ANMA TMS370C056ANML TMS370C056ANMT TMS370C356ANMA TMS370C356ANML TMS370C356ANMT TMS370C756ANMT TMS370C058ANMA TMS370C058ANML TMS370C058ANMT TMS370C358ANMA TMS370C358ANML TMS370C358ANMT TMS370C758ANMT TMS370C758BNMT

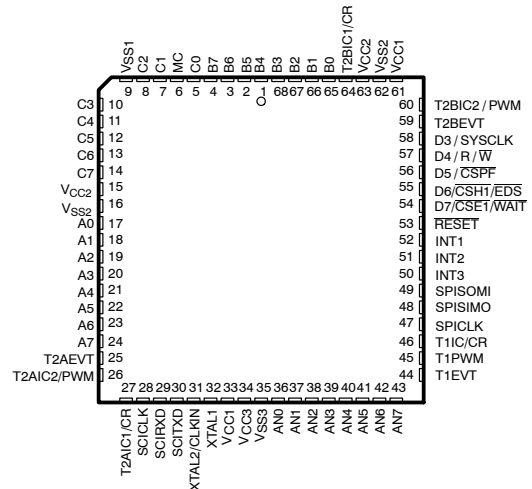
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- **CMOS/EEPROM/EPROM Technologies on a Single Device**
 - Mask-ROM Devices for High-Volume Production
 - One-Time-Programmable (OTP) EPROM Devices for Low-Volume Production
 - Reprogrammable EPROM Devices for Prototyping Purposes
- **Internal System Memory Configurations**
 - On-Chip Program Memory Versions
 - ROM: 24K, 32K, or 48K Bytes
 - EPROM: 32K or 48K Bytes
 - Data EEPROM: 256 Bytes
 - Static RAM: 1K or 3.5K Bytes
 - External Memory/Peripheral Wait States
 - Precoded External Chip-Select Outputs in Microcomputer Mode
- **Flexible Operating Features**
 - Low-Power Modes: STANDBY and HALT
 - Commercial, Industrial, and Automotive Temperature Ranges
 - Clock Options
 - Divide-by-4 (0.5 MHz – 5 MHz SYSCLK)
 - Divide-by-1 (2 MHz – 5 MHz SYSCLK) PLL
 - Supply Voltage (V_{CC}): 5 V $\pm$ 10%
- **Eight-Channel 8-Bit Analog-to-Digital Converter 1 (ADC1)**
- **Three 16-Bit General Purpose Timers**
 - Software Configurable as
 - Three 16-Bit Event Counters, or
 - Three 16-Bit Pulse Accumulators, or
 - Five 16-Bit Input Capture Functions, or
 - Six Compare Registers, or
 - Three Self-Contained PWM Functions
 - One Timer Has an 8-Bit Prescaler, Providing a 24-Bit Real-Time Timer
- **On-Chip 24-Bit Watchdog Timer**
 - EPROM/OTP: Standard Watchdog
 - Mask-ROM Devices: Hard Watchdog, Simple Counter, or Standard Watchdog
- **Serial Communications Interface (SCI1)**
 - Asynchronous and Isosynchronous[†] Modes
 - Full Duplex, Double-Buffered RX and TX
 - Two Multiprocessor Communication Formats

**FN/FZ PACKAGE
(TOP VIEW)**



- **Serial Peripheral Interface (SPI)**
 - Variable-Length High-Speed Shift Register
 - Synchronous Master/Slave Operation
- **Flexible Interrupt Handling**
 - Two S/W Programmable Interrupt Levels
 - Global- and Individual-Interrupt Masking
 - Programmable Rising- or Falling-Edge Detect
- **TMS370 Series Compatibility**
 - Register-to-Register Architecture
 - 256 General-Purpose Registers
 - 14 Powerful Addressing Modes
 - Instructions Upwardly Compatible With All TMS370 Devices
- **CMOS/Package/TTL-Compatible I/O Pins**
 - 46 Bidirectional Pins, 9 Input Pins
 - 68-Pin Plastic and Ceramic Leaded Chip Carrier Packages
 - All Peripheral Function Pins Are Software Configurable for Digital I/O
- **Workstation/PC-Based Development System**
 - C Compiler and C Source Debugger
 - Real-Time In-Circuit Emulation
 - Extensive Breakpoint/Trace Capability
 - Software Performance Analysis
 - Multi-Window User Interface
 - Microcontroller Programmer



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[†] Isosynchronous = Isochronous

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TMS370Cx6x 8-BIT MICROCONTROLLER

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Pin Descriptions

PIN			I/O†	DESCRIPTION‡
NAME	ALTERNATE FUNCTION	PLCC (68)		
A0 A1 A2 A3 A4 A5 A6 A7	DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7	17 18 19 20 21 22 23 24	I/O	Single-chip mode: Port A is a general-purpose bidirectional I/O port. Expansion mode: Port A can be individually programmed as the external bidirectional data bus (DATA0 – DATA7).
B0 B1 B2 B3 B4 B5 B6 B7	ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7	65 66 67 68 1 2 3 4	I/O	Single-chip mode: Port B is a general-purpose bidirectional I/O port. Expansion mode: Port B can be individually programmed as the low-order address output bus (ADDR0 – ADDR7).
C0 C1 C2 C3 C4 C5 C6 C7	ADDR8 ADDR9 ADDR10 ADDR11 ADDR12 ADDR13 ADDR14 ADDR15	5 7 8 10 11 12 13 14	I/O	Single-chip mode: Port C is a general-purpose bidirectional I/O port. Expansion mode: Port C can be individually programmed as the high-order address output bus (ADDR8 – ADDR15).
INT1 INT2 INT3	NMI — —	52 51 50	I I/O I/O	External (nonmaskable or maskable) interrupt/general-purpose input pin External maskable interrupt input/general-purpose bidirectional pin External maskable interrupt input/general-purpose bidirectional pin
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	E0 E1 E2 E3 E4 E5 E6 E7	36 37 38 39 40 41 42 43	I	ADC1 analog input (AN0 – AN7) or positive reference pins (AN1 – AN7) Port E can be programmed individually as general-purpose input pins if not used as ADC1 analog input or positive reference input.
V _{CC3} V _{SS3}		34 35		ADC1 positive-supply voltage and optional positive-reference input pin ADC1 ground reference pin
RESET		53	I/O	System reset bidirectional pin. $\overline{\text{RESET}}$, as an input, initializes the microcontroller; as open-drain output, $\overline{\text{RESET}}$ indicates an internal failure was detected by the watchdog or oscillator fault circuit.
MC		6	I	Mode control (MC) pin. MC enables EEPROM write-protection override (WPO) mode, also EPROM V _{PP} .
XTAL2/CLKIN XTAL1		31 32	I O	Internal oscillator crystal input/external clock source input Internal oscillator output for crystal
V _{CC1}		33, 61		Positive supply voltage
V _{CC2}		15, 63		Positive supply voltage

† I = input, O = output

‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Also, port D3 can be configured as SYSCLK.



Pin Descriptions (Continued)

PIN			I/O†	DESCRIPTION‡
NAME	ALTERNATE FUNCTION	PLCC (68)		
V _{SS1}		9		Ground reference for digital logic
V _{SS2}		16,62		Ground reference for digital I/O logic
D3 D4 D5 D6 D7	FUNCTION A B		I/O	Single-chip mode: Port D is a general-purpose bidirectional I/O port. Each of the port D pins can be configured individually as a general-purpose I/O pin, primary memory control signal (function A), or secondary memory control signal (function B). All chip selects are independent and can be used for memory-bank switching. See Table 1 for function A memory accesses. I/O pin A, B: Internal clock signal is 1/1 (PLL) or 1/4 XTAL2/CLKIN frequency I/O pin A, B: Read/write output pin I/O pin A: Chip select peripheral output for peripheral file goes low during memory accesses I/O pin B: Reserved I/O pin A: Chip select half output 1 goes low during memory accesses I/O pin B: External data strobe output goes low during memory accesses from external memory and has the same timings as the five chip selects. I/O pin A: Chip select eighth output goes low during memory accesses. I/O pin B: Wait-input pin extends bus signals.
	SYSCLK	SYSCLK		
	R/W	R/W		
	CSPF	—		
	CSH1	EDS		
	CSE1	WAIT		
SCITXD	SCII01	30	I/O	SCI transmit data output pin/general-purpose bidirectional pin[§] SCI receive data input pin/general-purpose bidirectional pin SCI bidirectional serial clock pin/general-purpose bidirectional pin
SCIRXD	SCII02	29		
SCICLK	SCII03	28		
T1IC/CR	T1IO1	46	I/O	Timer1 input capture/counter reset input pin/general-purpose bidirectional pin Timer1 pulse width modulation (PWM) output pin/general-purpose bidirectional pin Timer1 external event input pin/general-purpose bidirectional pin
T1PWM	T1IO2	45		
T1EVT	T1IO3	44		
T2AIC1/CR	T2AIO1	27	I/O	Timer2A input capture 1/counter-reset input pin/general-purpose bidirectional pin Timer2A input capture 2/PWM output pin/general-purpose bidirectional pin Timer2A external event input pin/general-purpose bidirectional pin
T2AIC2/PWM	T2AIO2	26		
T2AEVT	T2AIO3	25		
T2BIC1/CR	T2BIO1	64	I/O	Timer2B input capture 1/counter-reset input pin/general-purpose bidirectional pin Timer2B input capture 2/PWM output pin/general-purpose bidirectional pin Timer2B external event input pin/general-purpose bidirectional pin
T2BIC2/PWM	T2BIO2	60		
T2BEVT	T2BIO3	59		
SPISOMI	SPIIO1	49	I/O	SPI slave output pin, master input pin/general-purpose bidirectional pin SPI slave input pin, master output pin/general-purpose bidirectional pin SPI bidirectional serial clock pin/general-purpose bidirectional pin
SPISIMO	SPIIO2	48		
SPICLK	SPIIO3	47		

† I = input, O = output

‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Port D3 also can be configured as SYSCLK.

§ The three-pin configuration SCI is referred to as SCI1.

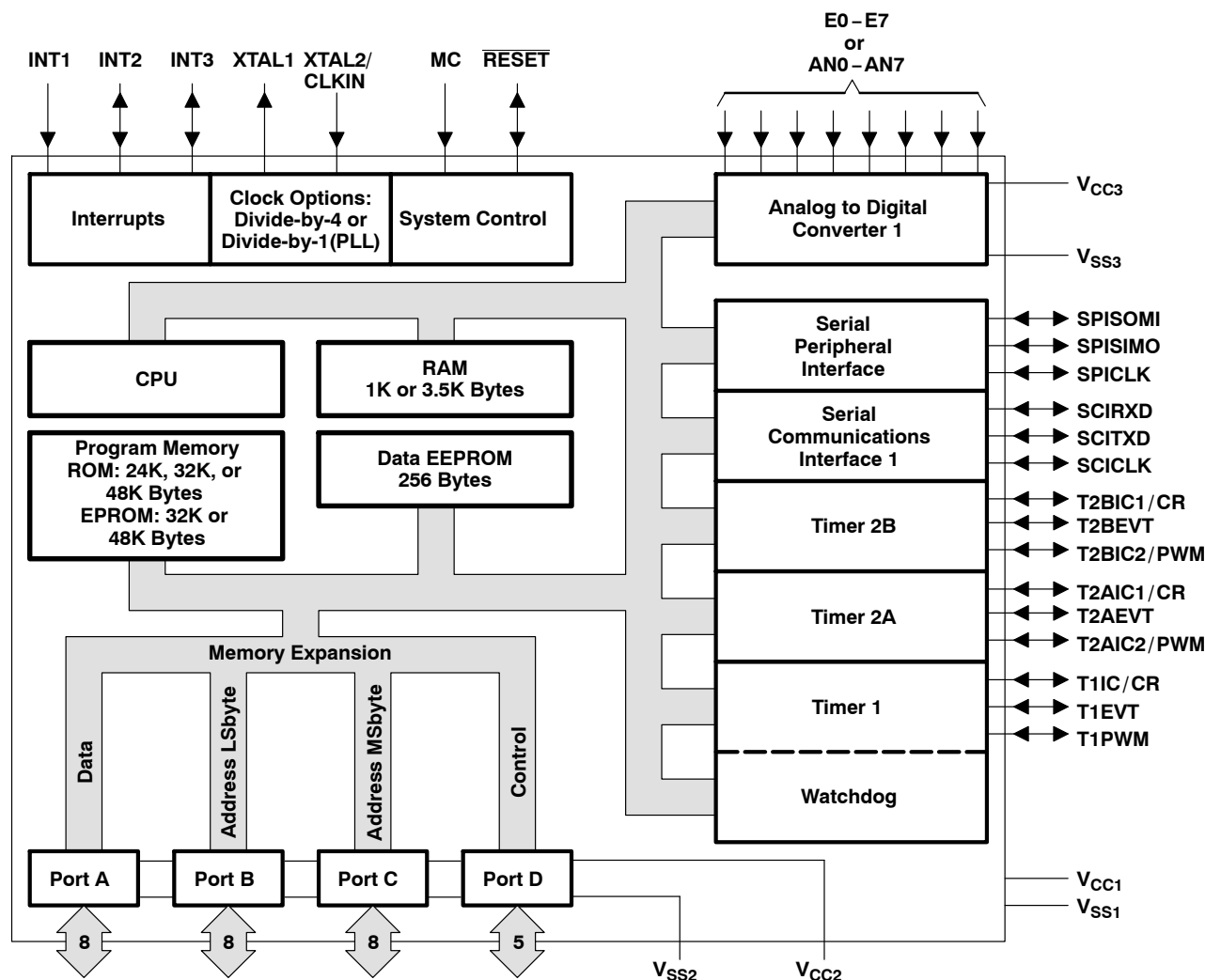
Table 1. Function A Memory-Access Locations for 'x6x Devices

FUNCTION A	'X67	'X68	'X69
CSE1	A000h – BFFFh (8K bytes)	A000h – BFFFh (8K bytes)	E000h – EFFFh (4K bytes)
CSH1	C000h – FFFFh (16K bytes)	C000h – FFFFh (16K bytes)	F000h – FFFFh (4K bytes)
CSPF	10C0h – 10FFh (64 bytes)	10C0h – 10FFh (64 bytes)	10C0h – 10FFh (64 bytes)

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functional block diagram



description

The TMS370C067, TMS370C068, TMS370C069, TMS370C768, TMS370C769, SE370C768, and SE370C769 devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx6x refers to these devices. The TMS370 family provides cost-effective real-time control through integration of advanced peripheral function modules and various on-chip memory configurations.

The TMS370Cx6x family of devices is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technologies. The low-operating power, wide-operating temperature range, and noise immunity of CMOS technology, coupled with the high performance and extensive on-chip peripheral functions, make the TMS370Cx6x devices attractive in system designs for automotive electronics, industrial motor control, computer peripheral control, telecommunications, and consumer application.

All TMS370Cx6x devices contain the following on-chip peripheral modules:

- 8-channel, 8-bit analog-to-digital converter 1 (ADC1)
- Serial communications interface 1 (SCI1)
- Serial peripheral interface (SPI)

description (continued)

- One 24-bit general-purpose watchdog timer
- Three 16-bit general-purpose timers (one with an 8-bit prescaler)

Table 2 provides a memory configuration overview of the TMS370Cx6x devices.

Table 2. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		OFF-CHIP MEMORY EXP. (BYTES)	DATA MEMORY (BYTES)		OPERATING MODES		PACKAGES 68-PIN PLCC/CLCC
	ROM	EPROM		RAM	EEPROM	μC [†]	μP [†]	
TMS370C067A	24K	—	24K	1K	256	√	√	FN – PLCC
TMS370C068A	32K	—	24K	1K	256	√	√	FN – PLCC
TMS370C069A	48K [‡]	—	8K	3.5K	256	√	√	FN – PLCC
TMS370C768A	—	32K	24K	1K	256	√	√	FN – PLCC
TMS370C769A	—	48K [‡]	8K	3.5K	256	√	√	FN – PLCC
SE370C768A [§]	—	32K	24K	1K	256	√	√	FZ – CLCC
SE370C769A [§]	—	48K [‡]	8K	3.5K	256	√	√	FZ – CLCC

[†] μC – Microcomputer mode

μP – Microprocessor mode

[‡] 'x69 can only operate up to 3 MHz SYSCLK.

[§] System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.

The suffix letter (A) appended to the device names shown in the device column of Table 2 indicates the configuration of the device. ROM or EPROM devices have different configurations as indicated in Table 3. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 3. Suffix Letter Configuration

DEVICE [¶]	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM A	Standard	Divide-by-4 (Standard oscillator)	Enabled
ROM A	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

[¶] Refer to the “device numbering conventions” section for device nomenclature and the “device part numbers” section for ordering.

The mask-programmable ROM in the associated TMS370C06x devices is replaced in the TMS370C76x with 32K or 48K bytes of EPROM while all the other available memory and on-chip peripherals are identical. One-time-programmable (OTP) (TMS370C768 and TMS370C769) and reprogrammable devices (SE370C768 and SE370C769) are available.

TMS370C768 and TMS370C769 are OTP devices that are available in plastic packages. This microcomputer is effective to use for immediate production updates for other members of the TMS370Cx6x family or for low-volume production runs when the mask charge or cycle time for low-cost mask-ROM devices is not practical.

The SE370C768 and SE370C769 have windowed ceramic packages to allow reprogramming of the program EPROM memory during the development/prototyping phase of design. The SE370C768 and SE370C769 devices allow quick updates to breadboards and prototype systems while iterating initial designs.

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description (continued)

The TMS370Cx6x family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all central processing unit (CPU) activity (i.e., no instructions are executed). In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx6x features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx6x family is fully instruction-set compatible, allowing easy transition between members of the TMS370 8-bit microcontroller family.

The SPI and the two operational modes of the SCI1 allow three methods of serial communications. The SCI1 allows standard RS-232-C communications interface between other common data transmission equipment, while the SPI gives high-speed communications between simpler shift-register type devices, such as display drivers, ADC1, phase-locked loop (PLL), I/O expansion, or other microcontrollers in the system.

For large memory applications, the TMS370Cx6x family provides an external bus with non-multiplexed address and data. Precoded memory chip-select outputs can be enabled, which allows minimum-chip-count system implementations. Wait-state support facilitates performance matching among the CPU, external memory, and the peripherals. All pins associated with memory expansion interface are individually software configurable for general purpose digital input/output (I/O) pins when operating in the microcomputer mode.

The TMS370Cx6x family provides the system designer with an economical, efficient solution to real-time control applications. The TMS370 family extended development system (XDS™) and compact development tool (CDT™) solve the challenge of efficiently developing the software and hardware required to design the TMS370Cx6x into an ever-increasing number of complex applications. The application source code can be written in assembly and C language, and the output code can be generated by the linker. The TMS370 family XDS development tools communicate through a standard RS-232-C interface with an existing personal computer. This allows the use of the personal computer editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes extensive use of menus and screen windowing so that a system designer with minimal training can begin developing software. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as reduced time-to-market cycle.

The TMS370Cx6x family together with the TMS370 family XDS/22, CDT370, starter kit, software tools, the SE370C76x reprogrammable devices, comprehensive product documentation, and customer support provide a complete solution to the needs of the system designer.

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modes

The TMS370Cx6x has four operating modes, two basic modes with each mode having two memory configurations. The basic operating modes are the microcomputer and microprocessor modes, which are selected by the voltage level applied to the dedicated MC pin two cycles before $\overline{\text{RESET}}$ goes inactive. The two memory configurations then are selected through software programming of the internal system configuration registers. The four operating modes are the microcomputer single chip, microcomputer with external expansion, microprocessor without internal program memory, and microprocessor with internal program memory. These modes are described in the following list.

- Microcomputer single chip mode:
 - Operates as a self-contained microcomputer with all memory and peripherals on-chip
 - Maximizes the general-purpose I/O capability for real-time control applications
- Microcomputer with external expansion mode:
 - Supports bus expansion to external memory or peripherals, while all on-chip memory (RAM, ROM, EPROM, and data EEPROM) remains active
 - Configures digital I/O ports (ports A, B, C, and D) through software, under control of the associated port control, to become external memory as follows:
 - Port A: 8-bit data memory
 - Port B and Port C: 16-bit address memory
 - Port D: 5-bit control memory (pin not used as function A or B can be configured as I/O)
 - Utilizes the pins available (not used for address, data, or control memory) as general-purpose input/output by programming them individually
 - Lowers the system cost by not requiring an external address/data latch (address memory and data memory are nonmultiplexed)
 - Reduces external interface decode logic by using the precoded chip select outputs that provide direct memory/peripheral chip select or chip enable functions
 - Function A maps up to 24K bytes of external memory into the address space by using $\overline{\text{CSE1}}$ and $\overline{\text{CSH1}}$ as memory-bank selects under software control.
 - Function B maps up to 24K bytes of external memory into the address space by using $\overline{\text{EDS}}$ under software control.
- Microprocessor without internal program memory mode:
 - Ports A, B, C, and D (these ports are not programmable) become the address, data, and control buses for interface to external memory and peripherals.
 - On-chip RAM and data EEPROM remain active, while the on-chip ROM or EPROM is disabled.
 - Program area and the reset, interrupt, and trap vectors are located in off-chip memory locations.
- Microprocessor with internal program memory mode:
 - Configured as the microprocessor without internal program memory mode with respect to the external bus interface
 - Application program in external memory enables the internal program ROM or EPROM to be active in the system. (Writing a zero to the MEMORY DISABLED control bit (SCCR1.2) of the SCCR1 control register accomplishes this.)

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memory/peripheral wait operation

The TMS370Cx6x enhances interface flexibility by providing $\overline{\text{WAIT}}$ -state support, decoupling the cycle time of the CPU from the read/write access of the external memory or peripherals. External devices can extend the read/write accesses indefinitely by placing an active low on the $\overline{\text{WAIT}}$ input pin. The CPU continues to wait as long as $\overline{\text{WAIT}}$ remains active.

Programmable automatic wait-state generation also is provided by the TMS370Cx6x on-chip bus controller. Following a hardware reset, the TMS370Cx6x is configured to add one wait state to all external bus transactions and memory and peripheral accesses, thus making every external access a minimum of three system clock cycles. The designer can disable the automatic wait-state generation if the AUTOWAIT DISABLE bit in SCCR1 is set to 1. Also, all accesses to the upper four frames of the peripheral file can be extended independently to four system clock cycles if the PF AUTO WAIT bit in SCCR0 is set to one. Programmable wait states can be used in conjunction with the external $\overline{\text{WAIT}}$ pin. In applications where the external device read/write access can interface with the TMS370Cx6x CPU using one wait state, the automatic wait-state generation can eliminate external $\overline{\text{WAIT}}$ interface logic, lowering system cost.



CPU

The CPU used on TMS370Cx6x devices is the high-performance 8-bit TMS370 CPU module. The 'x6x implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'x6x instruction set is summarized in Table 22. Figure 1 illustrates the CPU registers and memory blocks.

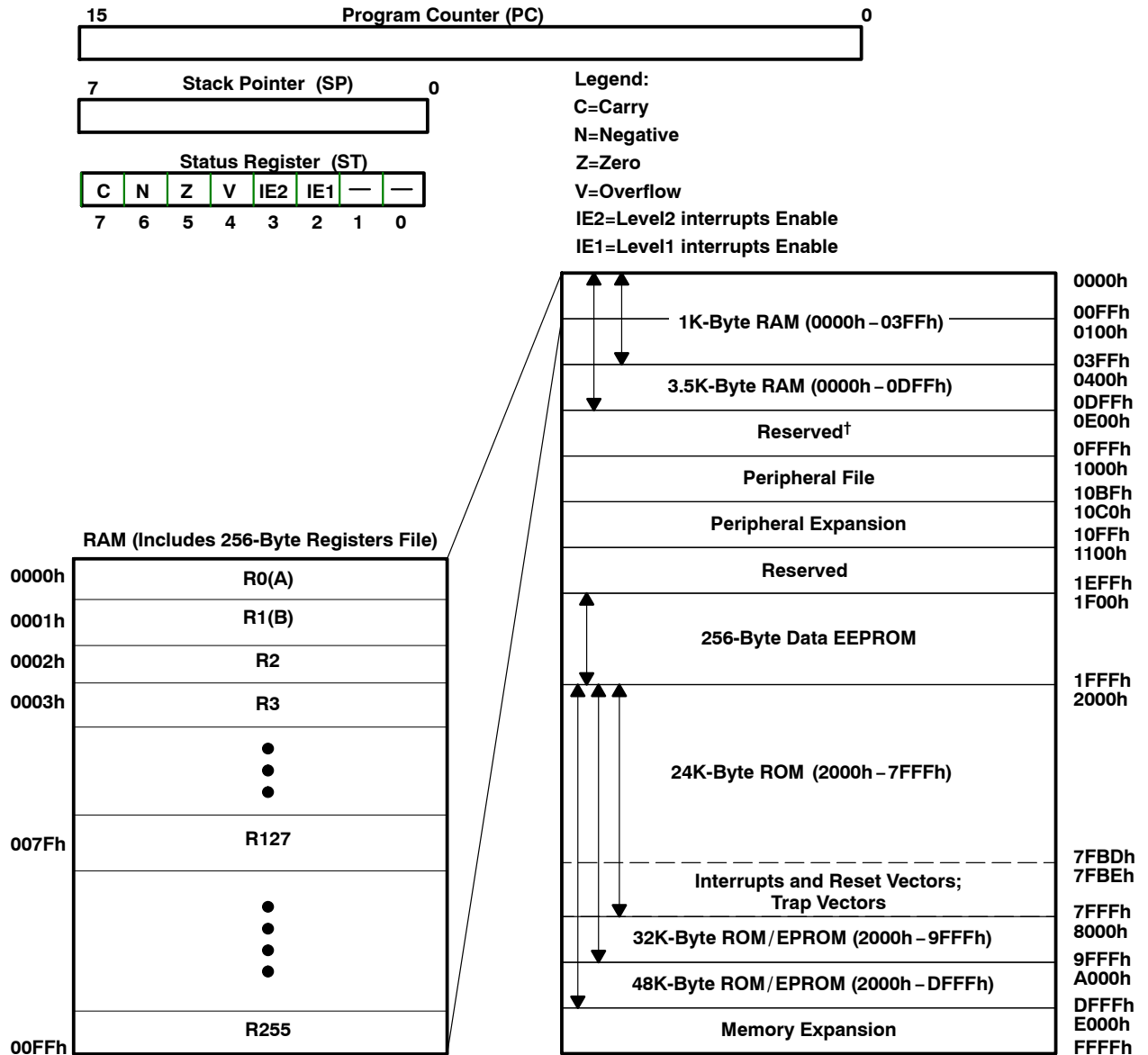


Figure 1. Programmer's Model

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CPU (continued)

The 'x6x CPU architecture provides the following components:

- CPU registers:
 - A stack pointer that points to the last entry in the memory stack
 - A status register that monitors the operation of the instructions and contains the global-interrupt-enable bits
 - A program counter (PC) that points to the memory location of the next instruction to be executed
- A memory map that includes :
 - 1K- or 3.5K-byte general-purpose RAM that can be used for data-memory storage, program instructions, general-purpose register, or the stack (can be located only in the first 256 bytes)
 - A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM/EPROM programming control
 - 256-byte EEPROM module that provides in-circuit programmability and data retention in power-off conditions
 - 24K-, 32K-, or 48K-byte ROM or 32K-, or 48K-byte EPROM program memory

stack pointer (SP)

The SP is an 8-bit CPU register. The stack operates as a last-in, first-out, read/write memory. The stack is used typically to store the return address on subroutine calls as well as the status-register contents during interrupt sequences.

The SP points to the last entry or to the top of the stack. The SP increments automatically before data is pushed onto the stack and decrements after data is popped from the stack. The stack can be located only in the first 256 bytes of the on-chip RAM memory.

status register (ST)

The ST monitors the operation of the instructions and contains the global-interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits:

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional-jump instructions) use these status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

The ST register, status bit notation, and status bit definitions are shown in Table 4.

Table 4. Status Registers

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset



CPU (continued)

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most-significant byte (MSbyte) and least-significant byte (LSbyte) of a 16-bit address.

The contents of the reset vector (7FFEh, 7FFFh) are loaded into the program counter during reset. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 6000h as the contents of memory locations 7FFEh and 7FFFh (reset vector).

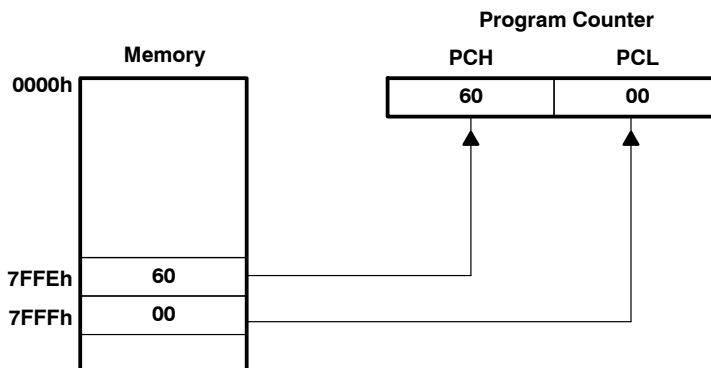


Figure 2. Program Counter After Reset

memory map

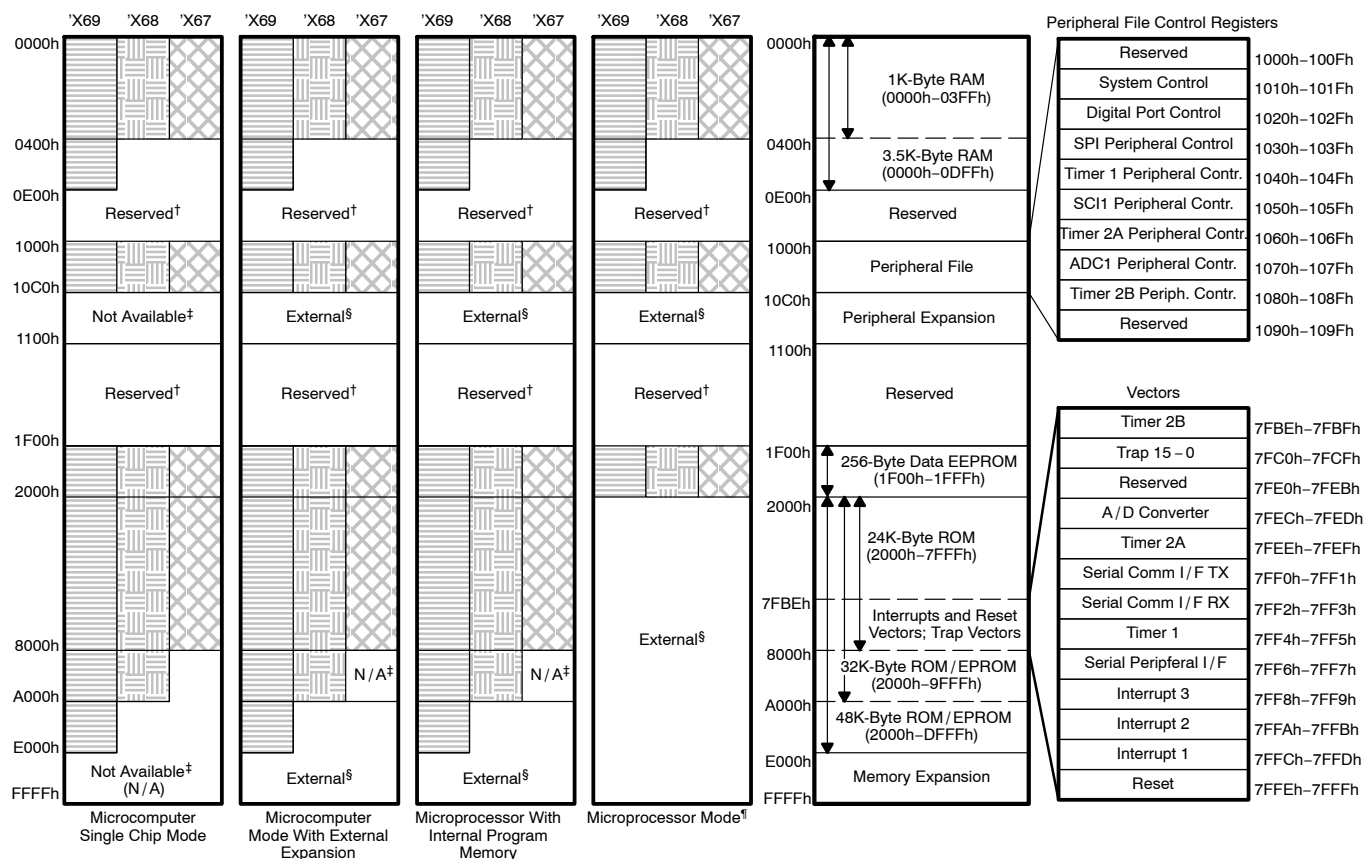
The TMS370Cx6x architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. In the expansion mode, external memory peripherals are also memory-mapped into this common address. As shown in Figure 3, the TMS370Cx6x provides a 16 bit-address range to access internal or external RAM, ROM, data EEPROM, EPROM input/output pins, peripheral functions, and system-interrupt vectors.

The peripheral file contains all input/output port control, on- and off-chip peripheral status and control, EPROM, EEPROM programming, and system-wide control functions. The peripheral file consists of 256 contiguous addresses located from 1000h to 10FFh. The 256 contiguous addresses are logically divided into 16 peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed. The TMS370Cx6x has its on-chip peripherals and system control assigned to peripheral file frames 1 through 8, addresses 1010h through 108Fh.

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memory map (continued)



† Reserved = the address space is reserved for future expansion.

‡ Not available (N/A) = address space is unavailable in the mode illustrated.

§ Precoded chip select outputs available on external expansion bus.

¶ Microprocessor mode is designed for ROM-less devices. ROM and EPROM devices also can be used in this mode, but all on-chip memory is ignored.

Figure 3. TMS370Cx6x Memory Map

RAM/register file (RF)

Locations within RAM address space can serve as either register file or general-purpose read/write memory, program memory, or stack instructions. The TMS370Cx67 and TMS370Cx68 devices contain 1K bytes of internal RAM, mapped beginning at location 0000h and continuing through location 03FFh, which is shown in Table 5 along with 'x69 devices.

Table 5. RAM Memory Map

	'x67 and 'x68	'x69
RAM Size	1K Bytes	3.5K Bytes
Memory Mapped	0000h – 03FFh	0000h – 0DFFh

The first 256 bytes of RAM (0000h – 00FFh) are register files, R0 through R255 (see Figure 1). The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370Cx6x control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or by P for a decimal designator. For example, the system control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 6 lists the TMS370Cx6x peripheral files.

Table 6. TMS370Cx6x Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h – 100Fh	P000 – P00F	Reserved for factory test
1010h – 101Fh	P010 – P01F	System and EEPROM/EPROM control registers
1020h – 102Fh	P020 – P02F	Digital I/O port control registers
1030h – 103Fh	P030 – P03F	Serial peripheral interface registers
1040h – 104Fh	P040 – P04F	Timer 1 registers
1050h – 105Fh	P050 – P05F	Serial communication interface 1 registers
1060h – 106Fh	P060 – P06F	Timer 2A registers
1070h – 107Fh	P070 – P07F	Analog-to-digital converter 1 registers
1080h – 108Fh	P080 – P08F	Timer 2B registers
1090h – 10BFh	P090 – P0BF	Reserved
10C0h – 10FFh	P0C0 – P0FF	External peripheral control

data EEPROM

The TMS370Cx6x devices contain 256 bytes of data EEPROM, and the memory is mapped beginning at location 1F00h and continuing through location 1FFFh.

Writing to the data EEPROM module is controlled by the data-EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Data Manual* (SPNS014B). The data EEPROM features include the following:

- Programming:
 - Bit, byte, and block write/erase modes

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data EEPROM (continued)

- Internal charge pump circuitry. No external EEPROM programming voltage supply is needed.
- Control register: Data EEPROM programming is controlled by the data EEPROM control register (DEECTL) located in the PF frame beginning at location P01A.
- In-circuit programming capability: There is no need to remove the device to program it.
- Write-protection: Writes to the data EEPROM are disabled during the following conditions:
 - Reset: All programming of the data EEPROM module is halted.
 - Write protection active: there is one write-protect bit per 32-byte EEPROM block.
 - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 7 shows the memory map of the control registers.

Table 7. Data EEPROM and Program EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME [†]
P014	EPCTLH	Program EPROM control register – high array
P015 – P016		Reserved
P017	INT1	External interrupt 1 control register
P018	INT2	External interrupt 2 control register
P019	INT3	External interrupt 3 control register
P01A	DEECTL	Data EEPROM control register
P01B		Reserved
P01C	EPCTLM	Program EPROM control register – middle array
P01D		Reserved
P01E	EPCTLL	Program EPROM control register – low array

[†] For the 24K- and 32K-byte EPROM device, the program memory is controlled by P01C and P01E; for the 48K-byte EPROM device, the program memory is controlled by P014, P01C, and P01E.

program EPROM

The '370C767 program EPROM consists of 24K bytes that are made up of one 16K-byte array and one 8K-byte array of EPROM; the 16K-byte array is located at address locations 2000h through 5FFFh, and the 8K-byte array is located at address locations 6000h through 7FFFh. The '370C768 program EPROM consists of 32K bytes that are made up of two 16K-byte arrays of EPROM; the first 16K-byte array is located at address locations 2000h through 5FFFh, and the second 16K-byte array is located at address locations 6000h through 9FFFh. The '370C769 program EPROM consists of 48K bytes that are made up of three 16K-byte arrays of EPROM; the first 16K-byte array is located at address locations 2000h through 5FFFh, the second 16K-byte array is located at address locations 6000h through 9FFFh, the third 16K-byte array is located at address locations A000h through DFFFh as shown in Table 8.



program EPROM (continued)

Table 8. EPROM Memory Map

	'767		'768		'769		
EPROM size	24K Bytes		32K Bytes		48K Bytes		
Memory mapped	16K 2000h–5FFFh	8K 6000h–7FFFh	First 16K 2000h–5FFFh	Second 16K 6000h–9FFFh	First 16K 2000h–5FFFh	Second 16K 6000h–9FFFh	Third 16K A000h–DFFFh
Control registers	EPCTLL P01E	EPCTLM P01C	EPCTLL P01E	EPCTLM P01C	EPCTLL P01E	EPCTLM P01C	EPCTLH P014

The EPROM memory map in Table 8 expresses the following:

- For the 24K-byte EPROM, the 16K-byte array is controlled by EPCTLL register, located at 101Eh (P01E); the 8K-byte array is controlled by EPCTLM register, located at 101Ch (P01C).
- For the 32K-byte EPROM, the first 16K-byte array is controlled by EPCTLL register, located at 101Eh (P01E); the second 16K-byte array is controlled by EPCTLM register, located at 101Ch (P01C).
- For the 48K-bytes EPROM, the first 16K-byte array is controlled by EPCTLL register, located at 101Eh (P01E); the second 16K-byte array is controlled by EPCTLM register, located at 101Ch (P01C); the third 16K-byte array is controlled by EPCTLH register, located at 1014h (P014).

Reading the program-EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the EPCTL. The program EPROM modules' features include:

- Programming
 - In-circuit programming capability if V_{PP} is applied to MC
 - Control register: Program EPROM programming is controlled by the program EPROM control registers (EPCTLL, EPCTLM, and EPCTLH) located in the PF frame as shown in Table 7.
 - Programming one EPROM module while executing the other
- Write protection: Writes to the program EPROM are disabled under the following conditions:
 - Reset: All programming to the EPROM module is halted.
 - Low-power modes
 - 13 V not applied to MC

program ROM

The program ROM consists of 24K, 32K or 48K bytes of mask-programmable ROM. The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication. Table 9 shows the program ROM memory map.

Table 9. ROM Memory Map[†]

	'067	'068	'069
ROM Size	24K Bytes	32K Bytes	48K Bytes
Memory Mapped	2000h – 7FFFh	2000h – 9FFFh	2000h – DFFFh

[†] Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments Incorporated. Memory addresses 7FBEh through 7FBFh and 7FECb through 7FFFh are reserved for interrupts and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located at addresses 7FC0h and 7FCFh.

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system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx6x CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are internally generated, while one ($\overline{\text{RESET}}$) is controlled externally. These actions are as follows:

- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside the recommended operating range. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B) for more information.
- External $\overline{\text{RESET}}$ Pin. A low level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x6x device to reset external system components. Additionally, if a cold start (V_{CC} is off for several hundred milliseconds) condition or oscillator failure occurs or $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator fault flag (OSC FLT FLAG, SCCR0.4), the cold start flag (COLD START, SCCR0.7) and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 10 lists the reset sources.

Table 10. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Registers A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to by the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state. During $\overline{\text{RESET}}$, the two basic operating modes which are the microcomputer and microprocessor modes can be selected by applying the desired voltage level to the dedicated MC pin two cycles before $\overline{\text{RESET}}$ goes inactive. See the mode section for operating modes description.

$\overline{\text{RESET}}$ must be held low until the clock signal is valid and V_{CC} is within the operating range, when an external reset circuit is connected to $\overline{\text{RESET}}$. Figure 4 shows a typical reset circuit.



system reset (continued)

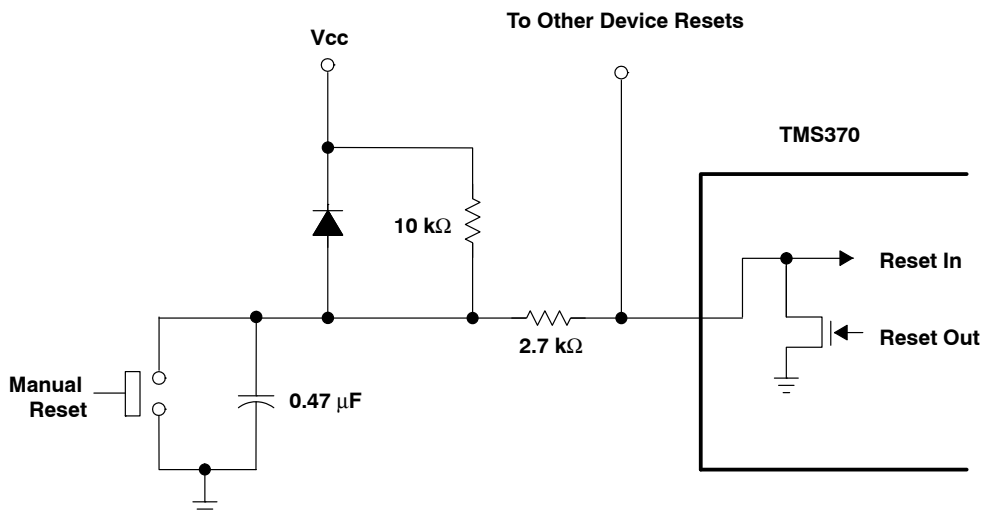


Figure 4. Typical Reset Circuit

interrupts

The TMS370 family software programmable interrupt structure permits flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be independently masked by the global-interrupt mask bits (IE1 and IE2) of the status register.

Each system interrupt is independently configured to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is selectively configured on either the high-or-low priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx6x has ten hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 11. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. A system interrupt can have multiple interrupt sources (e.g., SCI RXINT has two interrupt sources). All of the interrupt sources are individually maskable by local interrupt-enable control bits in the associated PF. Each interrupt source FLAG bit is individually readable for software polling or to determine which interrupt source generated the associated system interrupt. Interrupt control block diagram is illustrated in Figure 5.

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interrupts (continued)

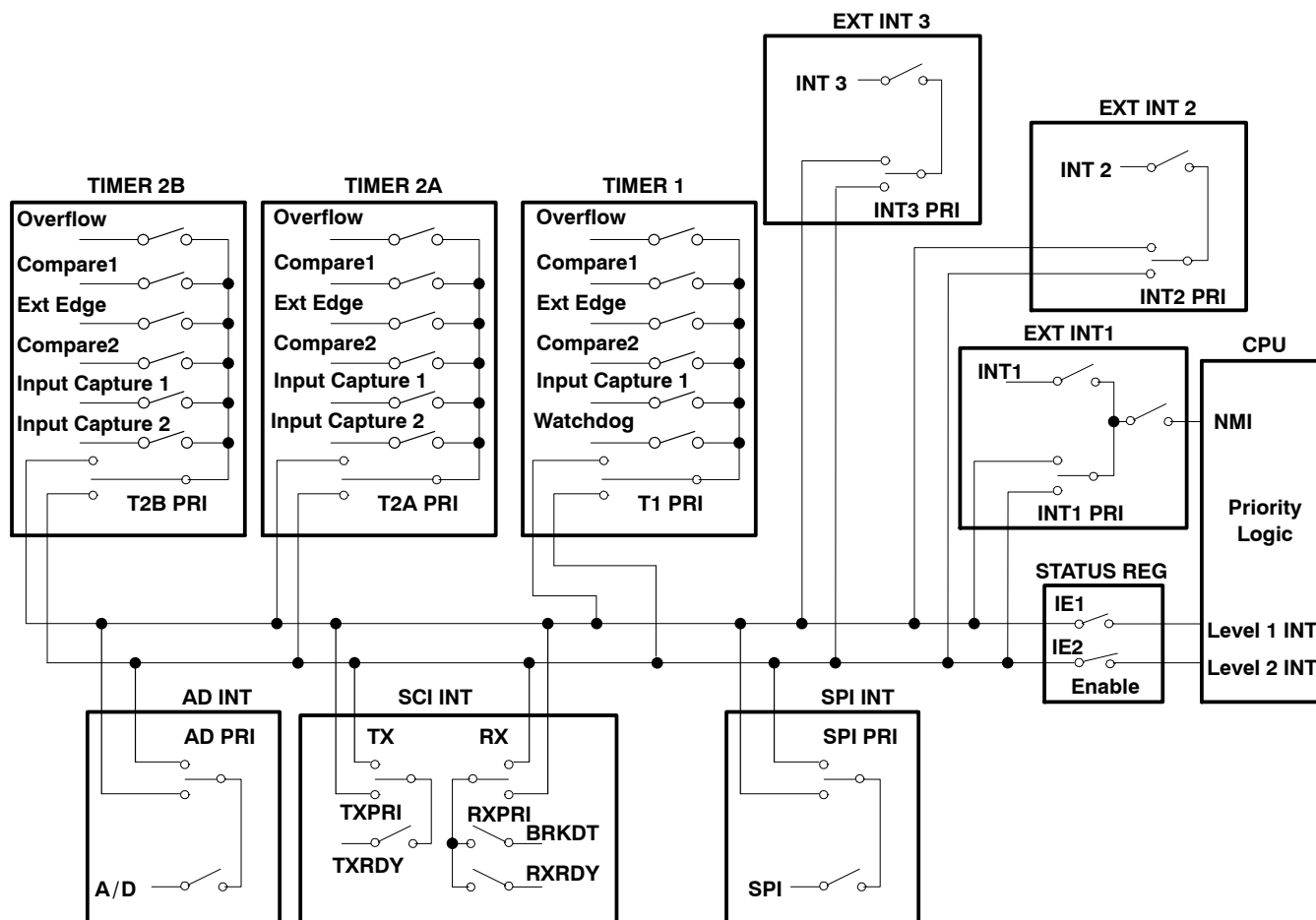


Figure 5. Interrupt Control

Seven of the system interrupts are generated by on-chip peripheral functions, and three external interrupts are supported. Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in PF frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as nonmaskable, it cannot be masked by the individual- or global-enable-mask bits. Recall that the INT1 NMI bit is protected during non-privileged operation and therefore should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software configured as general-purpose input/output pins if the interrupt function is not required (INT1 can be similarly configured as an input pin). Table 11 shows the interrupt-vector sources, corresponding addresses, and hardware priorities.

interrupts (continued)

Table 11. Hardware-System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY [†]
External RESET Watchdog overflow Oscillator fault detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	RESET [‡]	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1 [‡]	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2 [‡]	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3 [‡]	7FF8h, 7FF9h	4
SPI RX/TX complete	SPI INT FLAG	SPIINT	7FF6h, 7FF7h	5
Timer 1 overflow Timer 1 compare 1 Timer 1 compare 2 Timer 1 external edge Timer 1 input capture 1 Watchdog overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT [§]	7FF4h, 7FF5h	6
SCI RX data register full SCI RX break detect	RXRDY FLAG BRKDT FLAG	RXINT [‡]	7FF2h, 7FF3h	7
SCI TX data register empty	TXRDY FLAG	TXINT	7FF0h, 7FF1h	8
Timer 2A overflow Timer 2A compare 1 Timer 2A compare 2 Timer 2A external edge Timer 2A input capture 1 Timer 2A input capture 2	T2A OVRFL INT FLAG T2AC1 INT FLAG T2AC2 INT FLAG T2AEDGE INT FLAG T2AIC1 INT FLAG T2AIC2 INT FLAG	T2AINT	7FEEh, 7FEFh	9
ADC1 conversion complete	AD INT FLAG	ADINT	7FECh, 7FEDh	10
Timer 2B overflow Timer 2B compare 1 Timer 2B compare 2 Timer 2B external edge Timer 2B input capture 1 Timer 2B input capture 2	T2B OVRFL INT FLAG T2BC1 INT FLAG T2BC2 INT FLAG T2BEDGE INT FLAG T2BIC1 INT FLAG T2BIC2 INT FLAG	T2BINT	7FBEh, 7FBFh	11

[†] Relative priority within an interrupt level

[‡] Release microcontroller from STANDBY and HALT low-power modes

[§] Release microcontroller from STANDBY low-power mode

privileged operation and EEPROM write-protection override

The TMS370Cx6x family has significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a broad variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx6x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) should be set to 1 to enter the nonprivileged mode, disabling write operations to specific configuration control bits within the peripheral file. Table 12 lists the system configuration bits that are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

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privileged operation and EEPROM write-protection override (continued)

Table 12. Privileged Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCRO	P010.5 P010.6	PF AUTOWAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
SPIPRI	P03F.5 P03F.6 P03F.7	SPI ESPEN SPI PRIORITY SPI STEST
SCIPRI	P05F.4 P05F.5 P05F.6 P05F.7	SCI ESPEN SCIRX PRIORITY SCITX PRIORITY SCI STEST
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST
T2APRI	P06F.6 P06F.7	T2A PRIORITY T2A STEST
ADPRI	P07F.5 P07F.6 P07F.7	AD ESPEN AD PRIORITY AD STEST
T2BPRI	P08F.6 P08F.7	T2B PRIORITY T2B STEST

† The privileged bits are shown in a bold typeface in Table 14.

The write-protect override (WPO) mode provides an external hardware method of overriding the write-protection registers of data EEPROM on the TMS370Cx6x. The WPO mode is entered by applying a 12-V input to MC after RESET input goes high (logic 1). The high voltage on MC during the WPO mode is not the programming voltage for the data EEPROM or program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware system-level capability to modify the content of the data EEPROM while the device remains in the application but only while requiring a 12-V external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power and IDLE modes

The TMS370Cx6x devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time when the mask is manufactured.

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls which low-power mode is entered.



low-power and IDLE modes (continued)

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, timer 1, and the receive start-bit detection circuit of the serial communications interface remain active. System processing is suspended until a qualified interrupt (hardware RESET, external interrupt on INT1, INT2, INT3, timer 1 interrupt, or low level on the receive pin of the serial communications interface) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx6x is placed in its lowest power-consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware RESET, external interrupt on the INT1, INT2, INT3, or low level on the receive pin of the serial communications interface) is detected. The low-power mode selection bits are summarized in Table 13.

Table 13. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X	IDLE

X = don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6–7 bits is ignored. In addition, if an idle instruction executes when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method of always exiting low-power modes for mask-ROM devices, INT1 is automatically enabled as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI always is generated, regardless of the interrupt-enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the watchdog timer is inhibited.

clock modules

The 'x6x family provides two clock options which are referred to as divide-by-1 (PLL) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The 'x6x ROM-masked devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device. An EPROM has only the divide-by-1.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a 1-to-1 match between the external resonator frequency and the internal system clock (SYSCLK) frequency. The divide-by-4 produces a SYSCLK which is one-fourth the frequency of the external resonator. Inside the divide-by-1 module, the frequency of the external resonator is multiplied by four. The clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. The frequencies are formulated as follows

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clock modules (continued)

$$\text{Divide-by-4 option : SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option : SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the improved EMI performance. The harmonics of low-speed resonators extend through less of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 provides the capability of reducing the resonator speed by four times, and this results in a steeper decay of emissions produced by the oscillator.

system configuration registers

Table 14 contains system configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in bold typeface and shaded.

Table 14. Peripheral File Frame 1: System Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTOWAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013	Reserved								
P014	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLH
P015 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLM
P01D	Reserved								
P01E	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLL
P01F	Reserved								

digital port control

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 15 lists the specific addresses, registers, and control bits within this peripheral file frame.

Table 15. Peripheral File Frame 2: Digital Port Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P020	Reserved								APORT1
P021	Port A Control Register 2								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	Port B Control Register 2								BPORT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPORT1
P029	Port C Control Register 2								CPORT2
P02A	Port C Data								CDATA
P02B	Port C Direction								CDIR
P02C	Port D Control Register 1					—	—	—	DPORT1
P02D	Port D Control Register 2 [†]					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 16. Port Configuration Register Setup

PORT	PIN	INPUT	OUTPUT	FUNCTION A	FUNCTION B (μP MODE)
		XPORT1 = 0 [†] XPORT2 = 0 XDATA = y XDIR = 0	XPORT1 = 0 [†] XPORT2 = 0 XDATA = q XDIR = 1	XPORT1 = 0 [†] XPORT2 = 1 XDATA = x XDIR = x	XPORT1 = 1 [†] XPORT2 = 1 XDATA = x XDIR = x
A	0–7	Data In y	Data Out q	Data Bus	Reserved
B	0–7	Data In y	Data Out q	Low ADDR	Reserved
C	0–7	Data In y	Data Out q	Hi ADDR	Reserved
D	3	Data In y	Data Out q	SYSCLK	SYSCLK
	4			R/W	R/W
	5			CSPF	—
	6			CSH1	EDS
	7			CSE1	WAIT
XPORT1 = 1 XPORT2 = 0 XDATA = x XDIR = x } Not defined					

[†] DPORT only

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timer 1 module

The programmable timer 1 (T1) module of the TMS370Cx6x provides the designer with the enhanced timer resources required to perform real-time system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers (T1 and WD) allow program selection of input clock sources (real-time, external-event, or pulse-accumulate) with multiple 16-bit registers (input-capture and compare) for special timer function control. The T1 module includes three external device pins that can be used for multiple counter functions (operation mode dependent) or used as general-purpose I/O pins. The T1 module is shown in Figure 6.

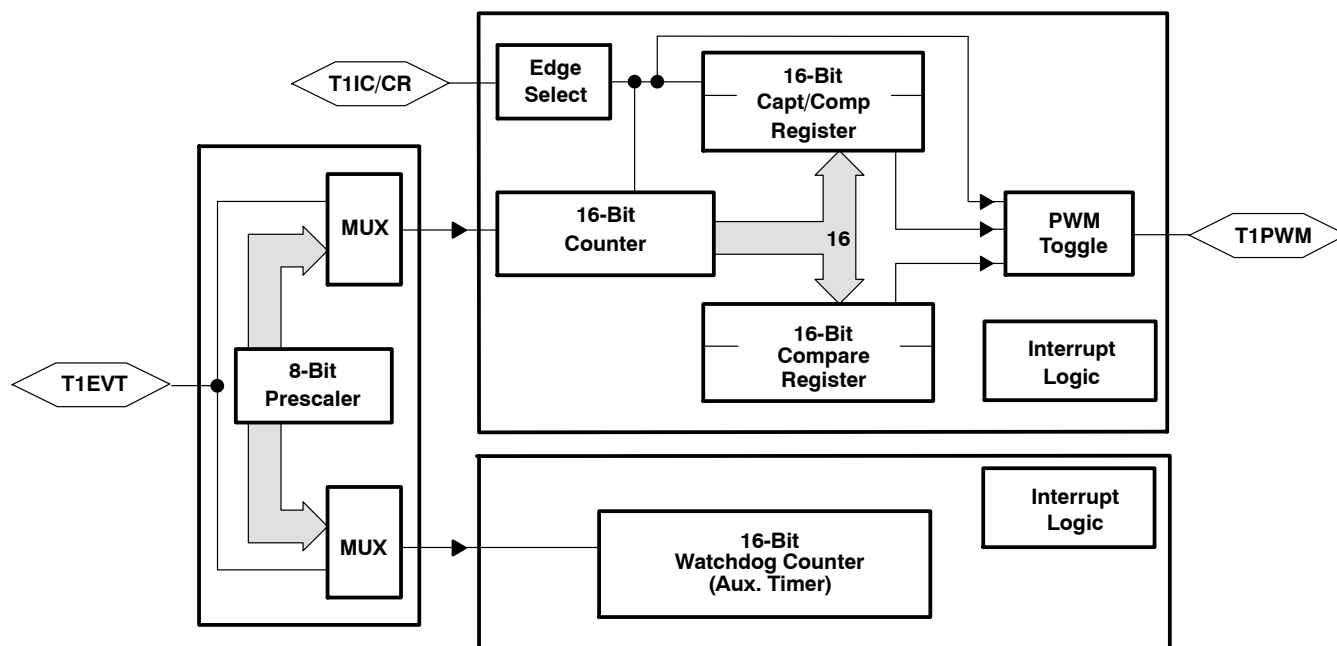


Figure 6. Timer 1 Block Diagram

- Three T1 I/O pins
 - T1IC/CR: Timer 1 input capture/counter reset input pin, or general-purpose bidirectional I/O pin
 - T1PWM: Timer 1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T1EVT: Timer 1 event input pin, or general-purpose bidirectional I/O pin
- Two operation modes:
 - Dual-compare mode: Provides PWM signal
 - Capture/compare mode: Provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either capture or compare register
- One 16-bit watchdog counter can be used as an event counter, a pulse accumulator, or an interval timer if watchdog feature is not needed.
- Prescaler/clock sources that determine one of eight clock sources for general-purpose timer

timer 1 module (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR)
- Interrupts that can be generated on the occurrence of:
 - A capture
 - A compare equal
 - A counter overflow
 - An external edge detection
- Sixteen T1 module control registers: Located in the PF frame beginning at address P040

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timer 1 module (continued)

Table 17 shows the T1 module control register memory map.

Table 17. Timer 1 Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Dual-Compare and Capture/Compare									
P040	Bit 15			T1 Counter MSbyte				Bit 8	T1CNTR
P041	Bit 7			T1 Counter LSbyte				Bit 0	
P042	Bit 15			Compare Register MSbyte				Bit 8	T1C
P043	Bit 7			Compare Register LSbyte				Bit 0	
P044	Bit 15			Capture/Compare Register MSbyte				Bit 8	T1CC
P045	Bit 7			Capture/Compare Register LSbyte				Bit 0	
P046	Bit 15			Watchdog Counter MSbyte				Bit 8	WDCNTR
P047	Bit 7			Watchdog Counter LSbyte				Bit 0	
P048	Bit 15			Watchdog Reset Key				Bit 0	WDRST
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

The timer 1 capture/compare mode block diagram is illustrated in Figure 7. The annotations in Figure 7 identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL0 is 104Ah, bit 0, in the T1CTL2 register.



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timer 1 module (continued)

The timer 1 dual-compare mode block diagram is illustrated in Figure 8. The annotations in Figure 8 identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

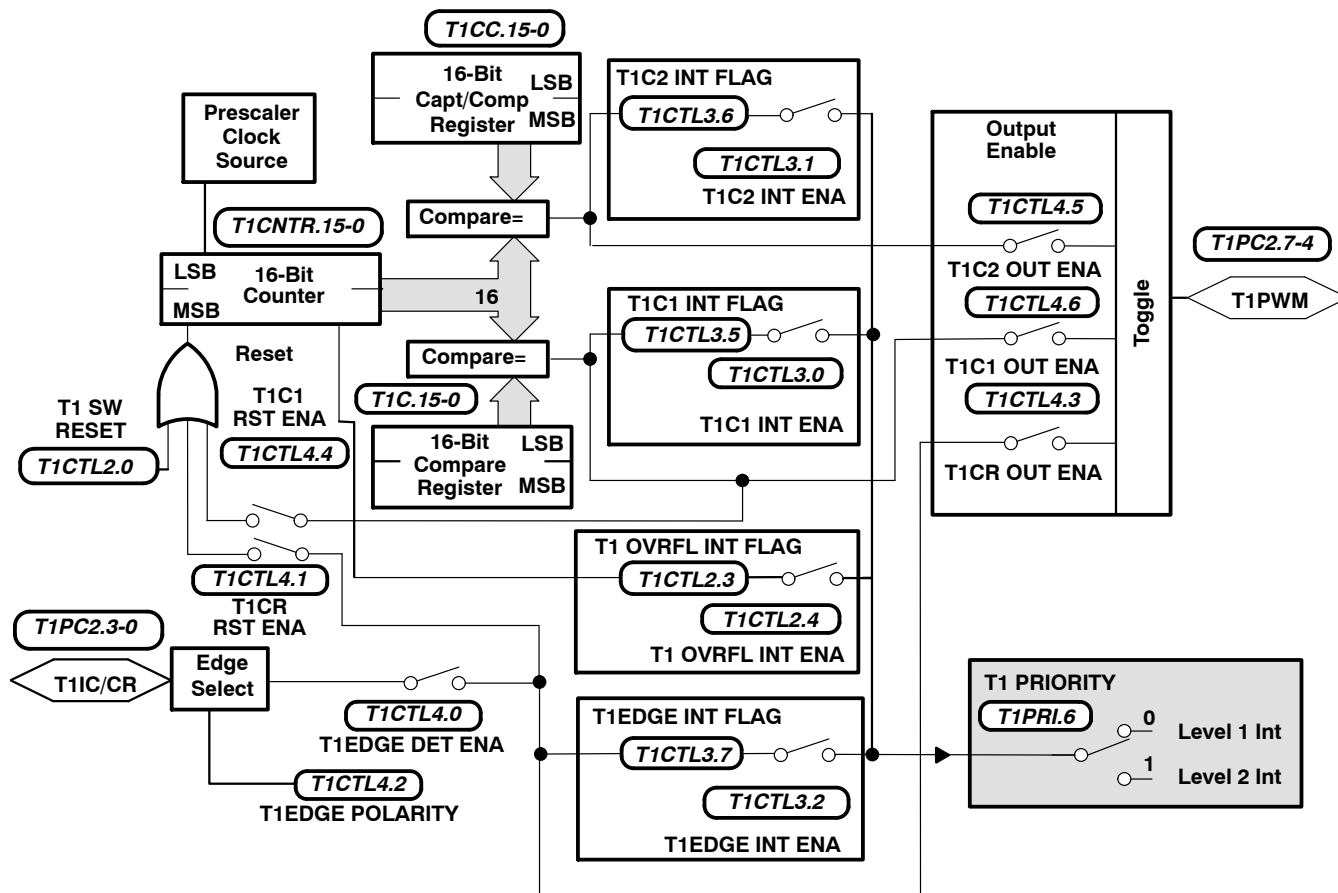


Figure 8. Dual-Compare Mode

timer 1 module (continued)

The TMS370Cx6x device includes a 24-bit watchdog (WD) timer, contained in the T1 module, which can be software programmed as an event counter, pulse accumulator, or interval timer if the watchdog function is not desired. The WD function is to monitor software and hardware operation and to implement a system reset when the WD counter is not serviced properly (WD counter overflow or WD counter is reinitialized by an incorrect value). The WD can be configured as one of three mask options: standard watchdog, hard watchdog, or simple counter.

- Standard watchdog configuration (see Figure 9) – for '76xA EPROM and mask-ROM devices
 - Watchdog mode
 - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows
 - A watchdog overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
 - Non-watchdog mode
 - Watchdog timer can be configured as an event counter, pulse accumulator, or an interval timer.

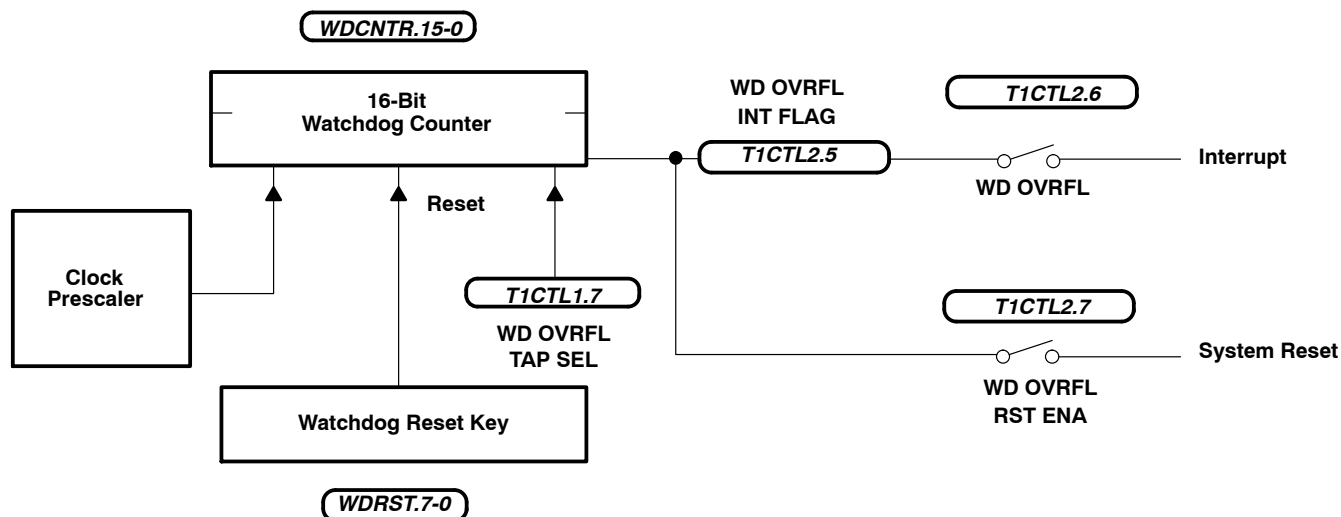


Figure 9. Standard Watchdog

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timer 1 module (continued)

- Hard watchdog configuration (see Figure 10) – for mask-ROM devices
 - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows
 - Automatic activation of the WD timer upon power-up reset
 - INT1 is enabled as nonmaskable interrupt during low-power modes
 - A watchdog overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset

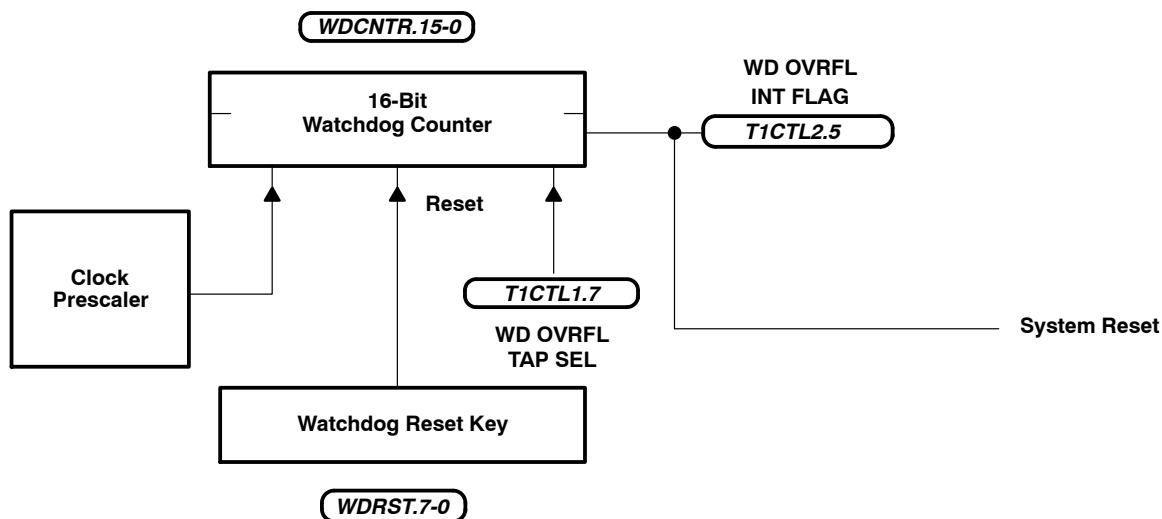


Figure 10. Hard Watchdog

timer 1 module (continued)

- Simple-counter configuration (see Figure 11) – for mask-ROM devices only
 - Simple counter can be configured as an event counter, pulse accumulator, or an interval timer

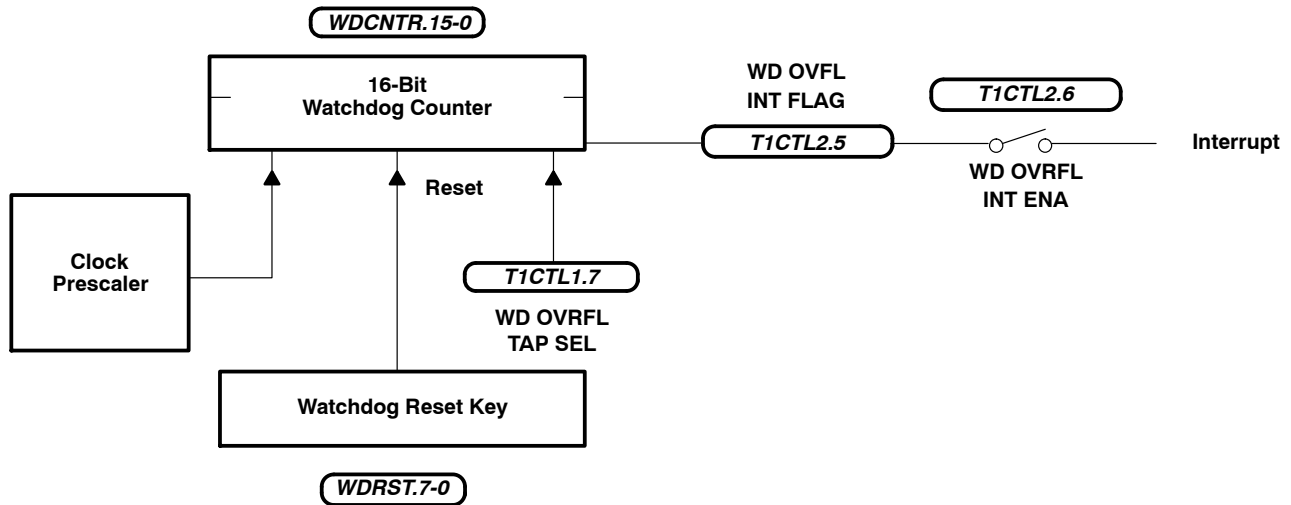


Figure 11. Simple Counter

timer 2n modules (T2A and T2B)

The TMS370Cx6x device includes two 16-bit general-purpose timer 2 modules (T2A and T2B). The T2A or T2B are referred to as T2n throughout this section. The T2n module contains a 16-bit resettable counter, 16-bit compare register with associated compare logic, 16-bit capture register, and a 16-bit register that functions as a capture register in one mode and as a compare register in the other mode. The T2n module adds additional timers that provide event counts, input captures, and compare functions. The T2n module includes three external-device pins that can be dedicated as timer functions or used as general-purpose I/O pins. The T2n module is shown in Figure 12.

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timer 2n modules (T2A and T2B) (continued)

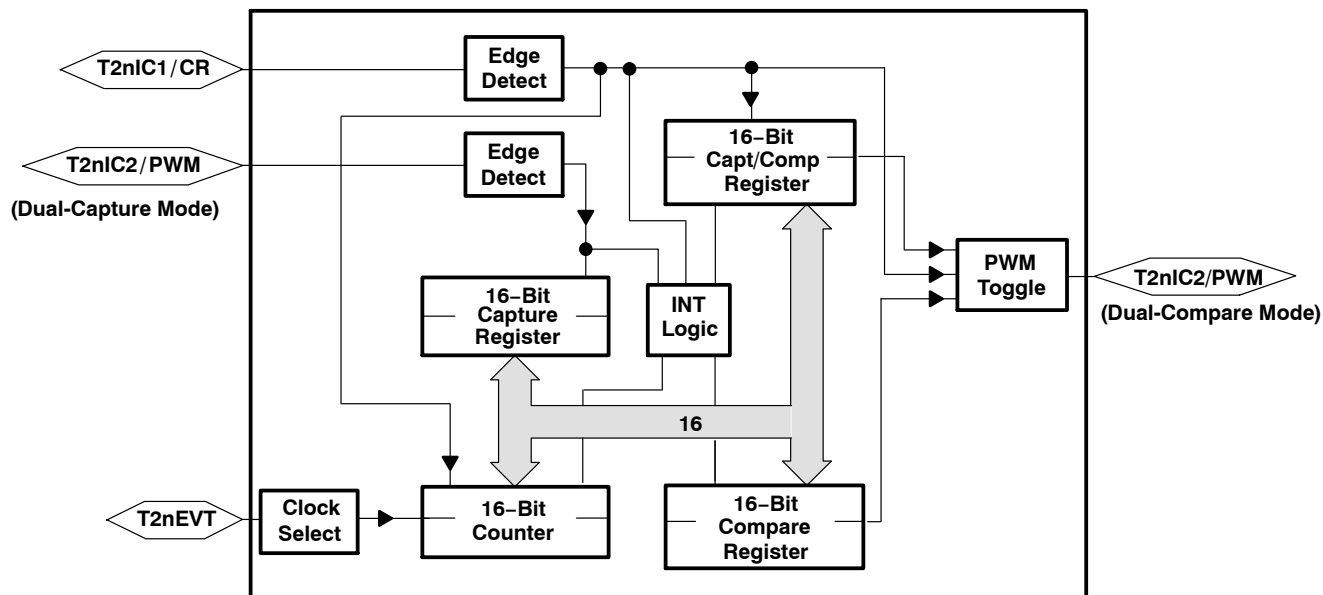


Figure 12. Timer 2n Block Diagram

The T2n module features include the following:

- Three T2A I/O pins
 - T2nIC1/CR: Timer 2n input capture 1 /counter-reset input pin, or general-purpose bidirectional I/O pin
 - T2nIC2/PWM: Timer 2n input capture 2/pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T2nEVT: Timer 2n event-input pin, or general-purpose bidirection I/O pin
- Two operation modes:
 - Dual-compare mode: Provides PWM signal
 - Dual-capture mode: Provides input-capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture register with associated capture logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either capture or compare registers
- T2n clock sources can be any of the following:
 - System clock
 - No clock (the counter is stopped)
 - External clock synchronized to the system clock (event counter)
 - System clock while external input is high (pulse accumulation)

timer 2n modules (T2A and T2B) (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input-capture pins (T2nIC1/CR)
- Interrupts that can be generated on the occurrence of:
 - A compare equal for dedicated-compare register
 - A compare equal for capture-compare register
 - A counter overflow
 - An external edge 1 detection
 - An external edge 2 detection
- Fourteen control registers for each Timer 2 module: Located in the PF frame beginning at address P060 and P080 for T2A and T2B, respectively.

The timer 2n module control registers are illustrated in Table 18.

Table 18. Timer 2n Module Register Memory Map

PF	PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
		Modes: Dual-Compare and Dual-Capture								
P060	P080	Bit 15				T2n Counter MSbyte			Bit 8	T2nCNTR
P061	P081	Bit 7				T2n Counter LSbyte			Bit 0	
P062	P082	Bit 15				Compare Register MSbyte			Bit 8	T2nC
P063	P083	Bit 7				Compare Register LSbyte			Bit 0	
P064	P084	Bit 15				Capture/Compare Register MSbyte			Bit 8	T2nCC
P065	P085	Bit 7				Capture/Compare Register LSbyte			Bit 0	
P066	P086	Bit 15				Capture Register 2 MSbyte			Bit 8	T2nIC
P067	P087	Bit 7				Capture Register 2 LSbyte			Bit 0	
P06A	P08A	—	—	—	T2n OVRFL INT ENA	T2n OVRFL INT FLAG	T2n INPUT SELECT1	T2n INPUT SELECT0	T2n SW RESET	T2nCTL1
		Mode: Dual-Compare								
P06B	P08B	T2nEDGE1 INT FLAG	T2nC2 INT FLAG	T2nC1 INT FLAG	—	—	T2nEDGE1 INT ENA	T2nC2 INT ENA	T2nC1 INT ENA	T2nCTL2
P06C	P08C	T2n MODE = 0	T2nC1 OUT ENA	T2nC2 OUT ENA	T2nC1 RST ENA	T2nEDGE1 OUT ENA	T2nEDGE1 POLARITY	T2nEDGE1 RST ENA	T2nEDGE1 DET ENA	T2nCTL3
		Mode: Dual-Capture								
P06B	P08B	T2nEDGE1 INT FLAG	T2nEDGE2 INT FLAG	T2nC1 INT FLAG	—	—	T2nEDGE1 INT ENA	T2nEDGE2 INT ENA	T2nC1 INT ENA	T2nCTL2
P06C	P08C	T2n MODE = 1	—	—	T2nC1 RST ENA	T2nEDGE2 POLARITY	T2nEDGE1 POLARITY	T2nEDGE2 DET ENA	T2nEDGE1 DET ENA	T2nCTL3
		Modes: Dual-Compare and Dual-Capture								
P06D	P08D	—	—	—	—	T2nEVT DATA IN	T2nEVT DATA OUT	T2nEVT FUNCTION	T2nEVT DATA DIR	T2nPC1
P06E	P08E	T2nIC2/PWM DATA IN	T2nIC2/PWM DATA OUT	T2nIC2/PWM FUNCTION	T2nIC2/PWM DATA DIR	T2nIC1/CR DATA IN	T2nIC1/CR DATA OUT	T2nIC1/CR FUNCTION	T2nIC1/CR DATA DIR	T2nPC2
P06F	P08F	T2n STEST	T2n PRIORITY	—	—	—	—	—	—	T2nPRI

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timer 2n modules (T2A and T2B) (continued)

The timer 2n dual-compare mode block diagram is illustrated in Figure 13. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2nCTL2.0 is 106Bh (n = A) or 108Bh (n = B), bit 0, in the T2nCTL2 register.

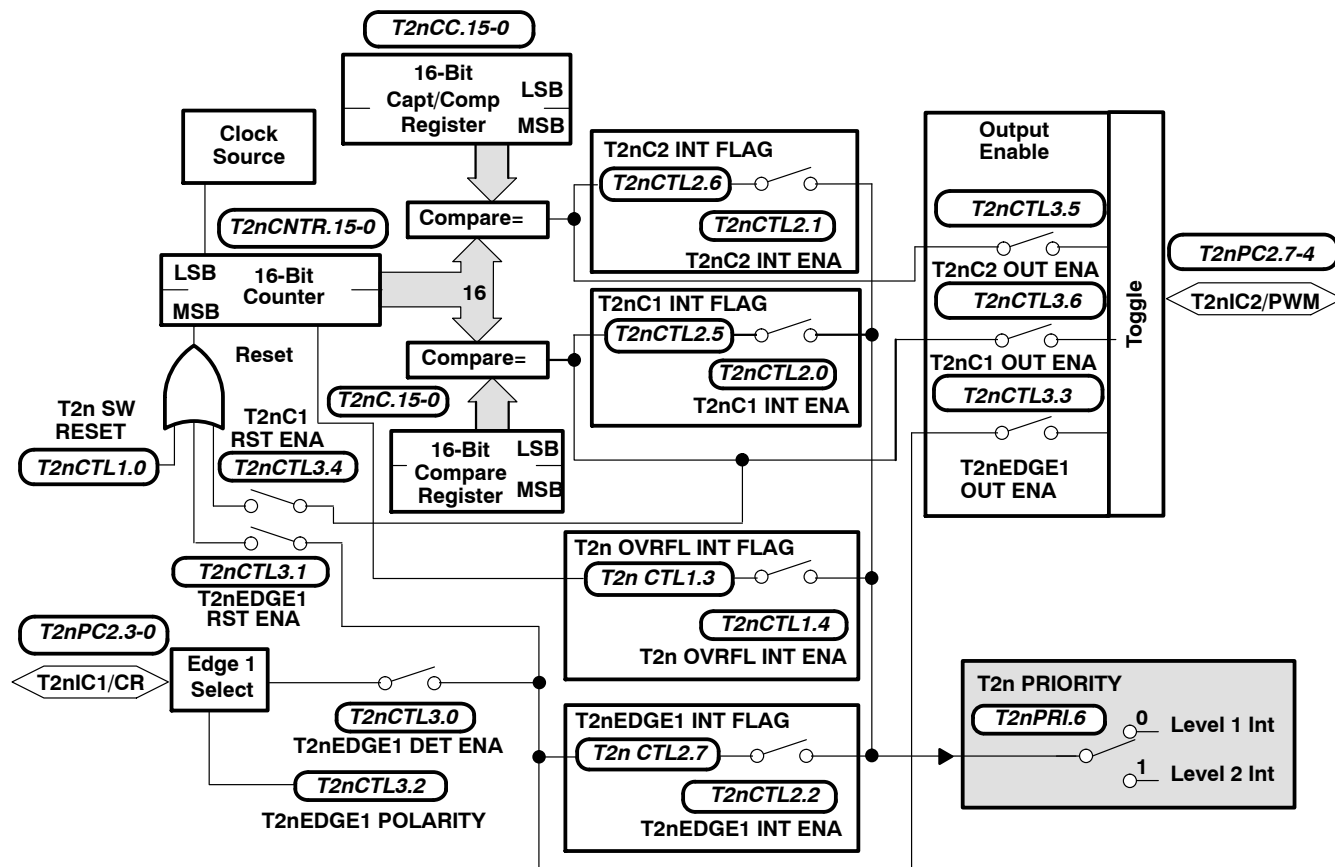


Figure 13. Dual-Compare Mode

The timer 2n dual-capture mode block diagram is illustrated in Figure 14. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2nCTL2.0 is 106Bh (n = A) or 108Bh (n = B), bit 0, in the T2nCTL2 register.



serial peripheral interface (SPI) module

The SPI is a high-speed, synchronous, serial I/O port that allows a serial bit stream of programmed length (1 to 8 bits) to be shifted into and out of the device at a programmable bit-transfer rate. The SPI is used normally for communications between the microcontroller and external peripherals or another microcontroller. Typical applications include external I/O or peripheral expansion using devices such as shift registers, display drivers, and analog-to-digital (A/D) converters. The master/slave operation of the SPI supports multi-device communications. The SPI module features include the following:

- Three external pins:
 - SPISOMI: SPI slave output/master input pin or general-purpose bidirectional I/O pin
 - SPISIMO: SPI slave input/master output pin or general-purpose bidirectional I/O pin
 - SPICLK: SPI serial-clock pin or general-purpose bidirectional I/O pin

- Two operational modes: master and slave

- Baud rate: Eight different programmable rates

- Maximum baud rate in master mode: 2.5M bps at 5-MHz SYSCLK

$$\text{SPI BAUD RATE} = \frac{\text{SYSCLK}}{2 \times 2^b}$$

where b = bit rate in SPICCR.5-3 (range 0–7)

- Maximum baud rate in slave mode: 625K bps at 5-MHz SYSCLK

For maximum slave SPI BAUD RATE < SYSCLK/8

- Data-word format: one to eight data bits
- Simultaneous receiver and transmitter operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Seven SPI module-control registers: located in control register frame beginning at address P030h

serial peripheral interface (SPI) module (continued)

The SPI module control registers are illustrated in Table 19.

Table 19. SPI Module Control Register Memory Map

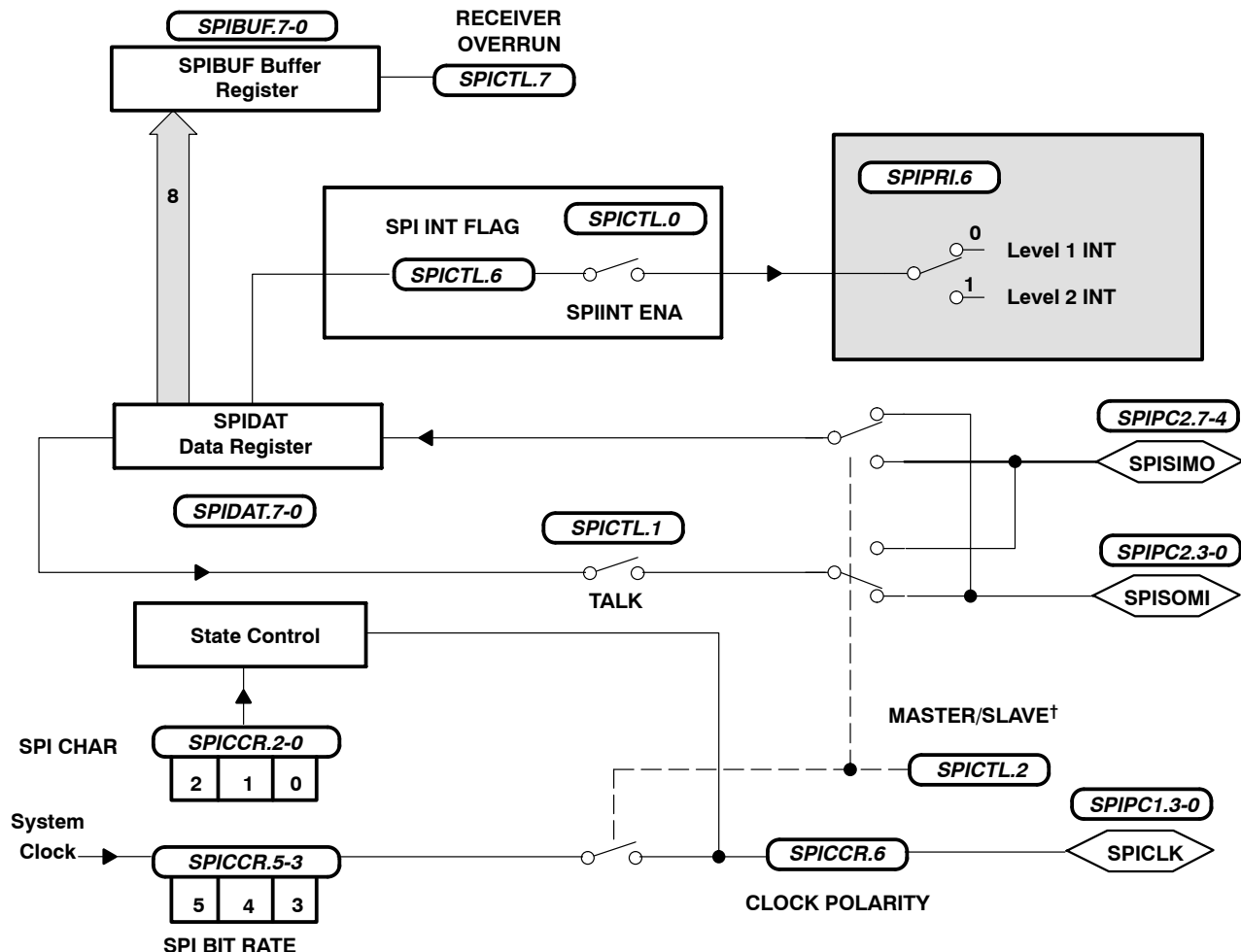
PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/SLAVE	TALK	SPI INT ENA	SPICTL
P032 to P036	Reserved								
P037	RCVD7	RCVD6	RCVD5	RCVD4	RCVD3	RCVD2	RCVD1	RCVD0	SPIBUF
P038	Reserved								
P039	SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0	SPIDAT
P03A to P03C	Reserved								
P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
P03F	SPI STEST	SPI PRIORITY	SPI ESPEN	—	—	—	—	—	SPIPRI

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serial peripheral interface (SPI) module (continued)

The SPI block diagram is illustrated in Figure 15.



† The diagram is shown in slave mode.

Figure 15. SPI Block Diagram

serial communications interface 1 (SCI1) module

The TMS370x6x devices include a serial communications interface (SCI1) module. The SCI1 module supports digital communications between the TMS370 devices and other asynchronous peripherals and uses the standard non-return-to-zero (NRZ) format. The SCI1's receiver and transmitter are double buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI1 checks received data for break detection, parity, overrun, and framing errors. The speed of bit rate (baud) is programmable to over 65,000 different speeds through a 16-bit baud-select register.

serial communications interface 1 (SCI1) module (continued)

Features of the SCI1 module include:

- Three external pins:
 - SCITXD: SCI transmit output pin or general-purpose bidirectional I/O pin
 - SCIRXD: SCI receive input pin or general-purpose bidirectional I/O pin
 - SCICLK: SCI bidirectional serial clock pin, or general-purpose bidirectional I/O pin
- Two communications modes: asynchronous and isosynchronous[†]
- Baud rate: 64K different programmable rates
 - Asynchronous mode: 3 bps to 156K bps at 5-MHz SYSCLK

$$\text{ASYNCHRONOUS BAUD} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 32}$$
 - Isosynchronous mode: 39 bps to 2.5M bps at 5-MHz SYSCLK

$$\text{ISOSYNCHRONOUS BAUD} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 2}$$
- Data-word format
 - One start bit
 - Data-word length programmable from one to eight bits
 - Optional even/odd/no parity bit
 - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: Idle-line and address bit
- Half or full-duplex operation
- Double-buffered receive and transmit functions
- Interrupt driven or polled algorithms with status flags accomplish transmitter and receiver operations.
 - Transmitter: TXRDY flag (transmitter buffer register is ready to receive another character) and TX EMPTY flag (transmitter shift register is empty)
 - Receiver: RXRDY flag (receive buffer register ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR monitoring four interrupt conditions
 - Separate enable bits for transmitter and receiver interrupts
 - NRZ (non-return-to-zero) format
- Eleven SCI1 module control registers are located in control register frame beginning at address P050h.

[†] Isosynchronous = Isochronous

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serial communications interface 1 (SCI1) module (continued)

The SCI1 module control registers are illustrated in Table 20.

Table 20. SCI1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNC/ ISOSYNC	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	Reserved								
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF
P05A P05B P05C	Reserved								
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	SCI STEST	SCITX PRIORITY	SCIRX PRIORITY	SCI ESPEN	—	—	—	—	SCIPRI

The SCI1 module block diagram is illustrated in Figure 16.

The diagram illustrates the internal architecture of the SCI module, divided into Transmit (TX) and Receive (RX) sections.

Transmit (TX) Path:

- TXWAKE (SCICTL.3)** is connected to the **WUT** (Wake-Up Timer) and the **TXSHF Reg.** (Transmit Shift Register).
- TXBUF.7-0** (Transmit Buffer) feeds into the **Transmit Data Buffer Reg.**, which is connected to the **TXSHF Reg.** via an 8-bit bus.
- The **TXSHF Reg.** is clocked by **CLOCK** and outputs **TXENA** (Transmit Enable) and **SCITXD** (Transmit Data).
- SCI TX Interrupt** is generated by **TXRDY (TXCTL.7)** (Transmit Ready) and **TX EMPTY (TXCTL.6)** (Transmit Empty). The interrupt is enabled by **SCI TX INT ENA** (Transmit Interrupt Enable).
- SCITX PRIORITY** is determined by **SCIPRI.6** (SCI Priority), which can be configured for **Level 1 INT** or **Level 2 INT**.
- SCIP.2.7-4** (SCI Priority 2.7-4) and **SCIP.1.3-0** (SCI Priority 1.3-0) are used to configure the **SCITXD** and **SCICLK** (SCI Clock) signals.

Receive (RX) Path:

- RXWAKE (RXCTL.1)** is connected to the **RXSHF Reg.** (Receive Shift Register) and the **RX ERROR** register.
- The **RXSHF Reg.** is clocked by **CLOCK** and outputs **RXENA** (Receive Enable) and **SCIRXD** (Receive Data).
- SCICTL.0** (SCI Control 0) is connected to the **RXSHF Reg.** via an 8-bit bus and the **Receive Data Buffer Reg.**.
- Receive Data Buffer Reg.** outputs **RXBUF.7-0** (Receive Buffer).
- SCI RX Interrupt** is generated by **RXRDY (RXCTL.6)** (Receive Ready) and **BRKDT (RXCTL.5)** (Break Detect). The interrupt is enabled by **SCI RX INT ENA** (Receive Interrupt Enable).
- SCIRX PRIORITY** is determined by **SCIPRI.5** (SCI Priority), which can be configured for **Level 1 INT** or **Level 2 INT**.
- SCIP.2.3-0** (SCI Priority 2.3-0) is used to configure the **SCIRXD** signal.

Other Components:

- Frame Format and Mode:** Includes **PARITY EVEN/ODD ENABLE** and **SCICCR.6** (SCI Control 6).
- Baud Rate MSbyte Reg.** and **Baud Rate LSbyte Reg.** are used to configure the **BAUD MSB. 7-0** and **BAUD LSB. 7-0** (Baud Rate).
- RX ERROR** register includes **ERR** (Error) and **FE** (Framing Error), **OE** (Overrun Error), and **PE** (Parity Error).

analog-to-digital converter 1 (ADC1) module

- Minimum conversion time: 32.8 μ s at 5-MHz SYSCLK
- Ten external pins:
 - Eight analog input channels (AN0–AN7), any of which can be software configured as digital inputs (E0–E7) if not needed as analog channels
 - AN1–AN7 also can be configured as positive-input voltage reference.
 - V_{CC3}: ADC1 module high-voltage reference input
 - V_{SS3}: ADC1 module low-voltage reference input

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analog-to-digital converter 1 (ADC1) module (continued)

- The ADDATA register, which contains the digital result of the last ADC1 conversion
- ADC1 operations can be accomplished through either interrupt driven or polled algorithms.
- Six ADC1 module control registers are located in the control register frame beginning at address 1070h.

The ADC1 module control registers are illustrated in Table 21.

Table 21. ADC1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A-to-D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI

analog-to-digital converter 1 (ADC1) module (continued)

The ADC1 module block diagram is illustrated in Figure 17.

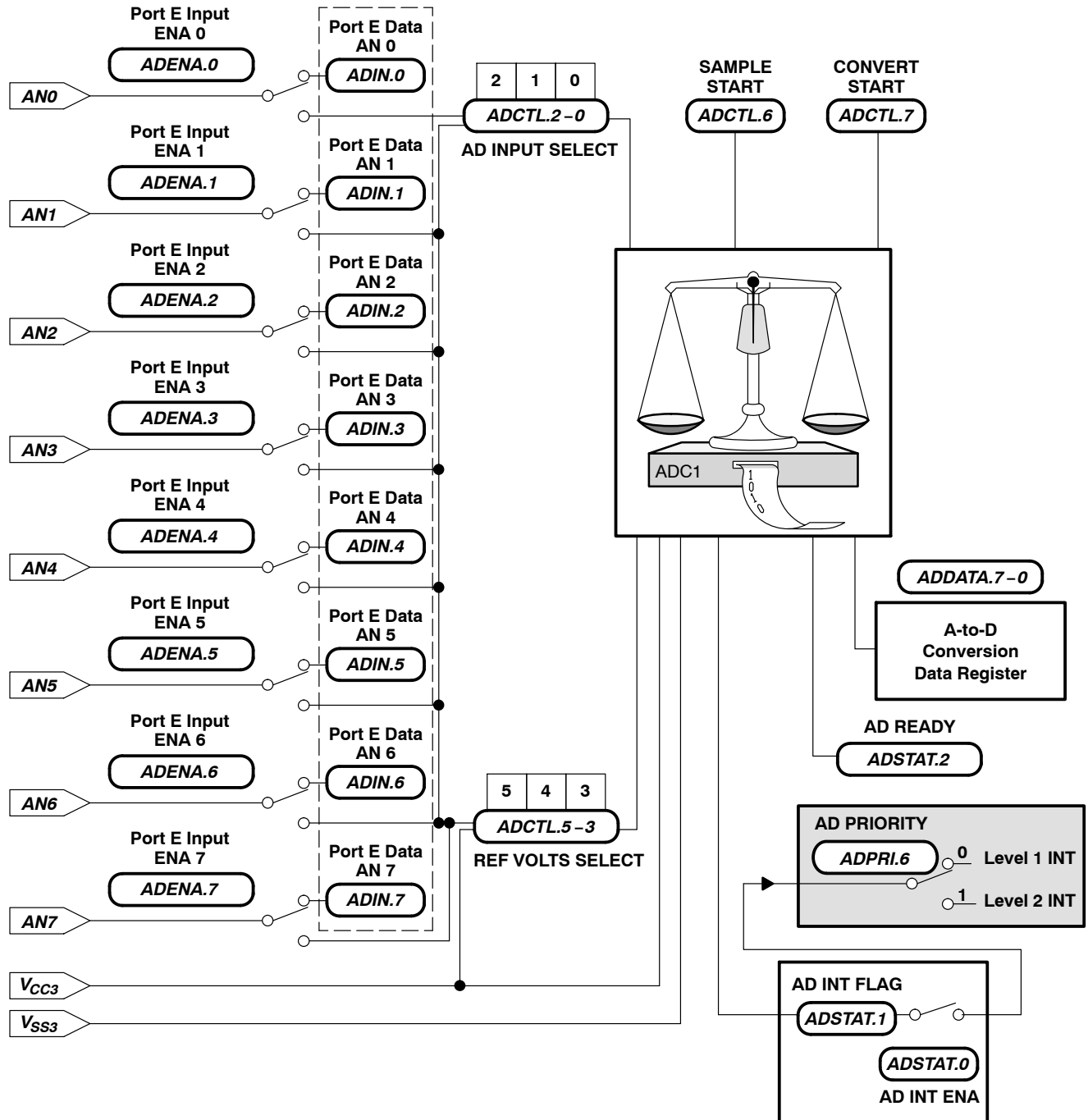


Figure 17. ADC1 Block Diagram

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instruction set overview

Table 22 provides an opcode-to-instruction cross-reference of all 73 instructions and 274 opcodes of the '370Cx6x instruction set. The numbers at the top of this table represent the most significant nibble of the opcode while the numbers at the left side of the table represent the least significant nibble. The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

Table 22. TMS370 Family Opcode/Instruction Map[†]

		MSN																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0		JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8				CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
1		JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7	
2		JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7	
3		JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8	
4		JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes	
5		JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14		
6		JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6	
7		JNC ra 2/5	BTJZ Rs,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10	
8		JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7	
9		JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9	
A		JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12	
B		JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A, *lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8	

[†] All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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Table 22. TMS370 Family Opcode/Instruction Map[†] (Continued)

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L S N	C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
	D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
	E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
	F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7
Second byte of two-byte instructions (F4xx):														F4	8	MOVW *n[Rn] 4/15	DIV Rn,A 3/14-63
														F4	9	JMPL *n[Rn] 4/16	
														F4	A	MOV *n[Rn],A 4/17	
														F4	B	MOV A,*n[Rn] 4/16	
														F4	C	BR *n[Rn] 4/16	
														F4	D	CMP *n[Rn],A 4/18	
														F4	E	CALL *n[Rn] 4/20	
														F4	F	CALLR *n[Rn] 4/22	

Legend:

* = Indirect addressing operand prefix
 & = Direct addressing operand prefix
 # = immediate operand
 #16 = immediate 16-bit number
 lab = 16-label
 n = immediate 8-bit number
 Pd = Peripheral register containing destination type
 Pn = Peripheral register
 Ps = Peripheral register containing source byte
 ra = Relative address
 Rd = Register containing destination type
Rn = Register file
 Rp = Register pair
 Rpd = Destination register pair
 Rps = Source Register pair
 Rs = Register containing source byte

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

development system support

The TMS370 family development support tools include an assembler, a C compiler, a linker, an in-circuit emulator (XDS/22 – extended development support), compact development tool, and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
 - Provides extensive macro capability
 - Allows high-speed operation
 - Includes format conversion utilities for popular formats
- ANSI C Compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, Sun-3™ or Sun-4™)
 - Generates assembly code for the TMS370 that can be inspected easily
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables the user to directly reference the TMS370 port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (compact development tool) Timer real-time in-circuit emulation
 - Base (Part No. EDSCDT37T – for PC, requires cable)
 - Cable for 68-pin PLCC (Part No. EDSTRG68PLCC)
 - Provides EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Uploads/downloads program and data memory
 - Executes programs and software routines
 - Includes 1024 samples trace buffer
 - Includes single-step executable instructions
 - Uses software breakpoints to halt program execution at selected address
- Microcontroller programmer
 - Base (Part No. TMDS3760500A – for PC, requires programmer head)
 - Single unit head for 68-pin PLCC (Part No. TMDS3780510A)
 - PC-based, window/function-key-oriented user interface for ease of use and rapid learning environment
- Starter Kit (Part No. TMDX37000 – for PC)
 - Includes TMS370 Assembler diskette and documentation
 - Includes TMS370 Simulator
 - Includes programming adapter board and programming software
 - Not included – to be supplied by the user:

HP700 is a trademark of Hewlett-Packard Company.
Sun-3 and Sun-4 are trademarks of Sun Microsystems, Inc.



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development system support (continued)

- + 5 V power supply
- ZIF sockets
- 9-pin RS232 cable

device numbering conventions

Figure 18 illustrates the numbering and symbol nomenclature for the TMS370Cx6x family.

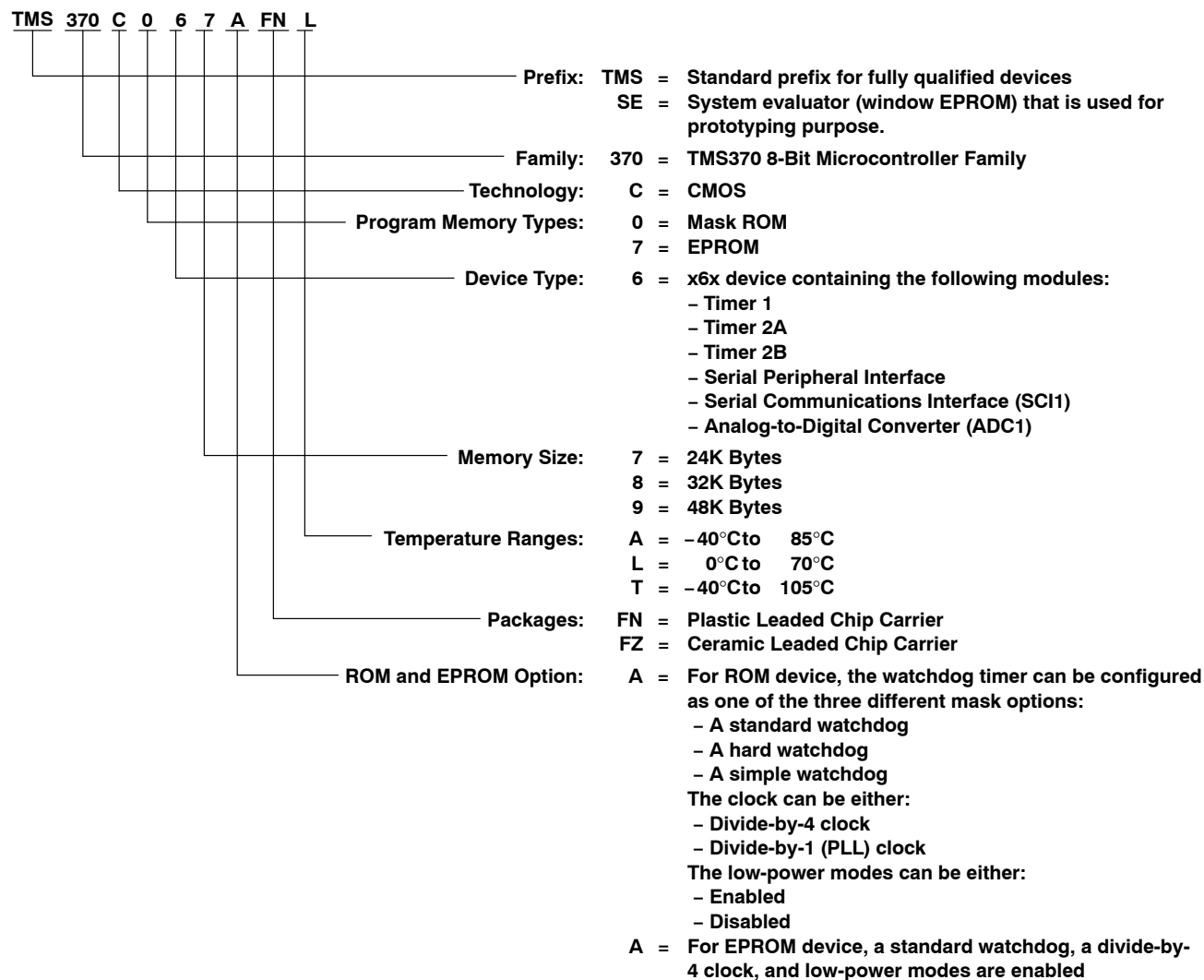


Figure 18. TMS370Cx6x Family Nomenclature

device part numbers

Table 23 lists all the 'x6x devices available. The device part number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog timer options desired. Remember that each device can have only one of the possible three watchdog timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 23. Device Part Numbers

DEVICE PART NUMBERS FOR 68 PINS
TMS370C067AFNA TMS370C067AFNL TMS370C067AFNT
TMS370C068AFNA TMS370C068AFNL TMS370C068AFNT
TMS370C069AFNA TMS370C069AFNL TMS370C069AFNT
TMS370C768AFNT
TMS370C769AFNT
SE370C768AFZT [†] SE370C769AFZT [†]

[†] System evaluators are for use only in prototype environment and their reliability has not been characterized.

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new code release form

Figure 19 shows a sample of the new code release form.

NEW CODE RELEASE FORM TEXAS INSTRUMENTS TMS370 MICROCONTROLLER PRODUCTS				DATE: _____																
To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information: 1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media) 2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.																				
Company Name: _____ Street Address: _____ Street Address: _____ City: _____ State _____ Zip _____		Contact Mr./Ms.: _____ Phone: (_____) _____ Ext.: _____ Customer Purchase Order Number: _____ Customer Print Number *Yes: _____ # _____ No: _____ (Std. spec to be followed) *If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.																		
Customer Part Number: _____ Customer Application: _____																				
TMS370 Device: _____ TI Customer ROM Number: _____ (provided by Texas Instruments)																				
OSCILLATOR FREQUENCY <table border="1" style="width: 100%; border-collapse: collapse;"><thead><tr><th></th><th style="text-align: center;">MIN</th><th style="text-align: center;">TYP</th><th style="text-align: center;">MAX</th></tr></thead><tbody><tr><td>☐ External Drive (CLKIN)</td><td>_____</td><td>_____</td><td>_____</td></tr><tr><td>☐ Crystal</td><td>_____</td><td>_____</td><td>_____</td></tr><tr><td>☐ Ceramic Resonator</td><td>_____</td><td>_____</td><td>_____</td></tr></tbody></table> ☐ Supply Voltage MIN: _____ MAX: _____ (std range: 4.5V to 5.5V)						MIN	TYP	MAX	☐ External Drive (CLKIN)	_____	_____	_____	☐ Crystal	_____	_____	_____	☐ Ceramic Resonator	_____	_____	_____
	MIN	TYP	MAX																	
☐ External Drive (CLKIN)	_____	_____	_____																	
☐ Crystal	_____	_____	_____																	
☐ Ceramic Resonator	_____	_____	_____																	
CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS <table style="width: 100%;"><tr><td style="vertical-align: top;">Low Power Modes ☐ Enabled ☐ Disabled</td><td style="vertical-align: top;">Watchdog counter ☐ Standard ☐ Hard Enabled ☐ Simple Counter</td><td style="vertical-align: top;">Clock Type ☐ Standard (/4) ☐ PLL (/1)</td></tr></table> NOTE: Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the <i>TMS370 Family User's Guide</i> (literature number SPNU127) or the <i>TMS370 Family Data Manual</i> (literature number SPNS014B).					Low Power Modes ☐ Enabled ☐ Disabled	Watchdog counter ☐ Standard ☐ Hard Enabled ☐ Simple Counter	Clock Type ☐ Standard (/4) ☐ PLL (/1)													
Low Power Modes ☐ Enabled ☐ Disabled	Watchdog counter ☐ Standard ☐ Hard Enabled ☐ Simple Counter	Clock Type ☐ Standard (/4) ☐ PLL (/1)																		
TEMPERATURE RANGE <table style="width: 100%;"><tr><td>☐ 'L': 0° to 70°C (standard)</td></tr><tr><td>☐ 'A': -40° to 85°C</td></tr><tr><td>☐ 'T': -40° to 105°C</td></tr></table>					☐ 'L': 0° to 70°C (standard)	☐ 'A': -40° to 85°C	☐ 'T': -40° to 105°C													
☐ 'L': 0° to 70°C (standard)																				
☐ 'A': -40° to 85°C																				
☐ 'T': -40° to 105°C																				
PACKAGE TYPE <table style="width: 100%;"><tr><td>☐ 'N' 28-pin PDIP</td><td>☐ "FN" 44-pin PLCC</td></tr><tr><td>☐ "FN" 28-pin PLCC</td><td>☐ "FN" 68-pin PLCC</td></tr><tr><td>☐ "N" 40-pin PDIP</td><td>☐ "NM" 64-pin PSDIP</td></tr><tr><td colspan="2">☐ "NJ" 40-pin PSDIP (formerly known as N2)</td></tr></table>					☐ 'N' 28-pin PDIP	☐ "FN" 44-pin PLCC	☐ "FN" 28-pin PLCC	☐ "FN" 68-pin PLCC	☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP	☐ "NJ" 40-pin PSDIP (formerly known as N2)									
☐ 'N' 28-pin PDIP	☐ "FN" 44-pin PLCC																			
☐ "FN" 28-pin PLCC	☐ "FN" 68-pin PLCC																			
☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP																			
☐ "NJ" 40-pin PSDIP (formerly known as N2)																				
SYMBOLIZATION <table style="width: 100%;"><tr><td>☐ TI standard symbolization</td></tr><tr><td>☐ TI standard w/customer part number</td></tr><tr><td>☐ Customer symbolization (per attached spec, subject to approval)</td></tr></table>					☐ TI standard symbolization	☐ TI standard w/customer part number	☐ Customer symbolization (per attached spec, subject to approval)													
☐ TI standard symbolization																				
☐ TI standard w/customer part number																				
☐ Customer symbolization (per attached spec, subject to approval)																				
BUS EXPANSION <table style="width: 100%;"><tr><td>☐ YES</td><td>☐ NO</td></tr></table>					☐ YES	☐ NO														
☐ YES	☐ NO																			
NON-STANDARD SPECIFICATIONS: ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.																				
RELEASE AUTHORIZATION: This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cycletime commences when this document is signed off and the verification code is approved by the customer.																				
1. Customer: _____ Date: _____		2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____																		

Figure 19. Sample New Code Release Form



Table 24 is a collection of all the peripheral file frames using the 'Cx6x, (provided for a quick reference).

Table 24. Peripheral File Frame Compilation

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	System Configuration Registers								
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011		—	—	AUTOWAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013	Reserved								
P014	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLH
P015 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLM
P01D	Reserved								
P01E	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLL
P01F	Reserved								
	Digital Port Control Registers								
P020	Reserved								APORT1
P021	Port A Control Register 2								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	Port B Control Register 2								BPORT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPORT1
P029	Port C Control Register 2								CPORT2
P02A	Port C Data								CDATA
P02B	Port C Direction								CDIR
P02C	Port D Control Register 1					—	—	—	DPORT1
P02D	Port D Control Register 2†					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

† To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

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Table 24. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
SPI Module Control Memory Map									
P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/SLAVE	TALK	SPI INT ENA	SPICTL
P032 to P036	Reserved								
P037	RCVD7	RCVD6	RCVD5	RCVD4	RCVD3	RCVD2	RCVD1	RCVD0	SPIBUF
P038	Reserved								
P039	SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0	SPIDAT
P03A to P03C	Reserved								
P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
P03F	SPI STEST	SPI PRIORITY	SPI ESPEN	—	—	—	—	—	SPIPRI
Timer 1 Module Register Memory Map									
Modes: Dual-Compare and Capture/Compare									
P040	Bit 15	T1 Counter MSbyte						Bit 8	T1CNTR
P041	Bit 7	T1 Counter LSbyte						Bit 0	
P042	Bit 15	Compare Register MSbyte						Bit 8	T1C
P043	Bit 7	Compare Register LSbyte						Bit 0	
P044	Bit 15	Capture/Compare Register MSbyte						Bit 8	T1CC
P045	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P046	Bit 15	Watchdog Counter MSbyte						Bit 8	WDCNTR
P047	Bit 7	Watchdog Counter LSbyte						Bit 0	
P048	Bit 15	Watchdog Reset Key						Bit 0	WDRST
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

Table 24. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Dual-Compare and Capture/Compare									
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI
Serial Communications Interface 1 Memory Map									
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNCR/ ISOSYNCR	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	Reserved								
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF
P05A P05B P05C	Reserved								
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	SCI STEST	SCITX PRIORITY	SCIRX PRIORITY	SCI ESPEN	—	—	—	—	SCIPRI
Timer 2A Control Registers Memory Map									
Modes: Dual-Compare and Dual-Capture									
P060	Bit 15	T2A Counter MSbyte						Bit 8	T2ACNTR
P061	Bit 7	T2A Counter LSbyte						Bit 0	
P062	Bit 15	Compare Register MSbyte						Bit 8	T2AC
P063	Bit 7	Compare Register LSbyte						Bit 0	
P064	Bit 15	Capture/Compare Register MSbyte						Bit 8	T2ACC
P065	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P066	Bit 15	Capture Register 2 MSbyte						Bit 8	T2AIC
P067	Bit 7	Capture Register 2 LSbyte						Bit 0	
P06A	—	—	—	T2A OVRFL INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1

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Table 24. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Mode: Dual-Compare									
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC2 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
Mode: Dual-Capture									
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
Modes: Dual-Compare and Dual-Capture									
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2/PWM DATA IN	T2AIC2/PWM DATA OUT	T2AIC2/PWM FUNCTION	T2AIC2/PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC1/CR DATA DIR	T2APC2
P06F	T2A STEST	T2A PRIORITY	—	—	—	—	—	—	T2APRI
Analog-To-Digital Converter 1 Control Registers									
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A-to-D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI
Timer 2B Control Registers Memory Map									
Modes: Dual-Compare and Dual-Capture									
P080	T2B Counter MSbyte							BIT 8	T2BCNTR
P081	T2B Counter LSbyte							BIT 0	
P082	Compare Register MSbyte							BIT 8	T2BC
P083	Compare Register LSbyte							BIT 0	
P084	Capture/Compare Register MSbyte							BIT 8	T2BCC
P085	Capture/Compare Register LSbyte							BIT 0	
P086	Capture Register 2 MSbyte							BIT 8	T2BIC
P087	Capture Register 2 LSbyte							BIT 0	
P08A	—	—	—	T2B OVRFL INT ENA	T2B OVRFL INT FLAG	T2B INPUT SELECT1	T2B INPUT SELECT0	T2B SW RESET	T2BCTL1

Table 24. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Mode: Dual-Compare									
P08B	T2BEDGE1 INT FLAG	T2BC2 INT FLAG	T2BC1 INT FLAG	—	—	T2BEDGE1 INT ENA	T2BC2 INT ENA	T2BC1 INT ENA	T2BCTL2
P08C	T2B MODE = 0	T2BC1 OUT ENA	T2BC2 OUT ENA	T2BC1 RST ENA	T2BEDGE1 OUT ENA	T2BEDGE1 POLARITY	T2BEDGE1 RST ENA	T2BEDGE1 DET ENA	T2BCTL3
Mode: Dual-Capture									
P08B	T2BEDGE1 INT FLAG	T2BEDGE2 INT FLAG	T2BC1 INT FLAG	—	—	T2BEDGE1 INT ENA	T2BEDGE2 INT ENA	T2BC1 INT ENA	T2BCTL2
P08C	T2B MODE = 1	—	—	T2BC1 RST ENA	T2BEDGE2 POLARITY	T2BEDGE1 POLARITY	T2BEDGE2 DET ENA	T2BEDGE1 DET ENA	T2BCTL3
Modes: Dual-Compare and Dual-Capture									
P08D	—	—	—	—	T2BEVT DATA IN	T2BEVT DATA OUT	T2BEVT FUNCTION	T2BEVT DATA DIR	T2BPC1
P08E	T2BIC2/PWM DATA IN	T2BIC2/PWM DATA OUT	T2BIC2/PWM FUNCTION	T2BIC2/PWM DATA DIR	T2BIC1/CR DATA IN	T2BIC1/CR DATA OUT	T2BIC1/CR FUNCTION	T2BIC1/CR DATA DIR	T2BPC2
P08F	T2B STEST	T2B PRIORITY	—	—	—	—	—	—	T2BPRI

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range [‡] , V_{CC1} , V_{CC2} , V_{CC3} (see Note 1)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC1}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC1}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC1}) (see Note 1)	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	1 W
Operating free-air temperature range, T_A : L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] $V_{CC1} = V_{CC}$

NOTE 1: Electrical characteristics are specified with all output buffers loaded with the specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage (see Note 2)	4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 3)	3		5.5	
V_{CC2}	Digital I/O supply voltage (see Note 2)	4.5	5	5.5	V
V_{CC3}	Analog supply voltage (see Note 2)	4.5	5	5.5	
V_{SS2}	Digital I/O supply ground	–0.3	0	0.3	V
V_{SS3}	Analog supply ground	–0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC		V_{SS1}	V
		MC, normal operation		V_{SS1}	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET		2	V
		MC (non-WPO mode)		$V_{CC1} - 0.3$	
		XTAL2/CLKIN		$0.8 V_{CC1}$	
		RESET		$0.7 V_{CC1}$	
V_{MC}	MC (mode control) voltage (see Note 4)	EEPROM write protect override (WPO)		11.7	V
		EPROM programming voltage (V_{PP})		13	
		Microprocessor		$V_{CC1} - 0.3$	
		Microcomputer		V_{SS1}	
T_A	Operating free-air temperature	L version		0	°C
		A version		–40	
		T version		–40	

NOTES: 2. Unless otherwise noted, all voltage values are with respect to V_{SS1} .

3. RESET must be activated externally when V_{CC1} or SYSCLK is out of the recommended operating range.

4. The basic microcomputer and microprocessor operating modes are selected by the voltage level applied to the dedicated MC pin two system-clock cycles (t_c) before RESET goes inactive (high). The WPO mode can be selected anytime that a sufficient voltage is present on MC.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

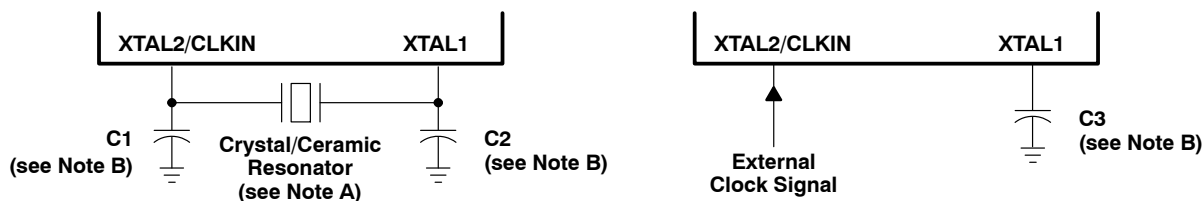
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V _{OL}	Low-level output voltage		I _{OL} = 1.4 mA				0.4	V	
V _{OH}	High-level output voltage		I _{OH} = − 50 μA		0.9 V _{CC1}			V	
			I _{OH} = − 2 mA		2.4				
I _I	Input current	MC	0 V < V _I ≤ 0.3 V				10	μA	
			0.3 V < V _I < V _{CC1} − 0.3 V				50		
			V _{CC1} − 0.3 V ≤ V _I ≤ V _{CC1} + 0.3 V				10		
			V _{CC1} + 0.3 V < V _I ≤ 13 V				650		
			12 V ≤ V _I ≤ 13 V (See Note 6)				50	mA	
	I/O pins	0 V ≤ V _I ≤ V _{CC1}				± 10			
I _{OL}	Low-level output current		V _{OL} = 0.4 V		1.4			mA	
I _{OH}	High-level output current		V _{OH} = 0.9 V _{CC1}		− 50			μA	
			V _{OH} = 2.4 V		− 2			mA	
I _{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 9)	TMS370Cx67A TMS370Cx68A	SYSCCLK = 5 MHz	See Notes 7 and 8		35	56	mA	
		TMS370Cx67A TMS370Cx68A	SYSCCLK = 3 MHz	See Notes 7 and 8		25	36	mA	
		TMS370Cx69A	SYSCCLK = 3 MHz	See Notes 5 and 7		46	55	mA	
		TMS370Cx67A TMS370Cx68A	SYSCCLK = 0.5 MHz	See Notes 7 and 8		13	18	mA	
		TMS370Cx69A	SYSCCLK = 0.5 MHz	See Notes 5 and 7		22	28		
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 10)			SYSCCLK = 5 MHz	See Notes 7 and 8		12	17	mA
				SYSCCLK = 3 MHz	See Notes 7 and 8		8	11	
				SYSCCLK = 0.5 MHz	See Notes 7 and 8		2.5	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 11)			SYSCCLK = 3 MHz	See Notes 7 and 8		6	8.6	mA
				SYSCCLK = 0.5 MHz	See Notes 7 and 8		2	3	
	Supply current (HALT mode)		XTAL2/CLKIN < 0.2 V		See Note 7		2	30	μA

- NOTES: 5. 'x69 operates up to 3 MHz SYSCLOCK. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns.
6. Input current I_{PP} is a maximum of 50 mA only when programming EPROM.
7. Single chip mode, ports configured as inputs or outputs with no load. All inputs $\leq 0.2 \text{ V}$ or $\geq V_{CC1} - 0.2 \text{ V}$.
8. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLOCK, this extra current = $0.01 \text{ mA} \times (\text{total load capacitance} + \text{crystal capacitance in pF})$.
9. Maximum operating current for TMS370Cx6x = $10 (\text{SYSCLOCK}) + 5.8 \text{ mA}$.
10. Maximum standby current for TMS370Cx6x = $3 (\text{SYSCLOCK}) + 2 \text{ mA}$. (OSC POWER bit = 0).
11. Maximum standby current for TMS370Cx6x = $2.24 (\text{SYSCLOCK}) + 1.9 \text{ mA}$. (OSC POWER bit = 1, only valid up to 3 MHz SYSCLOCK).

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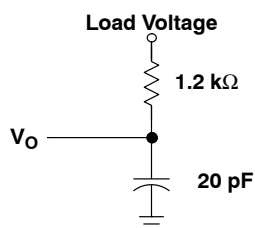
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PARAMETER MEASUREMENT INFORMATION



NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
B. The values of C1 and C2 typically are 15 pF and the value of C3 is typically 50pF. See the manufacturer's recommendations for ceramic resonators.

Figure 20. Recommended Crystal/Clock Connections (See Note A)



Case 1: $V_O = V_{OH} = 2.4 \text{ V}$; Load Voltage = 0 V
Case 2: $V_O = V_{OL} = 0.4 \text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 21. Typical Output Load Circuit

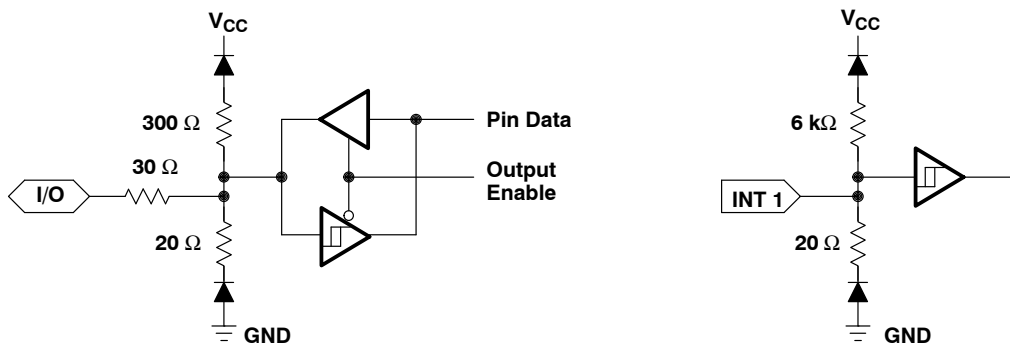


Figure 22. Typical Buffer Circuitry

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

A	Address	RXD	SCIRXD
AR	Array	S	Slave mode
B	Byte	SC	SYSCLK
CI	XTAL2/CLKIN	SCC	SCICLK
D	Data	SIMO	SPISIMO
E	$\overline{EDS}$	SOMI	SPISOMI
FE	Final	SPC	SPICLK
IE	Initial	TXD	SCITXD
M	Master mode	W	Write
PGM	Program	WT	$\overline{WAIT}$
R	Read		

Lowercase subscripts and their meanings are:

c	cycle time (period)	r	rise time
d	delay time	su	setup time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid
Z	High impedance

All timings are measured between high and low measurement points as indicated in Figure 23 and Figure 24.

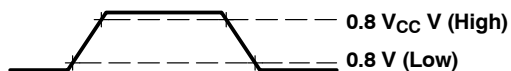


Figure 23. XTAL2/CLKIN Measurement Points

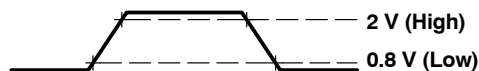


Figure 24. General Measurement Points

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external clocking requirements for clock divided by 4[†] (see Figure 25)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 12)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN [§] Crystal operating frequency	2	20	MHz
	SYSCLK [¶] System clock [‡]	0.5	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions table.

[‡] SYSCLK = CLKIN/4

[§] 'x69A operates up to 12 MHz CLKIN

[¶] 'x69A operates up to 3 MHz SYSCLK

NOTE 12: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

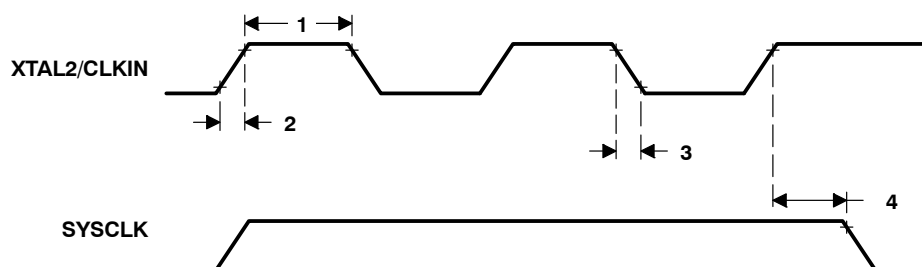


Figure 25. External Clock Divide-by-4

external clocking requirements for clock divided by 1 (PLL)[†] (see Figure 26)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 12)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN [#] Crystal operating frequency	2	5	MHz
	SYSCLK [¶] System clock [§]	2	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions table.

[§] SYSCLK = CLKIN/1

[¶] 'x69A operates up to 3 MHz SYSCLK

[#] 'x69A operates up to 3 MHz CLKIN (for divide-by-1 clock option)

NOTE 12: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

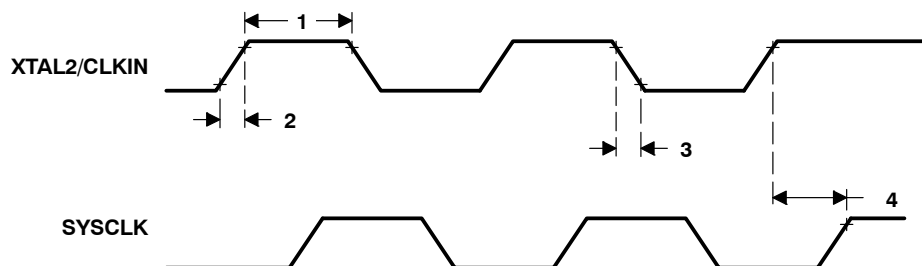


Figure 26. External Clock Divide-by-1

general purpose output signal switching time requirements (see Figure 27)

	MIN	NOM	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns

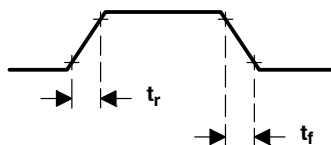


Figure 27. Signal Switching Timing

recommended EEPROM timing requirements for programming

	MIN	MAX	UNIT
$t_{w(PGM)B}$ Pulse duration, programming signal to ensure valid data is stored (byte mode)	10		ms
$t_{w(PGM)AR}$ Pulse duration, programming signal to ensure valid data is stored (array mode)	20		ms

recommended EPROM operating conditions for programming

	MIN	NOM	MAX	UNIT
V_{CC1} Supply voltage	4.75	5.5	6	V
V_{PP} Supply voltage at MC pin	13	13.2	13.5	V
I_{PP} Supply current at MC pin during programming ($V_{PP} = 13$ V)		30	50	mA
SYSCLK System clock	Divide-by-4	0.5	5	MHz
	Divide-by-1	2	5	

recommended EPROM timing requirements for programming

	MIN	NOM	MAX	UNIT
$t_{w(EPGM)}$ Pulse duration, programming signal (see Note 13)	0.40	0.50	3	ms

NOTE 13: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.

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switching characteristics and timing requirements for external read and write[†] (see Figure 28 and Figure 29)

NO.	PARAMETER		MIN	MAX	UNIT	
5	t_c	Cycle time, SYSCLK (system clock)	Divide-by-4 clock	200	2000	ns
			Divide-by-1 PLL	200	500	
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low	$0.5t_c-25$	$0.5t_c$	ns	
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high	$0.5t_c$	$0.5t_c+20$	ns	
8	$t_{d(SCL-A)}$	Delay time, SYSCLK low to address R/W and $\overline{OCF}$ valid		$0.25t_c+75$	ns	
9	$t_{v(A)}$	Valid time, address to $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSH1}$, and $\overline{CSPF}$ low	$0.5t_c-90$		ns	
10	$t_{su(D)}$	Setup time, write data time to $\overline{EDS}$ high	$0.75t_c-80^\ddagger$		ns	
11	$t_{h(EH-A)}$	Hold time, address, R/W and $\overline{OCF}$ from $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSH1}$ and $\overline{CSPF}$ high	$0.5t_c-60$		ns	
12	$t_{h(EH-D)W}$	Hold time, write data time from $\overline{EDS}$ high	$0.75t_c+15$		ns	
13	$t_{d(DZ-EL)}$	Delay time, data bus high impedance to $\overline{EDS}$ low (read cycle)	$0.25t_c-35$		ns	
14	$t_{d(EH-D)}$	Delay time, $\overline{EDS}$ high to data bus enable (read cycle)	$1.25t_c-40$		ns	
15	$t_{d(EL-DV)R}$	Delay time, $\overline{EDS}$ low to read data valid		$t_c-95^\ddagger$	ns	
16	$t_{h(EH-D)R}$	Hold time, read time from $\overline{EDS}$ high	0		ns	
17	$t_{su(WT-SCH)}$	Setup time, $\overline{WAIT}$ time to SYSCLK high	$0.25t_c+70^\S$		ns	
18	$t_{h(SCH-WT)}$	Hold time, $\overline{WAIT}$ time from SYSCLK high	0		ns	
19	$t_{d(EL-WTV)}$	Delay time, $\overline{EDS}$ low to $\overline{WAIT}$ valid		$0.5t_c-60$	ns	
20	t_w	Pulse duration, $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSH1}$ and $\overline{CSPF}$ low	$t_c-80^\ddagger$	$t_c+40^\ddagger$	ns	
21	$t_{d(AV-DV)R}$	Delay time, address valid to read data valid		$1.5t_c-115^\ddagger$	ns	
22	$t_{d(AV-WTV)}$	Delay time, address valid to $\overline{WAIT}$ valid		t_c-115	ns	
23	$t_{d(AV-EH)}$	Delay time, address valid to $\overline{EDS}$ high (end of write)	$1.5t_c-85^\ddagger$		ns	

[†] t_c = system-clock cycle time = $1/\text{SYSCLK}$

[‡] If wait states, PFWait, or the autowait feature is used, add t_c to this value for each wait state invoked.

[§] If the autowait feature is enabled, the $\overline{WAIT}$ input can assume a "don't care" condition until the third cycle of the access. The $\overline{WAIT}$ signal must be synchronized with the high pulse of the SYSCLK signal while still conforming to the minimum set-up time.



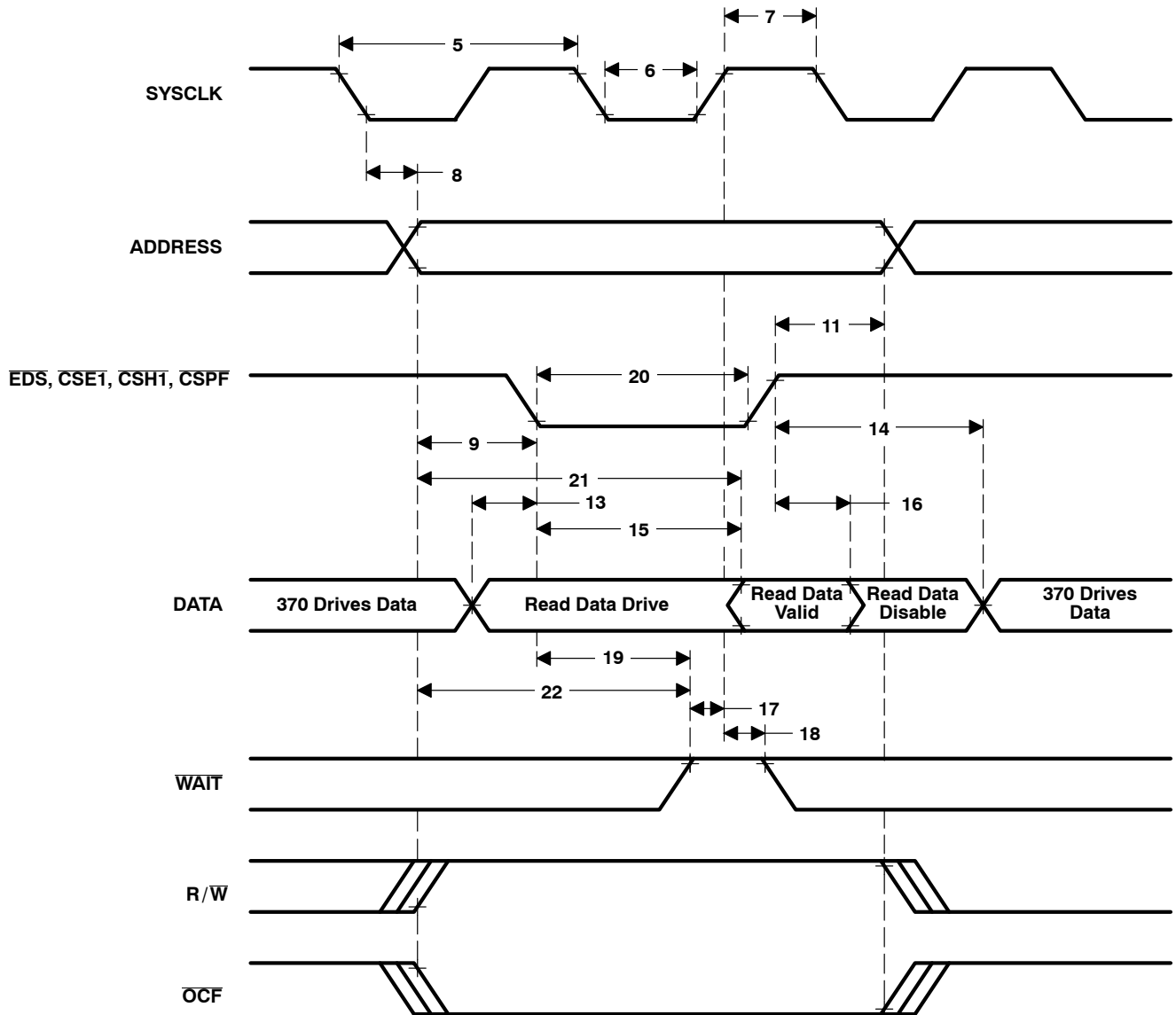


Figure 28. External-Read Timing

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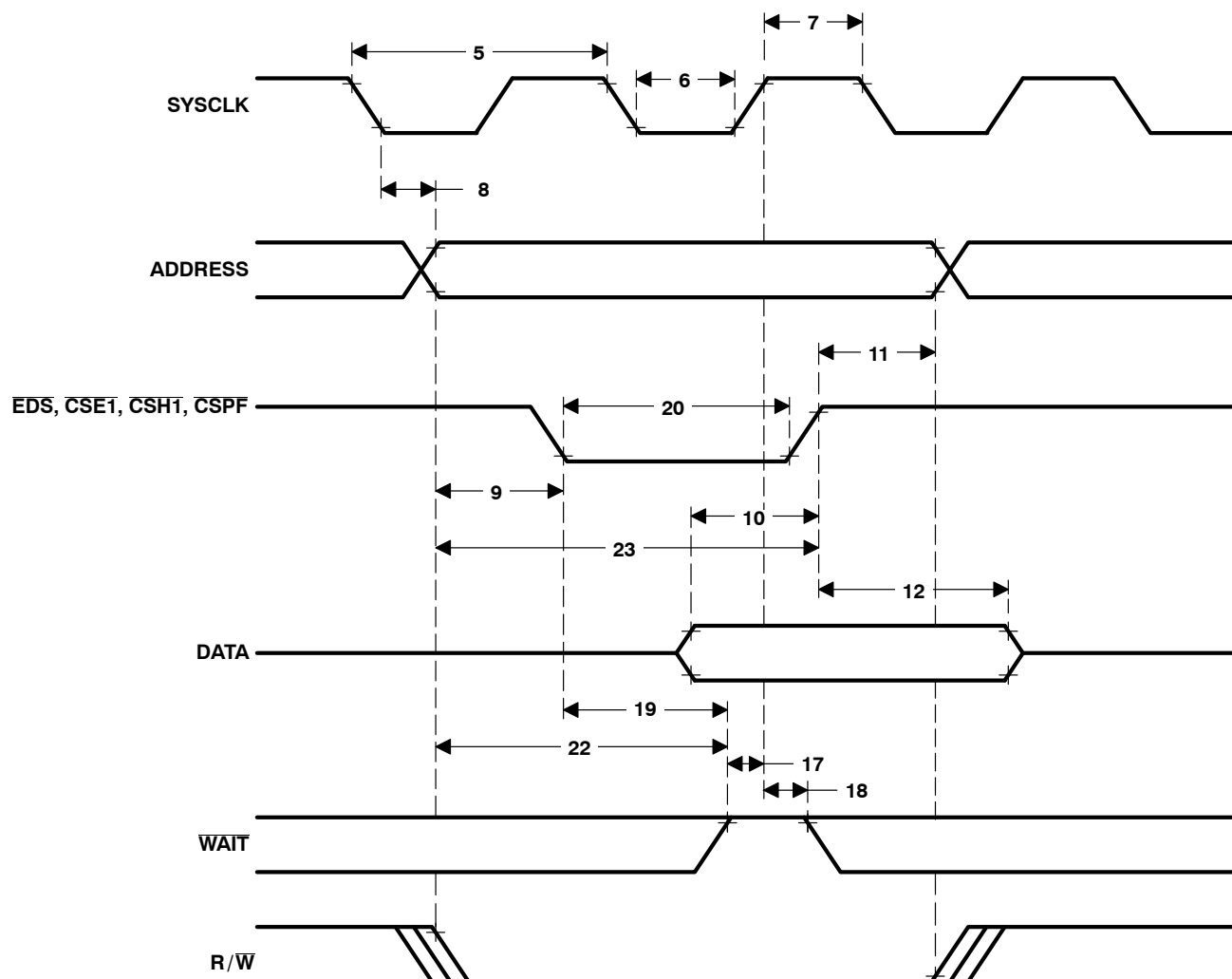


Figure 29. External-Write Timing

SCI1 isosynchronous-mode timing characteristics and requirements for internal clock
(see Note 14 and Figure 30)

NO.		MIN	MAX	UNIT
24	$t_{c(SCC)}$ Cycle time, SCICLK	$2t_c$	$131\,072t_c$	ns
25	$t_{w(SCCL)}$ Pulse duration, SCICLK low	$t_c - 45$	$0.5t_{c(SCC)} + 45$	ns
26	$t_{w(SCCH)}$ Pulse duration, SCICLK high	$t_c - 45$	$0.5t_{c(SCC)} + 45$	ns
27	$t_{d(SCCL-TXD)}$ Delay time, SCITXD valid after SCICLK low	- 50	60	ns
28	$t_{v(SCCH-TXD)}$ Valid time, SCITXD data valid after SCICLK high	$t_{w(SCCH)} - 50$		ns
29	$t_{su(RXD-SCCH)}$ Setup time, SCIRXD to SCICLK high	$0.25 t_c + 145$		ns
30	$t_{v(SCCH-RXD)}$ Valid time, SCIRXD data valid after SCICLK high	0		ns

NOTE 14: t_c = system-clock cycle time = $1/\text{SYSCLK}$

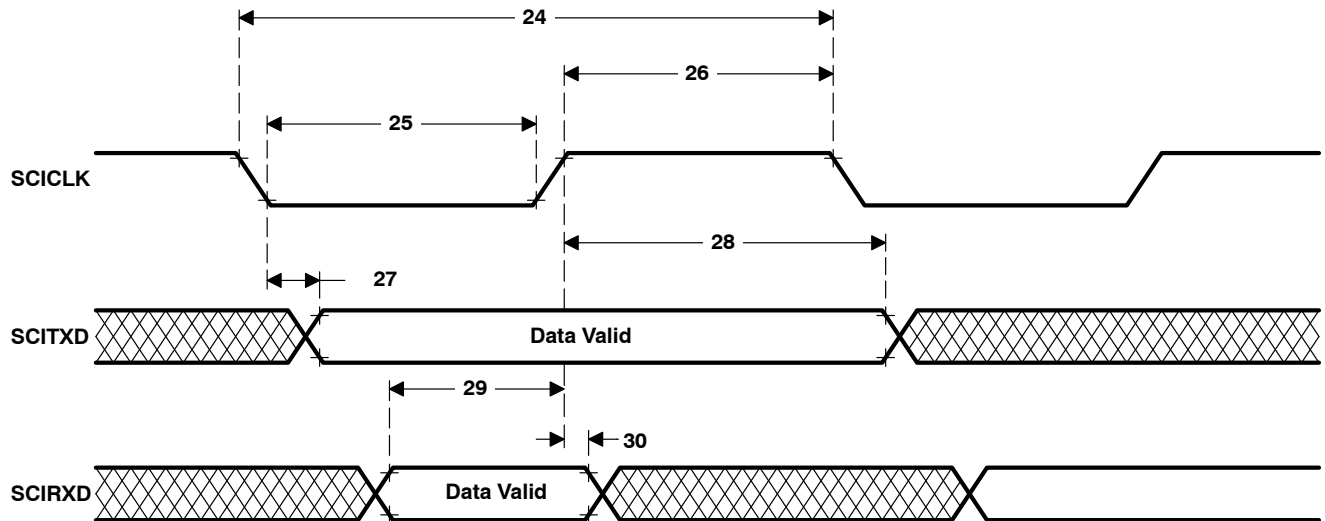


Figure 30. SCI1 Isosynchronous-Mode Timing for Internal Clock

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SCI1 isosynchronous-mode timing characteristics and requirements for external clock (see Note 14 and Figure 31)

NO.		MIN	MAX	UNIT
31	$t_{c(SCC)}$ Cycle time, SCICLK	$10t_c$		ns
32	$t_w(SCCL)$ Pulse duration, SCICLK low	$4.25t_c + 120$		ns
33	$t_w(SCCH)$ Pulse duration, SCICLK high	$t_c + 120$		ns
34	$t_d(SCCL-TXDV)$ Delay time, SCITXD valid after SCICLK low		$4.25t_c + 145$	ns
35	$t_v(SCCH-TXD)$ Valid time, SCITXD data valid after SCICLK high	$t_w(SCCH)$		ns
36	$t_{su}(SIMO-SCCH)$ Setup time, SCIRXD to SCICLK high	40		ns
37	$t_v(SCCH-RXD)$ Valid time, SCIRXD data after SCICLK high	$2t_c$		ns

NOTE 14: t_c = system-clock cycle time = 1 / SYSCLK

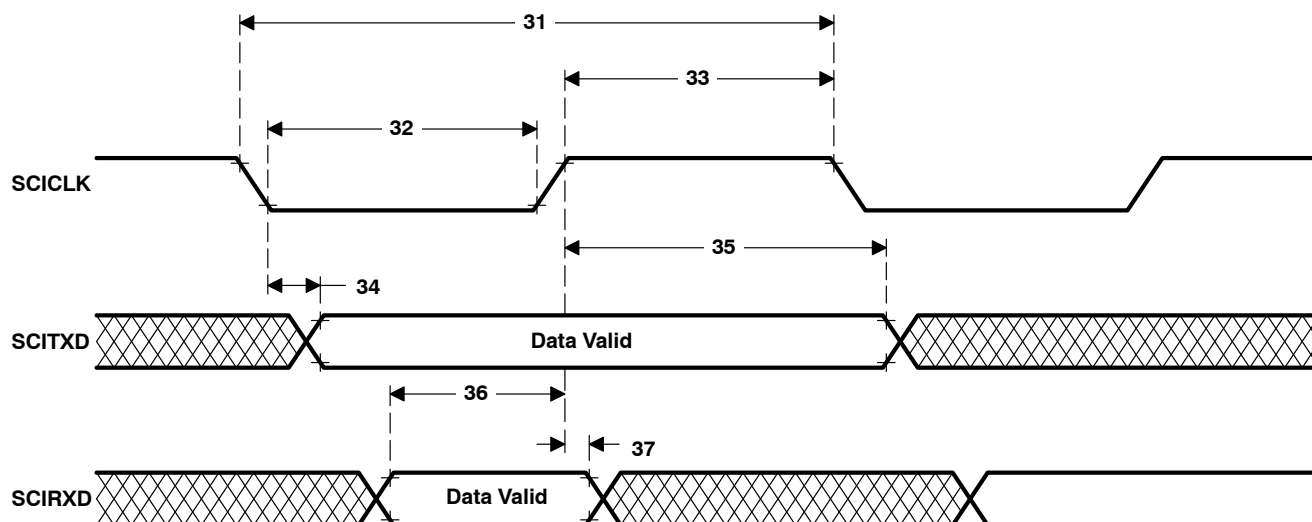
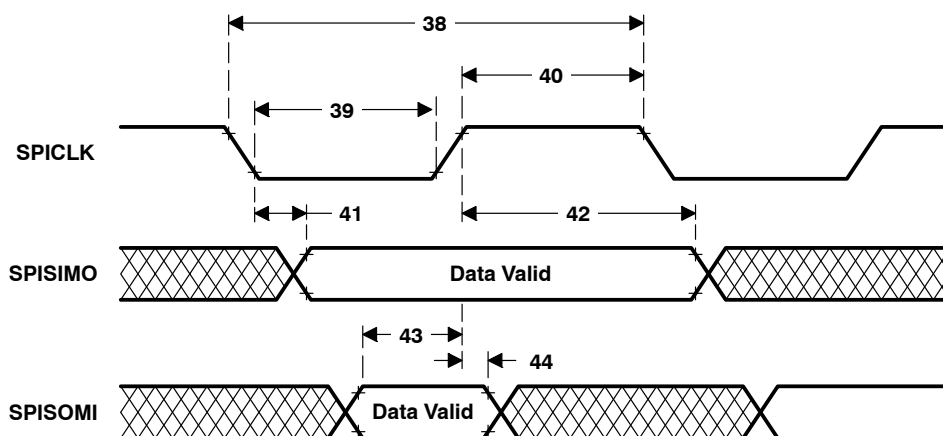


Figure 31. SCI1 Isosynchronous-Mode Timing for External Clock

SPI-master mode external timing characteristics and requirements (see Note 14 and Figure 32)

NO.			MIN	MAX	UNIT
38	$t_{c(SPC)}M$	Cycle time, SPICLK	$2t_c$	$256t_c$	ns
39	$t_{w(SPCL)}M$	Pulse duration, SPICLK low	$t_c - 45$	$0.5t_{c(SPC)} + 45$	ns
40	$t_{w(SPCH)}M$	Pulse duration, SPICLK high	$t_c - 55$	$0.5t_{c(SPC)} + 45$	ns
41	$t_{d(SPCL-SIMOV)}M$	Delay time, SPISIMO valid after SPICLK low (polarity = 1)	- 65	50	ns
42	$t_{v(SPCH-SIMO)}M$	Valid time, SPISIMO data valid after SPICLK high (polarity = 1)	$t_{w(SPCH)} - 50$		ns
43	$t_{su(SOMI-SPCH)}M$	Setup time, SPISOMI to SPICLK high (polarity = 1)	$0.25 t_c + 150$		ns
44	$t_{v(SPCH-SOMI)}M$	Valid time, SPISOMI data valid after SPICLK high (polarity = 1)	0		ns

NOTE 14: t_c = system-clock cycle time = $1 / \text{SYSCLK}$



NOTE A: The diagram shows polarity = 1. SPICLK is inverted when polarity = 0.

Figure 32. SPI-Master External Timing

TMS370Cx6x

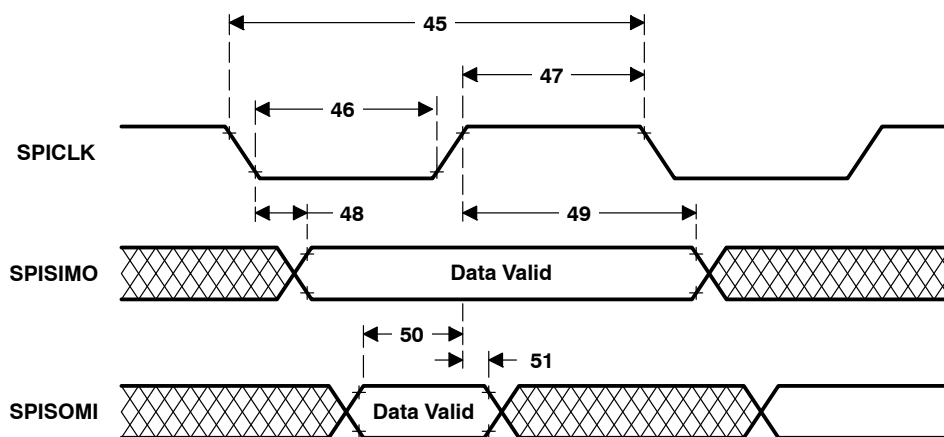
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SPI-slave mode external timing characteristics and requirements (see Note 14 and Figure 33)

NO.		MIN	MAX	UNIT
45	$t_{c(SPC)}S$ Cycle time, SPICLK	$8t_c$		ns
46	$t_{w(SPCL)}S$ Pulse duration, SPICLK low	$4t_c - 45$	$0.5t_{c(SPC)}S + 45$	ns
47	$t_{w(SPCH)}S$ Pulse duration, SPICLK high	$4t_c - 45$	$0.5t_{c(SPC)}S + 45$	ns
48	$t_{d(SPCL-SOMI)}S$ Delay time, SPISOMI valid after SPICLK low (polarity = 1)		$3.25t_c + 130$	ns
49	$t_{v(SPCH-SOMI)}S$ Valid time, SPISOMI data valid after SPICLK high (polarity = 1)	$t_{w(SPCH)}S$		ns
50	$t_{su(SIMO-SPCH)}S$ Setup time, SPISIMO to SPICLK high (polarity = 1)	0		ns
51	$t_{v(SPCH-SIMO)}S$ Valid time, SPISIMO data after SPICLK high (polarity = 1)	$3t_c + 100$		ns

NOTE 14: t_c = system-clock cycle time = 1 / SYSCLK



NOTE A: The diagram shows polarity = 1. SPICLK is inverted when polarity = 0.

Figure 33. SPI-Slave External Timing

analog-to-digital converter 1 (ADC1)

The ADC1 converter has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3} . The purpose is to enhance ADC1 performance by preventing digital switching noise of the logic circuitry that can be present on V_{SS1} and V_{CC1} from coupling into the ADC1 analog stage. All ADC1 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution 8-bits (256 values)
 Monotonic Yes
 Output conversion mode 00h to FFh (00 for $V_I \leq V_{SS3}$; FF for $V_I \leq V_{ref}$)
 Conversion time (excluding sample time) $164 t_c$

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC3} Analog supply voltage	4.5	5	5.5	V
	$V_{CC3}-3$		$V_{CC3}+0.3$	
V_{SS3} Analog ground	$V_{SS3}-3$		$V_{SS3}+0.3$	V
V_{ref} Non- V_{CC3} reference†	2.5	V_{CC3}	$V_{CC3} + 0.1$	V
Analog input for conversion	V_{SS3}		V_{ref}	V

† V_{ref} must be stable, within $\pm 1/2$ LSB of the required resolution, during the entire conversion time.

operating characteristics over recommended ranges operating conditions

PARAMETER			MIN	MAX	UNIT
Absolute accuracy†		V _{CC3} = 5.5 V V _{ref} = 5.1 V	±1.5		LSB
Differential/integral linearity error†‡		V _{CC3} = 5.5 V V _{ref} = 5.1 V	±0.9		LSB
I _{CC3}	Analog supply current	Converting	2		mA
		Nonconverting	5		μA
I _I	Input current, AN0 – AN7	0 V ≤ V _I ≤ 5.5 V	2		μA
	I _{ref} input charge current		1		mA
Z _{ref}	Source impedance of V _{ref}	SYSCLK ≤ 3 MHz	24		kΩ
		3 MHz < SYSCLK ≤ 5 MHz	10		kΩ

† Absolute resolution = 20 mV. At $V_{ref} = 5 \text{ V}$, this is one LSB. As V_{ref} decreases, LSB size decreases. Therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

‡ Excluding quantization error of $1/2$ LSB

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analog-to-digital converter 1 (ADC1) (continued)

The ADC1 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined so that the high-impedance can be accommodated without penalty to the low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC1 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter will reset the SAMPLE START and CONVERT START bits, signaling that a conversion has started and that the analog signal can be removed.

analog timing requirements

	MIN	MAX	UNIT
$t_{su(S)}$ Setup time, analog to sample command	0		ns
$t_{h(AN)}$ Hold time, analog input from start of conversion	$18t_c$		ns
$t_w(S)$ Pulse duration, sample time per kilohm of source impedance [†]	1		$\mu s/k\Omega$

[†] The value given is valid for a signal with a source impedance > 1 k Ω . If the source impedance is < 1 k Ω , use a minimum sampling time of 1 μs .

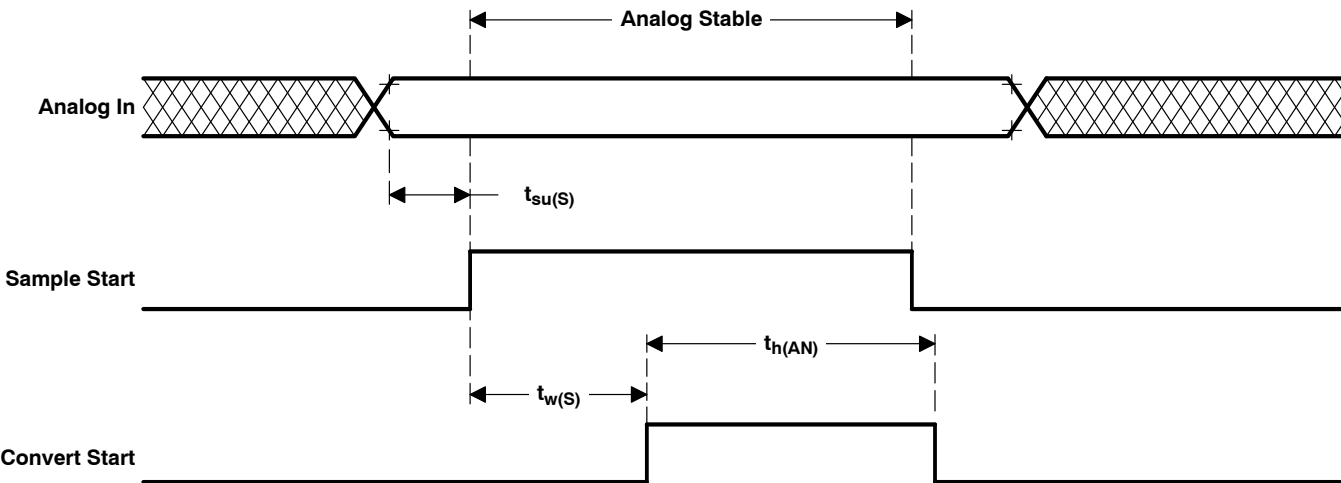


Figure 34. Analog Timing

Table 25 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

Table 25. TMS370Cx6x Family Package Type and Mechanical Cross-Reference

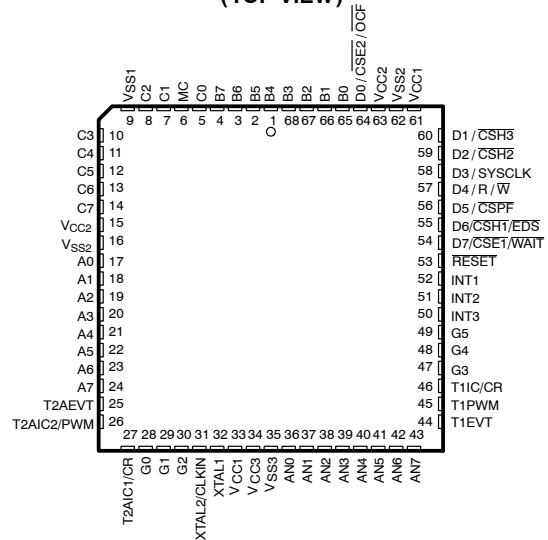
PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 68 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C067AFNA TMS370C067AFNL TMS370C067AFNT TMS370C068AFNA TMS370C068AFNL TMS370C068AFNT TMS370C069AFNA TMS370C069AFNL TMS370C069AFNT TMS370C768AFNT TMS370C769AFNT
FZ – 68 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C768AFZT SE370C769AFZT



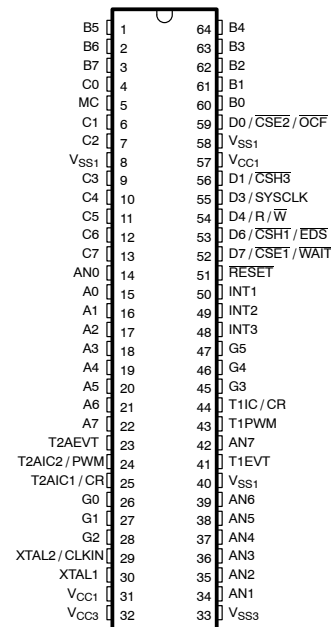
General Information	1
Selection Guide/Tools	2
Ops Cond/Timing/Glossary	3
TMS370Cx0x Data Sheet	4
TMS370Cx1x Data Sheet	5
TMS370Cx2x Data Sheet	6
TMS370Cx32 Data Sheet	7
TMS370Cx36 Data Sheet	8
TMS370Cx4x Data Sheet	9
TMS370Cx5x Data Sheet	10
TMS370Cx6x Data Sheet	11
TMS370Cx7x Data Sheet	12
TMS370Cx8x Data Sheet	13
TMS370Cx9x Data Sheet	14
TMS370CxAx Data Sheet	15
TMS370CxBx Data Sheet	16
TMS370CxCx Data Sheet	17
Mechanical Data	18
Quality and Reliability	19
Electrostatic Discharge Guidelines	20

- **CMOS/EEPROM/EPROM Technologies on a Single Device**
 - Mask-ROM Devices for High-Volume Production
 - One-Time-Programmable (OTP) EPROM Devices for Low-Volume Production
 - Reprogrammable EPROM Devices for Prototyping Purposes
- **Internal System Memory Configurations**
 - On-Chip Program Memory Versions
 - ROM: 24K Bytes
 - EPROM: 24K Bytes
 - Data EEPROM: 256 Bytes
 - Static RAM: 512 Bytes
 - External Memory/Peripheral Wait States
 - Precoded External Chip-Select Outputs in Microcomputer Mode
- **Flexible Operating Features**
 - Low-Power Modes: STANDBY and HALT
 - Commercial, Industrial, and Automotive Temperature Ranges
 - Clock Options:
 - Divide-by-4 (0.5 MHz – 5 MHz SYSCLK)
 - Divide-by-1 (2 MHz – 5 MHz SYSCLK)
 - Phase-Locked Loop (PLL)
 - Supply Voltage (V_{CC}): 5 V $\pm$ 10%
- **Eight-Channel 8-Bit Analog-to-Digital Converter 1 (ADC1)**
- **TMS370 Series Compatibility**
 - Instructions Upwardly Compatible With All TMS370 Devices
 - Register-to-Register Architecture
 - 256 General-Purpose Registers
 - 14 Powerful Addressing Modes
- **Two 16-Bit General-Purpose Timers**
- **On-Chip 24-Bit Watchdog Timer**
- **Flexible Interrupt Handling**
- **CMOS/Package/TTL-Compatible I/O Pins**
 - 64-Pin Plastic and Ceramic Shrink Dual-In-Line Packages /44 Bidirectional, 9 Input Pins
 - 68-Pin Plastic and Ceramic Leaded Chip Carrier Packages /46 Bidirectional, 9 Input Pins
 - All Peripheral Function Pins Are Software Configurable for Digital I/O

**FN/FZ PACKAGE
(TOP VIEW)**



**JN/NM PACKAGE
(TOP VIEW)**



- **Workstation/PC-Based Software Development System**
 - C Compiler and C Source Debugger
 - Real-Time In-Circuit Emulation
 - Extensive Breakpoint/Trace Capability
 - Software Performance Analysis
 - Multi-Window User Interface
 - Microcontroller Programmer



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TMS370Cx7x 8-BIT MICROCONTROLLER

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Pin Descriptions

PIN				I/O†	DESCRIPTION‡
NAME	ALTERNATE FUNCTION	SDIP (64)	LCC (68)		
A0 A1 A2 A3 A4 A5 A6 A7	DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7	15 16 17 18 19 20 21 22	17 18 19 20 21 22 23 24	I/O	Single-chip mode: Port A is a general-purpose bidirectional I/O port. Expansion mode: Port A can be programmed individually as the external bidirectional data bus (DATA0 – DATA7).
B0 B1 B2 B3 B4 B5 B6 B7	ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7	60 61 62 63 64 1 2 3	65 66 67 68 1 2 3 4	I/O	Single-chip mode: Port B is a general-purpose bidirectional I/O port. Expansion mode: Port B can be programmed individually as the low-order address output bus (ADDR0 – ADDR7).
C0 C1 C2 C3 C4 C5 C6 C7	ADDR8 ADDR9 ADDR10 ADDR11 ADDR12 ADDR13 ADDR14 ADDR15	4 6 7 9 10 11 12 13	5 7 8 10 11 12 13 14	I/O	Single-chip mode: Port C is a general-purpose bidirectional I/O port. Expansion mode: Port C can be programmed individually as the high-order address output bus (ADDR8 – ADDR15).
INT1 INT2 INT3	NMI — —	50 49 48	52 51 50	I I/O I/O	External (nonmaskable or maskable) interrupt/general-purpose input pin External maskable interrupt input/general-purpose bidirectional pin External maskable interrupt input/general-purpose bidirectional pin
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	E0 E1 E2 E3 E4 E5 E6 E7	14 34 35 36 37 38 39 42	36 37 38 39 40 41 42 43	I	ADC1 analog input (AN0 – AN7) or positive reference pins (AN1 – AN7) Port E can be programmed individually as general-purpose input pins if not used as ADC1 analog input or positive reference input.
V _{CC3} V _{SS3}		32 33	34 35		ADC1 positive-supply voltage and optional positive-reference input pin ADC1 ground reference pin
RESET		51	53	I/O	System reset bidirectional pin. As an input, $\overline{\text{RESET}}$ initializes the microcontroller; as open-drain output, RESET indicates that an internal failure was detected by the watchdog or oscillator fault circuit.
MC		5	6	I	Mode control (MC) pin. MC enables EEPROM write-protection-override (WPO) mode, also EPROM V _{PP} .
XTAL2/CLKIN XTAL1		29 30	31 32	I O	Internal oscillator crystal input/external clock source input Internal oscillator output for crystal
V _{CC1}		31, 57	33, 61		Positive supply voltage
V _{CC2}		—	15, 63		Positive supply voltage for digital I/O

† I = input, O = output

‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Also, port D3 can be configured as SYSCLK.



Pin Descriptions (Continued)

PIN				I/O†	DESCRIPTION‡		
NAME	ALTERNATE FUNCTION		SDIP (64)			LCC (68)	
V _{SS1}			8, 58,40	9		Ground reference for digital logic	
V _{SS2}			—	16,62		Ground reference for digital I/O logic	
	FUNCTION					Single-chip mode: Port D is a general-purpose bidirectional I/O port. Each of the port D pins can be configured individually as a general-purpose I/O pin, primary memory control signal (function A), or secondary memory control signal (function B). All chip selects are independent and can be used for memory bank switching. Refer to Table 1 for function A memory accesses.	
	A	B					
D0	$\overline{\text{CSE}}_2$	$\overline{\text{OCF}}$	59	64	I/O		I/O pin A: Chip-select eighth output 2 goes low during memory accesses. I/O pin B: Opcode fetch goes low during the opcode fetch memory cycle.
D1	$\overline{\text{CSH}}_3$	—	56	60	I/O		I/O pin A: Chip-select half output 3 goes low during memory accesses. I/O pin B: Reserved
D2	$\overline{\text{CSH}}_2$	—	—	59	I/O		I/O pin A: Chip-select half output 2 goes low during memory accesses. I/O pin B: Reserved
D3	SYSCLK	SYSCLK	55	58	I/O		I/O pin A, B: Internal clock signal is 1/1 (PLL) or 1/4 XTAL2/CLKIN frequency.
D4	R/ $\overline{\text{W}}$	R/ $\overline{\text{W}}$	54	57	I/O		I/O pin A, B: Read/write output pin
D5	$\overline{\text{CSPF}}$	—	—	56	I/O		I/O pin A: Chip-select peripheral output for peripheral file goes low during memory accesses. I/O pin B: Reserved
D6	$\overline{\text{CSH}}_1$	EDS	53	55	I/O	I/O pin A: Chip-select half output 1 goes low during memory accesses. I/O pin B: External data strobe output goes low during memory accesses from external memory and has the same timings as the five chip selects.	
D7	$\overline{\text{CSE}}_1$	WAIT	52	54	I/O	I/O pin A: Chip-select eighth output goes low during memory accesses. I/O pin B: Wait input pin extends bus signals.	
G0 G1 G2 G3 G4 G5			26 27 28 45 46 47	28 29 30 47 48 49	I/O	Port G is a general-purpose bidirectional port.	
T1IC/CR	T1IO1		44	46	I/O	Timer1 input capture/counter-reset input pin/general-purpose bidirectional pin	
T1PWM	T1IO2		43	45	I/O	Timer1 pulse-width-modulation (PWM) output pin/general-purpose bidirectional pin	
T1EVT	T1IO3		41	44	I/O	Timer1 external event input pin/general-purpose bidirectional pin	
T2AIC1/CR	T2AIO1		25	27	I/O	Timer2A input capture 1/counter reset input pin/general-purpose bidirectional pin	
T2AIC2/PWM	T2AIO2		24	26	I/O	Timer2A input capture 2/PWM output pin/general-purpose bidirectional pin	
T2AEVT	T2AIO3		23	25	I/O	Timer2A external event input pin/general-purpose bidirectional pin	

† I = input, O = output

‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Port D3 also can be configured as SYSCLK.

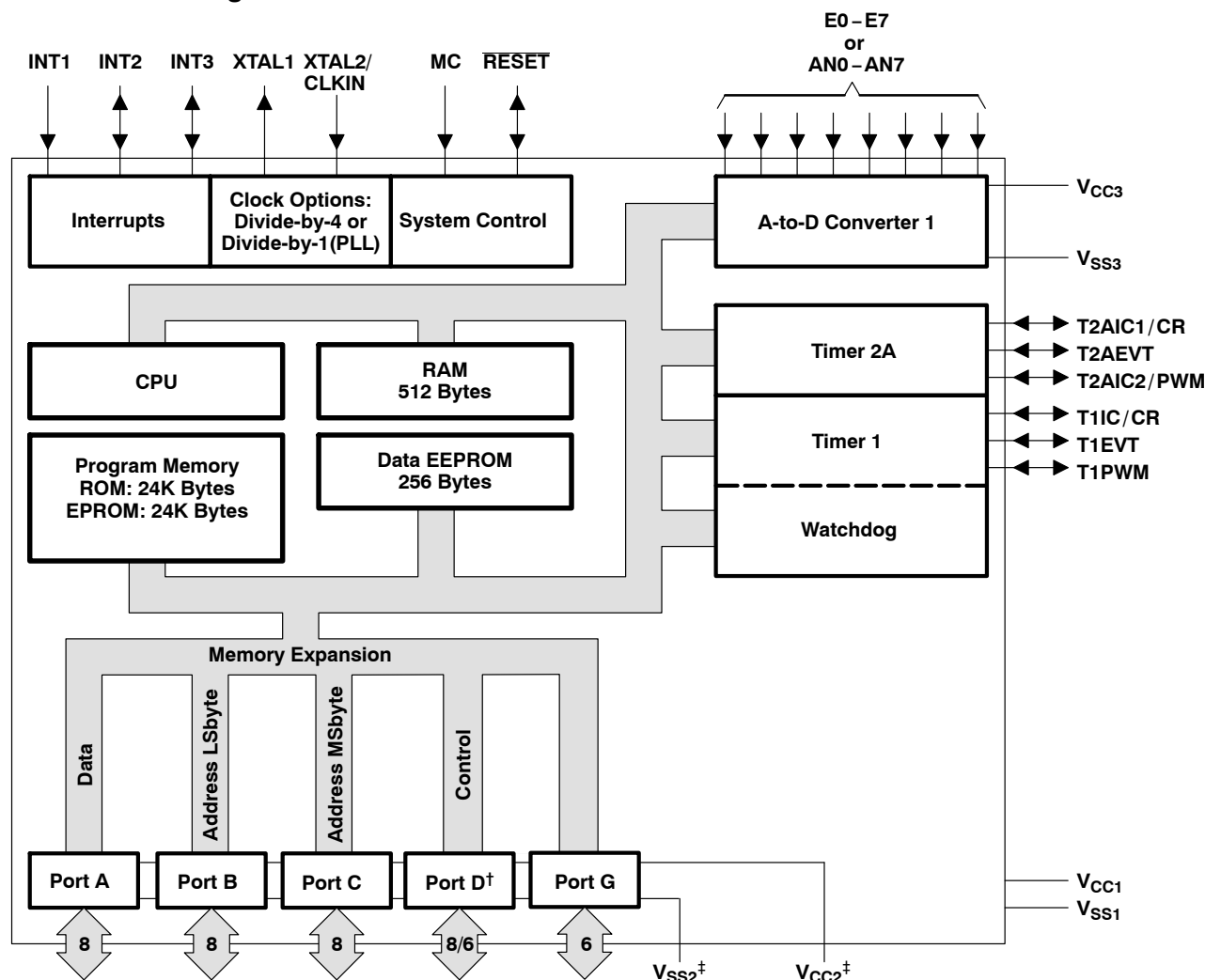
Table 1. Function A: Memory Access Locations for 'x77 Device

FUNCTION A	TMS370Cx77
$\overline{\text{CSE}}_x$	A000h – BFFFh (8K bytes)
$\overline{\text{CSH}}_x$	C000h – FFFFh (16K bytes)
$\overline{\text{CSPF}}$	10C0h – 10FFh (64 bytes)

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functional block diagram



† For the 64-pin devices, there are only six pins for port D.

‡ For the 64-pin devices, omit these power pins

description

The TMS370C077, TMS370C777, and SE370C777 devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx7x refers to these devices. The TMS370 family provides cost-effective real-time system control through integration of advanced peripheral function modules and various on-chip memory configurations.

The TMS370Cx7x family is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technologies. The low-operating power, wide-operating temperature range, and noise immunity of CMOS technology, coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx7x devices attractive in system designs for automotive electronics, industrial motor control, computer peripheral control, telecommunications, and consumer application.

All TMS370Cx7x devices contain the following on-chip peripheral modules:

- Eight-channel, 8-bit analog-to-digital converter 1 (ADC1)
- One 24-bit general-purpose watchdog timer
- Two 16-bit general-purpose timers (one with an 8-bit prescaler)

description (continued)

Table 2 provides a memory configuration overview of the TMS370Cx7x devices.

Table 2. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		OFF-CHIP MEMORY EXPANSION (BYTES)	DATA MEMORY (BYTES)		OPERATING MODES		PACKAGES 68-PIN PLCC/CLCC, OR 64-PIN PSDIP/CSDIP
	ROM	EPROM		RAM	EEPROM	μC†	μP†	
TMS370C077A	24K	—	64K	512	256	√	√	FN – PLCC / NM – PSDIP
TMS370C777A	—	24K	64K	512	256	√	√	FN – PLCC / NM – PSDIP
SE370C777A‡	—	24K	64K	512	256	√	√	FZ – CLCC / JN – CSDIP

† μC – Microcomputer mode

μP – Microprocessor mode

‡ System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.

The suffix letter A appended to the device names shown in the device column of Table 2 indicates the configuration of the device. ROM and EPROM devices have a different configuration as indicated in Table 3. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 3. Suffix Letter Configuration

DEVICE§	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM A	Standard	Divide-by-4 (Standard oscillator)	Enabled
ROM A	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

§ Refer to the “device numbering conventions” section for device nomenclature and the “device part numbers” section for ordering.

The 24K bytes of mask-programmable ROM in the associated TMS370C077 device are replaced with 24K bytes of EPROM in the TMS370C777 while all other available memory and on-chip peripherals are identical. A one-time-programmable device (OTP) (TMS370C777) and a reprogrammable device (SE370C777) are available.

The TMS370C777 OTP device is available in a plastic package. This microcontroller is effective for use as an immediate production update for the TMS370C077 ROM device or for low-volume production runs when the mask charge or cycle time for the low-cost mask-ROM device is not practical.

The SE370C777 has a windowed ceramic package that allows reprogramming of the program EPROM memory during the development/prototyping design phase. The SE370C777 device allows quick updates to breadboards and prototype systems while iterating initial designs.

The TMS370Cx7x family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all CPU activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx7x features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx7x family is fully instruction-set-compatible, allowing easy transition between members of the TMS370 8-bit microcontroller family.

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description (continued)

For large memory applications, the TMS370Cx7x family provides an external bus with non-multiplexed address and data. Precoded memory chip-select outputs can be enabled, allowing minimum-chip-count system implementations. Wait-state support facilitates performance matching among the CPU, external memory, and the peripherals. All pins associated with memory expansion interface are individually software configurable for general-purpose digital input/output (I/O) pins when operating in the microcomputer mode.

The TMS370Cx7x family provides the system designer with very economical, efficient solutions to real-time control applications. The TMS370 family extended development system (XDS™) and compact development tool (CDT™) solve the challenge of efficiently developing the software and hardware required to design the TMS370Cx7x into an ever-increasing number of complex applications. The application source code can be written in assembly and C language, and the output code can be generated by the linker. The TMS370 family XDS development tools communicate through a standard RS-232-C interface with an existing personal computer. This allows the use of personal-computer editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes ease-of-use through extensive use of menus and screen windowing so that a system designer with minimal training can begin developing software. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as a reduced time-to-market cycle.

The TMS370Cx7x family, together with the TMS370 family XDS/22, CDT370, starter kit, software tools, the SE370C777 reprogrammable device, comprehensive product documentation, and customer support, provide a complete solution to the needs of the system designer.

modes

The TMS370Cx7x has four operating modes, two basic modes with each mode having two memory configurations. The basic operating modes are the microcomputer and microprocessor modes, which are selected by the voltage level applied to the dedicated MC pin two cycles before $\overline{\text{RESET}}$ goes inactive. The two memory configurations then are selected through software programming of the internal system configuration registers. The four operating modes are the microcomputer single chip, microcomputer with external expansion, microprocessor without internal program memory, and microprocessor with internal program memory. These modes are described in the following list.

- Microcomputer single-chip mode:
 - Operates as a self-contained microcomputer with all memory and peripherals on-chip
 - Maximizes the general-purpose I/O capability for real-time control applications
- Microcomputer with external expansion mode:
 - Supports bus expansion to external memory or peripherals, while all on-chip memory (RAM, ROM, EPROM, and data EEPROM) remains active
 - Configures digital I/O ports (ports A, B, C, and D) through software, under control of the associated port control, to become external memory as follows:
 - Port A: 8-bit data memory
 - Port B and Port C: 16-bit address memory
 - Port D: 8-bit control memory (pin not used as function A or B can be configured as I/O)
 - Utilizes the pins available (not used for address, data, or control memory) as general-purpose input/output by programming them individually

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modes (continued)

- Lowers the system cost by not requiring an external address/data latch (address memory and data memory are nonmultiplexed)
- Reduces external interface decode logic by using the precoded chip-select outputs that provide direct memory/peripheral chip-select or chip-enable functions
- Function A maps up to 64K bytes of external memory into the address space by using $\overline{\text{CSE1}}$, $\overline{\text{CSE2}}$, $\overline{\text{CSH1}}$, $\overline{\text{CSH2}}$, and $\overline{\text{CSH3}}$ as memory-bank selects under software control.
- Function B maps up to 24K bytes of external memory into the address space by using $\overline{\text{EDS}}$ under software control.
- Microprocessor without internal program memory mode:
 - Ports A, B, C, and D (these ports are not programmable) become the address, data, and control buses for interface to external memory and peripherals.
 - On-chip RAM and data EEPROM remain active, while the on-chip ROM or EPROM is disabled.
 - Program area and the reset, interrupt, and trap vectors are located in off-chip memory locations.
- Microprocessor with internal program memory mode:
 - Configured as the microprocessor without internal program-memory mode with respect to the external bus interface
 - Application program in external memory enables the internal program ROM or EPROM to be active in the system. (Writing a 0 to the memory disabled control bit (SCCR1.2) of the SCCR1 control register accomplishes this.)

memory/peripheral wait operation

The TMS370Cx7x enhances interface flexibility by providing $\overline{\text{WAIT}}$ -state support, decoupling the cycle time of the CPU from the read/write access of the external memory or peripherals. External devices can extend the read/write accesses indefinitely by placing an active low on the $\overline{\text{WAIT}}$ input pin. The CPU continues to wait as long as $\overline{\text{WAIT}}$ remains active.

Programmable automatic wait-state generation is provided also by the TMS370Cx7x on-chip bus controller. Following a hardware reset, the TMS370Cx7x is configured to add automatically one wait state to all external bus transactions and memory and peripheral accesses, making every external access a minimum of three system-clock cycles. The designer can disable the automatic wait-state generation if the AUTOWAIT DISABLE bit in SCCR1 is set to 1. Also, all accesses to the upper four frames of the peripheral file can be extended independently to four system-clock cycles if the PF AUTO WAIT bit in SCCR0 is set to 1. Programmable wait states can be used in conjunction with the external $\overline{\text{WAIT}}$ pin. In applications where the external device read/write access can interface with the TMS370Cx7x CPU using one wait state, the automatic wait-state generation can eliminate external $\overline{\text{WAIT}}$ interface logic, lowering system cost.

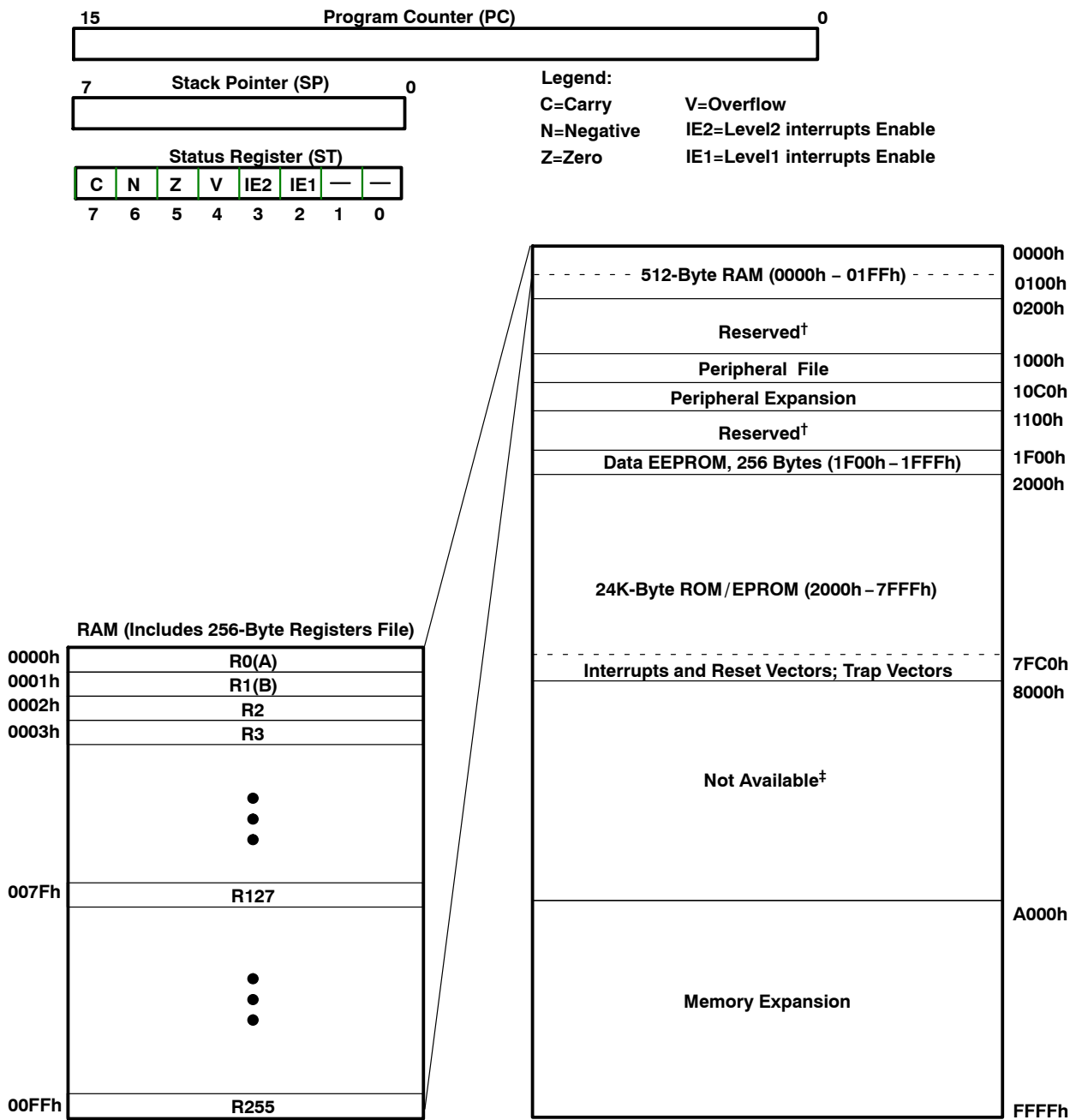
CPU

The CPU used on TMS370Cx7x devices is the high-performance 8-bit TMS370 CPU module. The 'x7x implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'x7x instruction set is summarized in Table 18. Figure 1 illustrates the CPU registers and memory blocks.

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CPU (continued)



† Reserved means that the address space is reserved for future expansion.

‡ Not available means that the address space is not accessible.

Figure 1. Programmer's Model

CPU (continued)

The 'x7x CPU architecture provides the following components:

- CPU registers:
 - A stack pointer that points to the last entry in the memory stack
 - A status register that monitors the operation of the instructions and contains the global-interrupt-enable bits
 - A program counter (PC) that points to the memory location of the next instruction to be executed
- A memory map that includes :
 - 512 bytes of general-purpose RAM that can be data memory storage, program instructions, general-purpose register, or the stack (can be located only in the first 256 bytes)
 - A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM/EPROM programming control
 - A 256-byte EEPROM module that provides in-circuit programmability and data retention in power-off conditions
 - 24K-bytes of ROM or 24K-bytes of EPROM program memory

stack pointer (SP)

The SP is an 8-bit CPU register. Stack operates as a last-in, first-out, read/write memory. The stack is used typically to store the return address on subroutine calls as well as the status register contents during interrupt sequences.

The SP points to the last entry or to the top of the stack. The SP increments automatically before data is pushed onto the stack and decrements after data is popped from the stack. The stack can be located only in the first 256 bytes of the on-chip RAM memory.

status register (ST)

The ST monitors the operation of the instructions and contains the global-interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits:

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional jump instructions) use these status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

The ST register and status-bit notation are shown in Table 4.

Table 4. Status Register

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

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CPU (continued)

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most-significant byte (MSbyte) and least-significant byte (LSbyte) of a 16-bit address.

The contents of the reset vector (7FFEh, 7FFFh) are loaded into the program counter during reset. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 2000h as the contents of memory locations 7FFEh and 7FFFh (reset vector).

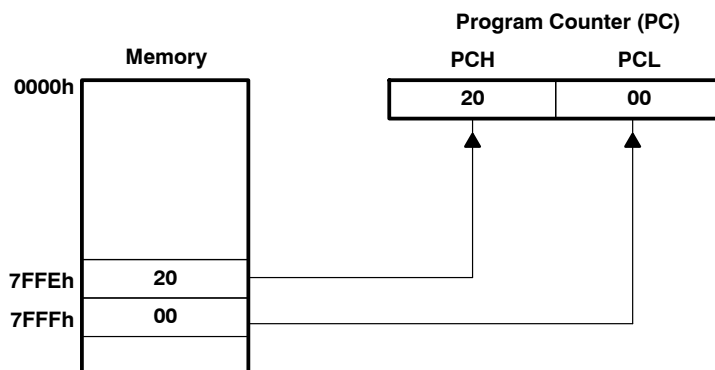


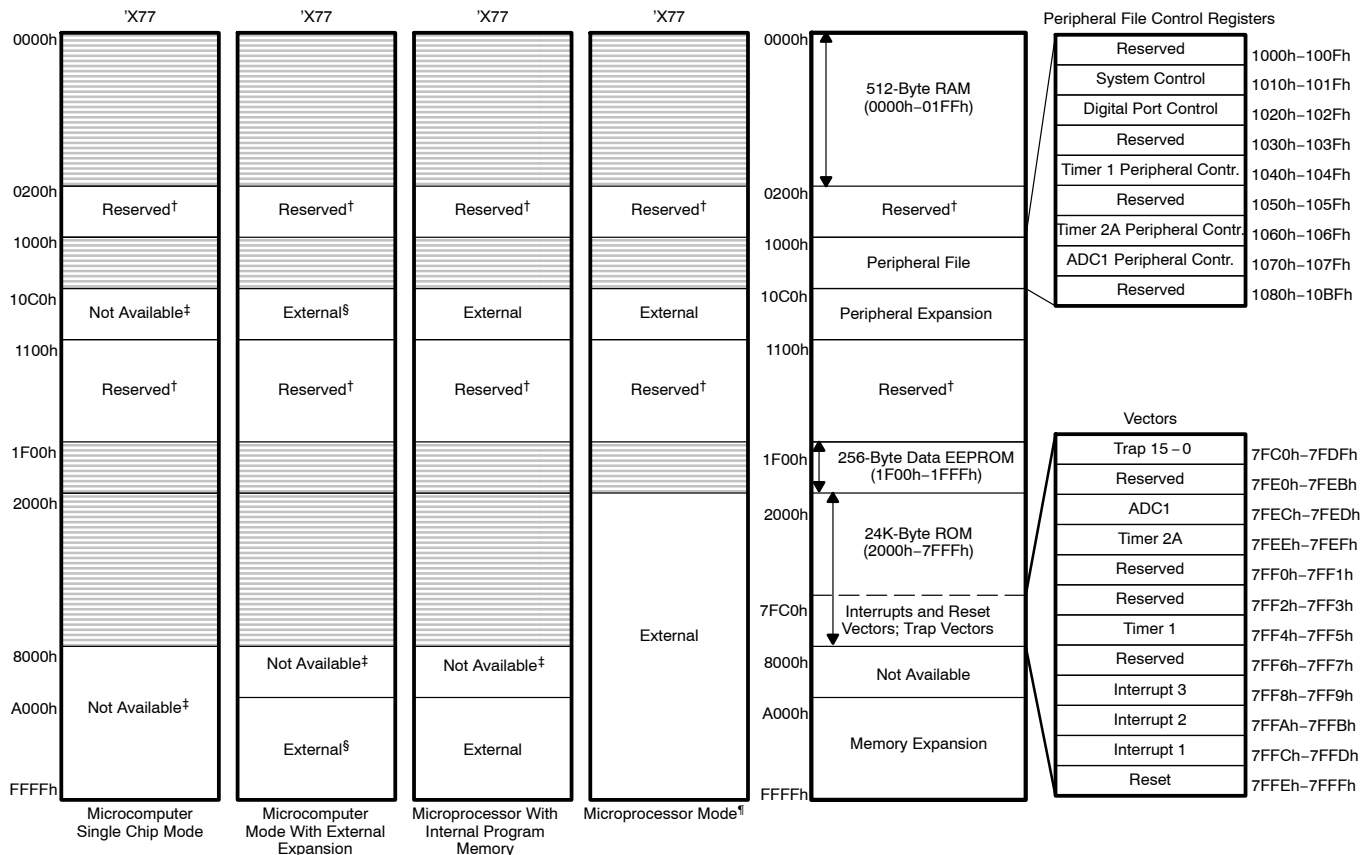
Figure 2. Program Counter After Reset

memory map

The TMS370Cx7x architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory-mapped in this same common address space. In the expansion mode, external memory peripherals are also memory-mapped into this common address. As shown in Figure 3, the TMS370Cx7x provides a 16-bit address range to access internal or external RAM, ROM, data EEPROM, EPROM input/output pins, peripheral functions, and system-interrupt vectors.

The peripheral file contains all input/output port control, on- and off-chip peripheral status and control, EPROM, EEPROM programming, and system-wide control functions. The peripheral file consists of 256 contiguous addresses located from 1000h to 10FFh. The 256 contiguous addresses are divided logically into 16 peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed. The TMS370Cx7x has its on-chip peripherals and system control assigned to peripheral file frames 1 through 7, addresses 1010h through 107Fh.

memory map (continued)



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[†] Reserved = the address space is reserved for future expansion.

[‡] Not available = address space is unavailable in the mode illustrated.

[§] Precoded chip-select outputs available on external expansion bus.

[¶] Microprocessor mode is designed for ROM-less devices, ROM and EPROM devices also can be used but in this mode all on-chip memory is ignored.

Figure 3. TMS370Cx7x Memory Map

RAM/register file (RF)

Locations within RAM address space can serve as either register file or general-purpose read/write memory, program memory, or stack instructions. The TMS370Cx7x device contains 512 bytes of internal RAM mapped beginning at location 0000h and continuing through location 01FFh which is shown in Figure 3. The first 256 bytes of RAM (0000h – 00FFh) are the register files, R0 through R255.

The first two registers, R0 and R1, are also called registers A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

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peripheral file (PF)

The TMS370Cx7x control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the peripheral file (PF) directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator, or by P for a decimal designator. For example, the system control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 5 shows the TMS370Cx7x peripheral files.

Table 5. TMS370Cx7x Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h–100Fh	P000–P00F	Reserved for factory test
1010h–101Fh	P010–P01F	System and EEPROM/EPROM control registers
1020h–103Fh	P020–P03F	Digital I/O port control registers
1040h–104Fh	P040–P04F	Timer 1 registers
1050h–105Fh	P050–P05F	Reserved
1060h–106Fh	P060–P06F	Timer 2A registers
1070h–107Fh	P070–P07F	Analog-to-digital converter 1 registers
1080h–10BFh	P080–P0BF	Reserved
10C0h–10FFh	P0C0–P0FF	External peripheral control

data EEPROM

The TMS370Cx7x devices contain 256 bytes of data EEPROM, and have a memory map beginning at location 1F00h, and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127), or the *TMS370 Family Data Manual* (SPNS014B). The data EEPROM features include the following:

- Programming:
 - Bit, byte, and block write/erase modes
 - Internal charge pump circuitry: No external EEPROM programming voltage supply is needed.
 - Control register: Data EEPROM programming is controlled by the data EEPROM control register (DEECTL) located in the PF frame beginning at location P01A.
 - In-circuit programming capability: There is no need to remove the device to program.
- Write-protection: Writes to the data EEPROM are disabled during the following conditions:
 - Reset: All programming of the data EEPROM module is halted.
 - Write protection active: There is one write-protect bit per 32-byte EEPROM block.
 - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 6 shows the memory map of the control registers.

data EEPROM (continued)

Table 6. Data EEPROM and Program EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME†
101Ah (P01A)	DEECTL	Data EEPROM control register
101Bh (P01B)		Reserved
101Ch (P01C)	EPCTLM	Program EPROM control register – middle array
101Dh (P01D)		Reserved
101Eh (P01E)	EPCTLL	Program EPROM control register – low array

† For the 24K-byte EPROM device, the program memory is controlled by P01C and P01E.

program EPROM

The TMS370C777 contains 24K bytes of program EPROM made up of one 16K-byte array and one 8K-byte array. The 16K-byte array is located at address locations 2000h through 5FFFh, and the 8K-byte array is located at address locations 6000h through 7FFFh, as shown in Table 7.

Table 7. TMS370C777 EPROM Memory Map

PARAMETER	VALUE	
EPROM size	24K Bytes	
Memory mapped	16K Bytes at 2000h – 5FFFh	8K Bytes at 6000h – 7FFFh
Control registers	EPCTLL (P01E)	EPCTLM (P01C)

As shown in Table 7 for the two EPROM areas, the 16K-byte array is controlled by register EPCTLL located at 101Eh (P01E), and the 8K-byte array is controlled by register EPCTLM located at 101Ch (P01C).

Reading the program-EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the program EPROM control registers EPCTLL and EPCTLM. The program EPROM modules' features include:

- Programming
 - In-circuit programming capability if V_{PP} is applied to the MC pin
 - Control register: Program EPROM programming is controlled by the program EPROM control registers EPCTLL and EPCTLM, located at the addresses in PF frame 1 as shown in Table 6.
 - Programming one EPROM module while executing the other
- Write-protection: Writes to the program EPROM are disabled under the following conditions:
 - Reset: All programming to the EPROM module is halted.
 - Low-power modes
 - 13 V not applied to MC

program ROM

The program ROM consists of 24K bytes of mask-programmable ROM. The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication. Memory addresses 7FE0h – 7FEBh is reserved for Texas Instruments (TI™). 7FECh to 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh.

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system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx7x CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are generated internally, while one ($\overline{\text{RESET}}$) is controlled externally. These actions are as follows:

- External $\overline{\text{RESET}}$ pin. A low-level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle (it is possible, however, that a signal of less than one SYSCLK could cause a reset). See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.
- Watchdog (WD) timer. A watchdog-generated reset occurs when an improper value is written to the WD key register or when the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside the recommended operating range. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x7x device to reset external system components. Additionally, if a cold-start condition (e.g., V_{CC} is off for several hundred milliseconds) exists, an oscillator failure occurs, or the $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator fault flag (OSC FLT FLAG, SCCR0.4), the cold start flag (COLD START, SCCR0.7), and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 8 lists the reset sources.

Table 8. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT NAME	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers initialize: ST = 00h, SP = 01h (reset state).
2. Registers A and B initialize to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to by the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state. During $\overline{\text{RESET}}$, the two basic operating modes, which are the microcomputer and microprocessor modes, can be selected by applying the desired voltage level to the dedicated MC pin two cycles before $\overline{\text{RESET}}$ goes inactive (refer to modes section for operating modes description).

When an external reset circuit is connected to $\overline{\text{RESET}}$, $\overline{\text{RESET}}$ must be held low until the clock signal is valid and V_{CC1} is within the operating range. Figure 4 shows a typical reset circuit.



system reset (continued)

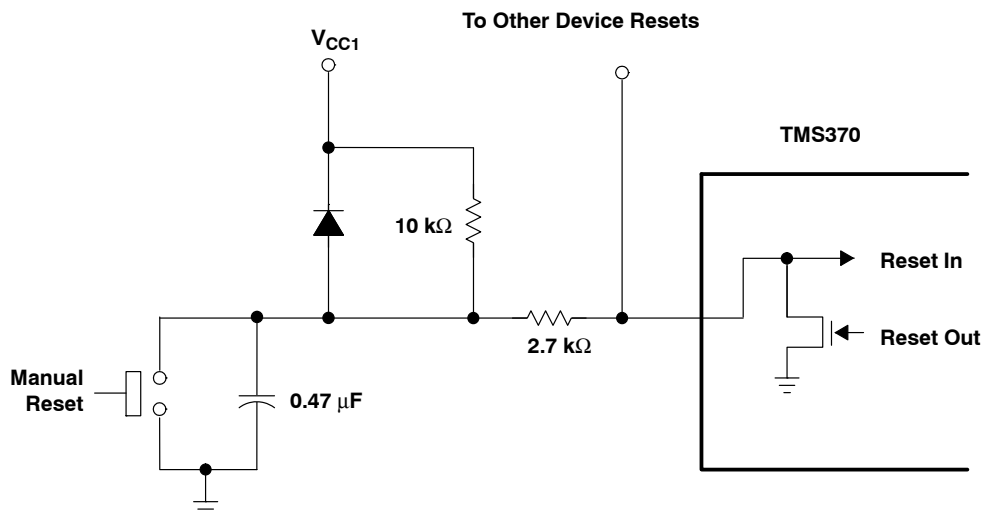


Figure 4. Typical Reset Circuit

interrupts

The TMS370 family software programmable interrupt structure permits flexible on-chip and external-interrupt configurations to meet real-time interrupt-driven application requirements. The hardware-interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global-interrupt mask bits (IE1 and IE2) of the status register.

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is configured selectively on either the high- or low-priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx7x has six hardware-system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 9. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. All of the interrupt sources are maskable individually by local interrupt-enable control bits in the associated peripheral file (PF). Each interrupt source FLAG bit is readable individually for software polling or for determining which interrupt source generated the associated system interrupt. The interrupt-control block diagram is illustrated in Figure 5.

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interrupts (continued)

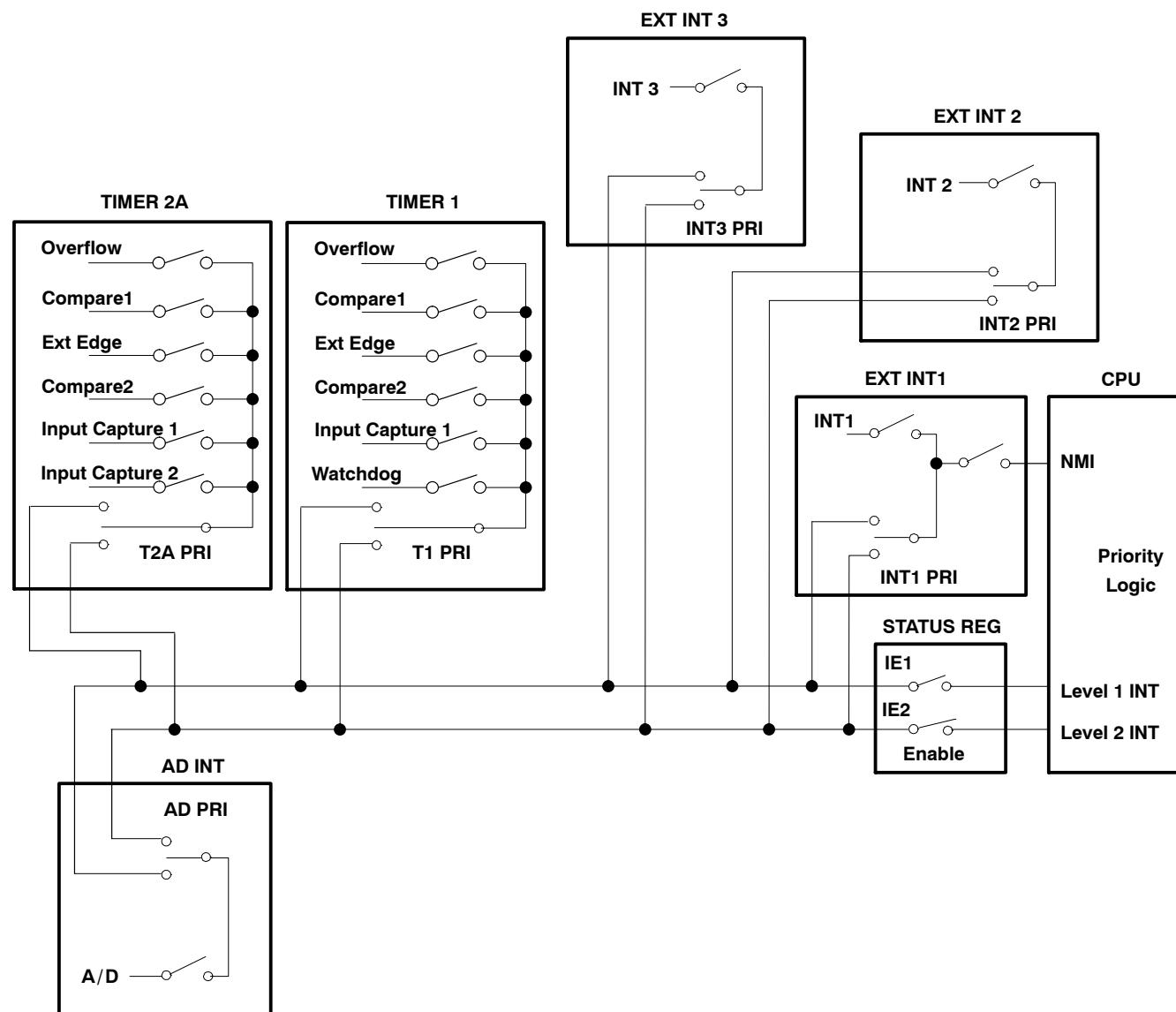


Figure 5. Interrupt Control

Of the six system interrupts, three are generated by on-chip peripherals (T1INT, T2AINT, and ADINT) and three are external interrupts (INT1 – INT3). Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in PF frame 1.

Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as nonmaskable, it cannot be masked by the individual- or global-enable mask bits. The INT1 NMI bit is protected during non-privileged operation and therefore should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software configured as general-purpose input/output pins if the interrupt function is not required (INT1 can be configured similarly as an input pin). Table 9 lists the interrupt vector sources, corresponding addresses, and hardware priorities.

interrupts (continued)

Table 9. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY [†]
External RESET Watchdog overflow Oscillator fault detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	RESET [‡]	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1 [‡]	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2 [‡]	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3 [‡]	7FF8h, 7FF9h	4
Timer 1 overflow Timer 1 compare 1 Timer 1 compare 2 Timer 1 external edge Timer 1 input capture 1 Watchdog overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT [§]	7FF4h, 7FF5h	5
Timer 2A overflow Timer 2A compare 1 Timer 2A compare 2 Timer 2A external edge Timer 2A input capture 1 Timer 2A input capture 2	T2A OVRFL INT FLAG T2AC1 INT FLAG T2AC2 INT FLAG T2AEDGE INT FLAG T2AIC1 INT FLAG T2AIC2 INT FLAG	T2AINT	7FEEh, 7FEFh	6
ADC1 conversion complete	AD INT FLAG	ADINT	7FECh, 7FEDh	7

[†] Relative priority within an interrupt level

[‡] Releases microcontroller from STANDBY and HALT low-power modes

[§] Releases microcontroller from STANDBY low-power mode

privileged operation and EEPROM write-protection override

The TMS370Cx7x family has significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a broad variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx7x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) should be set to 1 to enter the nonprivileged mode, thereby disabling write operations to specific configuration control bits within the peripheral file. Table 10 lists the system configuration bits that are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

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privileged operation and EEPROM write-protection override (continued)

Table 10. Privileged Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCRO	P010.5 P010.6	PF AUTOWAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU TEST BUS TEST PWRDWN/IDLE HALT/STANDBY
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 TEST
T2APRI	P06F.6 P06F.7	T2A PRIORITY T2A TEST
ADPRI	P07F.5 P07F.6 P07F.7	AD ESPEN AD PRIORITY AD TEST

† The privileged bits are shown in a bold typeface in the peripheral file frame 1 section.

The write-protect-override (WPO) mode provides an external hardware method of overriding the write-protection registers of the data EEPROM on the TMS370Cx7x. To enter the WPO mode apply a 12-V input to the MC pin after the **RESET** input goes high (logic 1). The high voltage on MC during the WPO mode is not the programming voltage for the data EEPROM or program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware-system-level capability to modify the content of the data EEPROM while the device remains in the application but only while requiring a 12-V external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power and IDLE modes

The TMS370Cx7x devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time when the mask is manufactured.

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the idle instruction when the PWRDWN/IDLE bit in register SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls which low-power mode is entered.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, and timer 1 remain active. System processing is suspended until a qualified interrupt (hardware **RESET**, external interrupt on INT1, INT2, INT3, or timer 1 interrupt) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx7x is placed in its lowest power-consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware **RESET** or an external interrupt on INT1, INT2, INT3) is detected. The low-power mode selection bits are summarized in Table 11.

low-power and IDLE modes (continued)

Table 11. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X	IDLE

X = don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6–7 bits is ignored. In addition, if an IDLE instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method of always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog is selected. This means that the NMI always is generated, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the watchdog timer is inhibited.

clock modules

The '370Cx7x family provides two clock options which are referred to as divide-by-1 (PLL) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The '370Cx7x ROM-masked devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on the ROM device while the EPROM devices have the divide-by-4 option.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a 1-to-1 match of the external resonator frequency to the internal system clock (SYSCLK) frequency. The divide-by-4 produces a SYSCLK which is one-fourth the frequency of the external resonator. Inside the divide-by-1 module, the frequency of the external resonator is multiplied by four. The clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. The frequencies are formulated as follows:

$$\text{Divide-by-4 option : SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option : SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the improved EMI performance. The harmonics of low-speed resonators extend through less of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 provides the capability of reducing the resonator speed by four times, and this results in a steeper decay of emissions produced by the oscillator.

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system configuration registers

Table 12 lists system configuration, control functions, and registers for controlling EEPROM programming. The privileged bits are bold typefaced and shaded.

Table 12. Peripheral File Frame 1: System Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011		—	—	AUTOWAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLM
P01D	Reserved								
P01E	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLL
P01F	Reserved								

digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 13 lists the specific addresses, registers, and control bits within this peripheral file frame.

Table 13. Peripheral File Frame 2: Digital Port Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P020	Reserved								APORT1
P021	Port A Control Register 2								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	Port B Control Register 2								BPORT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPORT1
P029	Port C Control Register 2								CPORT2
P02A	Port C Data								CDATA
P02B	Port C Direction								CDIR
P02C	Port D Control Register 1								DPORT1
P02D	Port D Control Register 2 [†]								DPORT2
P02E	Port D Data								DDATA
P02F	Port D Direction								DDIR
P030 to P035	Reserved								
P036	–	–	Port G Data						GDATA
P037	–	–	Port G Direction						GDIR

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

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digital port control registers (continued)

Table 14. Port Configuration Register Setup

PORT	PIN	INPUT	OUTPUT	FUNCTION A	FUNCTION B (μ P MODE)
		XPORT1 = 0 [†] XPORT2 = 0 XDATA = y XDIR = 0	XPORT1 = 0 [†] XPORT2 = 0 XDATA = q XDIR = 1	XPORT1 = 0 [†] XPORT2 = 1 XDATA = x XDIR = x	XPORT1 = 1 [†] XPORT2 = 1 XDATA = x XDIR = x
A	0–7	Data In y	Data Out q	Data Bus	Reserved
B	0–7	Data In y	Data Out q	Low ADDR	Reserved
C	0–7	Data In y	Data Out q	Hi ADDR	Reserved
D	0	Data In y	Data Out q	$\overline{\text{CSE2}}$	$\overline{\text{OCF}}$
	1			$\overline{\text{CSH3}}$	—
	2			$\overline{\text{CSH2}}$	—
	3			SYSCLK	SYSCLK
	4			R/ $\overline{\text{W}}$	R/ $\overline{\text{W}}$
	5			$\overline{\text{CSPF}}$	—
	6			$\overline{\text{CSH1}}$	$\overline{\text{EDS}}$
	7			$\overline{\text{CSE1}}$	WAIT
G	0–5	Data In y	Data Out q	Reserved	Reserved
XPORT1 = 1 XPORT2 = 0 XDATA = x XDIR = x } Not defined					

[†] DPORT only

timer 1 (T1) module

The programmable timer 1 (T1) module of the TMS370Cx7x provides the designer with the enhanced timer resources required to perform real-time system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers, T1 and WD, allow program selection of input clock sources (real-time, external event, or pulse-accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The T1 module includes three external device pins that can be used for multiple counter functions (operation-mode dependent) or used as general-purpose I/O pins. The T1 module block diagram is shown in Figure 6.

timer 1 (T1) module (continued)

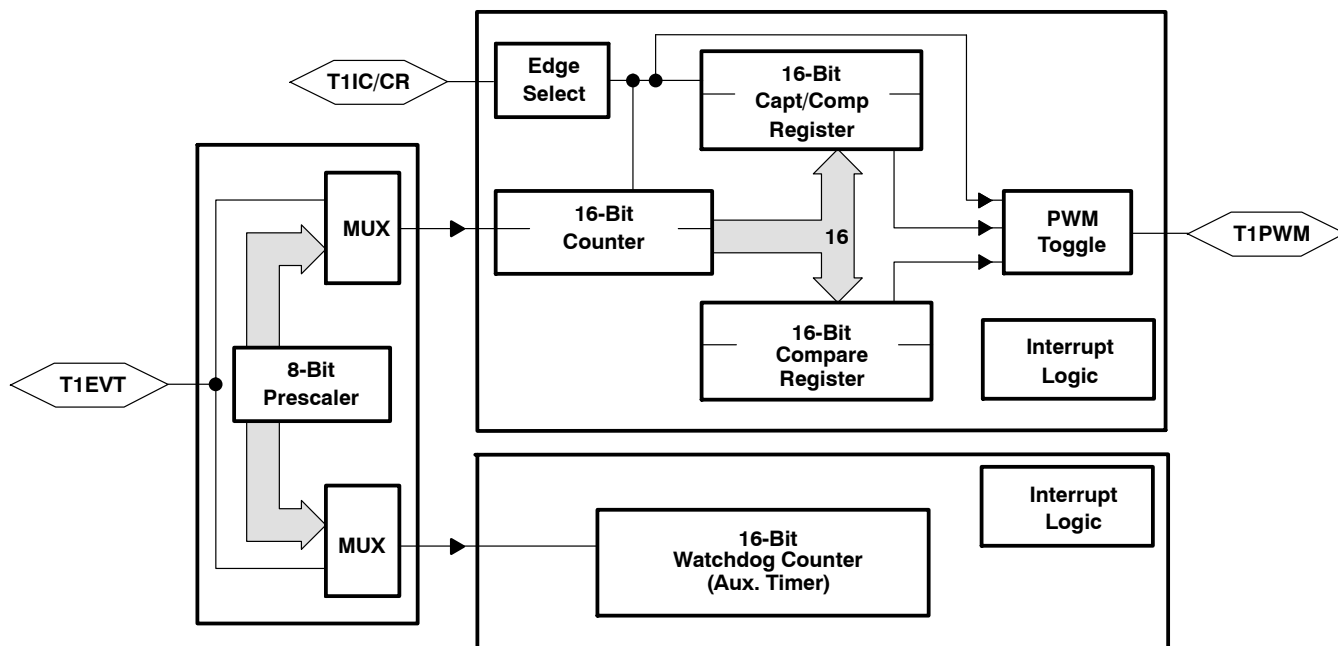


Figure 6. Timer 1 Block Diagram

- Three T1 I/O pins:
 - T1IC/CR: Timer 1 input capture / counter reset input pin, or general-purpose bidirectional I/O pin
 - T1PWM: Timer 1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T1EVT: Timer 1 event input pin, or general-purpose bidirectional I/O pin
- Two operation modes:
 - Dual-compare mode: Provides PWM signal
 - Capture/compare mode: Provides input-capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either capture or compare register.
- One 16-bit watchdog counter can be used as an event counter, a pulse accumulator, or an interval timer if watchdog feature is not needed.
- Prescaler/clock sources that determine one of eight clock sources for general-purpose timer
- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR).

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timer 1 (T1) module (continued)

- Interrupts that can be generated on the occurrence of:
 - A capture
 - A compare equal
 - A counter overflow
 - An external edge detection
- Sixteen T1 module control registers: Located in the PF frame beginning at address P040

Table 15 lists the T1 module control register.

Table 15. Timer 1 Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Capture/Compare and Dual-Compare									
P040	Bit 15			T1 Counter MSbyte				Bit 8	T1CNTR
P041	Bit 7			T1 Counter LSbyte				Bit 0	
P042	Bit 15			Compare Register MSbyte				Bit 8	T1C
P043	Bit 7			Compare Register LSbyte				Bit 0	
P044	Bit 15			Capture/Compare Register MSbyte				Bit 8	T1CC
P045	Bit 7			Capture/Compare Register LSbyte				Bit 0	
P046	Bit 15			Watchdog Counter MSbyte				Bit 8	WDCNTR
P047	Bit 7			Watchdog Counter LSbyte				Bit 0	
P048	Bit 7			Watchdog Reset Key				Bit 0	WDRST
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Capture/Compare and Dual-Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

timer 1 (T1) module (continued)

The T1 capture/compare-mode block diagram is illustrated in Figure 7. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

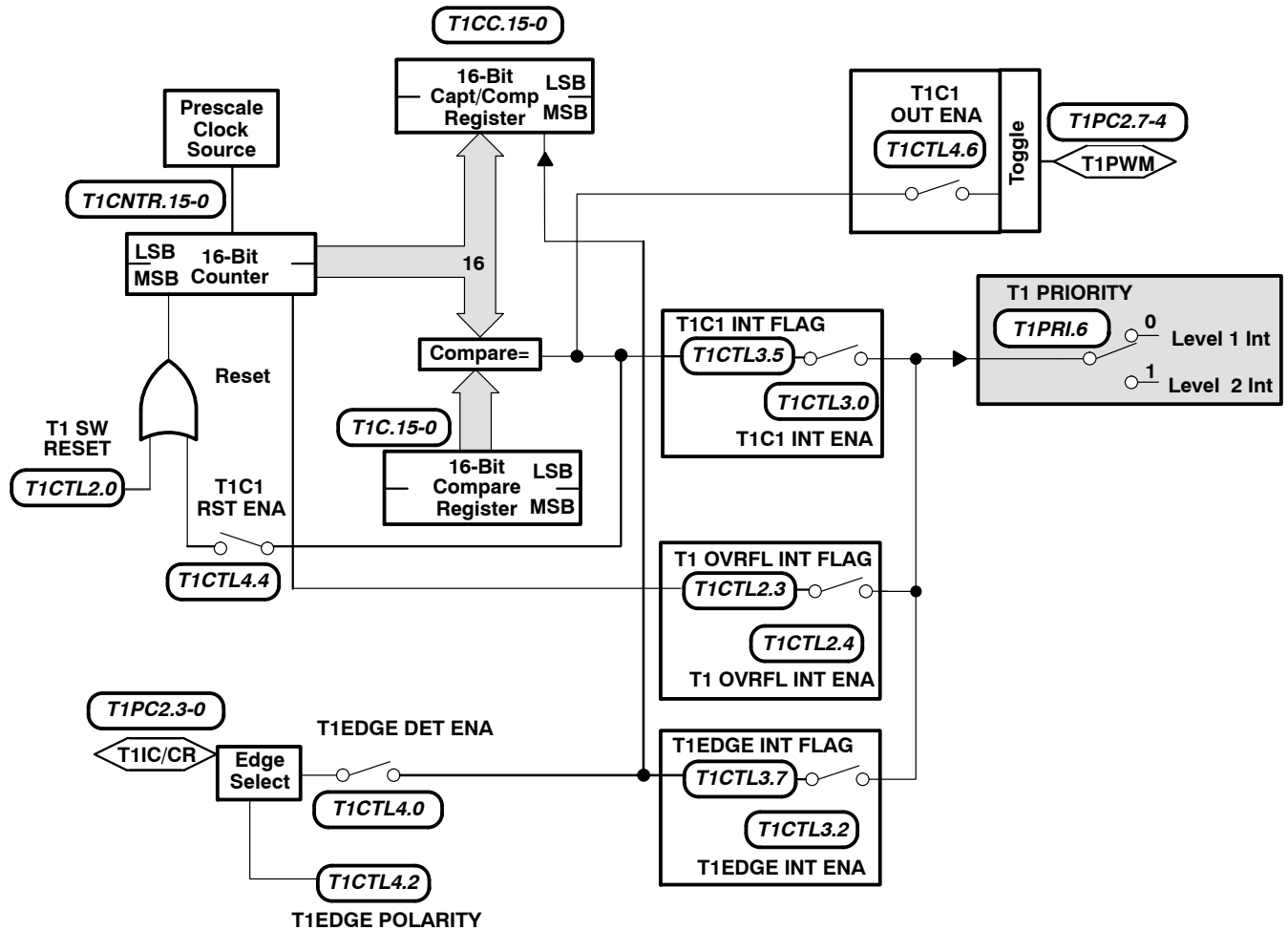


Figure 7. Capture/Compare Mode

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timer 1 (T1) module (continued)

The T1 dual-compare mode block diagram is illustrated in Figure 8. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

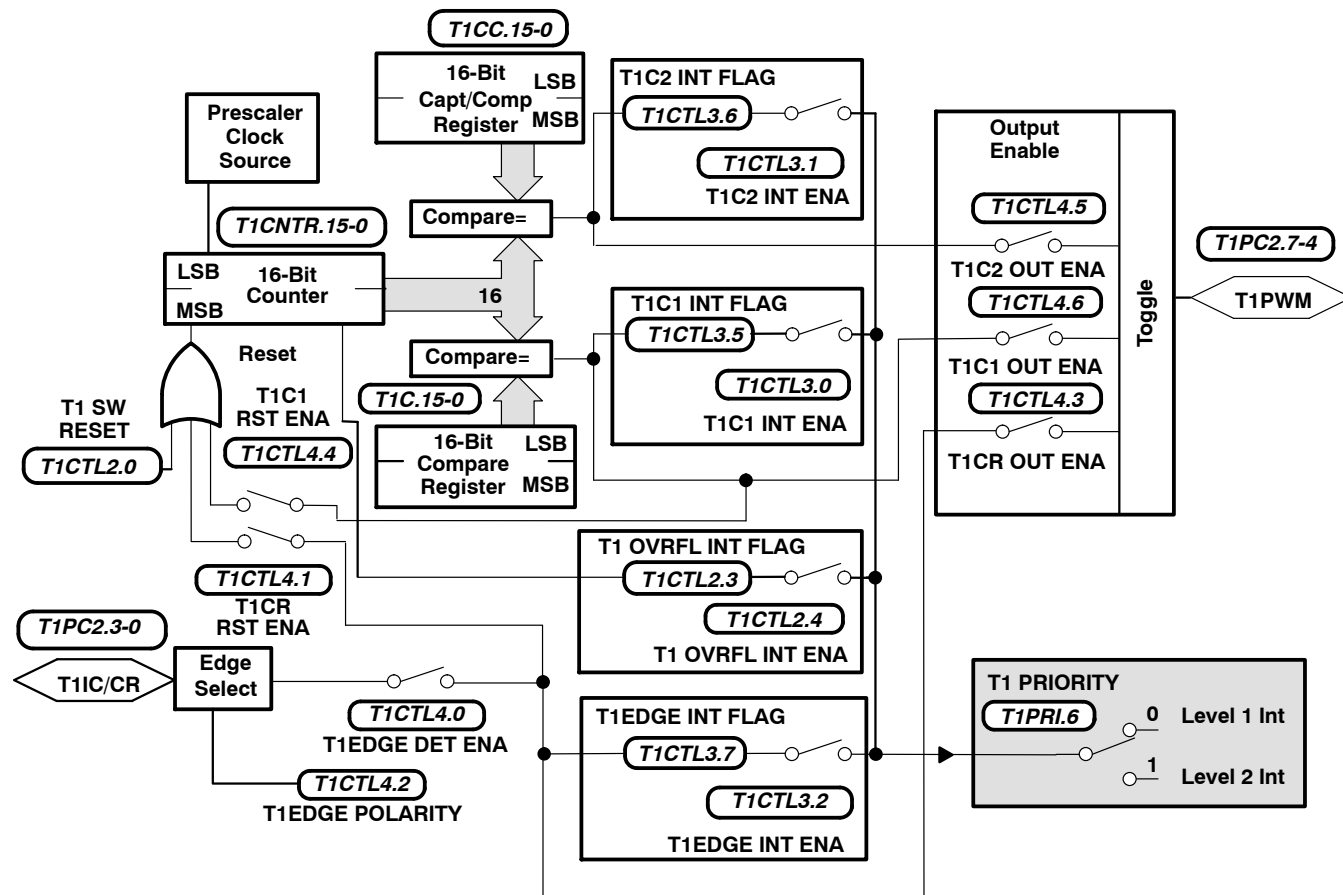


Figure 8. Dual-Compare Mode

timer 1 (T1) module (continued)

The TMS370Cx7x device includes a 24-bit watchdog (WD) timer, contained in the T1 module, which can be software programmed as an event counter, pulse accumulator, or interval timer if the WD function is not used. The WD function is to monitor software and hardware operation, and it implements a system reset when the WD counter is not serviced properly (WD counter overflow or WD counter is reinitialized by an incorrect value). The WD can be configured as one of the three mask options: standard WD, hard WD, or simple counter.

- Standard watchdog configuration for EPROM and mask-ROM devices (see Figure 9)
 - Watchdog
 - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the WD reset key or if the counter overflows
 - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
 - Non-watchdog
 - Watchdog timer can be configured as an event counter, pulse accumulator, or an interval timer

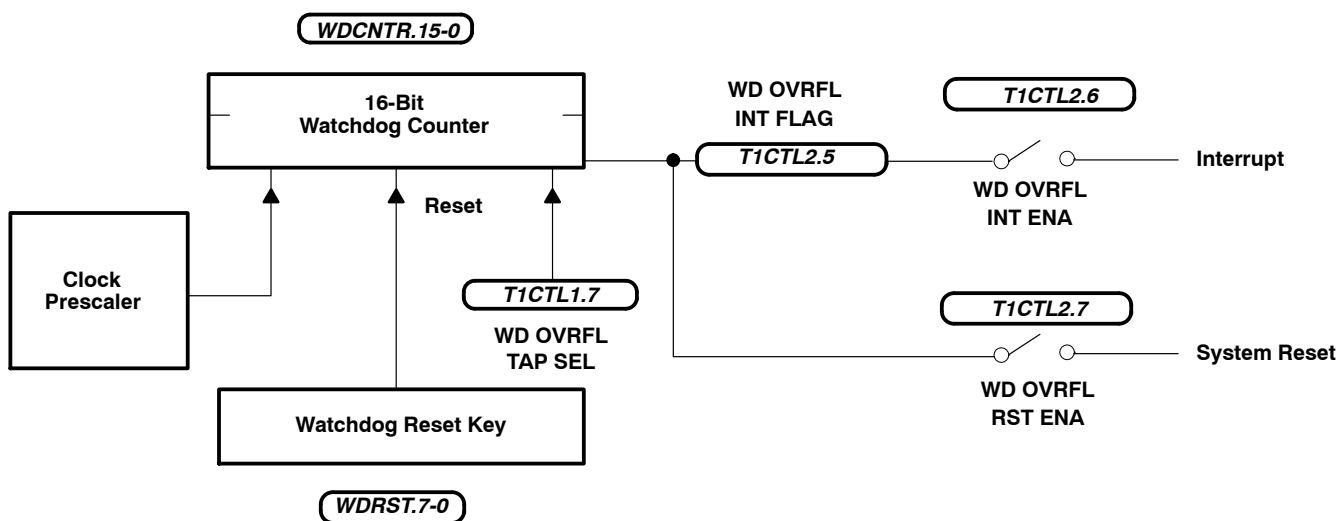


Figure 9. Standard Watchdog

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timer 1 (T1) module (continued)

- Hard watchdog configuration for mask-ROM device (see Figure 10)
 - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows
 - Automatic activation of the WD timer upon power-up reset
 - INT1 is enabled as nonmaskable interrupt during low-power modes
 - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset

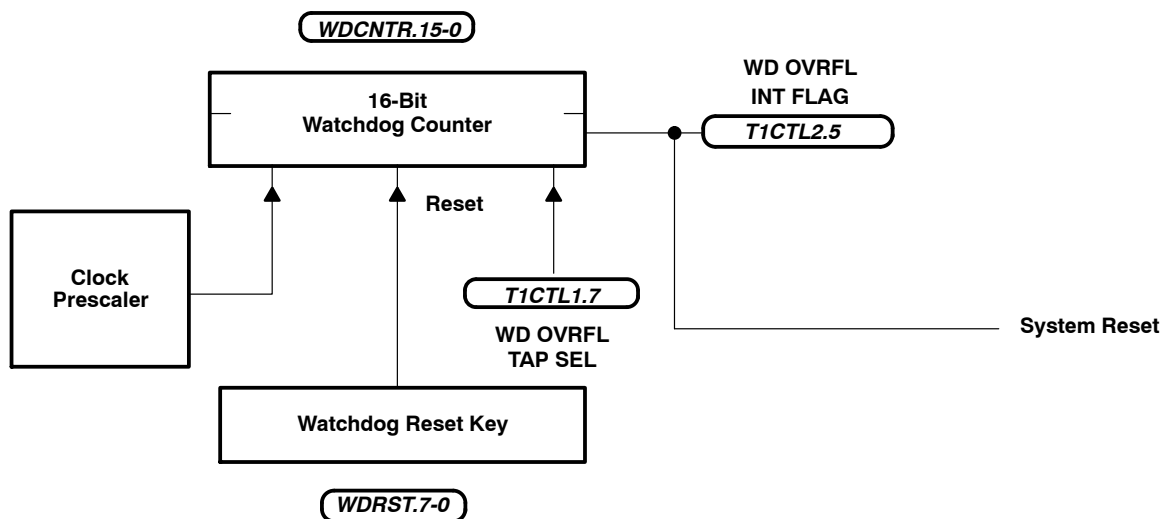


Figure 10. Hard Watchdog

timer 1 (T1) module (continued)

- Simple-counter configuration for mask-ROM devices only (see Figure 11)
 - Simple counter can be configured as an event counter, pulse accumulator, or an interval timer.

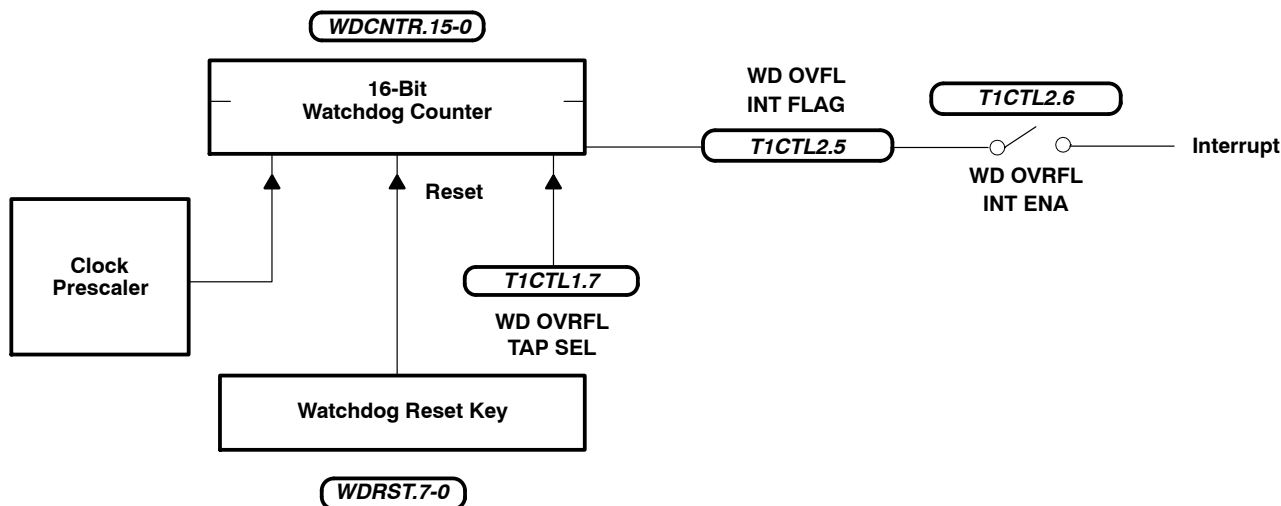


Figure 11. Simple Counter

timer 2A (T2A) module

The 16-bit general-purpose timer 2A (T2A) module is composed of a 16-bit resettable counter, 16-bit compare register with associated compare logic, 16-bit capture register, and a 16-bit register that functions as a capture register in one mode and as a compare register in the other mode. The T2A module adds an additional timer that provides event count, input capture, and compare functions. The T2A module includes three external device pins that can be dedicated as timer functions or used as general-purpose I/O pins. The T2A module block diagram is shown in Figure 12.

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timer 2A (T2A) module (continued)

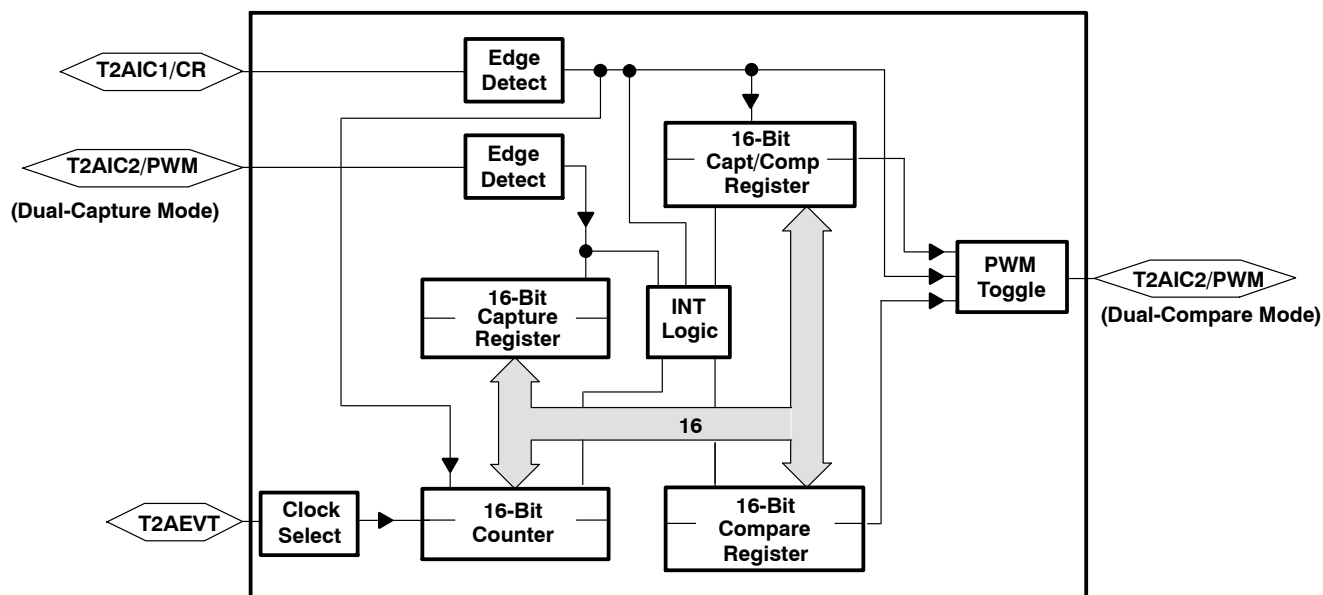


Figure 12. Timer 2A Block Diagram

The T2A module features include the following:

- Three T2A I/O pins:
 - T2AIC1/CR: T2A input capture 1/counter reset input pin, or general-purpose bidirectional I/O pin
 - T2AIC2/PWM: T2A input capture 2/pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T2AEVT: T2A event input pin, or general-purpose bidirectional I/O pin
- Two operation modes:
 - Dual-compare mode: Provides PWM signal
 - Dual-capture mode: Provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture register with associated capture logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register
- T2A clock sources can be any of the following:
 - System clock
 - No clock (the counter is stopped)
 - External clock synchronized to the system clock (event counter)
 - System clock while external input is high (pulse accumulation)

timer 2A (T2A) module (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T2AIC1/CR)
- Interrupts that can be generated on the occurrence of:
 - A compare equal to dedicated-compare register
 - A compare equal to capture-compare register
 - A counter overflow
 - An external edge 1 detection
 - An external edge 2 detection
- Fourteen T2A module control registers located in the PF frame beginning at address P060

The T2A module control registers are listed in Table 16.

Table 16. Timer 2A Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Dual-Compare and Dual-Capture									
P060	Bit 15			T2A Counter MSbyte				Bit 8	T2ACNTR
P061	Bit 7			T2A Counter LSbyte				Bit 0	
P062	Bit 15			Compare Register MSbyte				Bit 8	T2AC
P063	Bit 7			Compare Register LSbyte				Bit 0	
P064	Bit 15			Capture/Compare Register MSbyte				Bit 8	T2ACC
P065	Bit 7			Capture/Compare Register LSbyte				Bit 0	
P066	Bit 15			Capture Register 2 MSbyte				Bit 8	T2AIC
P067	Bit 7			Capture Register 2 LSbyte				Bit 0	
P06A	—	—	—	T2A OVRFL INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1
Mode: Dual-Compare									
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC2 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
Mode: Dual-Capture									
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
Modes: Dual-Compare and Dual-Capture									
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2/PWM DATA IN	T2AIC2/PWM DATA OUT	T2AIC2/PWM FUNCTION	T2AIC2/PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC/CR DATA DIR	T2APC2
P06F	T2A STEST	T2A PRIORITY	—	—	—	—	—	—	T2APRI

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timer 2A (T2A) module (continued)

The timer 2A dual-compare mode block diagram is illustrated in Figure 13. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2ACTL2.0 is 106Bh, bit 0, in the T2ACTL2 register.

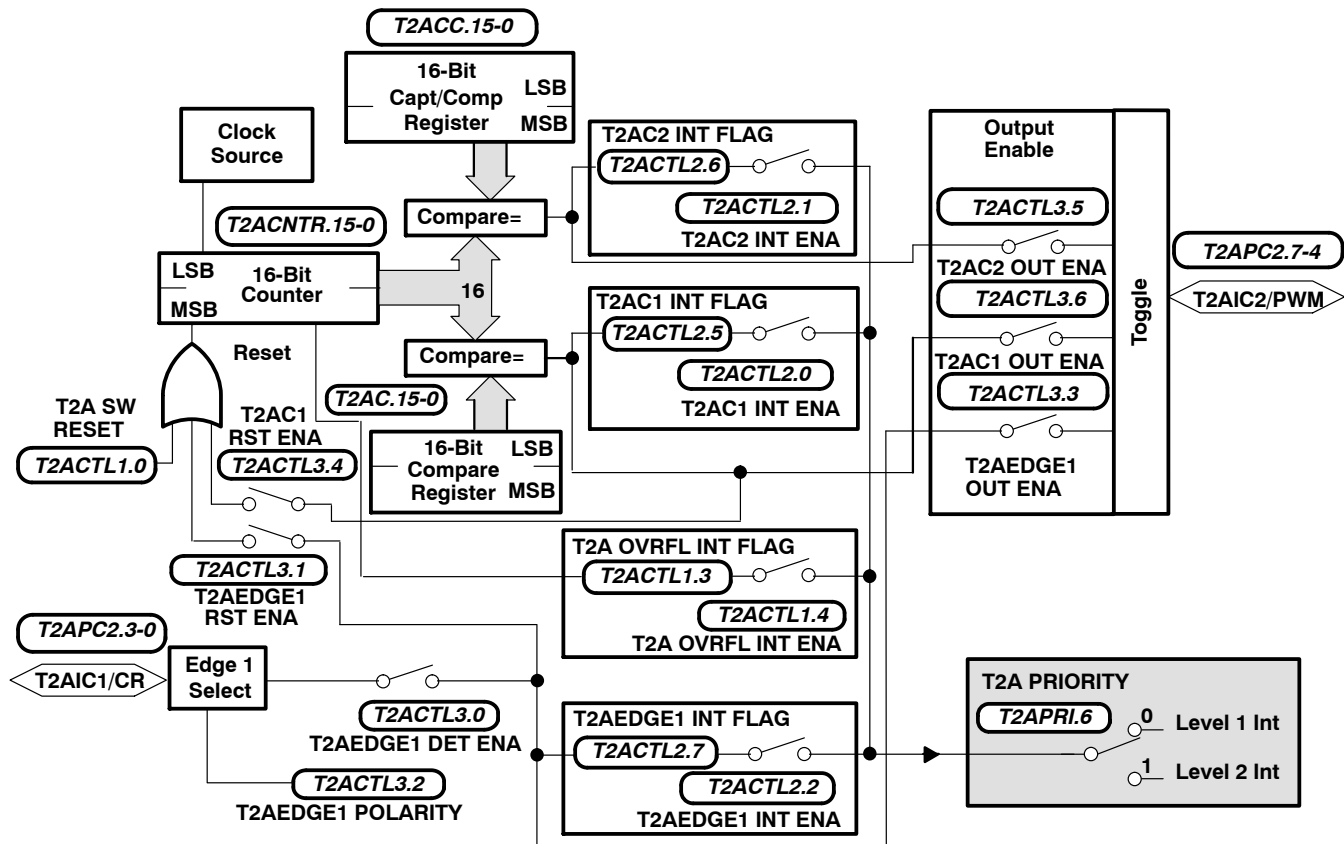


Figure 13. Dual-Compare Mode

timer 2A (T2A) module (continued)

The timer 2A dual-capture mode block diagram is illustrated in Figure 14. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2ACTL2.0 is 106Bh, bit 0, in the T2ACTL2 register.

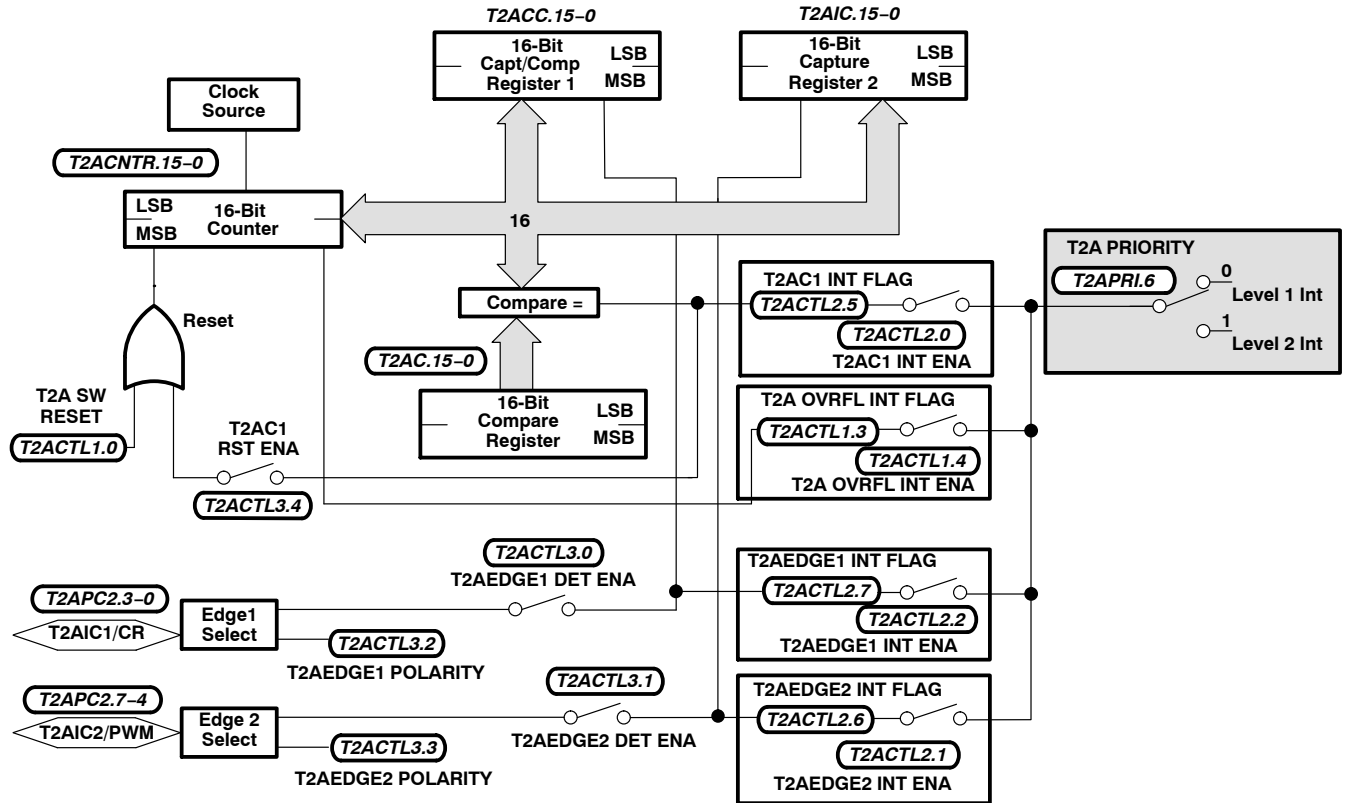


Figure 14. Dual-Capture Mode

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analog-to-digital converter 1 (ADC1) module

The analog-to-digital converter 1 (ADC1) module is an 8-bit, successive approximation converter with internal sample-and-hold circuitry. The module has eight multiplexed analog input channels that allow the processor to convert the voltage levels from up to eight different sources. The ADC1 module features include the following:

- Minimum conversion time: 32.8 μ s at 5-MHz SYSCLK
- Ten external pins:
 - Eight analog input channels (AN0–AN7), any of which can be software configured as digital inputs (E0–E7) if not needed as analog channels. AN1–AN7 also can be configured as positive input voltage reference.
 - V_{CC3} : ADC1 module high-voltage reference input
 - V_{SS3} : ADC1 module low-voltage reference input
- The ADDATA register which contains the digital result of the last ADC1 conversion
- ADC1 operations can be accomplished through either interrupt driven or polled algorithms
- Six ADC1 module control registers are located in the control register frame beginning at address 1070h.

The ADC1 module control registers are listed in Table 17.

Table 17. ADC1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A/D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI

analog-to-digital converter 1 (ADC1) module (continued)

The ADC1 module block diagram is illustrated in Figure 15.

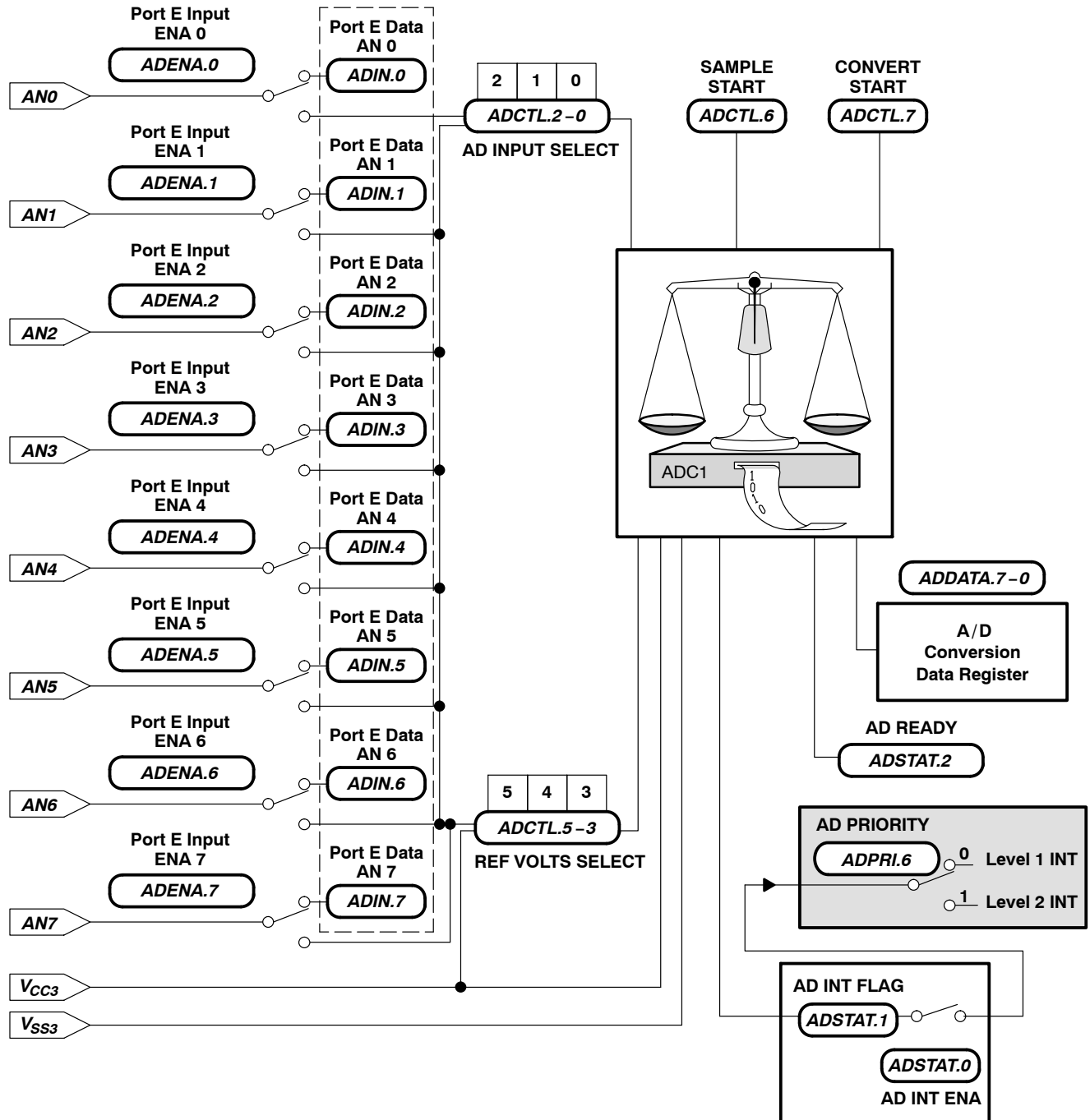


Figure 15. ADC1 Block Diagram

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instruction set overview

Table 18 provides an opcode-to-instruction cross reference of all 73 instructions and 274 opcodes of the '370Cx7x instruction set. The numbers at the top of this table represent the most significant nibble of the opcode while the numbers at the left side of the table represent the least significant nibble. The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

Table 18. TMS370 Family Opcode/Instruction Map†

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JMP #ra 2/7								INCW #ra,Rd 3/11	MOV Ps,A 2/8			CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
1	JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7					MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7
2	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8				MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7
3	JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8	
4	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes	
5	JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14		
6	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6	
7	JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10	
8	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7	
9	JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9	
A	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12	
B	JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8	

† All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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Table 18. TMS370 Family Opcode/Instruction Map[†] (Continued)

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L S N	C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
	D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
	E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
	F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7
Second byte of two-byte instructions (F4xx):														F4	8	MOVW *n[Rn] 4/15	DIV Rn,A 3/14-63
														F4	9	JMPL *n[Rn] 4/16	
														F4	A	MOV *n[Rn],A 4/17	
														F4	B	MOV A,*n[Rn] 4/16	
														F4	C	BR *n[Rn] 4/16	
														F4	D	CMP *n[Rn],A 4/18	
														F4	E	CALL *n[Rn] 4/20	
														F4	F	CALLR *n[Rn] 4/22	

Legend:

- * = Indirect addressing operand prefix
- & = Direct addressing operand prefix
- # = immediate operand
- #16 = immediate 16-bit number
- lab = 16-label
- n = immediate 8-bit number
- Pd = Peripheral register containing destination type
- Pn = Peripheral register
- Ps = Peripheral register containing source byte
- ra = Relative address
- Rd = Register containing destination type
- Rn = **Register file**
- Rp = Register pair
- Rpd = Destination register pair
- Rps = Source Register pair
- Rs = Register containing source byte

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

development system support

The TMS370 family development support tools include an assembler, a C compiler, a linker, an in-circuit emulator (XDS/22), compact development tool, and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
 - Includes extensive macro capability
 - Provides high-speed operation
 - Provides format conversion utilities for popular formats
- ANSI C compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, Sun-3™, or Sun-4™)
 - Generates assembly code for the TMS370 that can be easily inspected
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables direct referencing of the TMS370's port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (compact development tool) Timer real-time in-circuit emulation
 - Base (Part Number EDSCDT37T – for PC, requires cable)
 - Cable for 68-pin PLCC (Part No. EDSTRG68PLCC)
 - Cable for 64-pin SDIP (Part No. EDSTRG64SDIL)
 - Includes EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Uploads/downloads program and data memory
 - Executes programs and software routines
 - Includes 1024 samples trace buffer
 - Includes single-step executable instructions
 - Uses software breakpoints to halt program execution at selected address
- Microcontroller programmer
 - Base (Part No. TMDS3760500A — for PC, requires programmer head)
 - Single unit head for 68-pin PLCC (Part No. TMDS3780510A)
 - Single unit head for 64-pin SDIP (Part No. TMDS3780511A)
 - Includes PC-based, window/function-key oriented user interface for ease of use and rapid learning environment

HP700 is a trademark of Hewlett-Packard Company.
Sun-3 and Sun-4 are trademarks of Sun Microsystems, Inc.



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development system support (continued)

- Starter Kit (Part No. TMDX37000 — for PC)
 - Includes TMS370 assembler diskette and documentation
 - Includes TMS370 simulator
 - Includes programming adapter board and programming software
 - Not included (to be supplied by the user):
 - + 5 V power supply
 - ZIF sockets
 - 9-pin RS232 cable

device numbering conventions

Figure 16 illustrates the numbering and symbol nomenclature for the TMS370Cx7x family.

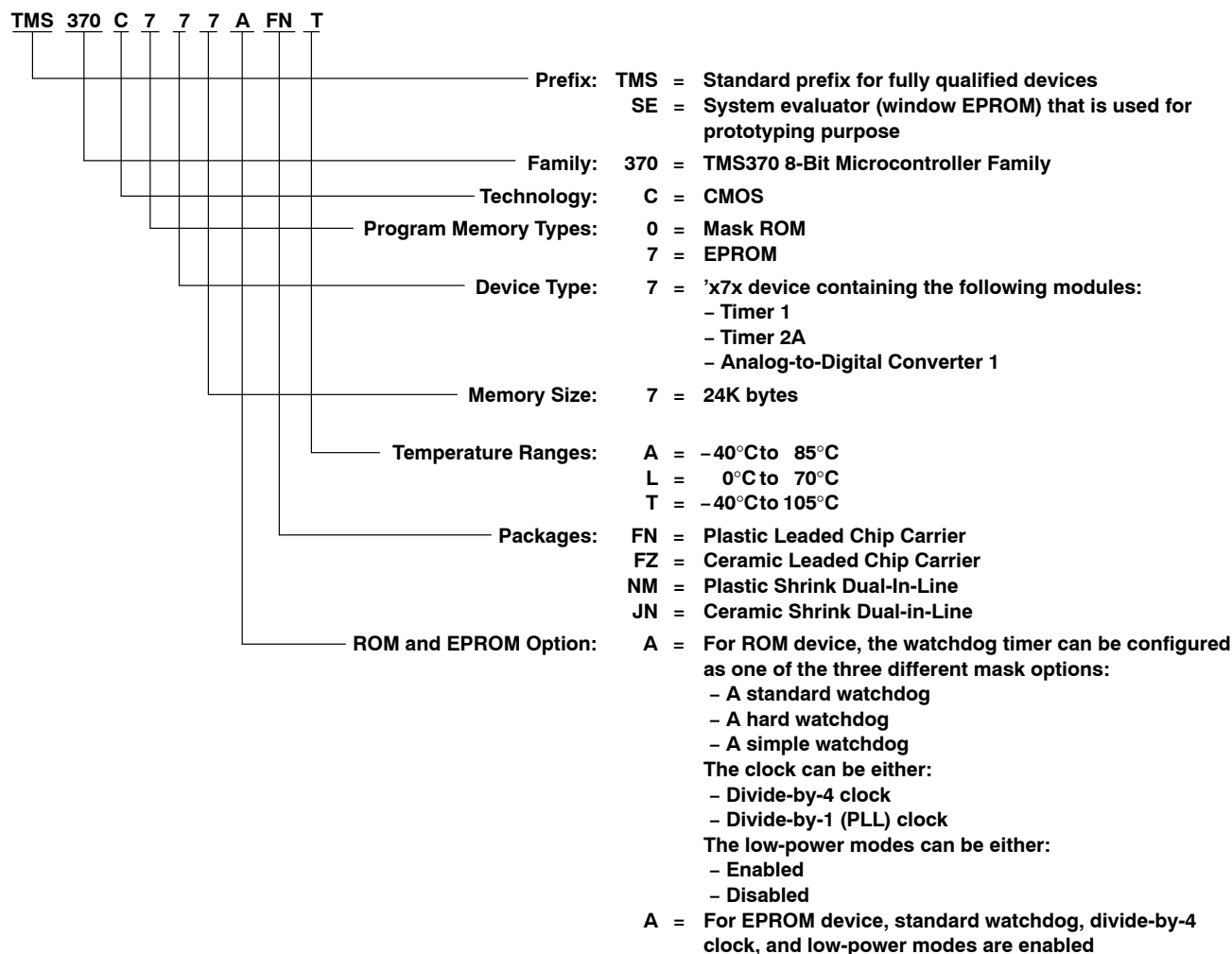


Figure 16. TMS370Cx7x Family Nomenclature

device part numbers

Table 19 lists all the TMS370Cx7x devices available. The device part-number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog-timer options desired. Each device can have only one of the three possible watchdog-timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 19. Device Part Numbers

DEVICE PART NUMBERS FOR 68 PINS (LCC)	DEVICE PART NUMBERS FOR 64 PINS (DIP)
TMS370C077AFNA TMS370C077AFNL TMS370C077AFNT	TMS370C077ANMA TMS370C077ANML TMS370C077ANMT
TMS370C777AFNT	TMS370C777ANMT
SE370C777AFZT [†]	SE370C777AJNT [†]

[†] System evaluators are for use only in prototype environment, and their reliability has not been characterized.

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new code release form

Figure 17 shows a sample of the new code release form.

NEW CODE RELEASE FORM TEXAS INSTRUMENTS TMS370 MICROCONTROLLER PRODUCTS				DATE: _____																
To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information: 1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media) 2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.																				
Company Name: _____ Street Address: _____ Street Address: _____ City: _____ State _____ Zip _____		Contact Mr./Ms.: _____ Phone: (_____) _____ Ext.: _____ Customer Purchase Order Number: _____ Customer Print Number *Yes: _____ # _____ No: _____ (Std. spec to be followed) *If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.																		
Customer Part Number: _____ Customer Application: _____																				
TMS370 Device: _____ TI Customer ROM Number: _____ (provided by Texas Instruments)																				
OSCILLATOR FREQUENCY <table border="1" style="width: 100%; border-collapse: collapse;"><thead><tr><th></th><th>MIN</th><th>TYP</th><th>MAX</th></tr></thead><tbody><tr><td>☐ External Drive (CLKIN)</td><td>_____</td><td>_____</td><td>_____</td></tr><tr><td>☐ Crystal</td><td>_____</td><td>_____</td><td>_____</td></tr><tr><td>☐ Ceramic Resonator</td><td>_____</td><td>_____</td><td>_____</td></tr></tbody></table> ☐ Supply Voltage MIN: _____ MAX: _____ (std range: 4.5V to 5.5V)						MIN	TYP	MAX	☐ External Drive (CLKIN)	_____	_____	_____	☐ Crystal	_____	_____	_____	☐ Ceramic Resonator	_____	_____	_____
	MIN	TYP	MAX																	
☐ External Drive (CLKIN)	_____	_____	_____																	
☐ Crystal	_____	_____	_____																	
☐ Ceramic Resonator	_____	_____	_____																	
TEMPERATURE RANGE <table border="1" style="width: 100%; border-collapse: collapse;"><tbody><tr><td>☐ 'L':</td><td>0° to 70°C (standard)</td></tr><tr><td>☐ 'A':</td><td>-40° to 85°C</td></tr><tr><td>☐ 'T':</td><td>-40° to 105°C</td></tr></tbody></table>					☐ 'L':	0° to 70°C (standard)	☐ 'A':	-40° to 85°C	☐ 'T':	-40° to 105°C										
☐ 'L':	0° to 70°C (standard)																			
☐ 'A':	-40° to 85°C																			
☐ 'T':	-40° to 105°C																			
SYMBOLIZATION ☐ TI standard symbolization ☐ TI standard w/customer part number ☐ Customer symbolization (per attached spec, subject to approval)																				
NON-STANDARD SPECIFICATIONS: ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.																				
RELEASE AUTHORIZATION: This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cycletime commences when this document is signed off and the verification code is approved by the customer.																				
1. Customer: _____ Date: _____		2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____																		

CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS

Low Power Modes	Watchdog counter	Clock Type
☐ Enabled	☐ Standard	☐ Standard (/4)
☐ Disabled	☐ Hard Enabled	☐ PLL (/1)
	☐ Simple Counter	

NOTE:
Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B).

PACKAGE TYPE

☐ 'N' 28-pin PDIP	☐ "FN" 44-pin PLCC
☐ "FN" 28-pin PLCC	☐ "FN" 68-pin PLCC
☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP
☐ "NJ" 40-pin PSDIP (formerly known as N2)	

BUS EXPANSION

☐ YES ☐ NO

Figure 17. Sample New Code Release Form



Table 20 is a collection of all the peripheral file frames using the 'Cx7x (provided for a quick reference).

Table 20. Peripheral File Frame Compilation

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	System Configuration Registers								
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011		—	—	AUTOWAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLM
P01D	Reserved								
P01E	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLL
P01F	Reserved								
	Digital Port Control Registers								
P020	Reserved								APORT1
P021	Port A Control Register 2								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	Port B Control Register 2								BPORT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPORT1
P029	Port C Control Register 2								CPORT2
P02A	Port C Data								CDATA
P02B	Port C Direction								CDIR
P02C	Port D Control Register 1								DPORT1
P02D	Port D Control Register 2†								DPORT2
P02E	Port D Data								DDATA
P02F	Port D Direction								DDIR
P030 to P035	Reserved								
P036	—	—	Port G Data						GDATA
P037	—	—	Port G Direction						GDIR

† To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

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Table 20. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Timer 1 Module Register									
Modes: Capture/Compare and Dual-Compare									
P040	T1 Counter MSbyte							Bit 8	T1CNTR
P041	T1 Counter LSbyte							Bit 0	
P042	Compare Register MSbyte							Bit 8	T1C
P043	Compare Register LSbyte							Bit 0	
P044	Capture/Compare Register MSbyte							Bit 8	T1CC
P045	Capture/Compare Register LSbyte							Bit 0	
P046	Watchdog Counter MSbyte							Bit 8	WDCNTR
P047	Watchdog Counter LSbyte							Bit 0	
P048	Watchdog Reset Key							Bit 0	WDRST
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Capture/Compare and Dual-Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI
T2A Module Register									
Modes: Dual-Compare and Dual-Capture									
P060	T2A Counter MSbyte							Bit 8	T2ACNTR
P061	T2A Counter LSbyte							Bit 0	
P062	Compare Register MSbyte							Bit 8	T2AC
P063	Compare Register LSbyte							Bit 0	
P064	Capture/Compare Register MSbyte							Bit 8	T2ACC
P065	Capture/Compare Register LSbyte							Bit 0	
P066	Capture Register 2 MSbyte							Bit 8	T2AIC
P067	Capture Register 2 LSbyte							Bit 0	

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard WD and to simple counter. The WD input select 2 bits are ignored.



Table 20. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P06A	—	—	—	T2A OVRFL INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1
Mode: Dual-Compare									
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC2 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
Mode: Dual-Capture									
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
Modes: Dual-Compare and Dual-Capture									
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2/PWM DATA IN	T2AIC2/PWM DATA OUT	T2AIC2/PWM FUNCTION	T2AIC2/PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC1/CR DATA DIR	T2APC2
P06F	T2A STEST	T2A PRIORITY	—	—	—	—	—	—	T2APRI
ADC1 Module Control Register									
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A/D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range [‡] V_{CC1} , V_{CC2} , V_{CC3} (see Note 1)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC1}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC1}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC1}) [§]	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	1 W
Operating free-air temperature range, T_A : L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] $V_{CC1} = V_{CC}$

[§] Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

NOTE 1: Unless otherwise noted, all voltage values are with respect to V_{SS1} .

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage (see Note 1)	4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)	3		5.5	
V_{CC2}	Digital I/O supply voltage (see Note 1)	4.5	5	5.5	V
V_{CC3}	Analog supply voltage (see Note 1)	4.5	5	5.5	
V_{SS2}	Digital I/O supply ground	–0.3	0	0.3	V
V_{SS3}	Analog supply ground	–0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC		0.8	V
		MC, normal operation		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET		V_{CC}	V
		MC (non-WPO mode)		$V_{CC1} - 0.3$ to $V_{CC1} + 0.3$	
		XTAL2/CLKIN		$0.8 V_{CC1}$ to V_{CC1}	
		RESET		$0.7 V_{CC1}$ to V_{CC1}	
V_{MC}	MC (mode control) voltage (see Note 3)	EEPROM write protect override (WPO)		11.7 to 13	V
		EPROM programming voltage (V_{PP})		13 to 13.5	
		Microprocessor		$V_{CC1} - 0.3$ to $V_{CC1} + 0.3$	
		Microcomputer		V_{SS1} to 0.3	
T_A	Operating free-air temperature	L version		0 to 70	°C
		A version		–40 to 85	
		T version		–40 to 105	

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS1} .

2. RESET must be activated externally when V_{CC1} or SYSCLK is out of the recommended operating range.

3. The basic microcomputer and microprocessor operating modes are selected by the voltage level applied to the dedicated MC pin two system clock cycles (t_c) before RESET goes inactive (high). The WPO mode can be selected anytime a sufficient voltage is present on MC.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

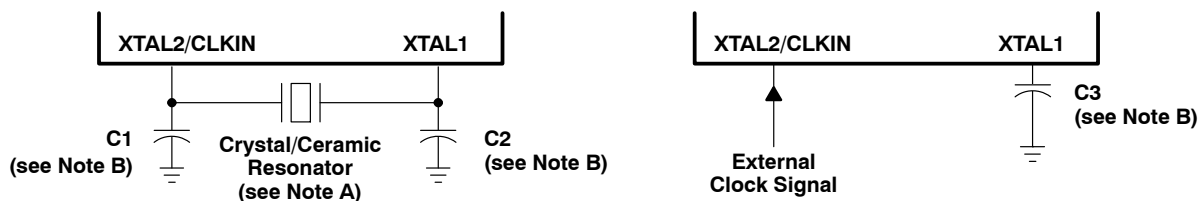
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	$I_{OL} = 1.4 \text{ mA}$			0.4	V
V_{OH}	High-level output voltage	$I_{OH} = -50 \mu\text{A}$	$0.9 V_{CC1}$			V
		$I_{OH} = -2 \text{ mA}$	2.4			
I_I	Input current	MC	$0 \text{ V} < V_I \leq 0.3 \text{ V}$		10	μA
			$0.3 \text{ V} < V_I < V_{CC1} - 0.3 \text{ V}$		50	
			$V_{CC1} - 0.3 \text{ V} \leq V_I \leq V_{CC1} + 0.3 \text{ V}$		10	
			$V_{CC1} + 0.3 \text{ V} < V_I \leq 13 \text{ V}$		650	
			$12 \text{ V} \leq V_I \leq 13 \text{ V}$ See Note 4		50	mA
	I/O pins	$0 \text{ V} \leq V_I \leq V_{CC1}$			± 10	
I_{OL}	Low-level output current	$V_{OL} = 0.4 \text{ V}$	1.4			mA
I_{OH}	High-level output current	$V_{OH} = 0.9 V_{CC1}$	- 50			μA
		$V_{OH} = 2.4 \text{ V}$	- 2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 7)	SYSCLK = 5 MHz See Notes 5 and 6		35	56	mA
		SYSCLK = 3 MHz See Notes 5 and 6		25	36	
		SYSCLK = 0.5 MHz See Notes 5 and 6		13	18	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 8)	SYSCLK = 5 MHz See Notes 5 and 6		12	17	mA
		SYSCLK = 3 MHz See Notes 5 and 6		8	11	
		SYSCLK = 0.5 MHz See Notes 5 and 6		2.5	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 9)	SYSCLK = 3 MHz See Notes 5 and 6		6	8.6	mA
		SYSCLK = 0.5 MHz See Notes 5 and 6		2	3	
	Supply current (HALT mode)	XTAL2/CLKIN < 0.2 V See Note 5		2	30	μA

- NOTES: 4. Input current I_{pp} is a maximum of 50 mA only when programming EPROM.
5. In single chip mode, ports are configured as inputs or outputs with no load. All inputs $\leq 0.2 \text{ V}$ or $\geq V_{CC1} - 0.2 \text{ V}$.
6. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = $0.01 \text{ mA} \times (\text{total load capacitance} + \text{crystal capacitance in pF})$.
7. Maximum operating current for TMS370Cx7x = $10 (\text{SYSCLK}) + 5.8 \text{ mA}$.
8. Maximum standby current for TMS370Cx7x = $3 (\text{SYSCLK}) + 2 \text{ mA}$. (OSC POWER bit = 0).
9. Maximum standby current for TMS370Cx7x = $2.24 (\text{SYSCLK}) + 1.9 \text{ mA}$. (OSC POWER bit = 1, only valid up to 3 MHz SYSCLK).

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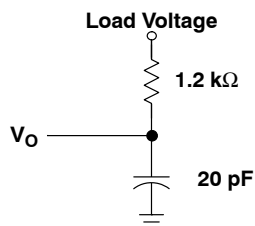
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PARAMETER MEASUREMENT INFORMATION



NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
B. The values of C1 and C2 are typically 15 pF and C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 18. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4 \text{ V}$; Load Voltage = 0 V
Case 2: $V_O = V_{OL} = 0.4 \text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 19. Typical Output Load Circuit (see Note A)

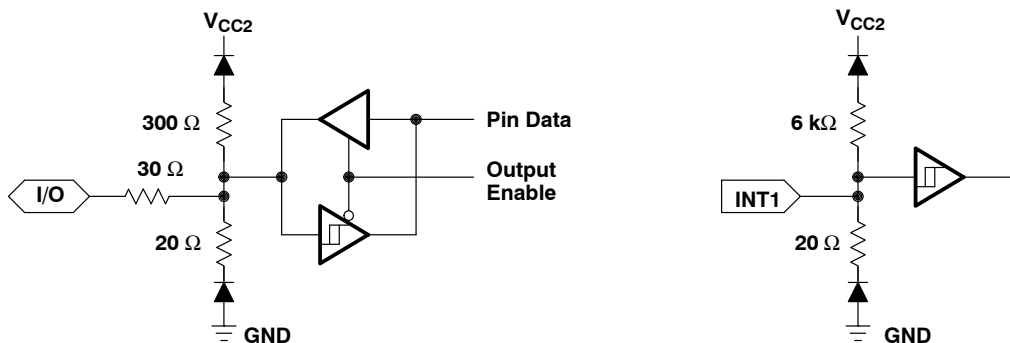


Figure 20. Typical Buffer Circuitry

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

A	Address	IE	Initial
AR	Array	PGM	Program
B	Byte	R	Read
CI	XTAL2/CLKIN	SC	SYSCLK
D	Data	W	Write
E	$\overline{EDS}$	WT	$\overline{WAIT}$
FE	Final		

Lowercase subscripts and their meanings are:

c	cycle time (period)	r	rise time
d	delay time	su	setup time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid
Z	High impedance

All timings are measured between high and low measurement points as indicated in Figure 21 and Figure 22.

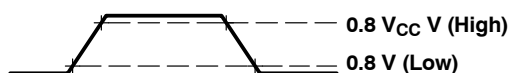


Figure 21. XTAL2/CLKIN Measurement Points

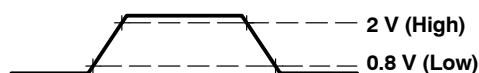


Figure 22. General Measurement Points

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external clocking requirements for clock divided by 4[†]

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 10)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN Crystal operating frequency	2	20	MHz
	SYSCLK System clock [‡]	0.5	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions.

[‡] SYSCLK = CLKIN/4

NOTE 10: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

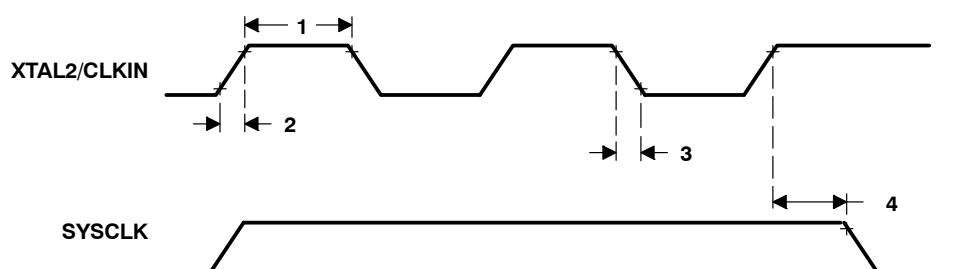


Figure 23. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL)[†]

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 10)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN Crystal operating frequency	2	5	MHz
	SYSCLK System clock [§]	2	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions.

[§] SYSCLK = CLKIN/1

NOTE 10: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

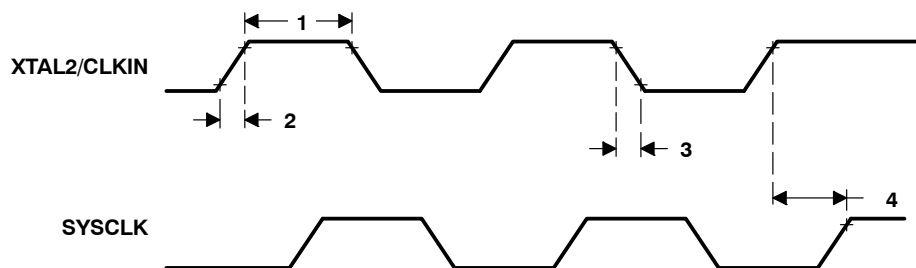


Figure 24. External Clock Timing for Divide-by-1



general purpose output signal switching time requirements

	MIN	NOM	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns

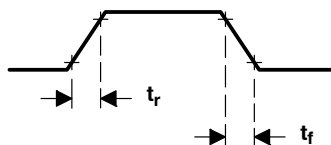


Figure 25. Signal Switching Timing

recommended EEPROM timing requirements for programming

	MIN	MAX	UNIT
$t_{w(PGM)B}$ Pulse duration, programming signal to ensure valid data is stored (byte mode)	10		ms
$t_{w(PGM)AR}$ Pulse duration, programming signal to ensure valid data is stored (array mode)	20		ms

recommended EPROM operating conditions for programming

	MIN	NOM	MAX	UNIT
V_{CC1} Supply voltage	4.75	5.5	6	V
V_{PP} Supply voltage at MC pin	13	13.2	13.5	V
I_{PP} Supply current at MC pin during programming ($V_{PP} = 13$ V)		30	50	mA
SYSCLK System clock	Divide-by-4	0.5	5	MHz
	Divide-by-1	2	5	

recommended EPROM timing requirements for programming

	MIN	NOM	MAX	UNIT
$t_{w(EPGM)}$ Pulse duration, programming signal (see Note 11)	0.40	0.50	3	ms

NOTE 11: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.

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switching characteristics and timing requirements for external read and write[†] (see Figure 26 and Figure 27)

NO.	PARAMETER		MIN	MAX	UNIT	
5	t _c	Cycle time, SYSCLK (system clock)	Divide-by-4 clock	200	2000	ns
			Divide-by-1-(PLL)	200	500	
6	t _{w(SCL)}	Pulse duration, SYSCLK low	0.5t _c –25	0.5t _c	ns	
7	t _{w(SCH)}	Pulse duration, SYSCLK high	0.5t _c	0.5t _c +20	ns	
8	t _{d(SCL-A)}	Delay time, SYSCLK low to address R/ $\overline{W}$ and $\overline{OCF}$ valid		0.25t _c +75	ns	
9	t _{v(A)}	Valid time, address to $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ low	0.5t _c –90		ns	
10	t _{su(D)}	Setup time, write data time to $\overline{EDS}$ high	0.75t _c –80 [‡]		ns	
11	t _{h(EH-A)}	Hold time, address, R/ $\overline{W}$ and $\overline{OCF}$ from $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ high	0.5t _c –60		ns	
12	t _{h(EH-D)W}	Hold time, write data time from $\overline{EDS}$ high	0.75t _c +15		ns	
13	t _{d(DZ-EL)}	Delay time, data-bus high impedance to $\overline{EDS}$ low (read cycle)	0.25t _c –35		ns	
14	t _{d(EH-D)}	Delay time, $\overline{EDS}$ high to data-bus enable (read cycle)	1.25t _c –40		ns	
15	t _{d(EL-DV)R}	Delay time, $\overline{EDS}$ low to read data valid		t _c –95 [‡]	ns	
16	t _{h(EH-D)R}	Hold time, read time from $\overline{EDS}$ high	0		ns	
17	t _{su(WT-SCH)}	Setup time, $\overline{WAIT}$ time to SYSCLK high	0.25t _c +70 [§]		ns	
18	t _{h(SCH-WT)}	Hold time, $\overline{WAIT}$ time from SYSCLK high	0		ns	
19	t _{d(EL-WTV)}	Delay time, $\overline{EDS}$ low to $\overline{WAIT}$ valid		0.5t _c –60	ns	
20	t _w	Pulse duration, $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ low	t _c –80 [‡]	t _c +40 [‡]	ns	
21	t _{d(AV-DV)R}	Delay time, address valid to read data valid		1.5t _c –115 [‡]	ns	
22	t _{d(AV-WTV)}	Delay time, address valid to $\overline{WAIT}$ valid		t _c –115	ns	
23	t _{d(AV-EH)}	Delay time, address valid to $\overline{EDS}$ high (end of write)	1.5t _c –85 [‡]		ns	

[†] t_c = system-clock cycle time = $1/\text{SYSCLK}$

[‡] If wait states, PFWait, or the autowait feature is used, add t_c to this value for each wait state invoked.

[§] If the autowait feature is enabled, the WAIT input can assume a don't care condition until the third cycle of the access. The WAIT signal must be synchronized with the high pulse of the SYSCLK signal while still conforming to the minimum set-up time.



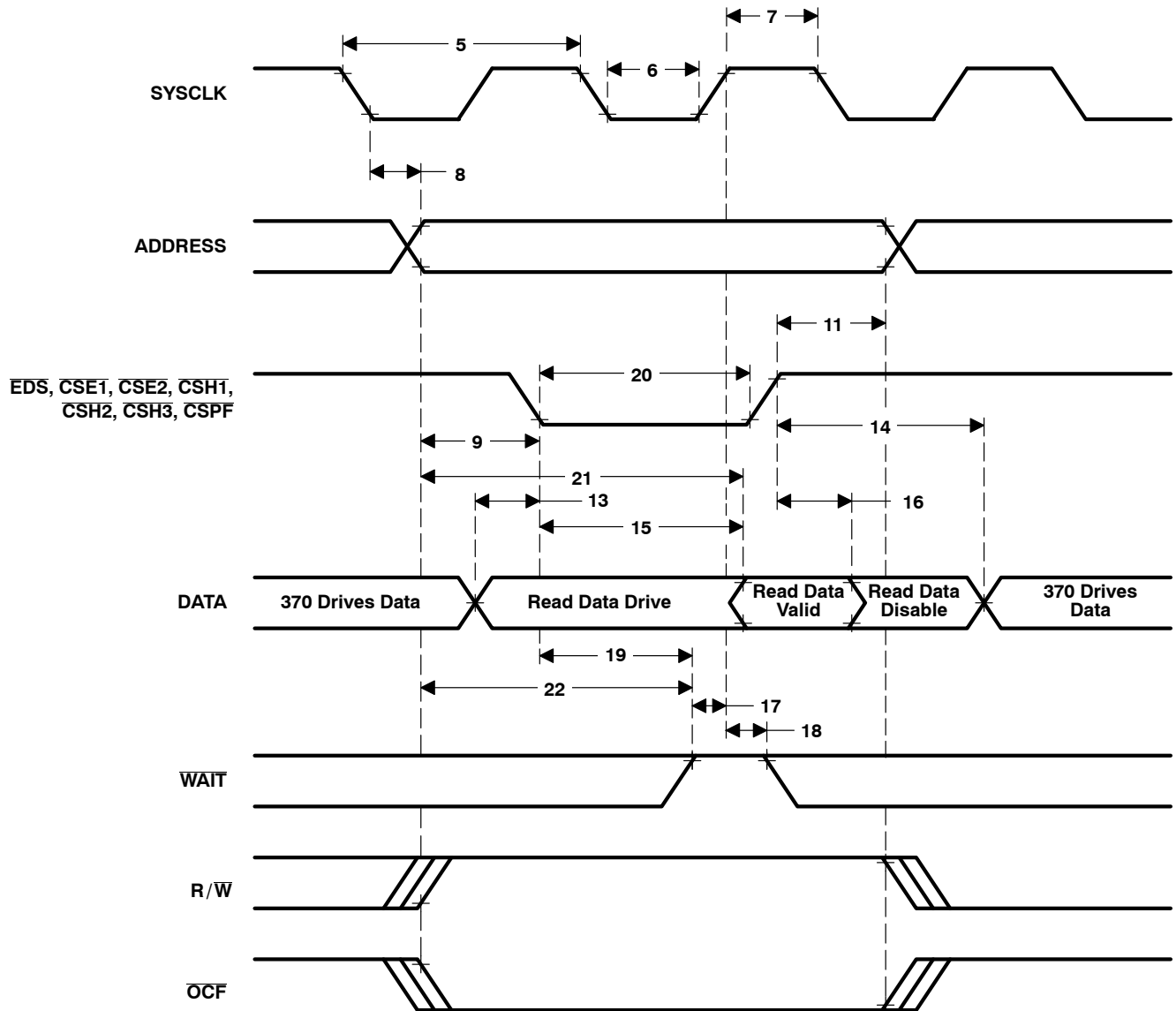


Figure 26. External-Read Timing

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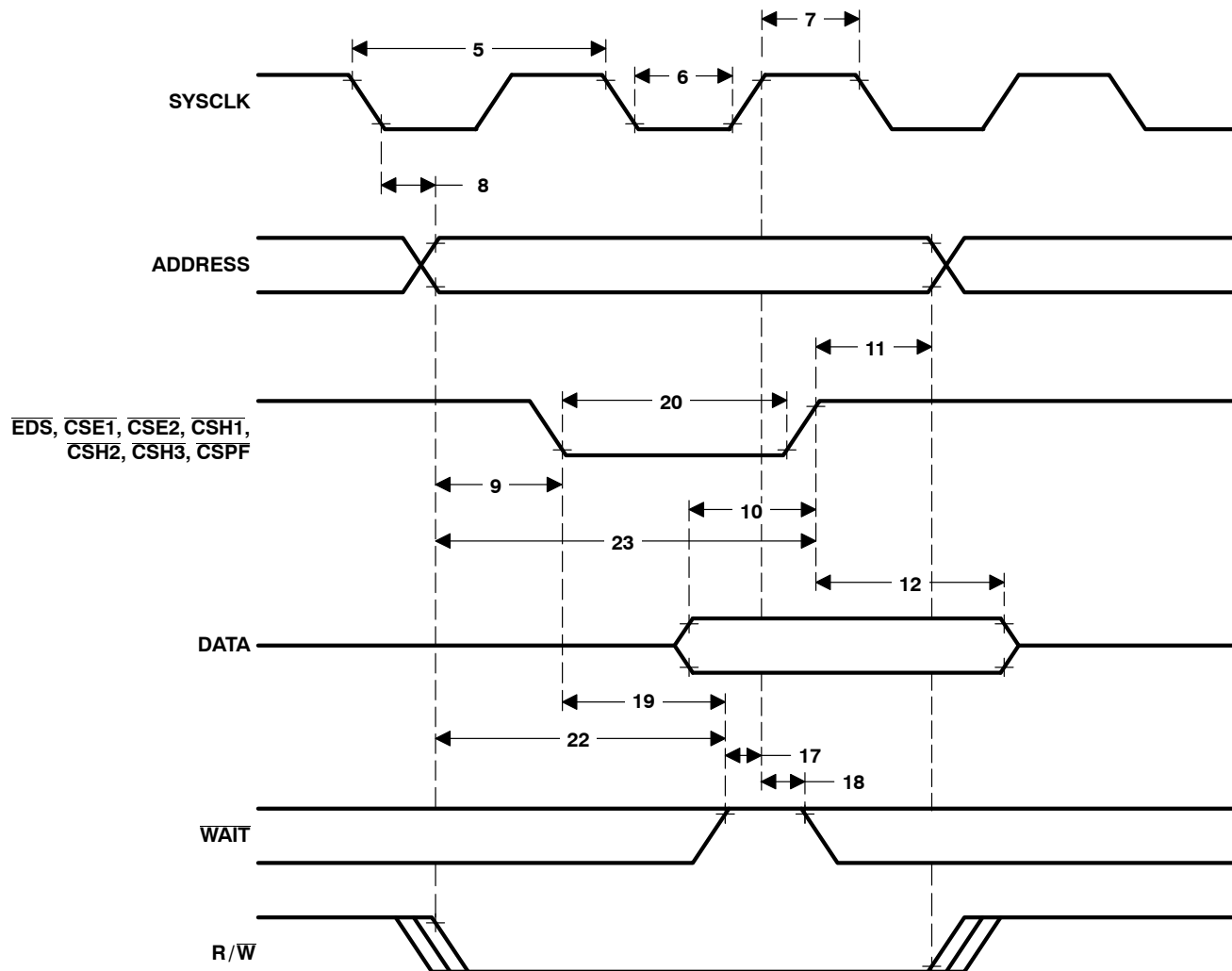


Figure 27. External-Write Timing

analog-to-digital converter 1 (ADC1)

The ADC1 has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3} . The purpose is to enhance ADC1 performance by preventing digital switching noise in the logic circuitry that can be present on V_{SS1} and V_{CC1} when coupling into the A/D analog stage. All ADC1 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution 8-bits (256 values)
 Monotonic Yes
 Output conversion mode 00h to FFh (00 for $V_I \leq V_{SS3}$; FF for $V_I \leq V_{ref}$)
 Conversion time (excluding sample time) $164 t_c$

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC3} Analog supply voltage	4.5	5	5.5	V
	$V_{CC3}-3$		$V_{CC3}+0.3$	
V_{SS3} Analog ground	$V_{SS3}-3$		$V_{SS3}+0.3$	V
V_{ref} Non- V_{CC3} reference†	2.5	V_{CC3}	$V_{CC3} + 0.1$	V
Analog input for conversion	V_{SS3}		V_{ref}	V

† V_{ref} must be stable, within $\pm 1/2$ LSB of the required resolution, during the entire conversion time,

operating characteristics over recommended ranges of operating conditions

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Absolute accuracy‡	$V_{CC3} = 5.5$ V $V_{ref} = 5.1$ V		± 1.5	LSB
Differential/integral linearity error‡§	$V_{CC3} = 5.5$ V $V_{ref} = 5.1$ V		± 0.9	LSB
I_{CC3} Analog supply current	Converting		2	mA
	Nonconverting		5	μ A
I_I Input current, AN0 – AN7	$0 \text{ V} \leq V_I \leq 5.5 \text{ V}$		2	μ A
I_{ref} Input charge current			1	mA
Z_{ref} Source impedance of V_{ref}	$\text{SYSCLK} \leq 3 \text{ MHz}$		24	k Ω
	$3 \text{ MHz} < \text{SYSCLK} \leq 5 \text{ MHz}$		10	k Ω

‡ Absolute resolution = 20 mV. At $V_{ref} = 5$ V, this is one LSB. As V_{ref} decreases, LSB size decreases; therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

§ Excluding quantization error of $1/2$ LSB

analog-to-digital converter 1 (ADC1) (continued)

The ADC1 module allows complete freedom in design of the sources that supply the analog inputs. The period of the sample time is user-defined so that the high impedance can be accommodated without penalty to the low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC1 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter resets the SAMPLE START and CONVERT START bits, signaling that a conversion has started and that the analog signal can be removed.

analog timing requirements

		MIN	MAX	UNIT
$t_{su(S)}$	Setup time, analog to sample command	0		ns
$t_{h(AN)}$	Hold time, analog input from start of conversion	$18t_c$		ns
$t_w(S)$	Pulse duration, sample time per kilohm of source impedance [†]	1		$\mu s/k\Omega$

[†] The value given is valid for a signal with a source impedance > 1 k Ω . If the source impedance is < 1 k Ω , use a minimum sampling time of 1 μs .

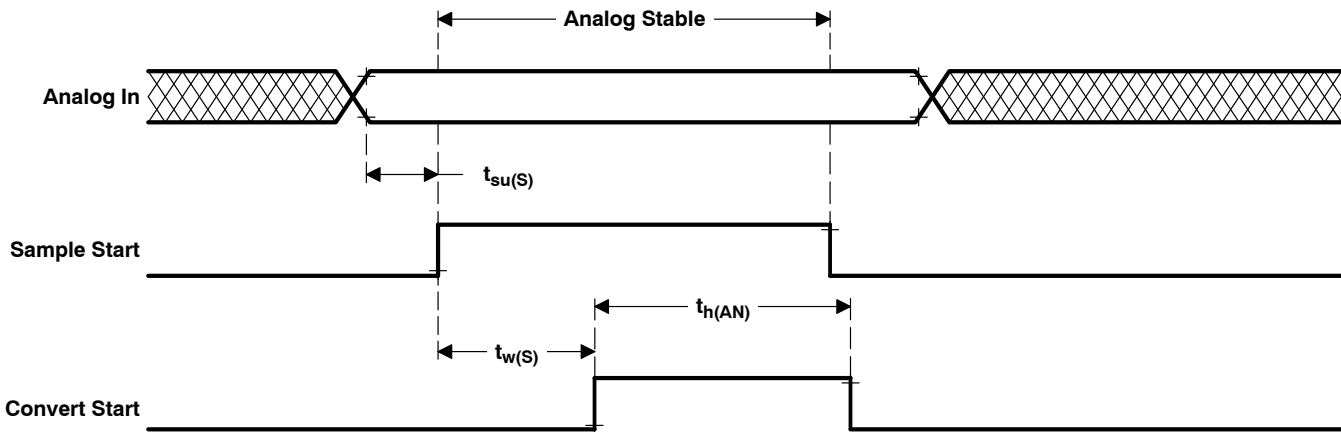


Figure 28. Analog Timing

Table 21 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

Table 21. TMS370Cx7x Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 68 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C077AFNA TMS370C077AFNL TMS370C077AFNT TMS370C777AFNT
FZ – 68 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C777AFZT
JN – 64 pin (70-mil pin spacing)	CERAMIC SHRINK DUAL-IN-LINE PACKAGE (CSDIP)	JN(R-CDIP-T64) CERAMIC DUAL-IN-LINE PACKAGE	SE370C777AJNT
NM – 64 pin (70-mil pin spacing)	PLASTIC SHRINK DUAL-IN-LINE PACKAGE (PSDIP)	NM(R-PDIP-T64) PLASTIC SHRINK DUAL-IN-LINE PACKAGE	TMS370C077ANMA TMS370C077ANML TMS370C077ANMT TMS370C777ANMT

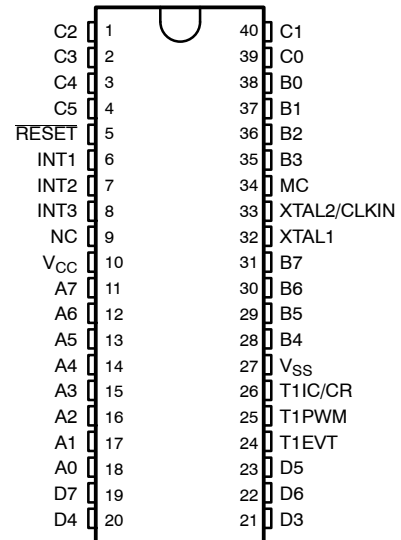
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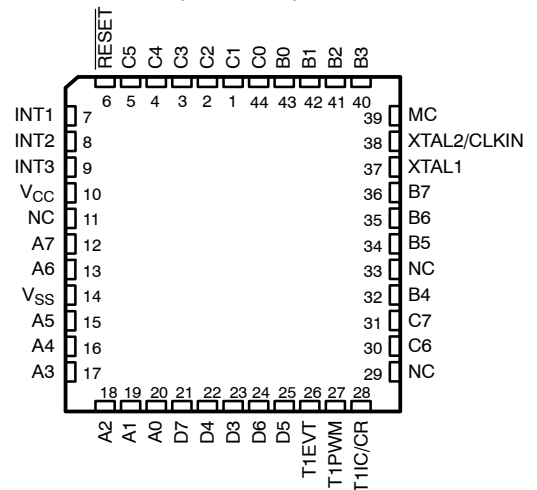
General Information	1
Selection Guide/Tools	2
Ops Cond/Timing/Glossary	3
TMS370Cx0x Data Sheet	4
TMS370Cx1x Data Sheet	5
TMS370Cx2x Data Sheet	6
TMS370Cx32 Data Sheet	7
TMS370Cx36 Data Sheet	8
TMS370Cx4x Data Sheet	9
TMS370Cx5x Data Sheet	10
TMS370Cx6x Data Sheet	11
TMS370Cx7x Data Sheet	12
TMS370Cx8x Data Sheet	13
TMS370Cx9x Data Sheet	14
TMS370CxAx Data Sheet	15
TMS370CxBx Data Sheet	16
TMS370CxCx Data Sheet	17
Mechanical Data	18
Quality and Reliability	19
Electrostatic Discharge Guidelines	20

- **CMOS/EEPROM/EPROM Technologies on a Single Device**
 - Mask-ROM Devices for High-Volume Production
 - One-Time-Programmable (OTP) EPROM Devices for Low-Volume Production
 - Reprogrammable EPROM Devices for Prototyping Purposes
- **Internal System Memory Configurations**
 - On-Chip Program Memory Versions
 - ROM: 4K Bytes
 - EPROM: 16K Bytes
 - Data EEPROM: 256 Bytes
 - Static RAM: 128 or 256 Bytes Usable as Registers
- **Flexible Operating Features**
 - Low-Power Modes: STANDBY and HALT
 - Commercial, Industrial, and Automotive Temperature Ranges
 - Clock Options
 - Divide-by-1 (2 MHz–5 MHz SYSCLK) PLL
 - Divide-by-4 (0.5 MHz–5 MHz SYSCLK)
 - Supply Voltage (V_{CC}) 5 V $\pm$ 10%
- **16-Bit General Purpose Timer**
 - Software Configurable as a 16-Bit Event Counter, or a 16-Bit Pulse Accumulator, or a 16-Bit Input Capture Functions, or Two Compare Registers, or a Self-Contained Pulse Width Modulation (PWM) Function
- **On-Chip 24-Bit Watchdog Timer**
 - EPROM/OTP Device: Standard Watchdog
 - Mask-ROM Devices: Hard Watchdog, Simple Counter, or Standard Watchdog
- **Flexible Interrupt Handling**
 - Two S/W Programmable Interrupt Levels
 - Global- and Individual-Interrupt Masking
 - Programmable Rising- or Falling-Edge Detect
 - Individual Interrupt Vectors
- **TMS370 Series Compatibility**
 - Register-to-Register Architecture
 - 256 General-Purpose Registers
 - 14 Powerful Addressing Modes
 - Instructions Upwardly Compatible With all TMS370 Devices

**N PACKAGE
(TOP VIEW)**



**FZ AND FN PACKAGES
(TOP VIEW)**



- **CMOS/Package/TTL Compatible I/O Pins**
 - 40-Pin Plastic Dual-In-Line Packages/ 32 Bidirectional Pins, 1 Input Pin
 - 44-Pin Plastic Leaded Chip Carrier (LCC) Packages/34 Bidirectional Pins, 1 Input Pin
- **Workstation/PC-Based Development System**
 - C Compiler and C Source Debugger
 - Real-Time In-Circuit Emulation
 - Extensive Breakpoint/Trace Capability
 - Multi-Window User Interface
 - Microcontroller Programmer



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**TEXAS
INSTRUMENTS**

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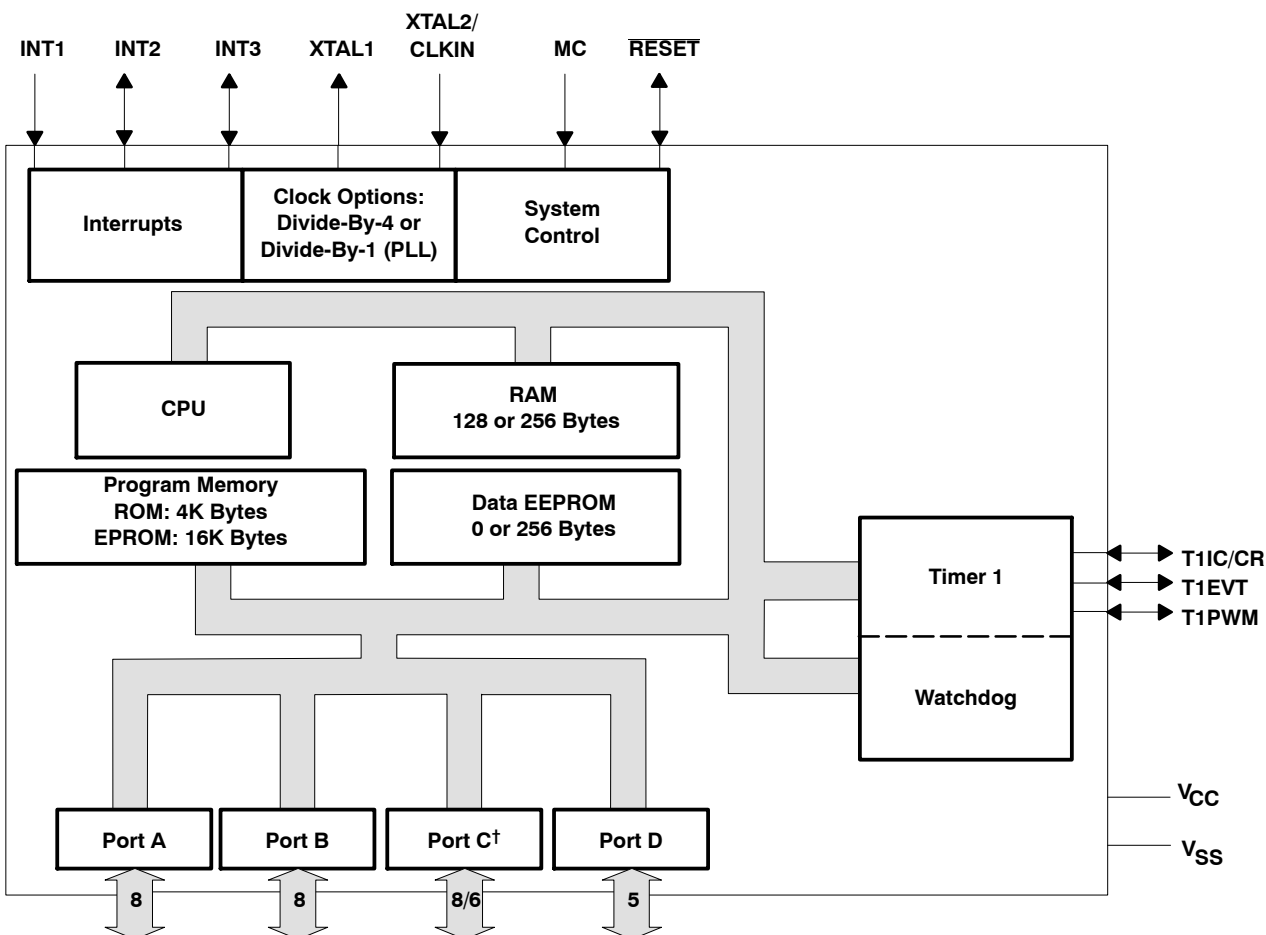
Pin Descriptions

PINS			TYPE†	DESCRIPTION
NAME	PDIP (40)	LCC (44)		
A0 A1 A2 A3 A4 A5 A6 A7	18 17 16 15 14 13 12 11	20 19 18 17 16 15 13 12	I / O	Port A is a general-purpose bidirectional I/O port.
B0 B1 B2 B3 B4 B5 B6 B7	38 37 36 35 28 29 30 31	43 42 41 40 32 34 35 36	I / O	Port B is a general-purpose bidirectional I/O port.
C0 C1 C2 C3 C4 C5 C6 C7	39 40 1 2 3 4 — —	44 1 2 3 4 5 30 31	I / O	Port C is a general-purpose bidirectional I/O port.
D3 D4 D5 D6 D7	21 20 23 22 19	23 22 25 24 21	I / O	Port D is a general-purpose bidirectional I/O port. D3 is also configurable as SYSCLK.
INT1 INT2 INT3	6 7 8	7 8 9	I I / O I / O	External (non-maskable or maskable) interrupt/general-purpose input pin External maskable interrupt input/general-purpose bidirectional pin External maskable interrupt input/general-purpose bidirectional pin
T1IC/CR T1PWM T1EVT	26 25 24	28 27 26	I / O	Timer1 input capture/counter reset input pin /general-purpose bidirectional pin Timer1 PWM output pin/general-purpose bidirectional pin Timer1 external event input pin/general-purpose bidirectional pin
RESET	5	6	I / O	System reset bidirectional pin: as input pin, $\overline{\text{RESET}}$ initializes the microcontroller; as open-drain output, RESET indicates that an internal failure was detected by the watchdog or oscillator fault circuit.
MC	34	39	I	Mode control pin; enables EEPROM write-protection override (WPO) mode, also EPROM V_{PP}
XTAL2/CLKIN XTAL1	33 32	38 37	I O	Internal oscillator crystal input/external clock source input Internal oscillator output for crystal
V_{CC}	10	10		Positive supply voltage
V_{SS}	27	14		Ground reference for digital logic
NC	9	11, 29, 33		These pins have no connection to the internal die.

† I = input, O = output



functional block diagram



† For the 40-pin devices, there are only six pins for port C.

description

The TMS370C080, TMS370C380, TMS370C686, and SE370C686 devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx8x refers to these devices. The TMS370 family provides cost-effective real-time system control through integration of advanced peripheral-function modules and various on-chip memory configurations.

The TMS370Cx8x family of devices is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technologies. Low-operating power, wide operating temperature range, and noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx8x devices attractive for system designs for automotive electronics, industrial motors, computer peripheral controls, telecommunications, and consumer applications.

All TMS370Cx8x devices contain the following on-chip peripheral modules:

- One 24-bit general-purpose watchdog timer
- One 16-bit general-purpose timer with an 8-bit prescaler

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description (continued)

Table 1 provides a memory configuration overview of the TMS370Cx8x devices.

Table 1. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		PACKAGES 44-PIN PLCC/CLCC, OR 40-PIN DIP
	ROM	EPROM	RAM	EEPROM	
TMS370C080A	4K	—	128	256	N – PDIP
TMS370C380A	4K	—	128	—	FN – PLCC
TMS370C686A	—	16K	256	—	FN – PLCC
SE370C686A [†]	—	16K	256	—	FZ – CLCC

[†] System evaluators and development are for use only in prototype environment and their reliability has not been characterized.

The suffix letter (A or B) appended to the device names shown in the device column of Table 1 and Table 2 indicates the configuration of the device. ROM or EPROM devices have different configurations as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 2. Suffix Letter Configuration

DEVICE [‡]	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM A	Standard	Divide-by-4 (Standard oscillator)	Enabled
ROM A	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

[‡] Refer to the “device numbering conventions” section for device nomenclature and to the “device part numbers” section for ordering.

The 4K bytes of mask-programmable ROM in the associated TMS370C380 device is replaced in the TMS370C686 with 16K bytes of EPROM. All other on-chip peripherals are identical. The one-time programmable (OTP) (TMS370C686) device and reprogrammable (SE370C686) device are available. The 4K-byte (TMS370C080) mask-programmable ROM device relies on the 68-pin (TMS370C758) development devices and an OTP converter socket (part # TMDX37788OTP) for prototyping and programming purposes.

TMS370C686 OTP devices are available in plastic packages. This microcontroller is effective to use for immediate production updates for other members of the TMS370Cx8x family or for low-volume production runs when the mask charge or cycle time for the low-cost mask ROM devices is not practical.

The SE370C686 has a windowed ceramic package to allow reprogramming of the program EPROM memory during the development/prototyping phase of design. The SE370C686 devices allow quick updates to breadboards and prototype systems while iterating initial designs.

The TMS370Cx8x family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all CPU activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx8x features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx8x family is fully instruction-set-compatible, providing easy transition between members of the TMS370 8-bit microcontroller family.



description (continued)

The TMS370Cx8x family provides the system designer with economical, efficient solutions to real-time control applications. The TMS370 family compact development tool (CDT™) solves the challenge of efficiently developing the software and hardware required to design the TMS370Cx8x into an ever-increasing number of complex applications. The application source code can be written in assembly and C languages, and the output code can be generated by the linker. The TMS370 family CDT development tool communicates through a standard RS-232-C interface with an existing personal computer. This allows the designer to use familiar personal computer editors and software utilities. Precise real-time, in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as reducing the time-to-market cycle.

The TMS370Cx8x family together with the TMS370 family CDT370, software tools, the SE370C686 and SE370C758 (FZ package) reprogrammable devices, comprehensive product documentation, and customer support provide a complete solution to the needs of the system designer.

central processing unit (CPU)

The CPU on the TMS370Cx8x device is the high-performance 8-bit TMS370 CPU module. The 'x8x implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'x8x instruction map is shown in Table 15 in the TMS370Cx8x instruction set overview section.

The '370Cx8x CPU architecture provides the following components:

- CPU registers:
 - A stack pointer that points to the last entry in the memory stack
 - A status register that monitors the operation of the instructions and contains the global interrupt-enable bits
 - A program counter (PC) that points to the memory location of the next instruction to be executed
- A memory map that includes:
 - 128- or 256-byte general-purpose RAM that can be used for data memory storage, program instructions, general purpose register, or the stack
 - A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM/EPROM programming control
 - 256-byte EEPROM module, that provides in-circuit programmability and data retention in power-off conditions
 - 4K-byte ROM or 16K-byte EPROM program memory

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central processing unit (CPU) (continued)

Figure 1 illustrates the CPU registers and memory blocks.

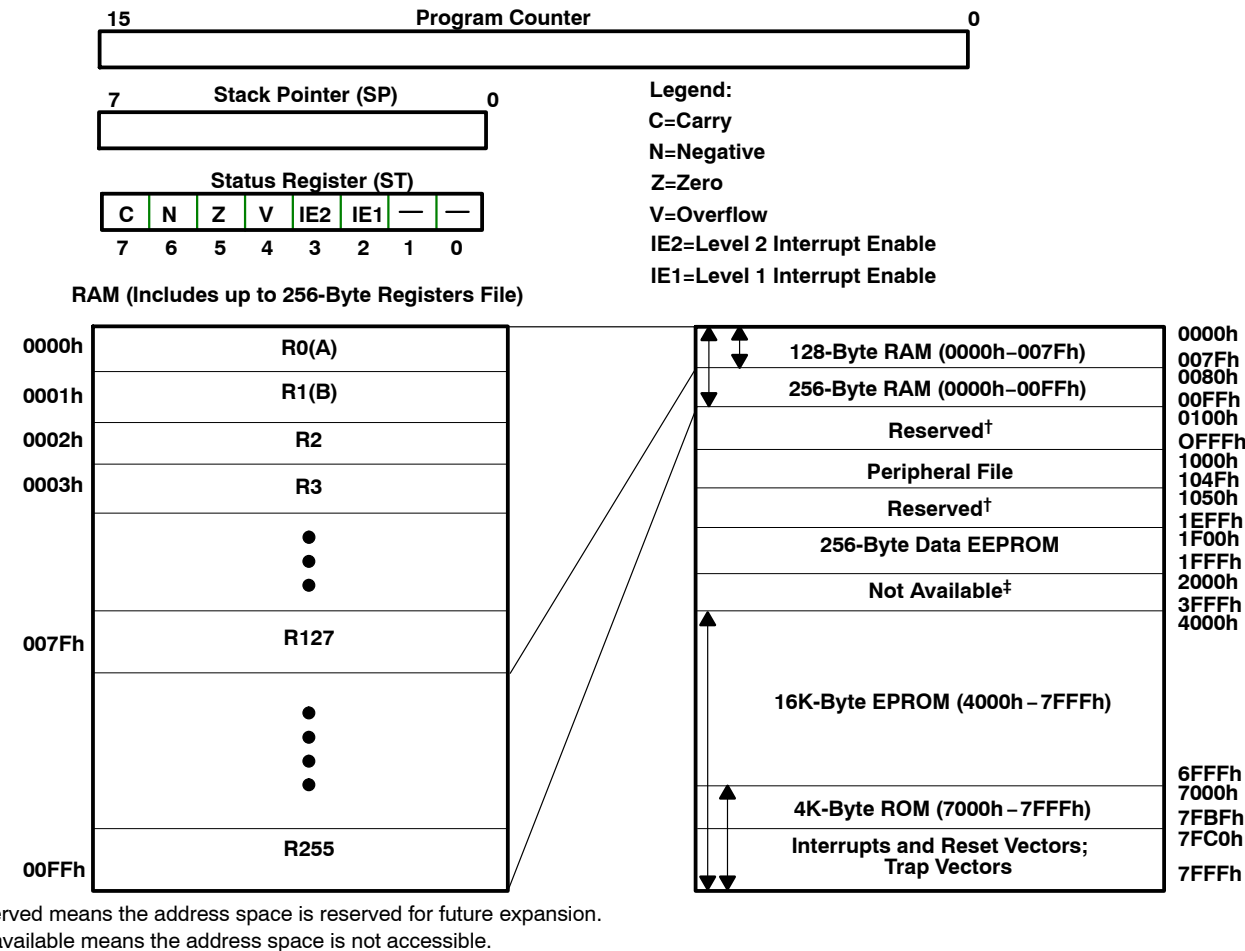


Figure 1. Programmer's Model

stack pointer (SP)

The SP is an 8-bit CPU register. Stack operates as a last-in, first-out, read/write memory. Typically, the stack is used to store the return address on subroutine calls as well as the status register (ST) contents during interrupt sequences.

The SP points to the last entry or top of the stack. The SP is incremented automatically before data is pushed onto the stack and decremented after data is popped from the stack. The stack can be placed anywhere in the on-chip RAM.

central processing unit (CPU) (continued)

status register

The ST monitors the operation of the instructions and contains the global interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits.

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional-jump instructions) use the status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

The ST, status-bit notation, and status-bit definitions are shown in Table 3.

Table 3. Status Registers

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH), and the program counter low (PCL). These registers contain the most significant byte (MSbyte) and least significant byte (LSbyte) of a 16-bit address.

During reset, the contents of the reset vector (7FFEh, 7FFFh) are loaded into the PC. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 6000h as the contents of the reset vector.

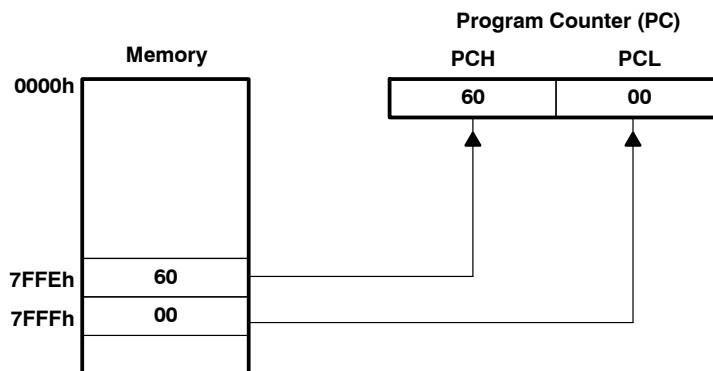


Figure 2. Program Counter After Reset

memory map

The TMS370Cx8x architecture is based on the Von Neuman architecture, in which the program memory and data memory share a common address space. All peripheral input/output is memory-mapped in this same common address space. As shown in Figure 3, the TMS370Cx8x provides memory-mapped RAM, ROM, data EEPROM, I/O pins, peripheral functions, and system-interrupt vectors.

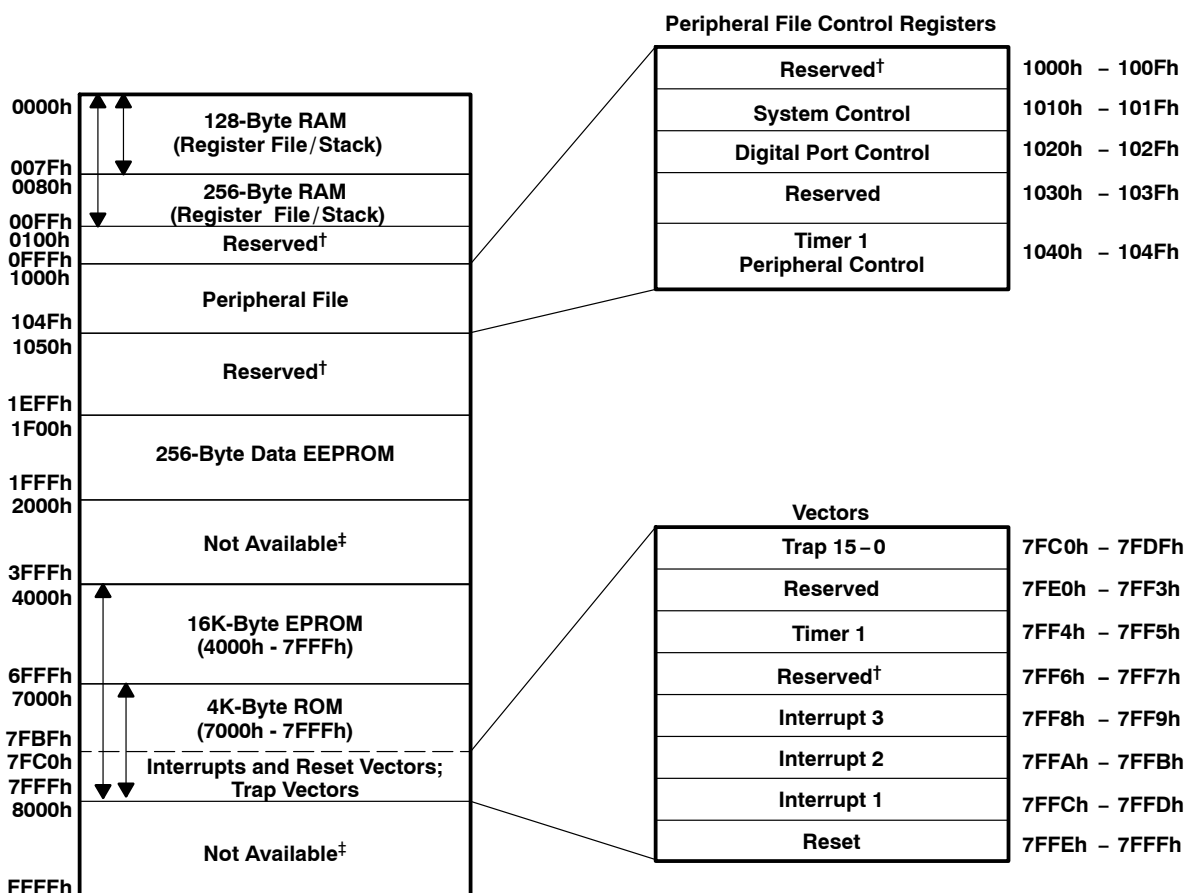
The peripheral file contains all I/O port control, peripheral status and control, EEPROM, EPROM, and system-wide control functions. The peripheral file consists of 256 contiguous addresses located from 1000h to 10FFh and is divided logically into 16 peripheral file frames of 16 bytes each. Each on-chip peripheral is

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TMS370Cx8x CPU (continued)

assigned to a separate frame through which peripheral control and data information is passed. The TMS370Cx8x has its on-chip peripherals and system control assigned to peripheral file frames 1 through 4, addresses 1010h through 104Fh.



† Reserved means that the address space is reserved for future expansion, means the address space is not accessible.

‡ Not available means that the address space is not accessible.

Figure 3. TMS370Cx8x Memory Map

RAM/register file (RF)

Locations within the RAM address space can serve as the RF, general-purpose read/write memory, program memory, or the stack instructions. The TMS370C080 and TMS370C380 contain 128 bytes of internal RAM memory mapped beginning at location 0000h (R0) and continuing through location 007Fh (R127), which is shown in Table 4 along with 'x86 devices.

Table 4. RAM Memory Map

	'x80	'x86
RAM size	128 bytes	256 bytes
Memory mapped	0000h – 007Fh	0000h – 00FFh

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction load SP (LDSP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370Cx8x control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or P for a decimal designator. For example, the system-control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 5 shows the TMS370Cx8x PF address map.

Table 5. TMS370Cx8x Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h – 100Fh	P000 – P00F	Reserved
1010h – 101Fh	P010 – P01F	System and EPROM/EEPROM control registers
1020h – 102Fh	P020 – P02F	Digital I/O port control registers
1030h – 103Fh	P030 – P03F	Reserved
1040h – 104Fh	P040 – P04F	Timer 1 registers
1050h – 10FFh	P050 – P0FF	Reserved

data EEPROM

The TMS370C080 device, containing 256 bytes of data EEPROM, has a memory mapped beginning at location 1F00h and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B). The data EEPROM features include the following:

- Programming:
 - Bit-, byte-, and block-write/erase modes
 - Internal charge pump circuitry. No external EEPROM programming voltage supply is needed.
 - Control register: Data EEPROM programming is controlled by the data EEPROM control register (DEECTL) located in the PF frame beginning at location P01A. See Table 6.
 - In-circuit programming capability. There is no need to remove the device to program.
- Write-protection. Writes to the data EEPROM are disabled during the following conditions.
 - Reset. All programming of the data EEPROM module is halted.
 - Write-protection active. There is one write-protect bit per 32-byte EEPROM block.
 - Low-power mode operation
- Write-protection can be overridden by applying 12 V to MC.

Table 6. Data EEPROM and PROGRAM EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME
P01A	DEECTL	Data EEPROM Control Register
P01B	—	Reserved
P01C	EPCTL	Program EPROM Control Register

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program EPROM[†]

The TMS370C686 device contains 16K bytes of EPROM memory, mapped beginning at location 4000h and continuing through location 7FFFh as shown in Figure 3. Reading the program EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the EPROM control register (EPCTL). The program EPROM module features include:

- Programming
 - In-circuit programming capability if V_{PP} is applied to MC
 - Control register EPROM programming is controlled by the EPROM control register (EPCTL) located in the peripheral file (PF) frame at location P01C as shown in Table 6.
- Write-protection writes to the program EPROM are disabled under the following conditions
 - Reset all programming to the EPROM module is halted
 - Low-power modes
 - 13 V not applied to MC

program ROM[†]

The program ROM consists of 4K bytes of mask-programmable read-only memory. The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication.

system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx8x CPU-based device. There are up to three different actions that can cause the system to reset the device. Two of these actions are generated internally, while one (RESET pin) is controlled externally. These actions are as follows:

- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 User's Guide* (literature number SPNU127) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside of the recommended operating range. See the *TMS370 User's Guide* (literature number SPNU127) for more information.
- External RESET pin. A low-level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 User's Guide* (literature number SPNU127) for more information.

Once a reset source is activated, the external RESET pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x8x device to reset external system components. Additionally, if a cold start (V_{CC} is off for several hundred milliseconds) condition or oscillator failure occurs, or the RESET pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator-fault flag (OSC FLT FLAG, SCCR0.4), the cold-start flag (COLD START, SCCR0.7) and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 7 depicts the reset sources.

[†] Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments Incorporated, and 7FF4h through 7FF5h along with 7FF8h through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh.

system reset (continued)

Table 7. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Register A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode-fetch from the address pointed to the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

When an external reset circuit is connected to the $\overline{\text{RESET}}$ pin, the $\overline{\text{RESET}}$ pin must be held low until the clock signal is valid and V_{CC} is within the operating range. Figure 4 shows a typical reset circuit.

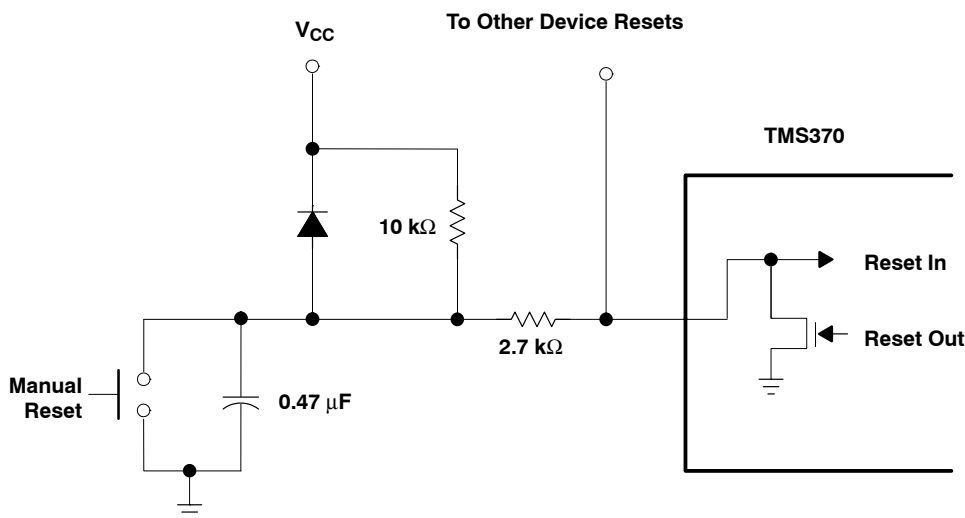


Figure 4. Typical Reset Circuit

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interrupts

The TMS370 family software-programmable interrupt structure permits flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The hardware-interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global interrupt mask bits (IE1 and IE2) of the ST.

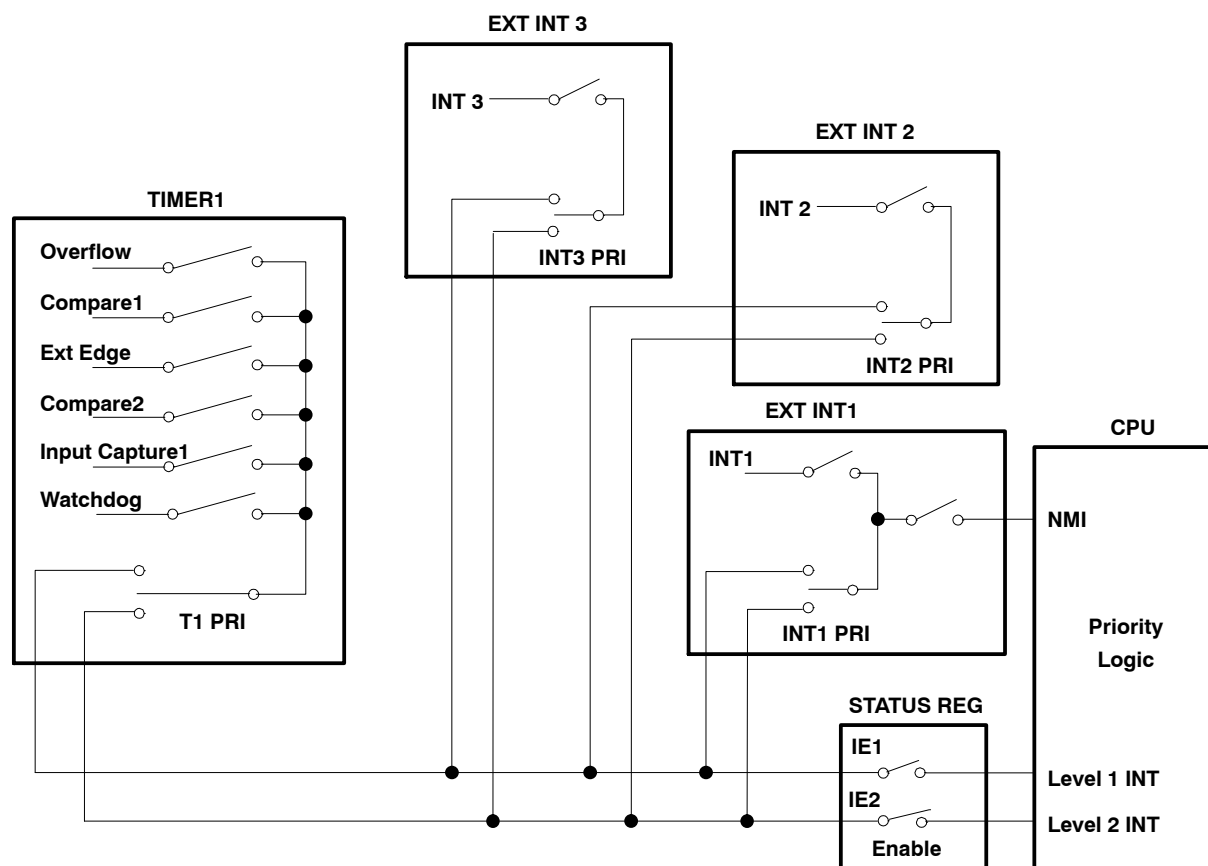


Figure 5. Interrupt Control

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is selectively configured on either the high- or low-priority-interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx8x has four hardware-system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 8. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. A system interrupt may have multiple interrupt sources. All of the interrupt sources are individually maskable by local interrupt-enable control bits in the associated peripheral file. Each interrupt source FLAG bit is individually readable for software polling or to determine which interrupt source generated the associated system interrupt.

interrupts (continued)

One of the system interrupts is generated by on-chip peripheral functions, and three external interrupts are supported. Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in peripheral file frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual or global enable mask bits. The INT1 NMI bit is protected during non-privileged operation. It, therefore, should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software-configured as general-purpose input/output pins if the interrupt function is not required (INT1 can be similarly configured as an input pin).

Table 8. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY [†]
External RESET Watchdog Overflow Oscillator Fault Detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	RESET [‡]	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1 [‡]	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2 [‡]	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3 [‡]	7FF8h, 7FF9h	4
Timer 1 Overflow Timer 1 Compare 1 Timer 1 Compare 2 Timer 1 External Edge Timer 1 Input Capture 1 Watchdog Overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT [§]	7FF4h, 7FF5h	5

[†] Relative priority within an interrupt level

[‡] Release microcontroller from STANDBY and HALT low-power modes

[§] Release microcontroller from STANDBY low-power mode

privileged operation and EEPROM write-protection override

The TMS370Cx8x family is designed with significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration once it is defined for an application. Following a hardware reset, the TMS370Cx8x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) is set to 1 to enter the nonprivileged mode, thus disabling write operations to specific configuration-control bits within the PF. Table 9 displays the system-configuration bits, which are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

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privileged operation and EEPROM write-protection override (continued)

Table 9. Privilege Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCRO	P010.5 P010.6	PF AUTO WAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST

† The privilege bits are shown in a bold typeface in the peripheral file frame 1 section.

The WPO mode provides an external hardware method of overriding the write-protection registers (WPRs) of data EEPROM on the TMS370C080. WPO mode is entered by applying a 12-V input to the MC pin after the RESET pin input goes high (logic 1). The high voltage on the MC pin during the WPO mode is not the programming voltage for the data EEPROM or program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware-system-level capability to modify the content of the data EEPROM while the device remains in the application but only while requiring a 12-V external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power and IDLE modes

The TMS370Cx8x devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time when the mask is manufactured.

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls the low-power mode selection.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, and Timer 1 remain active. System processing is suspended until a qualified interrupt (hardware RESET, external interrupt on INT1, INT2, INT3, or timer 1 interrupt) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx8x is placed in its lowest power-consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware RESET, external interrupt on the INT1, INT2, or INT3) is detected. The power-down mode-selection bits are summarized in Table 10.

low-power and IDLE modes (continued)

Table 10. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X [†]	IDLE

[†] Don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6-7 bits is ignored. In addition, if an IDLE instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method for always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI is generated always, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (SP, PC, and ST), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the WD timer is inhibited.

clock modules

The 'x8x family provides two clock options that are referred to as divide-by-1 (phase-locked loop) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The 'x8x masked ROM devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device. The '686A EPROM has only the divide-by-4.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a one-to-one match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency, whereas the divide-by-4 option produces a SYSCLK which is one-fourth of the frequency of the external resonator. Inside of the divide-by-1 module, the frequency of the external resonator is multiplied by four, and the clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. These are formulated as follows:

$$\text{Divide-by-4 option : } \text{SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option : } \text{SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the improved EMI performance. The harmonics of low-speed resonators extend through fewer of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 provides the capability of reducing the resonator speed by four times, and this results in a steeper decay of emissions produced by the oscillator.

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system configuration registers

Table 11 contains system-configuration, control functions, and registers for controlling EEPROM programming. The privileged bits are shown in bold typeface in shaded areas.

Table 11. Peripheral File Frame 1: System-Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTO WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D P01E P01F	Reserved								

digital port-control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 12 shows the specific addresses, registers, and control bits within this peripheral file frame. Table 13 shows the port-configuration register setup.

Table 12. Peripheral File Frame 2: Digital Port-Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
P020	Reserved								APOINT1
P021	Port A Control Register 2 (must be 0)								APOINT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPOINT1
P025	Port B Control Register 2 (must be 0)								BPOINT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPOINT1
P029	Port C Control Register 2 (must be 0)								CPOINT2
P02A	Port C Data								CDATA
P02B	Port C Direction								CDIR
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPOINT1
P02D	Port D Control Register 2 (must be 0) [†]					—	—	—	DPOINT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 13. Port-Configuration Register Setup

PORT	PIN	abcd 00q1	abcd 00y0
A	0 – 7	Data Out q	Data In y
B	0 – 7	Data Out q	Data In y
C	0 – 7	Data Out q	Data In y
D	3 – 7	Data Out q	Data In y
a = Port x Control Register 1 b = Port x Control Register 2 c = Data d = Direction			

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programmable timer 1

The programmable Timer 1 (T1) module of the TMS370Cx8x provides the designer with the enhanced timer resources required to perform real-time system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers, T1 and WD timer, allow program selection of input clock sources (real-time, external event, or pulse accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The Timer 1 module includes three external device pins that can be used for multiple counter functions (operation-mode dependent), or used as general-purpose I/O pins. The T1 module block diagram is shown in Figure 6.

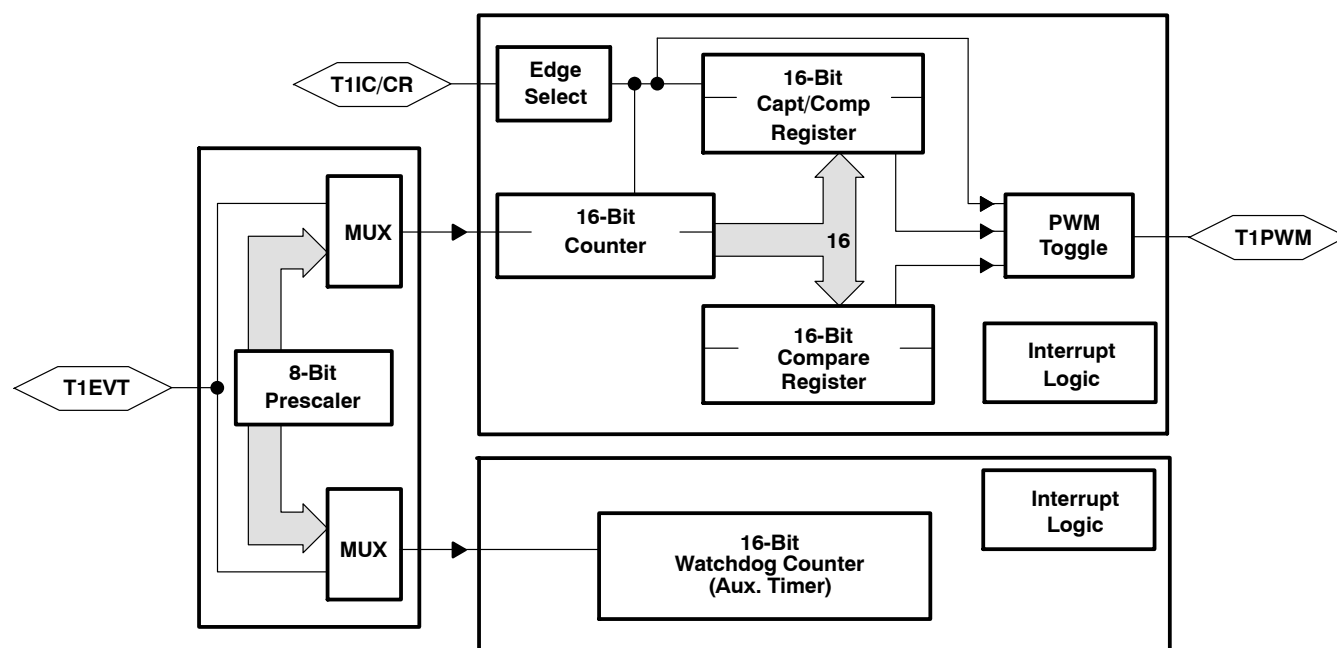


Figure 6. Timer 1 Block Diagram

- Three Timer1 I/O pins
 - T1IC/CR: T1 input capture / counter-reset input pin, or general-purpose bidirectional I/O pin
 - T1PWM: T1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T1EVT: T1 event input pin, or general-purpose bidirectional I/O pin
- Two operational modes:
 - Dual-compare mode: Provides PWM signal
 - Capture/compare mode: Provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either capture or compare registers.
- One 16-bit WD counter can be used as an event counter, a pulse accumulator, or an interval timer if WD feature is not needed.
- Prescaler/clock sources that determines one of eight clock sources for general-purpose timer

programmable timer 1 (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR)
- Interrupts that can be generated on the occurrence of:
 - A capture
 - A compare equal
 - A counter overflow
 - An external-edge detection
- Sixteen T1 module control registers located in the PF frame beginning at address P040

The T1 module control registers are illustrated in Table 14.

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programmable timer 1 (continued)

Table 14. Timer 1 Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Mode: Dual-Compare and Capture/Compare									
P040	T1 Counter MSbyte							Bit 8	T1CNTR
P041	T1 Counter LSbyte							Bit 0	
P042	Compare Register MSbyte							Bit 8	T1C
P043	Compare Register LSbyte							Bit 0	
P044	Capture/Compare Register MSbyte							Bit 8	T1CC
P045	Capture/Compare Register LSbyte							Bit 0	
P046	Watchdog Counter MSbyte							Bit 8	WDCNTR
P047	Watchdog Counter LSbyte							Bit 0	
P048	Watchdog Reset Key							Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE=0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Mode: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

Figure 7 shows the Timer 1 capture/compare mode block diagram. The annotations on the diagram identify the register and the bit(s) in the PF. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.



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programmable timer 1 (continued)

Figure 8 shows the Timer 1 dual-compare mode block diagram. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

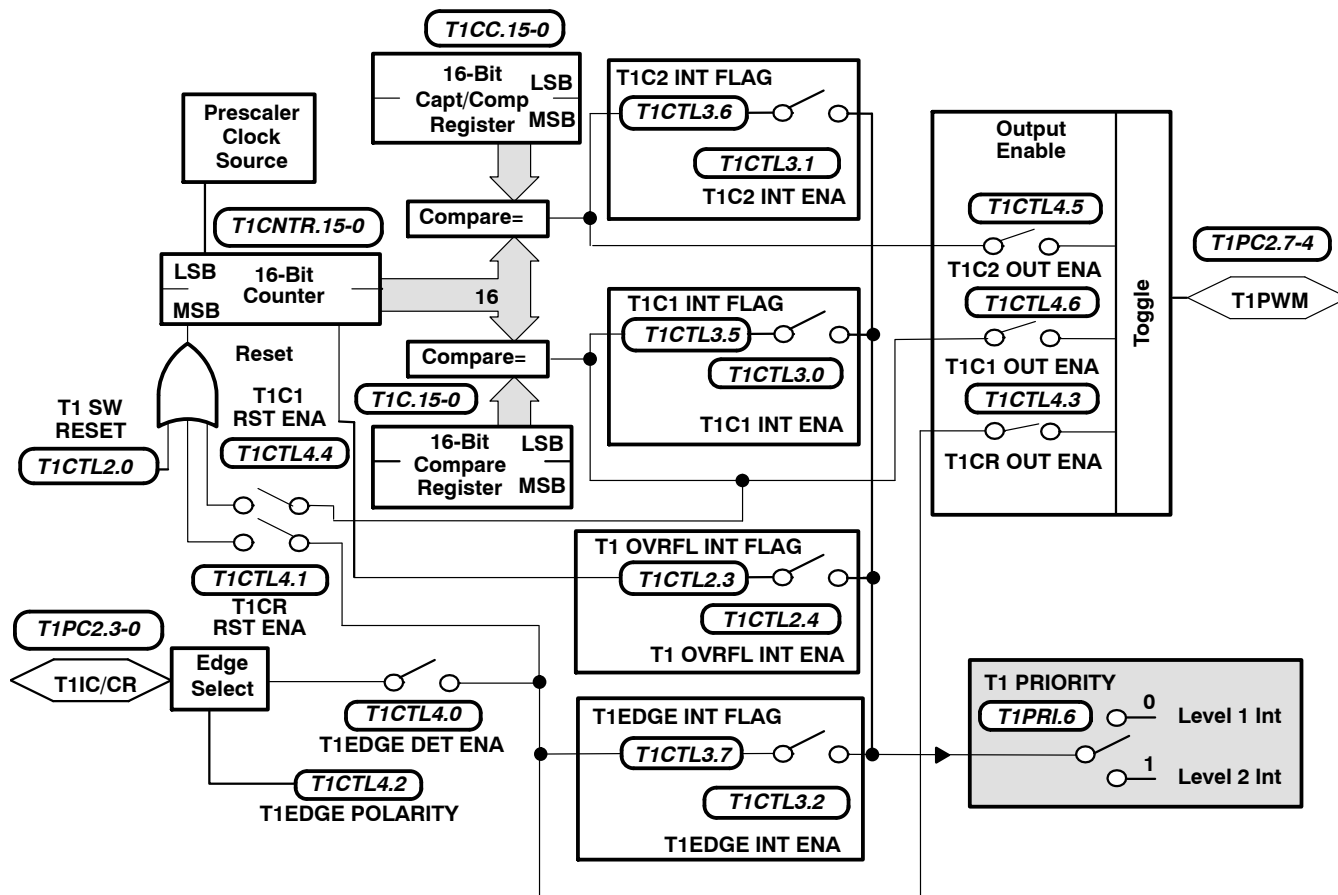


Figure 8. Dual-Compare Mode

programmable timer 1 (continued)

The TMS370Cx8x device includes a 24-bit WD timer, contained in the T1 module, which can be programmed as an event counter, pulse accumulator, or interval timer if the watchdog function is not used. The WD function is to monitor software and hardware operation and to implement a system reset when the WD counter is not properly serviced (WD counter overflow or WD counter is re-initialized by an incorrect value). The WD can be configured as one of three mask options as follows: standard watchdog, hard WD, or simple counter.

- Standard watchdog configuration (see Figure 9) for EPROM and mask-ROM devices:
 - Watchdog mode
 - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows
 - A watchdog overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
 - Non-watchdog mode
 - Watchdog timer can be configured as an event counter, pulse accumulator or an interval timer

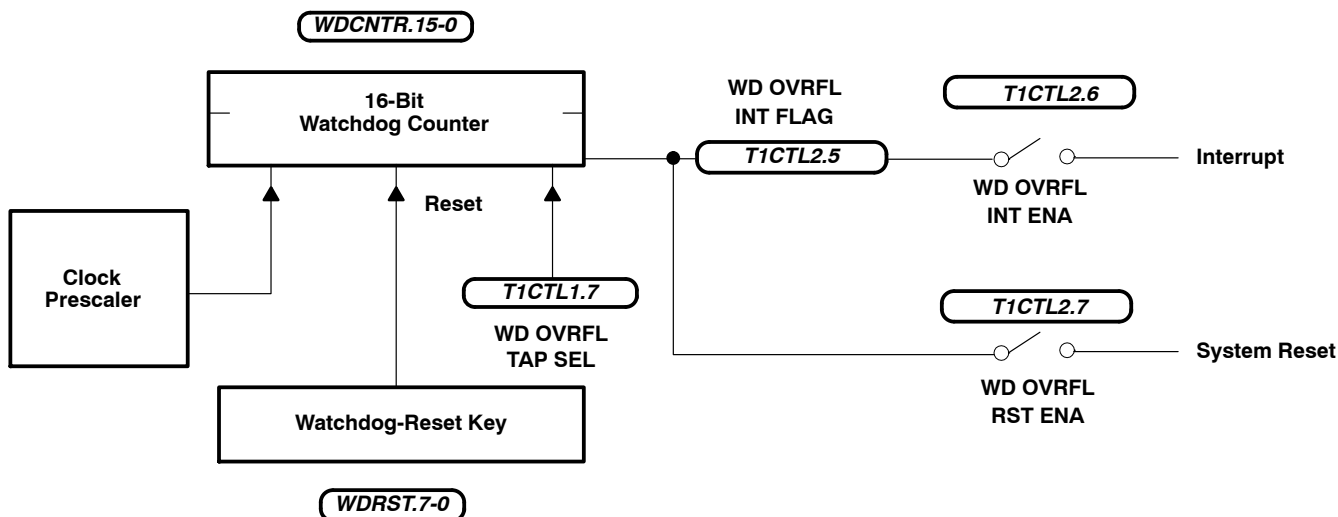


Figure 9. Standard Watchdog

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programmable timer 1 (continued)

- Hard watchdog configuration (see Figure 10) for mask-ROM devices:
 - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the WDRST or if the counter overflows.
 - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset.
 - Automatic activation of the WD timer upon power-up reset
 - INT1 is enabled as a nonmaskable interrupt during low-power modes.

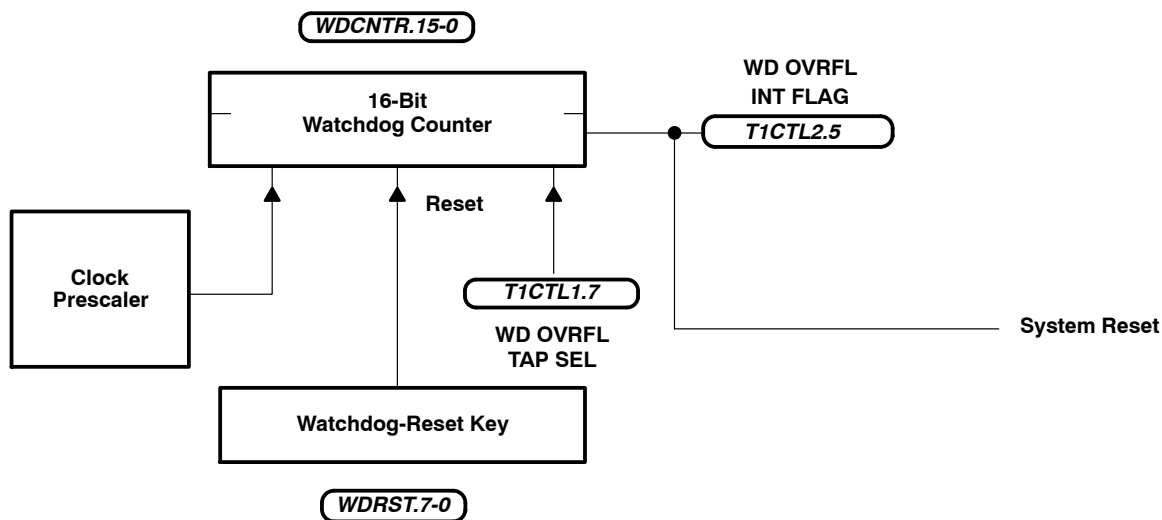


Figure 10. Hard Watchdog

programmable timer 1 (continued)

- Simple counter configuration (see Figure 11) for mask-ROM devices only
 - Simple counter can be configured as an event counter, pulse accumulator or an internal timer.

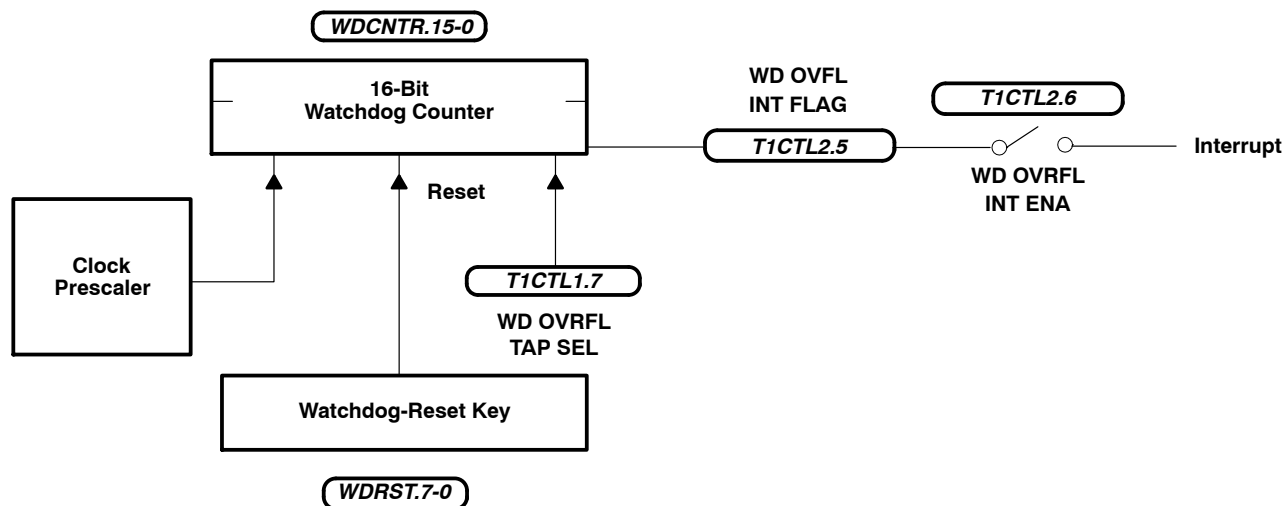


Figure 11. Simple Counter

instruction set overview

Table 15 provides an opcode-to-instruction cross reference of all 73 instructions and 274 opcodes of the '370Cx8x instruction set. The numbers at the top of this table represent the most significant nibble (MSN) of the opcode while the numbers at the left side of the table represent the least significant nibble (LSN). The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

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Table 15. TMS370 Family Opcode/Instruction Map[†]

		MSN																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
L S N	0	JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8				CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
	1	JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7	
	2	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7	
	3	JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8	
	4	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes	
	5	JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14		
	6	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6	
	7	JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10	
	8	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7	
	9	JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9	
	A	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12	
	B	JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8	

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

Table 15. TMS370 Family Opcode/Instruction Map[†] (Continued)

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L S N	C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
	D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
	E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
	F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):

F4	8	MOVW *n[Rn] 4/15	DIV Rn,A 3/14-63
F4	9	JMPL *n[Rn] 4/16	
F4	A	MOV *n[Rn],A 4/17	
F4	B	MOV A,*n[Rn] 4/16	
F4	C	BR *n[Rn] 4/16	
F4	D	CMP *n[Rn],A 4/18	
F4	E	CALL *n[Rn] 4/20	
F4	F	CALLR *n[Rn] 4/22	

Legend:

* = Indirect addressing operand prefix
 & = Direct addressing operand prefix
 # = immediate operand
 #16 = immediate 16-bit number
 lab = 16-label
 n = immediate 8-bit number
 Pd = Peripheral register containing destination type
 Pn = Peripheral register
 Ps = Peripheral register containing source byte
 ra = Relative address
 Rd = Register containing destination type
 Rn = Register file
 Rp = Register pair
 Rpd = Destination register pair
 Rps = Source Register pair
 Rs = Register containing source byte

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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development system support

The TMS370 family development support tools include an assembler, a C compiler, a linker, an in-circuit emulator XDS22, CDT and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
 - Includes extensive macro capability
 - Provides high-speed operation
 - Includes format conversion utilities for popular formats
- ANSI C Compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, Sun-3™ or Sun-4™)
 - Generates assembly code for the TMS370 that can be inspected easily
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables direct reference to the TMS370's port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (Compact Development Tool) real-time in-circuit emulation
 - Base (Part Number EDSCDT370 – for PC, requires cable)
 - Cable for 40-pin DIP (Part No. EDSTRG40DIL8X)
 - Cable for 44-pin PLCC (Part No. EDSTRG44PLCC8X)
 - Provides EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Includes compatibility to upload/download program and data memory
 - Executes programs and software routines
 - Includes 1 024-sample trace buffer
 - Includes single-step executable instructions
 - Uses software breakpoints to halt program execution at selected address
 - Provides timers for analyzing total and average time in routines
 - Contains an eight-line logic probe for adding visibility of external signals to the breakpoint qualifier and to trace display
- Microcontroller programmer
 - Base (Part No. TMDS3760500A – for PC, requires programmer head)
 - Single unit head for 44-pin PLCC (Part No. TMDS3780510A)
 - Single unit head for 40-pin DIP (Part No. TMDS3780511A)
 - PC-based, window/function-key-oriented user interface for ease of use and rapid learning environment
- Converter Socket (Part No. TMDS37788OTP)

HP700 is a trademark of Hewlett-Packard Company.
Sun-3 and Sun-4 are trademarks of Sun Microsystems, Incorporated.



device numbering conventions

Figure 12 illustrates the numbering and symbol nomenclature for the TMS370Cx8x family.

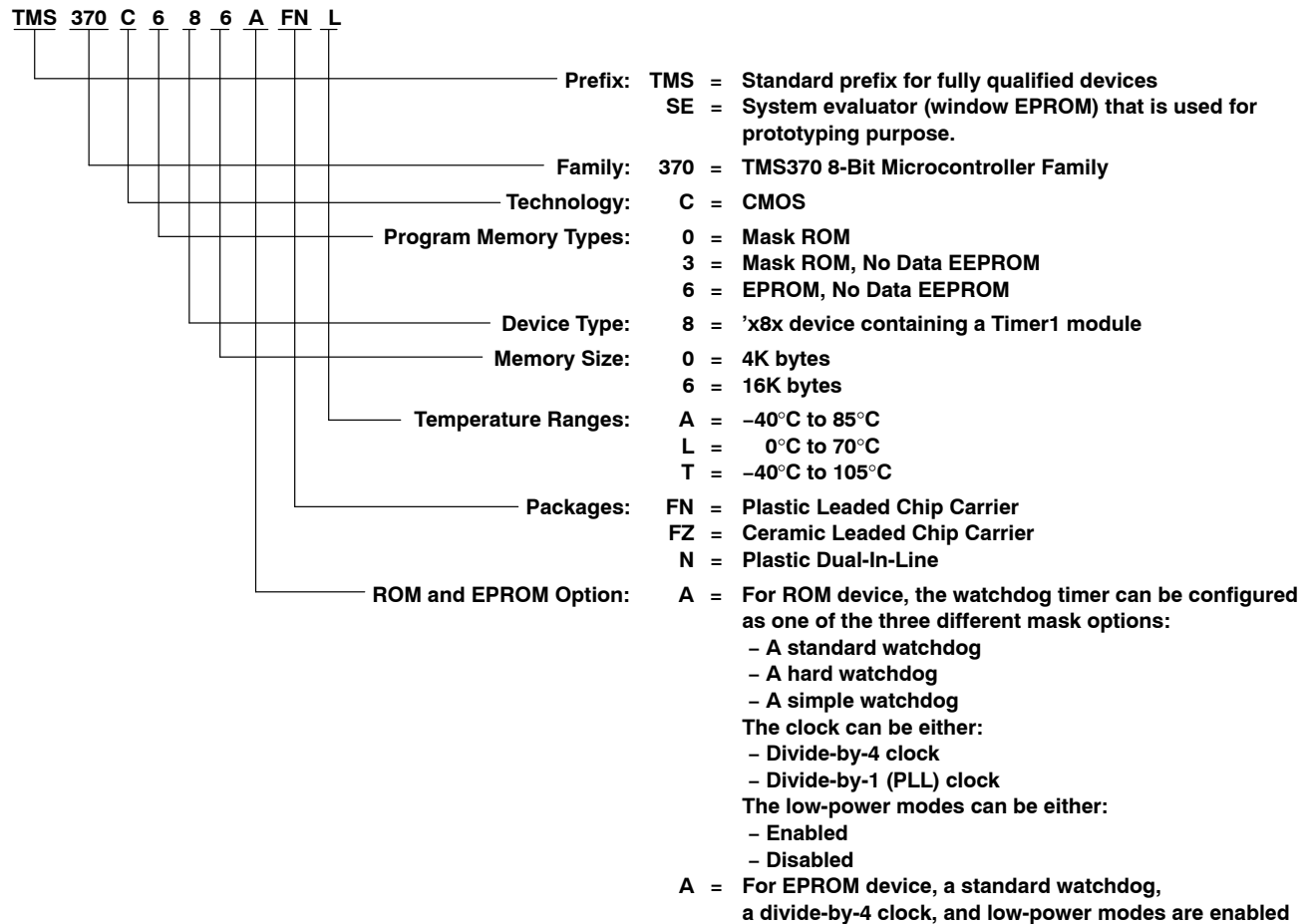


Figure 12. TMS370Cx8x Family Nomenclature

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device part numbers

Table 16 provides all of the 'x8x devices available. The device part number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog timer options desired. Each device can have only one of the three possible watchdog timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 16. Device Part Numbers

DEVICES PART NUMBERS FOR 44 PINS (LCC)	DEVICES PART NUMBERS FOR 40 PINS (PDIP)
TMS370C380AFNA TMS370C380AFNL TMS370C380AFNT	TMS370C080ANA TMS370C080ANL TMS370C080ANT
TMS370C686AFNT	—
SE370C686AFZT [†]	—

[†] System evaluators are for use in prototype environment and their reliability has not been characterized.

Figure 13 shows a sample of the new code release form.

Figure 13. Sample New Code Release Form

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Table 17 is a collection of all the peripheral file frames used in the 'Cx8x (provided for a quick reference).

Table 17. Peripheral File Frame Compilation

System Configuration Registers									
PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTO WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT / STANDBY	PWRDWN / IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D to P01F	Reserved								
Digital Port Control Registers									
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	Port B Control Register 2 (must be 0)								BPORT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPORT1
P029	Port C Control Register 2 (must be 0)								CPORT2
P02A	Port C Data								CDATA
P02B	Port C Direction								CDIR
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0)†					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR
Timer1 Module Register Memory Map									
Modes: Dual-Compare and Capture/Compare									
P040	Bit 15	T1Counter MSbyte						Bit 8	T1CNTR
P041	Bit 7	T1 Counter LSbyte						Bit 0	

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.



Table 17. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Dual-Compare and Capture/Compare (Continued)									
P042	Compare Register MSbyte							Bit 8	T1C
P043	Compare Register LSbyte							Bit 0	
P044	Capture/Compare Register MSbyte							Bit 8	T1CC
P045	Capture/Compare Register LSbyte							Bit 0	
P046	Watchdog Counter MSbyte							Bit 8	WDCNTR
P047	Watchdog Counter LSbyte							Bit 0	
P048	Watchdog Reset Key							Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE=0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC}) (see Note 2)	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	1 W
Operating free-air temperature range, T_A : L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS} .

2. Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 3)	3		5.5	V
V_{IL}	Low-level input voltage	All pins except MC		0.8	V
		MC, normal operation		0.3	
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET		V_{CC}	V
		XTAL2/CLKIN		$0.8 V_{CC}$	
		RESET		$0.7 V_{CC}$	
V_{MC}	MC (mode control) voltage	EEPROM write protect override (WPO)		11.7 12 13	V
		EPROM programming voltage (V_{PP})		13 13.2 13.5	
		Microcomputer		V_{SS} 0.3	
T_A	Operating free-air temperature	L version		0 70	°C
		A version		–40 85	
		T version		–40 105	

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS} .

3. RESET must be externally activated when V_{CC} or SYSCLK is not within the recommended operating range.



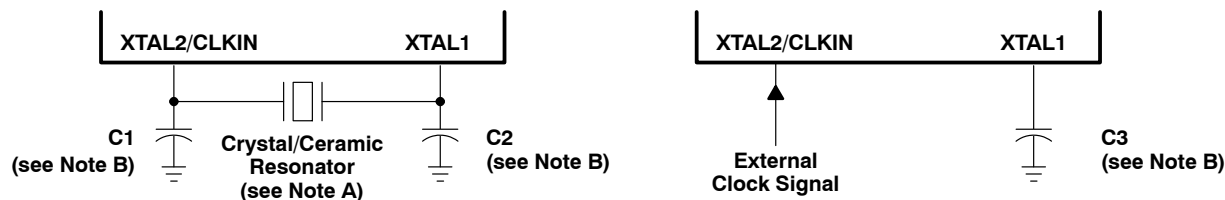
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	$I_{OL} = 1.4 \text{ mA}$			0.4	V
V_{OH}	High-level output voltage	$I_{OH} = -50 \mu\text{A}$	$0.9 V_{CC}$			V
		$I_{OH} = -2 \text{ mA}$	2.4			
I_I	Input current	MC	$0 \text{ V} < V_I \leq 0.3 \text{ V}$		10	μA
			$0.3 \text{ V} < V_I \leq 13 \text{ V}$		650	
			See Note 4 $12 \text{ V} \leq V_I \leq 13 \text{ V}$		50	mA
	I/O pins	$0 \text{ V} \leq V_I \leq V_{CC}$			± 10	μA
I_{OL}	Low-level output current	$V_{OL} = 0.4 \text{ V}$	1.4			mA
I_{OH}	High-level output current	$V_{OH} = 0.9 V_{CC}$	- 50			μA
		$V_{OH} = 2.4 \text{ V}$	- 2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 7)	See Notes 5 and 6 SYSCLK = 5 MHz		30	45	mA
		See Notes 5 and 6 SYSCLK = 3 MHz		20	30	
		See Notes 5 and 6 SYSCLK = 0.5 MHz		7	11	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 8)	See Notes 5 and 6 SYSCLK = 5 MHz		10	17	mA
		See Notes 5 and 6 SYSCLK = 3 MHz		8	11	
		See Notes 5 and 6 SYSCLK = 0.5 MHz		2	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 9)	See Notes 5 and 6 SYSCLK = 3 MHz		6	8.6	mA
		See Notes 5 and 6 SYSCLK = 0.5 MHz		2	3.0	
	Supply current (HALT mode)	See Note 5 XTAL2/CLKIN < 0.2 V		2	30	μA

- NOTES: 4. Input current I_{PP} is a maximum of 50 mA only when you are programming EPROM.
5. Single-chip mode, ports configured as inputs or outputs with no load. All inputs $\leq 0.2 \text{ V}$ or $\geq V_{CC} - 0.2\text{V}$.
6. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = $0.01 \text{ mA} \times (\text{total load capacitance} + \text{crystal capacitance in pF})$.
7. Maximum operating current = $7.6 (\text{SYSCLK}) + 7 \text{ mA}$.
8. Maximum standby current = $3 (\text{SYSCLK}) + 2 \text{ mA}$. (OSC POWER bit = 0).
9. Maximum standby current = $2.24 (\text{SYSCLK}) + 1.9 \text{ mA}$. (OSC POWER bit = 1, only valid up to 3 MHz SYSCLK).

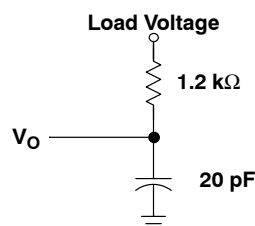
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NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
B. The values of C1 and C2 are typically 15 pF and the value of C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 14. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4 \text{ V}$; Load Voltage = 0 V
Case 2: $V_O = V_{OL} = 0.4 \text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 15. Typical Output Load Circuit (See Note A)

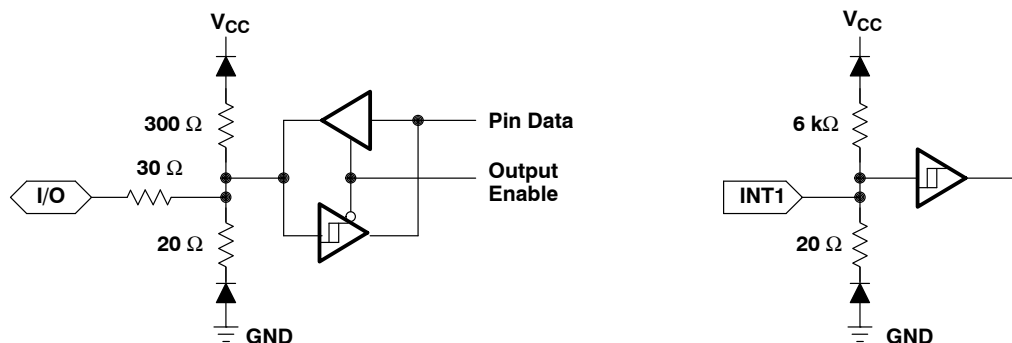


Figure 16. Typical Buffer Circuitry

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

AR	Array	CI	XTAL2/CLKIN
B	Byte	SC	SYSCLK

Lowercase subscripts and their meanings are:

c	cycle time (period)	su	setup time
d	delay time	v	valid time
f	fall time	w	pulse duration (width)
r	rise time		

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid

All timings are measured between high and low measurement points as indicated in Figure 17 and Figure 18.

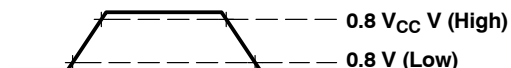


Figure 17. XTAL2/CLKIN Measurement Points

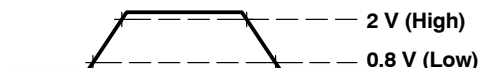


Figure 18. General Measurement Points

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external clocking requirements for clock divided by 4 (see Note 10 and Figure 19)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 11)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN Crystal operating frequency	2	20	MHz
	SYSCLK Internal system clock operating frequency [†]	0.5	5	MHz

[†] SYSCLK = CLKIN/4

NOTES: 10. For V_{IL} and V_{IH} , refer to recommended operating conditions.

11. This pulse may be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

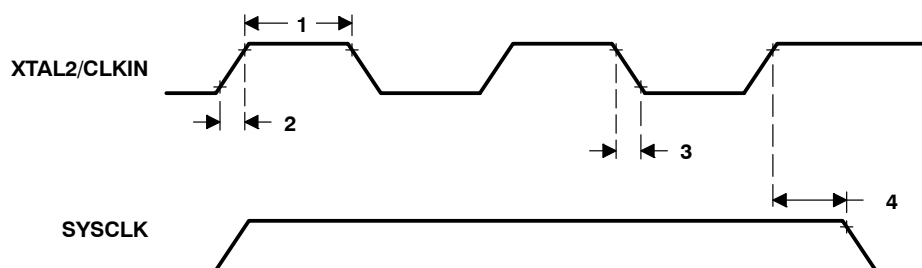


Figure 19. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL) (see Note 10 and Figure 20)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 11)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN Crystal operating frequency	2	5	MHz
	SYSCLK Internal system clock operating frequency [‡]	2	5	MHz

[‡] SYSCLK = CLKIN/1

NOTES: 10. For V_{IL} and V_{IH} , refer to recommended operating conditions.

11. This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

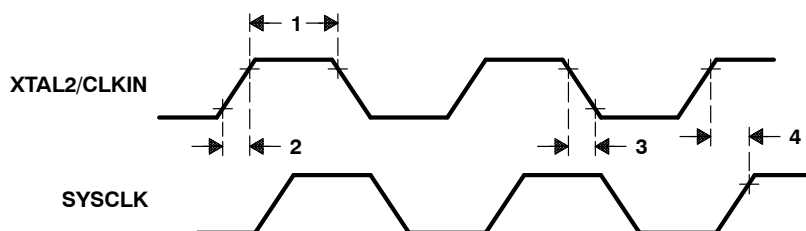


Figure 20. External Clock Timing for Divide-by-1

switching characteristics and timing requirements (see Note 12)

NO.	PARAMETER		MIN	MAX	UNIT
5	t_c	Cycle time, SYSCLK (system clock)	Divide-by-4	200	ns
			Divide-by-1	200	
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low	$0.5 t_c - 20$	$0.5 t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high	$0.5 t_c$	$0.5 t_c + 20$	ns

NOTE 12: t_c = system-clock cycle time = $1/\text{SYSCLK}$

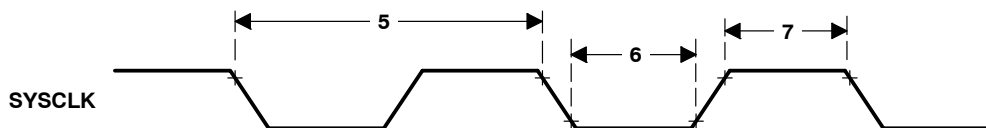


Figure 21. SYSCLK Timing

general purpose output signal switching time requirements

	MIN	NOM	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns

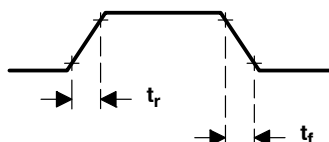


Figure 22. Signal Switching Timing

recommended EEPROM timing requirements for programming

	MIN	MAX	UNIT
$t_{w(PGM)B}$	Pulse duration, programming signal to ensure valid data is stored (byte mode)	10	ms
$t_{w(PGM)AR}$	Pulse duration, programming signal to ensure valid data is stored (array mode)	20	ms

recommended EPROM operating conditions for programming

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.75	5.5	6	V
V _{PP}	Supply voltage at MC pin		13	13.2	13.5	V
I _{PP}	Supply current at MC pin during programming (V _{PP} = 13 V)			30	50	mA
SYSCLK	System clock	Divide-by-4	0.5		5	MHz
		Divide-by-1	2		5	

recommended EPROM timing requirements for programming

		MIN	NOM	MAX	UNIT
t _w (EPGM)	Pulse duration, programming signal (see Note 13)	0.40	0.50	3	ms

NOTE 13: Programming pulse is active when both EXE (EPCTL.0) and VPPS (EPCTL.6) are set.

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Table 18 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

Table 18. TMS370Cx8x Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 44 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C380AFNA TMS370C380AFNL TMS370C380AFNT TMS370C686AFNT
FZ – 44 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C686AFZT
N – 40 pin (100-mil pin spacing)	PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	N(R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE	TMS370C080ANA TMS370C080ANL TMS370C080ANT



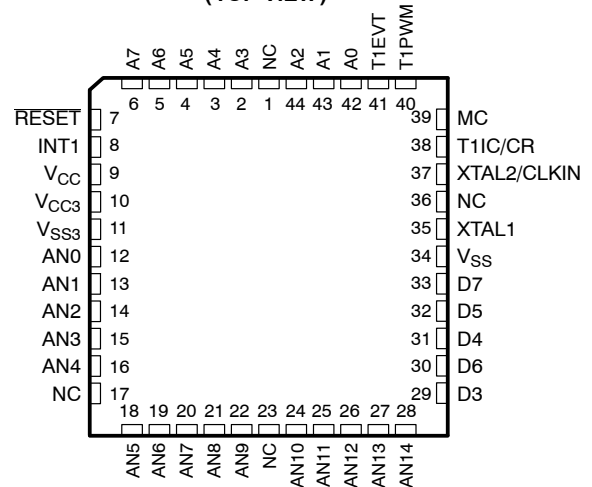
General Information	1
Selection Guide/Tools	2
Ops Cond/Timing/Glossary	3
TMS370Cx0x Data Sheet	4
TMS370Cx1x Data Sheet	5
TMS370Cx2x Data Sheet	6
TMS370Cx32 Data Sheet	7
TMS370Cx36 Data Sheet	8
TMS370Cx4x Data Sheet	9
TMS370Cx5x Data Sheet	10
TMS370Cx6x Data Sheet	11
TMS370Cx7x Data Sheet	12
TMS370Cx8x Data Sheet	13
TMS370Cx9x Data Sheet	14
TMS370CxAx Data Sheet	15
TMS370CxBx Data Sheet	16
TMS370CxCx Data Sheet	17
Mechanical Data	18
Quality and Reliability	19
Electrostatic Discharge Guidelines	20

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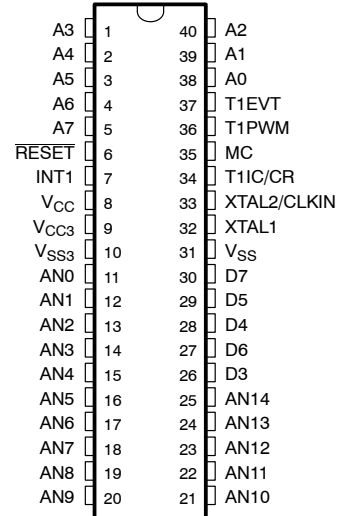
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- **CMOS/EEPROM/EPROM Technologies on a Single Device**
 - Mask-ROM Devices for High-Volume Production
 - One-Time-Programmable (OTP) EPROM Devices for Low-Volume Production
 - Reprogrammable EPROM Devices for Prototyping Purposes
- **Internal System Memory Configurations**
 - On-Chip Program Memory Versions
 - ROM: 4K Bytes
 - EPROM: 8K Bytes
 - Data EEPROM: 256 Bytes
 - Static RAM: 128 Bytes Usable as Registers
- **Flexible Operating Features**
 - Low-Power Modes: STANDBY and HALT
 - Commercial, Industrial, and Automotive Temperature Ranges
 - Clock Options:
 - Divide-by-4 (0.5 MHz – 5 MHz SYSCLK)
 - Divide-by-1 (2 MHz – 5 MHz SYSCLK)
 - PLL
 - Supply Voltage (V_{CC}): $5\text{ V} \pm 10\%$
- **15-Channel 8-Bit A/D Converter 3**
- **16-Bit General-Purpose Timer**
 - Software Configurable as
 - a 16-Bit Event Counter, or
 - a 16-Bit Pulse Accumulator, or
 - a 16-Bit Input Capture Function, or
 - Two Compare Registers, or
 - a Self-Contained Pulse-Width-Modulation (PWM) Function
 - 8-Bit Prescaler, Providing a 24-Bit Real-Time Timer
- **On-Chip 24-Bit Watchdog Timer**
 - EPROM/OTP Devices: Standard Watchdog
 - Mask ROM Devices: Hard Watchdog, Simple Counter, or Standard Watchdog
- **TMS370 Series Compatibility**
 - Instructions Upwardly Compatible With All TMS370 Devices
 - Register-to-Register Architecture
 - 128 or 256 General-Purpose Registers
 - 14 Powerful Addressing Modes
- **Flexible Interrupt Handling**

**FN AND FZ PACKAGES
(TOP VIEW)**



**JC AND NJ PACKAGES
(TOP VIEW)**



- **CMOS/Package /TTL-Compatible I/O Pins**
 - 40- and 44-Pin Plastic and Ceramic Shrink Dual-In-Line and Leaded Chip Carrier Packages / 16 Bidirectional; 9 Input Pins
 - All Peripheral Function Pins Are Software Configurable for Digital I/O
- **Workstation/PC-Based Software Development System**
 - C Compiler and C Source Debugger
 - Real-Time In-Circuit Emulation
 - Extensive Breakpoint/Trace Capability
 - Software Performance Analysis
 - Multi-Window User Interface
 - Microcontroller Programmer



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Pin Descriptions

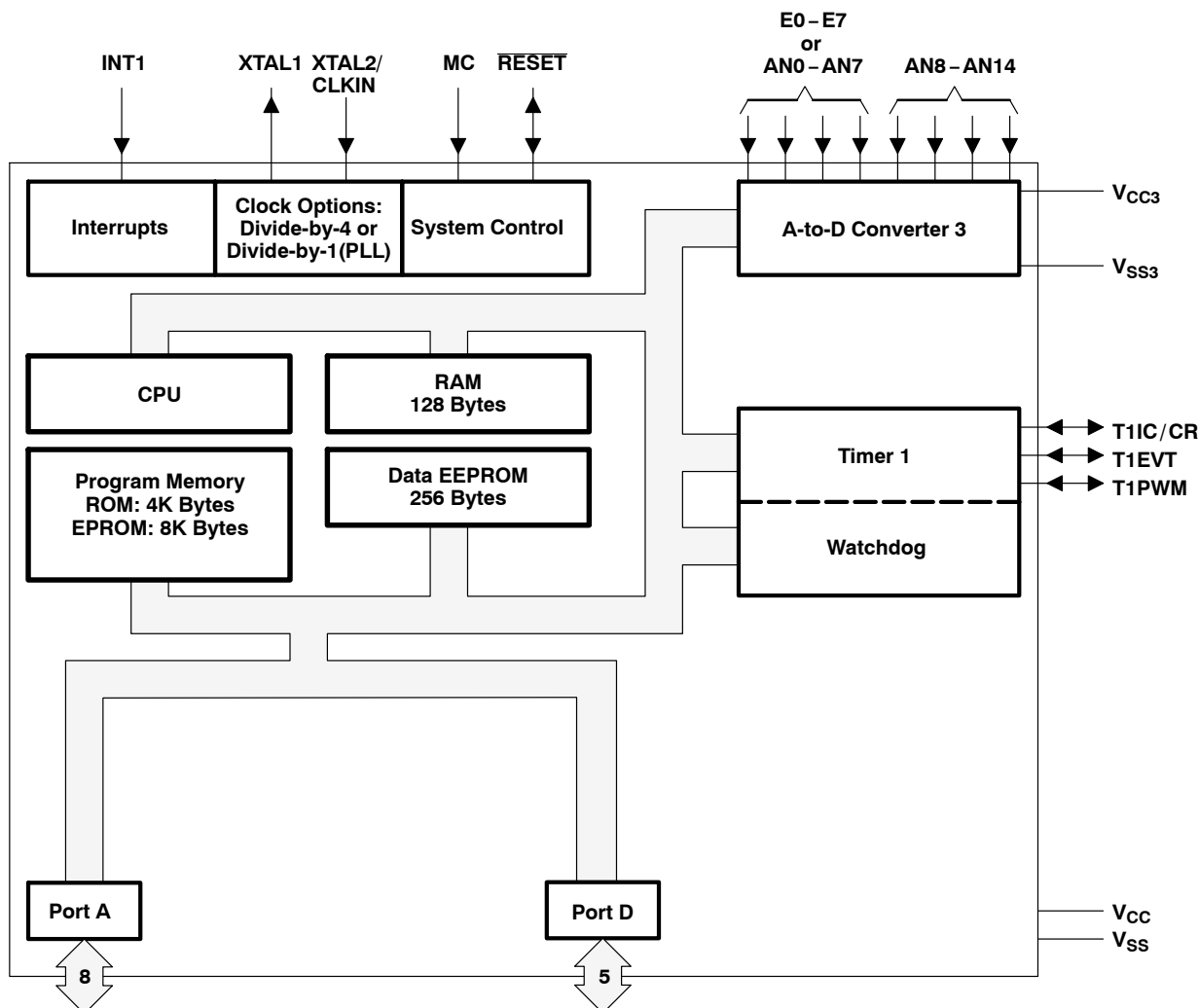
PIN			I/O†	DESCRIPTION‡
NAME	SDIP (40)	LCC (44)		
A0 A1 A2 A3 A4 A5 A6 A7	38 39 40 01 02 03 04 05	42 43 44 02 03 04 05 06	I/O	Port A is a general-purpose bidirectional I/O port.
D3/SYSCLK D4 D5 D6 D7	26 28 29 27 30	29 31 32 30 33	I/O	Port D is a general-purpose bidirectional I/O port. D3 is also configurable as SYSCLK.
AN0/E0 AN1/E1 AN2/E2 AN3/E3 AN4/E4 AN5/E5 AN6/E6 AN7/E7	11 12 13 14 15 16 17 18	12 13 14 15 16 18 19 20	I	ADC3 analog input (AN0 – AN7) or positive reference pins (AN6 – AN7) Port E can be individually programmed as general-purpose input pins if not used as ADC3 analog input. Only AN6 and AN7 can be software-configured as positive reference input.
AN8 AN9 AN10 AN11 AN12 AN13 AN14	19 20 21 22 23 24 25	21 22 24 25 26 27 28	I	ADC3 analog input pins
INT1	7	8	I	External (nonmaskable or maskable) interrupt/general-purpose input pin
T1IC/CR T1PWM T1EVT	34 36 37	38 40 41	I/O	Timer1 input capture/counter reset input pin/general-purpose bidirectional pin Timer1 PWM output pin/general-purpose bidirectional pin Timer1 external event input pin/general-purpose bidirectional pin
RESET	6	7	I/O	System-reset bidirectional pin. RESET, as an input, initializes the microcontroller; as open-drain output, RESET indicates an internal failure was detected by the watchdog or oscillator fault circuit.
MC	35	39	I	Mode control (MC) pin. MC enables EEPROM write-protection override (WPO) mode, also EPROM V _{PP} .
XTAL2/CLKIN XTAL1	33 32	37 35	I O	Internal oscillator crystal input/external clock source input Internal oscillator output for crystal
V _{CC}	8	9		Positive supply voltage for digital logic
V _{SS}	31	34		Ground reference for digital logic
V _{CC3}	9	10		Positive supply voltage for ADC3
V _{SS3}	10	11		Ground reference for ADC3
NC	—	1, 17, 23, 36		These pins have no connection to the internal die.

† I = input, O = output

‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Also, port D3 can be configured as SYSCLK.



functional block diagram



description

The TMS370C090A, TMS370C792, and SE370C792 devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx9x refers to these devices. The TMS370 family provides cost-effective real-time system control through integration of advanced peripheral function modules and various on-chip memory configurations.

The TMS370Cx9x family is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technologies. The low-operating power, wide-operating temperature range, and noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx9x devices attractive in system designs for automotive electronics, industrial motor control, computer peripheral control, telecommunications, and consumer application.

All TMS370Cx9x devices contain the following on-chip peripheral modules:

- Fifteen-channel, 8-bit analog-to-digital converter 3 (ADC3)
- One 24-bit general-purpose watchdog timer
- One 16-bit general-purpose timer with an 8-bit prescaler

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description (continued)

Table 1 provides a memory configuration overview of the TMS370Cx9x devices.

Table 1. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		PACKAGES 44 PIN PLCC/CLCC, OR 40 PIN PSDIP/CSDIP
	ROM	EPROM	RAM	EEPROM	
TMS370C090A	4K	—	128	256	FN – PLCC / NJ [‡] – PSDIP
TMS370C792	—	8K	128	256	FN – PLCC / NJ [‡] – PSDIP
SE370C792 [†]	—	8K	128	256	FZ – CLCC / JC – CSDIP

[†] System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.

[‡] The NJ designator for the 40-pin plastic shrink DIP package was formerly known as N2. The mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

The suffix letter A appended to the device names shown in the device column of Table 1 indicates the configuration of the device. ROM and EPROM devices have a different configuration as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 2. Suffix Letter Configuration

DEVICE [§]	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM without A	Standard	Divide-by-4 (Standard oscillator)	Enabled
ROM A	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

[§] Refer to the “device numbering conventions” section for device nomenclature and the “device part numbers” section for ordering.

The 4K bytes of mask-programmable ROM in the associated TMS370Cx9x device are replaced with 8K bytes of EPROM in the TMS370C792 while all other available memory and on-chip peripherals are identical. A one-time-programmable device (OTP) (TMS370C792) and a reprogrammable device (SE370C792) are available.

The TMS370C792 OTP device is available in a plastic package. This microcontroller is effective for use as an immediate production update for the TMS370Cx9x ROM device or for low-volume production runs when the mask charge or cycle time for the low-cost mask-ROM device is not practical.

The SE370C792 has a windowed ceramic package that allows reprogramming of the program EPROM memory during the development/prototyping design phase. The SE370C792 device allows quick updates to breadboards and prototype systems while iterating initial designs.

The TMS370Cx9x family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all CPU activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx9x features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx9x family is fully instruction-set-compatible, allowing easy transition between members of the TMS370 8-bit microcontroller family.



description (continued)

The TMS370Cx9x family provides the system designer with very economical, efficient solutions to real-time control applications. The TMS370 family extended development system (XDS™) and compact development tool (CDT™) solve the challenge of efficiently developing the software and hardware required to design the TMS370Cx9x into an ever-increasing number of complex applications. The application source code can be written in assembly and C-language, and the output code can be generated by the linker. The TMS370 family XDS development tools communicate through a standard RS-232-C interface with a personal computer. This allows the use of personal-computer editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes ease-of-use through extensive use of menus and screen windowing so that a system designer with minimal training can begin developing software. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as reduced time-to-market cycle.

The TMS370Cx9x family together with the TMS370 family XDS22, CDT370 PACT, software tools, the SE370C792 reprogrammable device, comprehensive product documentation, and customer support provide a complete solution to the needs of the system designer.

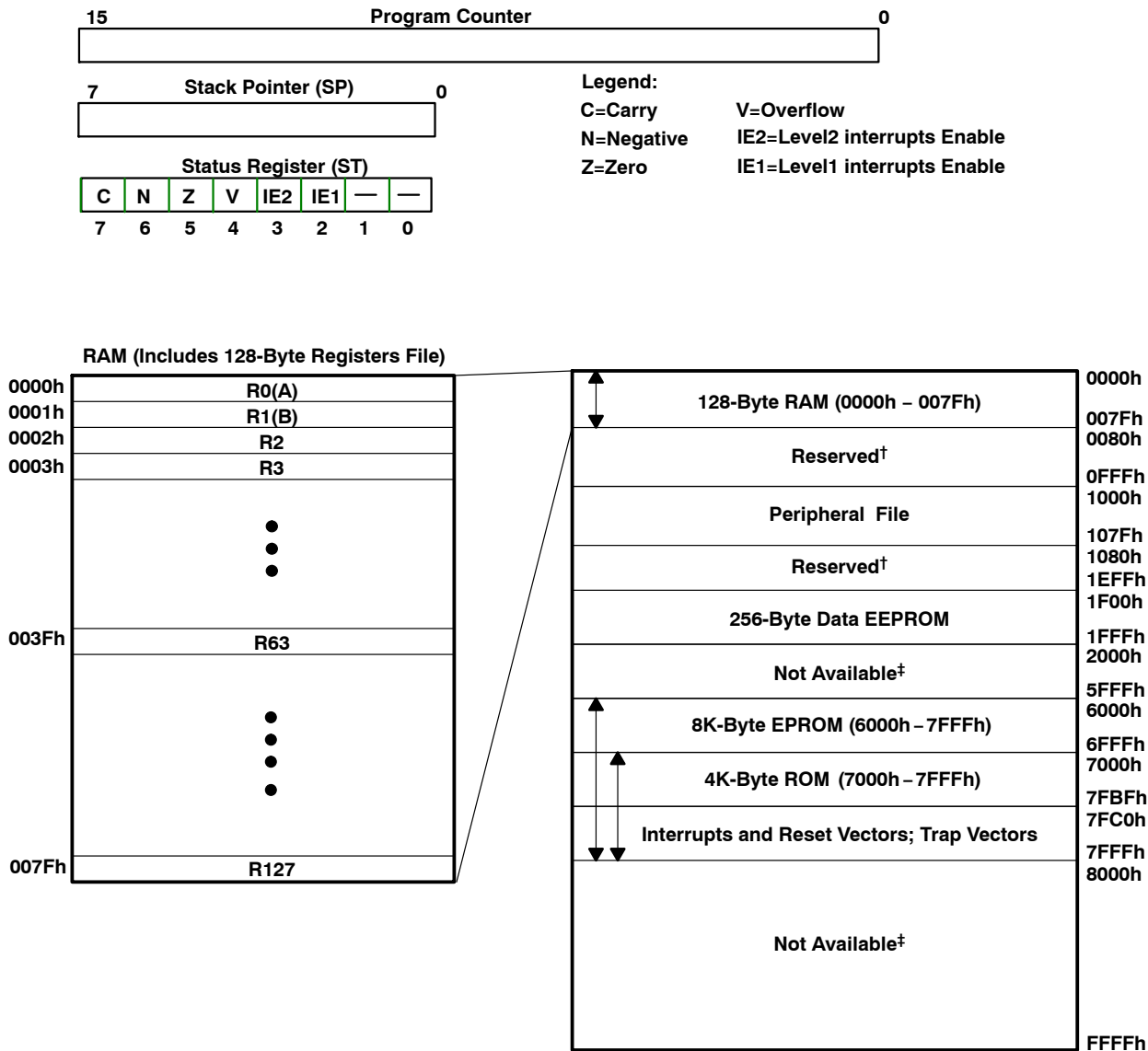
CPU

The CPU used on TMS370Cx9x devices is the high-performance 8-bit TMS370 CPU module. The 'x9x implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'x9x instruction set is summarized in Table 21. Figure 1 illustrates the CPU registers and memory blocks.

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CPU (continued)



† Reserved means that the address space is reserved for future expansion.

‡ Not available means that the address space is not accessible.

Figure 1. Programmer's Model

CPU (continued)

The 'x9x CPU architecture provides the following components:

- CPU registers:
 - A stack pointer that points to the last entry in the memory stack
 - A status register that monitors the operation of the instructions and contains the global-interrupt-enable bits
 - A program counter (PC) that points to the memory location of the next instruction to be executed
- A memory map that includes :
 - 128 bytes of general-purpose RAM that can be data memory storage, program instructions, general-purpose register, or the stack (can be located only in the first 128 bytes)
 - A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM/EPROM programming control
 - A 256-byte EEPROM module that provides in-circuit programmability and data retention in power-off conditions
 - 4K bytes of ROM or 8K bytes of EPROM program memory

stack pointer (SP)

The SP is an 8-bit CPU register. Stack operates as a last-in, first-out, read/write memory. The stack is used typically to store the return address on subroutine calls as well as the status register contents during interrupt sequences.

The SP points to the last entry or to the top of the stack. The SP increments automatically before data is pushed onto the stack and decrements after data is popped from the stack. The stack can be located only in the first 128 bytes of the on-chip RAM memory.

status register (ST)

The ST monitors the operation of the instructions and contains the global-interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits:

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional jump instructions) use these status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

The ST register and status bit notation are shown in Table 3.

Table 3. Status Register

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

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CPU (continued)

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most-significant byte (MSbyte) and least-significant byte (LSbyte) of a 16-bit address.

The contents of the reset vector (7FFEh, 7FFFh) are loaded into the program counter during reset. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 6000h as the contents of memory locations 7FFEh and 7FFFh (reset vector).

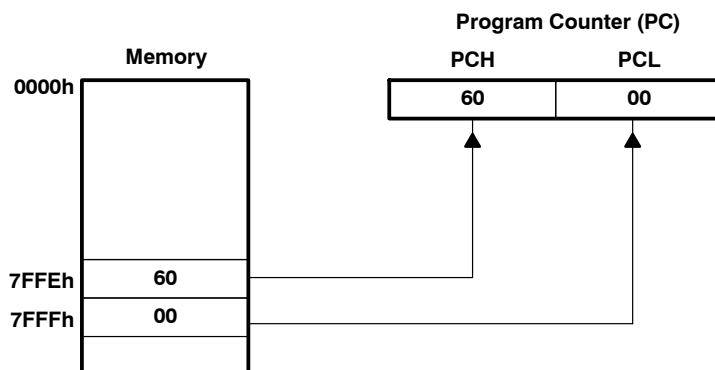


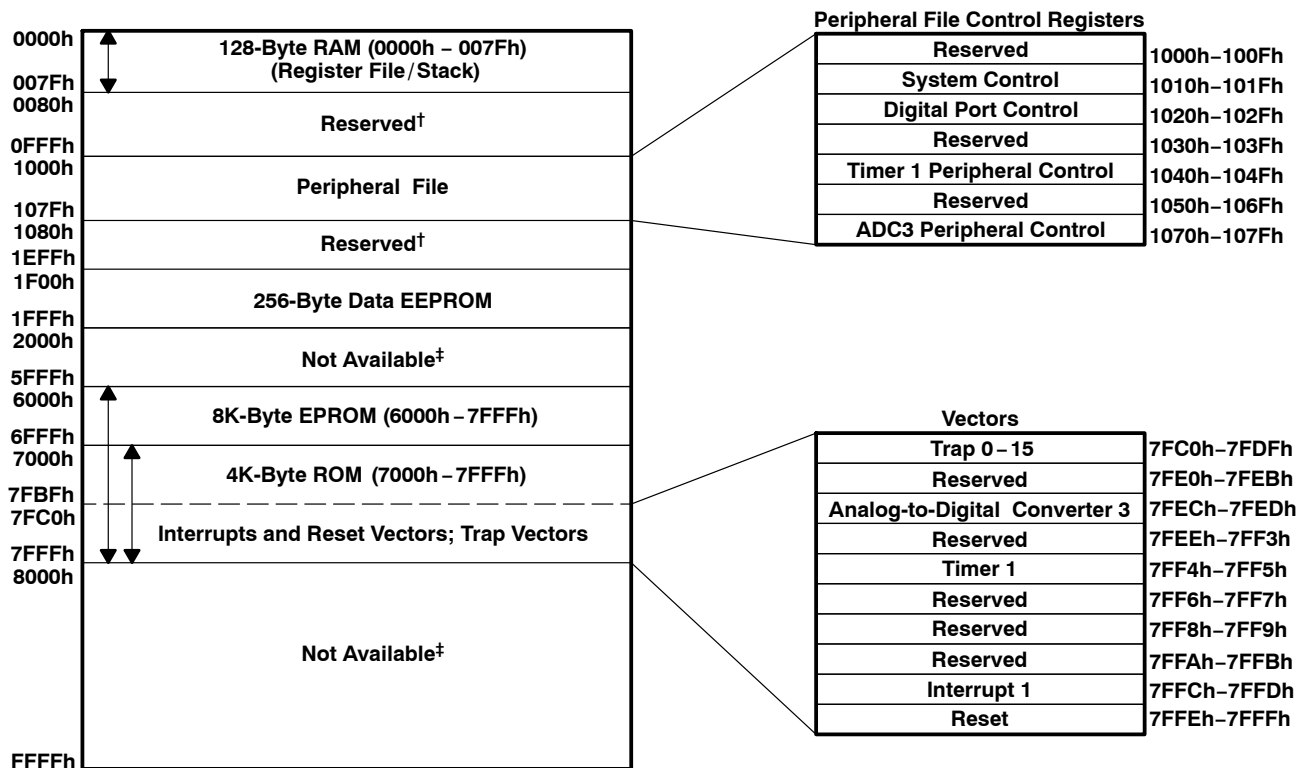
Figure 2. Program Counter After Reset

memory map

The TMS370Cx9x architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. As shown in Figure 3, the TMS370Cx9x provides a memory-mapped RAM, ROM, data EEPROM, EPROM, input/output pins, peripheral functions, and system-interrupt vectors.

The peripheral file contains all input/output port control, peripheral status and control, EPROM, EEPROM programming, and system-wide control functions. The peripheral file consists of 256 contiguous addresses located from 1000h to 107Fh and logically divided into seven peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed. The TMS370Cx9x has its on-chip peripherals and system control assigned to peripheral file frames 1 through 7, addresses 1010h through 107Fh.

CPU (continued)



† Reserved = the address space is reserved for future expansion.

‡ Not available = address space is unavailable in the mode illustrated.

Figure 3. TMS370Cx9x Memory Map

RAM/register file (RF)

Locations within RAM address space can serve as the register file, general-purpose read/write memory, program memory, or stack instructions. The TMS370Cx9x device contains 128 bytes of internal RAM mapped beginning at location 0000h (R0) and continuing through location 007Fh (R127) which is shown in Figure 3.

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370Cx9x control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the peripheral file (PF) directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or by P for a decimal designator. For example, the system control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 4 shows the TMS370Cx9x peripheral files address map.

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peripheral file (PF) (continued)

Table 4. TMS370Cx9x Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h–100Fh	P000–P00F	Reserved
1010h–101Fh	P010–P01F	System and EEPROM/EPROM control registers
1020h–103Fh	P020–P03F	Digital I/O port control registers
1030h–103Fh	P030–P03F	Reserved
1040h–104Fh	P040–P04F	Timer 1 registers
1050h–106Fh	P050–P06F	Reserved
1070h–107Fh	P070–P07F	Analog-to-digital converter 3 registers
1080h–10FFh	P080–P0FF	Reserved

data EEPROM

The TMS370Cx9x devices contain 256 bytes of data EEPROM and have a memory map beginning at location 1F00h and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127), or the *TMS370 Family Data Manual* (literature number SPNS014B). The data EEPROM features include the following:

- Programming:
 - Bit, byte, and block write/erase modes
 - Internal charge pump circuitry: No external EEPROM programming voltage supply is needed.
 - Control register: Data EEPROM programming is controlled by the data EEPROM control register (DEECTL) located in the PF frame beginning at location P01A.
 - In-circuit programming capability: There is no need to remove the device to program.
- Write-protection: Writes to the data EEPROM are disabled during the following conditions:
 - Reset: All programming of the data EEPROM module is halted.
 - Write protection active: there is one write-protect bit per 32-byte EEPROM block.
 - Low-power mode operation
- Write protection can be overridden by applying 12 V to the MC pin.

Table 5 shows the memory map of the control registers.

Table 5. Data EEPROM and Program EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME
101Ah (P01A)	DEECTL	Data EEPROM control register
101Bh (P01B)	—	Reserved
101Ch (P01C)	EPCTL	Program EPROM control register

program EPROM

The TMS370C792 contains 8K bytes of program EPROM memory mapped beginning at location 6000h and continuing through location 7FFFh as shown in Figure 3. Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments (TI™) and addresses 7FECb through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh. Reading the program EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the program EPROM control register (EPCTL). The program EPROM modules' features include:

- Programming
 - In-circuit programming capability if V_{PP} is applied to the MC pin
 - Control register: Program EPROM programming is controlled by the program EPROM control registers EPCTL located at the addresses in PF frame 1 as shown in Table 5.
- Write protection: Writes to the program EPROM are disabled under the following conditions:
 - Reset: All programming to the EPROM module is halted.
 - Low-power modes
 - 13 V not applied to MC

program ROM

The program ROM consists of 4K bytes of mask-programmable ROM. The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication. Memory addresses 7FE0h through 7FEBh are reserved for TI and addresses 7FECb through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh.

system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx9x CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are internally generated, while one ($\overline{\text{RESET}}$) is controlled externally. These actions are as follows:

- External $\overline{\text{RESET}}$ pin. A low level signal can trigger an external reset. To assure a reset, the external signal should be held low for one SYSCLK cycle (it is possible, however, that a signal of less than one SYSCLK could cause a reset). See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.
- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register or if the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside of the recommended operating range. See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x9x device to reset external system components. Additionally, if a cold start condition (V_{CC} is off for several hundred milliseconds), oscillator failure occurs, or $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator fault flag (OSC FLT FLAG, SCCR0.4), the cold start flag (COLD START, SCCR0.7), and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 6 depicts the reset sources.

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system reset (continued)

Table 6. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT NAME	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Registers A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to by the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

$\overline{\text{RESET}}$ must be held low until the clock signal is valid and V_{CC1} is within the operating range, when an external reset circuit is connected to $\overline{\text{RESET}}$. Figure 4 shows a typical reset circuit.

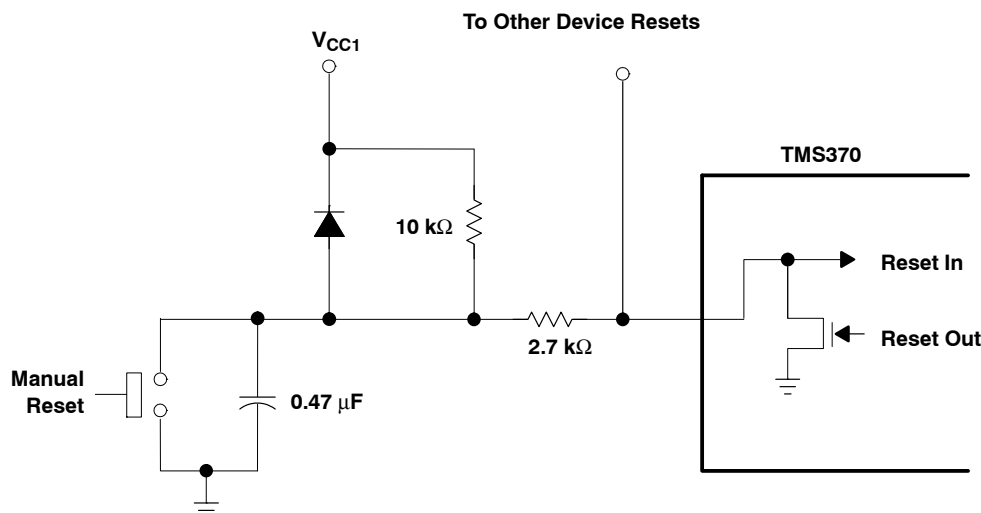


Figure 4. Typical Reset Circuit

interrupts

The TMS370 family software programmable interrupt structure permits flexible on-chip and external-interrupt configurations to meet real-time interrupt-driven application requirements. The hardware-interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global-interrupt mask bits (IE1 and IE2) of the status register.

interrupts (continued)

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is configured selectively on either the high- or low-priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

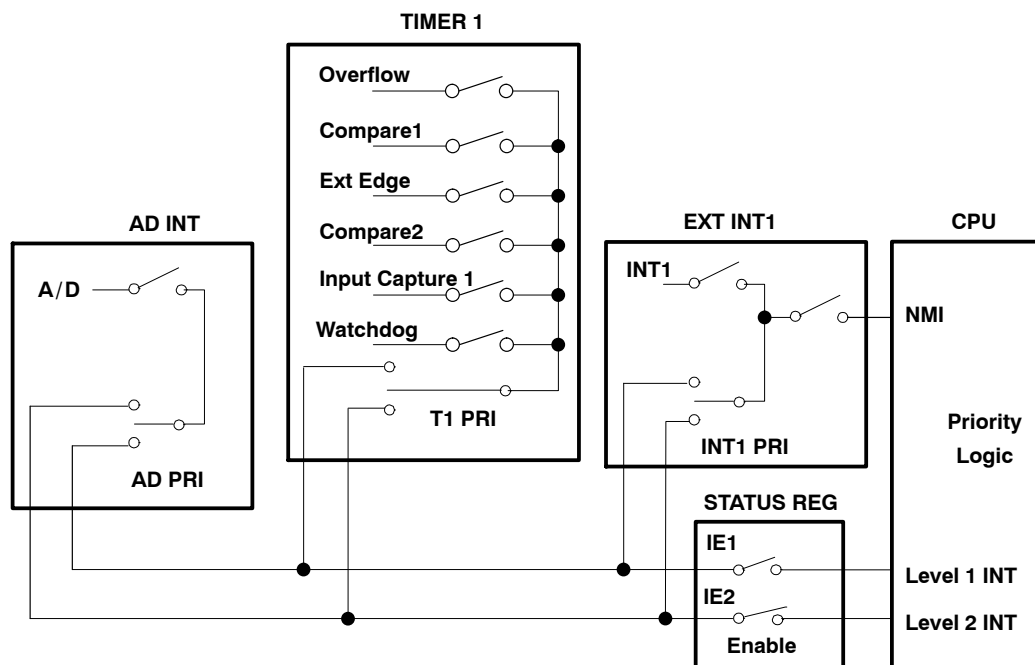


Figure 5. Interrupt Control

The TMS370Cx9x has three hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 7. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. A system interrupt can have multiple interrupt sources. All of the interrupt sources are individually maskable by local interrupt-enable control bits in the associated PF. Each interrupt source FLAG bit is individually readable for software polling or for determining which interrupt source generated the associated system interrupt.

Two of the system interrupts are generated by on-chip peripheral functions, and one external interrupt is supported. Software configuration of the external interrupt is performed through the INT1 control registers in peripheral file frame 1. The external is software-configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software-configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual or global enable mask bits. The INT1 NMI bit is protected during non-privileged operation and, therefore, should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupt INT1 can be software-configured as a general-purpose input pin if the interrupt function is not required.

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interrupts (continued)

Table 7. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY [†]
External RESET Watchdog overflow Oscillator fault detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	RESET [‡]	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1 [‡]	7FFCh, 7FFDh	2
Timer 1 overflow Timer 1 compare 1 Timer 1 compare 2 Timer 1 external edge Timer 1 input capture 1 Watchdog overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT [§]	7FF4h, 7FF5h	3
A/D conversion complete	AD INT FLAG	ADINT	7FECh, 7FEDh	4

[†] Relative priority within an interrupt level.

[‡] Releases microcontroller from STANDBY and HALT low-power modes.

[§] Releases microcontroller from STANDBY low-power mode.

privileged operation and EEPROM write-protection override

The TMS370Cx9x family has significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a broad variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx9x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) should be set to one to enter the nonprivileged mode; disabling write operations to specific configuration control bits within the peripheral file. Table 8 displays the system configuration bits that are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

Table 8. Privilege Bits

REGISTER [¶]		CONTROL BIT
NAME	LOCATION	
SCCRO	P010.6 P010.6	PF AUTO WAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST
ADPRI	P07F.5 P07F.6 P07F.7	AD ESPEN AD PRIORITY AD STEST

[¶] The privilege bits are shown in a bold typeface in the system configuration registers section.



privileged operation and EEPROM write-protection override (continued)

The write-protect override (WPO) mode provides an external hardware method of overriding the write-protection registers of data EEPROM on the TMS370Cx9x. Applying a 12-V input to the MC pin after the RESET input goes high (logic 1) enters the WPO mode. The high voltage on MC during the WPO mode is not the programming voltage for the data EEPROM or program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware system level capability to modify the content of the data EEPROM while the device remains in the application, but only while requiring a 12-V external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power and IDLE modes

The TMS370Cx9x devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time when the mask is manufactured.

The STANDBY and HALT low power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the idle instruction when the PWRDWN/IDLE bit in register SCCR2 has been set to one. The HALT/STANDBY bit in SCCR2 controls which low-power mode is entered.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, and timer 1 remain active. System processing is suspended until a qualified interrupt (hardware RESET, external interrupt on INT1, or timer 1 interrupt) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx9x is placed in its lowest power-consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware RESET or an external interrupt on INT1) is detected. The low-power mode selection bits are summarized in Table 9.

Table 9. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X	IDLE

X = don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6–7 bits is ignored. In addition, if an IDLE instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method of always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI is always generated, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the watchdog timer is inhibited.

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clock modules

The '370Cx9x family provides two clock options which are referred to as divide-by-1 (PLL) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The '370C090A ROM-masked devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on the ROM device while the EPROM device '792 has only the divide-by-4 clock.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a 1-to-1 match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency. The divide-by-4 produces a SYSCLK which is one-fourth the frequency of the external resonator. Inside the divide-by-1 module, the frequency of the external resonator is multiplied by four. The clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. The frequencies are formulated as follows:

$$\text{Divide-by-4 option : SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option : SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is that EMI is reduced. The harmonics of low-speed resonators extend through less of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 provides the capability of reducing the resonator speed by four times, and this results in a steeper decay of emissions produced by the oscillator.



system configuration registers

Table 10 contains system configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in a bold typeface and shaded.

Table 10. Peripheral File Frame 1: System Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTOWAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018 to P019	Reserved								
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D to P01F	Reserved								

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digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 11 displays the specific addresses, registers, and control bits within this peripheral file frame.

Table 11. Peripheral File Frame 2: Digital Port Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 [†] (must be 0)					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 12. Port Configuration Register Setup

PORT	PIN	abcd 00q1	abcd 00y0
A	0–7	Data out q	Data in y
D	3–7	Data out q	Data in y
a = Port x control register 1 b = Port x control register 2 c = Data d = Direction			

timer 1 module

The programmable timer 1 (T1) module of the TMS370Cx9x provides the designer with the enhanced timer resources required to perform real-time system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers, T1 and WD, allow program selection of input clock sources (real-time, external event, or pulse-accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The T1 module includes three external device pins that can be used for multiple counter functions (operation-mode dependent) or used as general-purpose I/O pins. The T1 module block diagram is shown in Figure 6.

timer 1 module (continued)

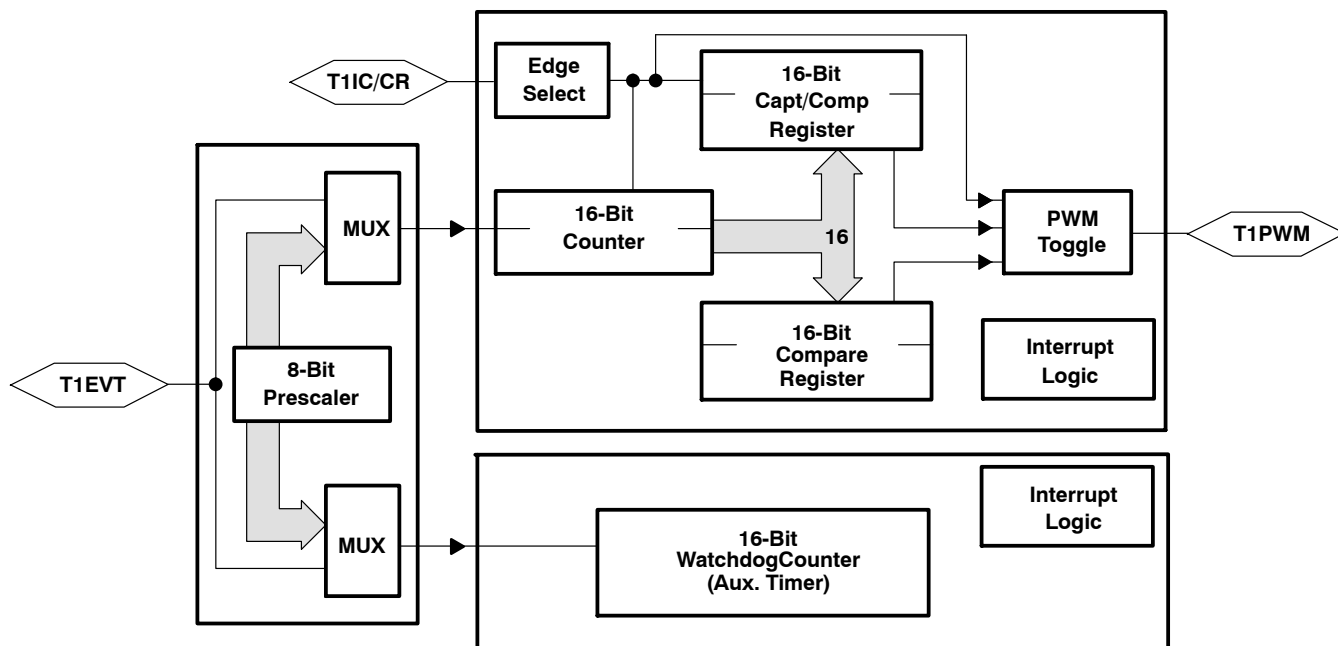


Figure 6. Timer 1 Block Diagram

- Three T1 I/O pins:
 - T1IC/CR: Timer 1 input capture / counter reset input pin, or general-purpose bidirectional I/O pin
 - T1PWM: Timer 1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T1EVT: Timer 1 event input pin, or general-purpose bidirectional I/O pin
- Two operation modes:
 - Dual-compare mode: Provides PWM signal.
 - Capture/compare mode: Provides input capture pin.
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either capture or compare registers.
- One 16-bit watchdog counter can be used as an event counter, a pulse accumulator, or an interval timer if watchdog feature is not needed.
- Prescaler/clock sources that determines one of eight clock sources for general-purpose timer
- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR).

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timer 1 module (continued)

- Interrupts that can be generated on the occurrence of:
 - A capture
 - A compare equal
 - A counter overflow
 - An external edge detection
- Sixteen T1 module control registers: Located in the PF frame beginning at address P040.

Table 13 lists the T1 module control registers.

Table 13. Timer 1 Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Capture/Compare and Dual-Compare									
P040	Bit 15			T1 Counter MSbyte				Bit 8	T1CNTR
P041	Bit 7			T1 Counter LSbyte				Bit 0	
P042	Bit 15			Compare Register MSbyte				Bit 8	T1C
P043	Bit 7			Compare Register LSbyte				Bit 0	
P044	Bit 15			Capture/Compare Register MSbyte				Bit 8	T1CC
P045	Bit 7			Capture/Compare Register LSbyte				Bit 0	
P046	Bit 15			Watchdog Counter MSbyte				Bit 8	WDCNTR
P047	Bit 7			Watchdog Counter LSbyte				Bit 0	
P048	Bit 7			Watchdog Reset Key				Bit 0	WDRST
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Capture/Compare and Dual-Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

timer 1 module (continued)

The T1 capture/compare mode block diagram is illustrated in Figure 7. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

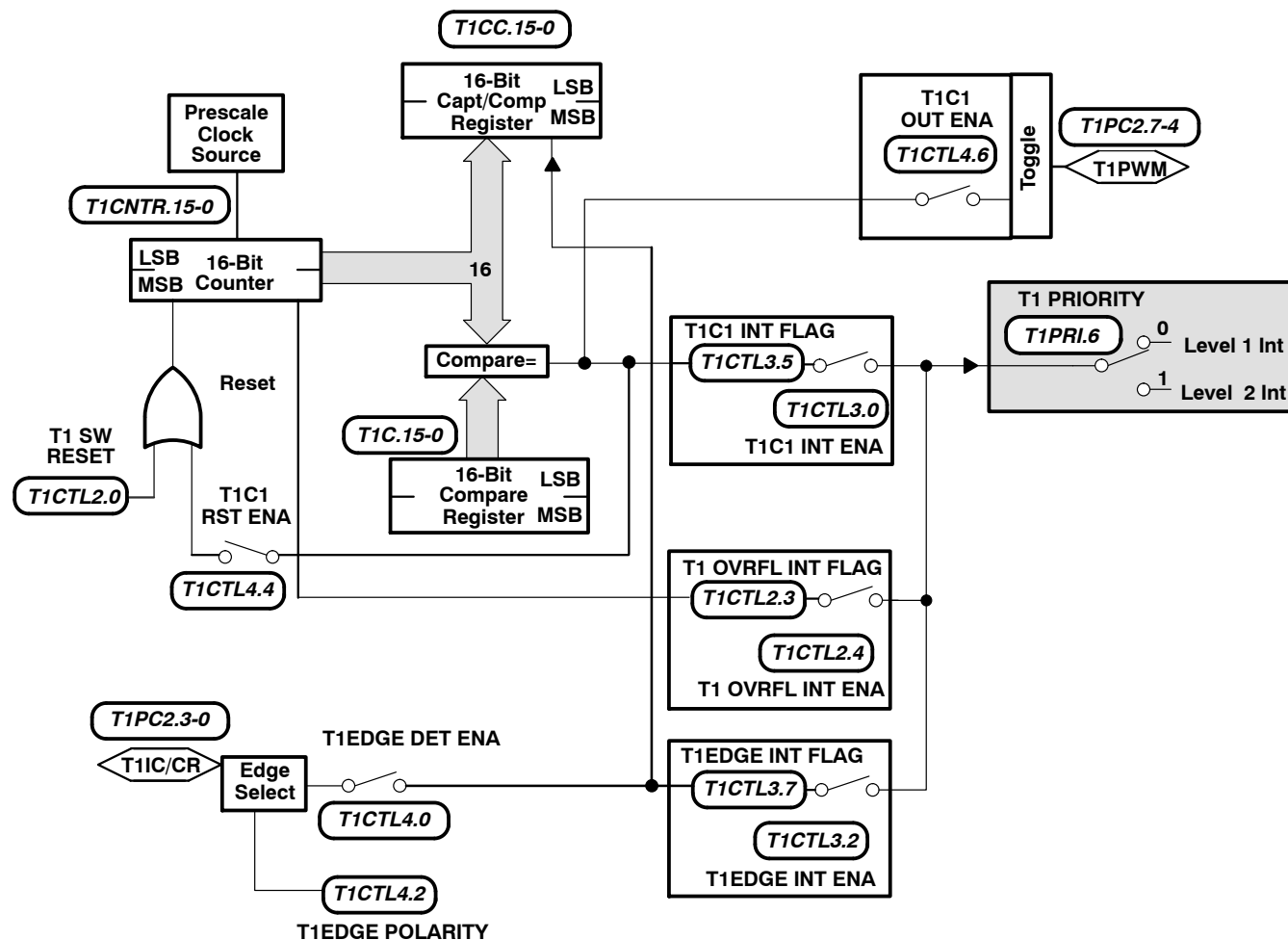


Figure 7. Capture/Compare Mode

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timer 1 module (continued)

The T1 dual-compare mode block diagram is illustrated in Figure 8. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

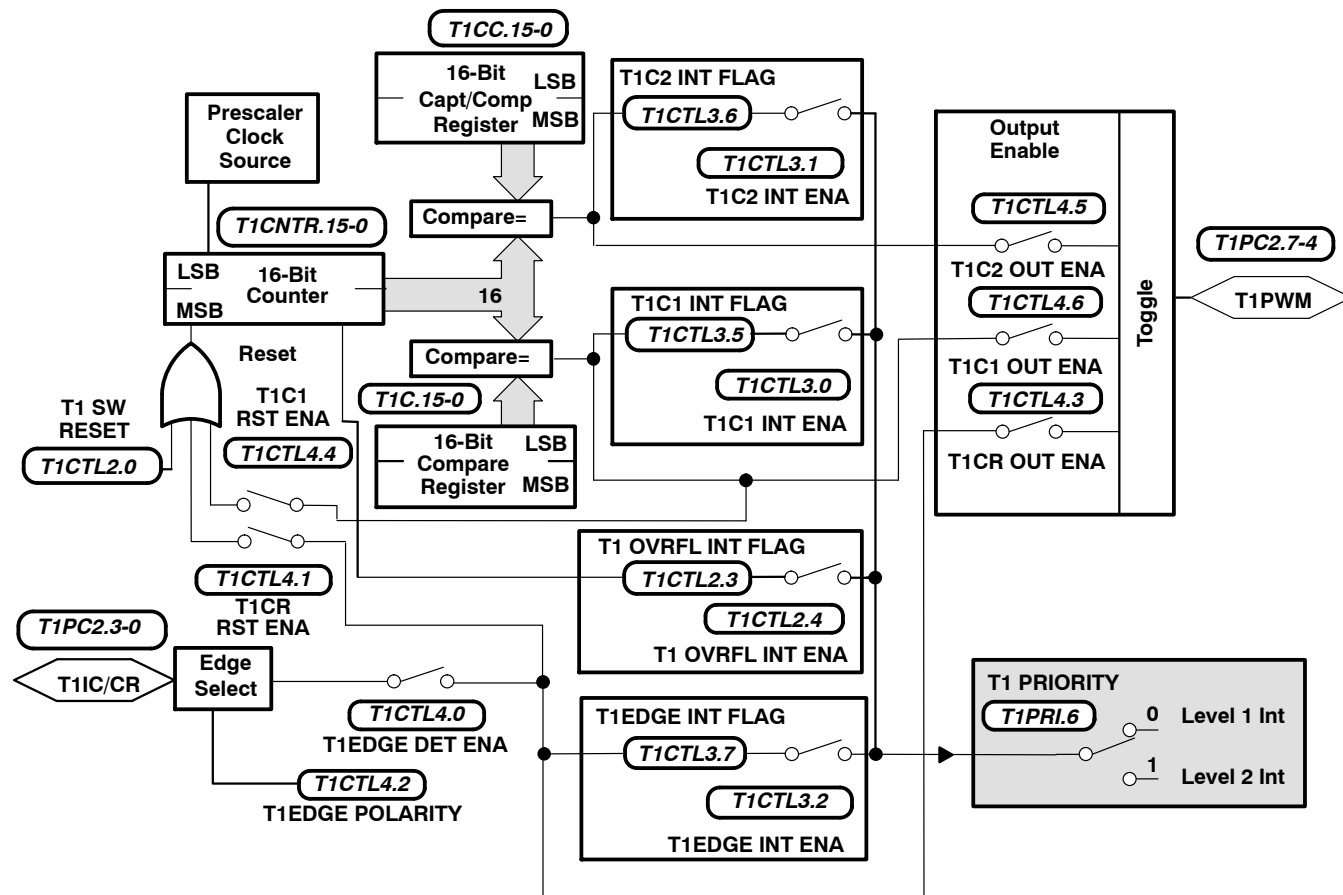


Figure 8. Dual-Compare Mode

timer 1 module (continued)

The TMS370Cx9x device includes a 24-bit watchdog (WD) timer, contained in the T1 module, which can be software programmed as an event counter, pulse accumulator, or interval timer if the WD function is not used. The WD function is to monitor software and hardware operation and implement a system reset when the WD counter is not serviced properly (WD counter overflow or WD counter is reinitialized by an incorrect value). The WD can be configured as one of the three mask options: standard WD, hard WD, or simple counter.

- Standard watchdog configuration for EPROM and mask-ROM devices (see Figure 9)
 - Watchdog mode
 - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the WD reset key or if the counter overflows
 - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
 - Non-watchdog mode
 - Watchdog timer can be configured as an event counter, pulse accumulator, or an interval timer

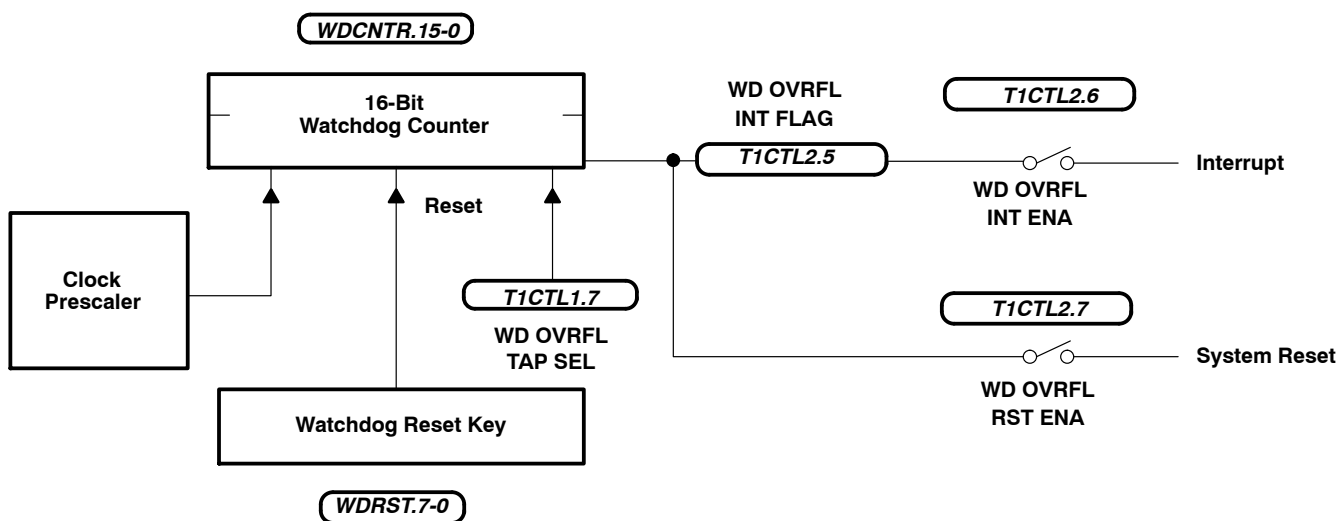


Figure 9. Standard Watchdog

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timer 1 module (continued)

- Hard watchdog configuration for mask-ROM device only (see Figure 10)
 - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows.
 - Automatic activation of the WD timer upon power-up reset
 - INT1 is enabled as nonmaskable interrupt during low-power modes
 - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset.

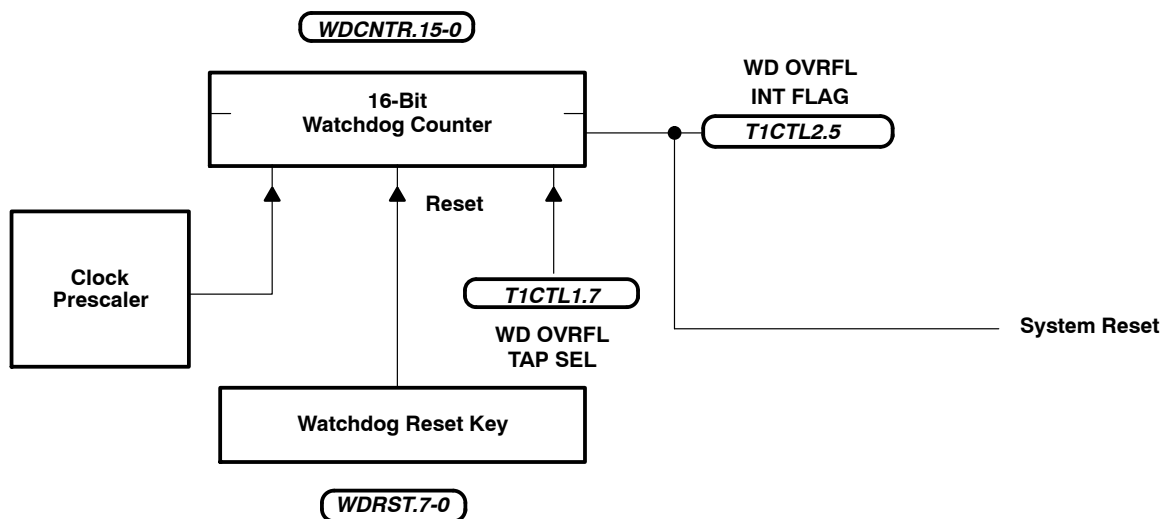


Figure 10. Hard Watchdog

timer 1 module (continued)

- Simple-counter configuration for mask-ROM devices only (see Figure 11)
 - Simple counter can be configured as an event counter, pulse accumulator, or an interval timer.

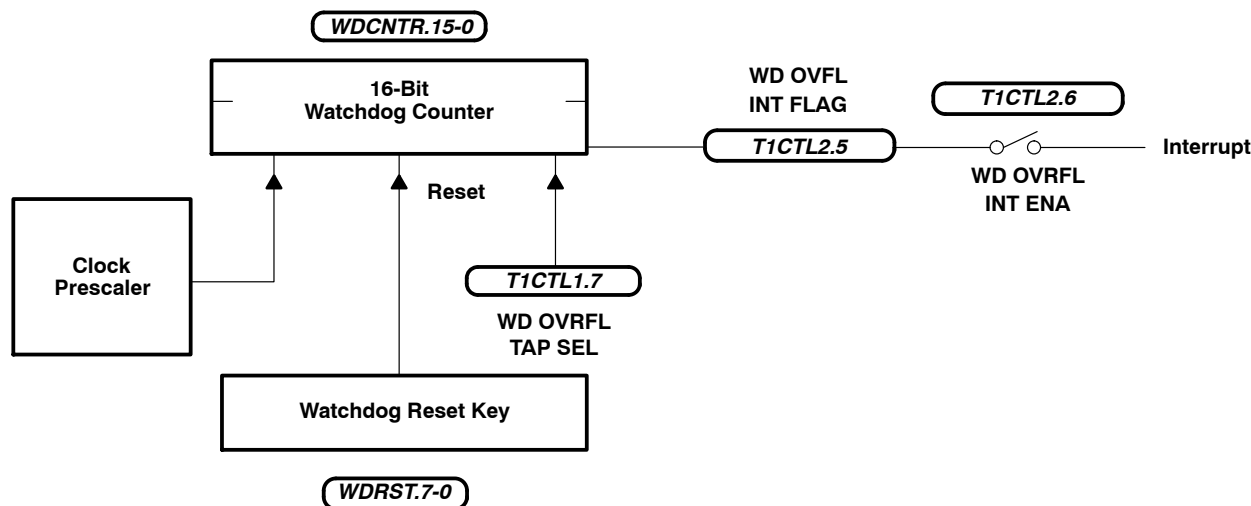


Figure 11. Simple Counter

analog-to-digital converter 3 module

The analog-to-digital converter 3 module is an 8-bit, successive approximation converter with internal sample-and-hold circuitry. The module has fifteen analog input channels – eight of the channels are multiplexed with port E – that allow the processor to convert the voltage levels from up to fifteen different sources. The ADC3 module features include the following:

- Minimum conversion time: 32.8 μ s at 5-MHz SYSCLK
- Seventeen external pins:
 - Fifteen analog input channels (AN0–AN14), eight (AN0–AN7) of which can be software configured as digital inputs (E0–E7) if not needed as analog channels
 - AN6–AN7 can also be configured as positive input voltage reference
 - V_{CC3}: ADC3 module high-voltage reference input
 - V_{SS3}: ADC3 module low-voltage reference input
- The ADDATA register, which contains the digital result of the last ADC3 conversion
- ADC3 operations can be accomplished through either interrupt driven or polled algorithms
- Six ADC3 module control registers are located in the ADC3 peripheral control register frame beginning at address 1070h.

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analog-to-digital converter 3 module (continued)

The ADC3 module control registers are illustrated in Table 14.

Table 14. ADC3 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P070	CONVERT START	SAMPLE START	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT3	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A/D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	AD RATE SELECT1	AD RATE SELECT0	ADPRI

analog-to-digital converter 3 module (continued)

The A/D module block diagram is illustrated in Figure 12.

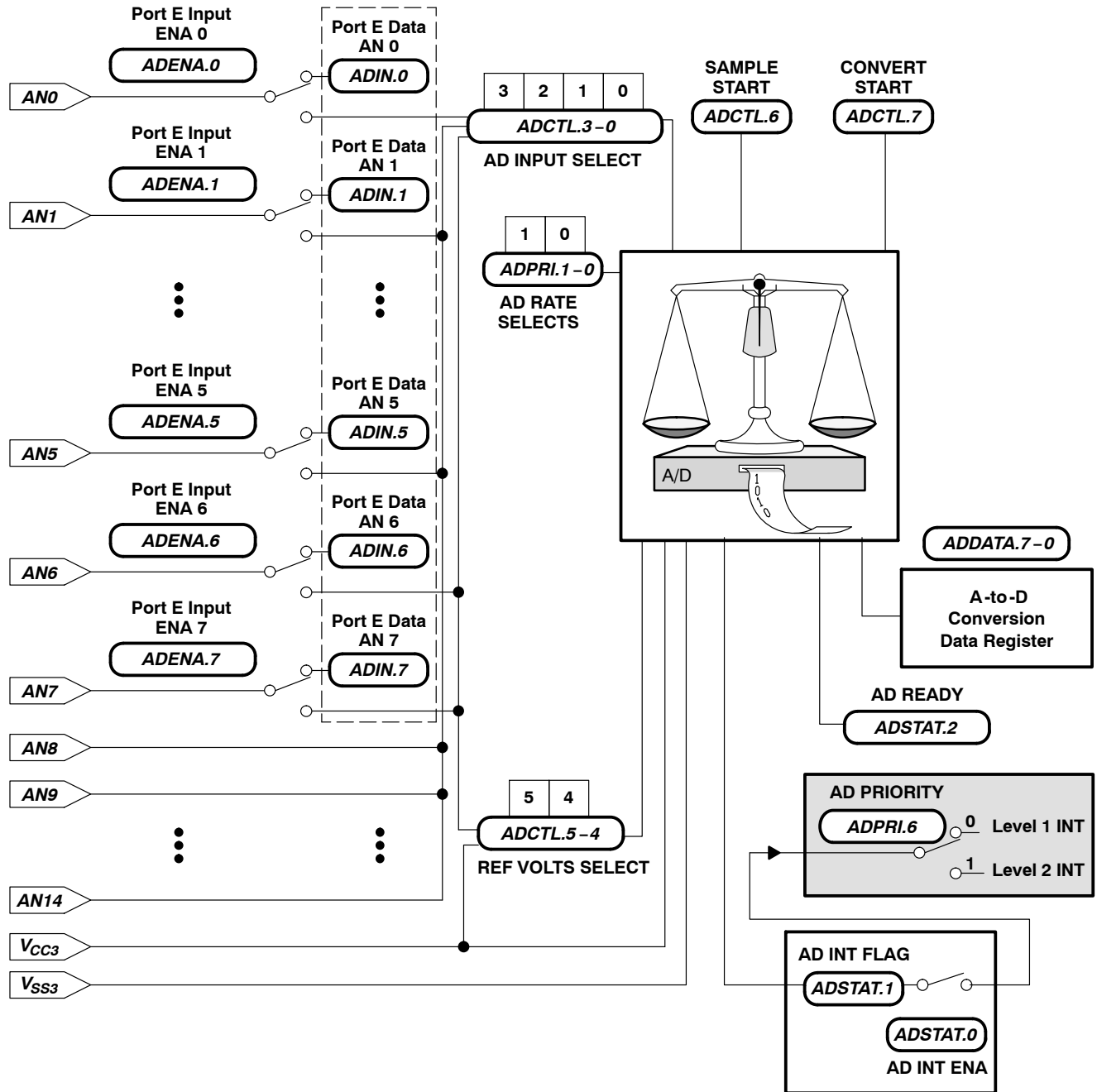


Figure 12. ADC3 Block Diagram

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analog-to-digital converter 3 module (continued)

Table 15. ADC3 Peripheral Control Register (ADCTL)

Bit #	7	6	5	4	3	2	1	0
P070	CONVERT START	SAMPLE START	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT3	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R = read, W = write, -n = value of the bit after the register is reset

BIT 0–3 AD INPUT SELECT 0–3 (Analog Input Channel Select Bits 0–3)

These bits select the channel used for conversion. Channels should be changed only after the ADC3 has cleared the SAMPLE START and CONVERT START bits. Changing the channel while either SAMPLE START or CONVERT START is 1 invalidates the conversion in progress.

AD INPUT SELECT 3	AD INPUT SELECT 2	AD INPUT SELECT 1	AD INPUT SELECT 0	AD INPUT CHANNEL
0	0	0	0	AN0
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	AN8
1	0	0	1	AN9
1	0	1	0	AN10
1	0	1	1	AN11
1	1	0	0	AN12
1	1	0	1	AN13
1	1	1	0	AN14

BIT 4–5 REF VOLT SELECT 4–5 (Reference Voltage (+V_{REF}) Select Bits 4–5)

These bits select the channel the ADC3 uses for the positive voltage reference. These bits must not change during the entire conversion.

REF VOLT SELECT 1	REF VOLT SELECT 0	+V _{REF} SOURCE
0	0	V _{CC3}
0	1	AN6
1	0	AN7

BIT 6 SAMPLE START (Sample Start)

Setting this bit stops any ongoing conversion and starts sampling the selected input channel to begin a new conversion. This bit is cleared by the ADC3. Entering HALT or STANDBY mode clears this bit and aborts any sampling in progress.

BIT 7 CONVERT START (Conversion Start)

Setting this bit starts the conversion. This bit is cleared by the ADC3. Entering HALT or STANDBY mode clears this bit and aborts any conversion in progress.



analog-to-digital converter 3 module (continued)

Table 16. ADC3 Peripheral Control Register (ADSTAT)

Bit #	7	6	5	4	3	2	1	0
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA
						R-0	RC-0	RW-0

R = read, W = write, C = clear only, -n = value of the bit after the register is reset

BIT 0 AD INT ENA (ADC3 Interrupt Enable)

This bit controls the ADC3 module's ability to generate an interrupt.

0 = Disable ADC3 interrupt.

1 = Enable ADC3 interrupt.

BIT 1 AD INT FLAG (ADC3 Interrupt Flag)

The ADC3 module sets this bit at the end of an A/D conversion. If this bit is set while the AD INT ENA bit is set, an interrupt request is generated. Clearing this flag clears pending ADC3 interrupt requests. This bit is cleared by the system reset or by entering HALT or STANDBY mode. Software cannot set this bit.

BIT 2 AD READY (ADC3 Converter Ready)

The ADC3 module sets this bit whenever a conversion is not in progress and the ADC3 is ready for a new conversion to start. Writing to this bit has no effect on its state.

0 = Conversion in process.

1 = Converter ready.

BIT 3-7 Reserved (Read data is indeterminate)

Table 17. ADC3 Conversion Data Register (DATA)

Bit #	7	6	5	4	3	2	1	0
P072	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R = read, -n = value of the bit after the register is reset

The analog-to-digital conversion data is loaded into this register at the end of a conversion and remains until replaced by another conversion

Table 18. AN0-AN7 Data Input Register (ADIN)

Bit #	7	6	5	4	3	2	1	0
P07D	PORT E DATA IN AN7	PORT E DATA IN AN6	PORT E DATA IN AN5	PORT E DATA IN AN4	PORT E DATA IN AN3	PORT E DATA IN AN2	PORT E DATA IN AN1	PORT E DATA IN AN0
	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R = read, -n = value of the bit after the register is reset

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analog-to-digital converter 3 module (continued)

The ADIN register shows the data present at the pins configured for general-purpose input instead of ADC3 channels. A bit is configured as general-purpose input if the corresponding bit of the port-enable register is a 1. Pins configured as ADC3 channels are read as 0's. Writing to this address has no effect.

Table 19. AN0–AN7 Input-Enable Register (ADENA)

Bit #	7	6	5	4	3	2	1	0
P07E	INPUT ENA 7	INPUT ENA 6	INPUT ENA 5	INPUT ENA 4	INPUT ENA 3	INPUT ENA 2	INPUT ENA 1	INPUT ENA 0
	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

R = read, –n = value of the bit after the register is reset

The ADENA register individually configures the pins AN0–AN7 as either analog input channels or as general-purpose input pins

0 = The pin becomes an analog-input channel for the ADC3. When the bit is 0, the corresponding bit in the ADIN register reads a 0.

1 = Enables the pin as a general-purpose input pin and its digital value can be read from the corresponding bit in the ADIN register.

Table 20. Analog Interrupt Priority/Conversion Rate Register (ADPRI)

Bit #	7	6	5	4	3	2	1	0
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	AD RATE SELECT1	AD RATE SELECT0
	RP–0	RP–0	RP–0				RW–0	RW–0

R = read, W = write, P = privileged write, –n = value of the bit after the register is reset

BIT 0–1 AD RATE SELECT 0–1 (ADC3 Conversion Rate Select Bits 0–1)

These bits determine the conversion rate of the ADC3 as a function of the system-clock frequency. Note that only the default selection (0,0) provides full XTAL2/CLKIN frequency range together with 8-bit precision. Other selections allow maintaining minimum conversion time at lower system-clock rates.

AD RATE SELECT 1	AD RATE SELECT 0	CONVERSION TIME (NUMBER OF SYSTEM CLOCK CYCLES)	MAXIMUM SYSCLK FREQUENCY
0	0	164	5 MHz ≥ SYSCLK > 2.5 MHz
0	1	84	2.5 MHz ≥ SYSCLK > 1.25 MHz
1	0	44	1.25 MHz ≥ SYSCLK > 0.625 MHz
1	1	22	0.625 MHz ≥ SYSCLK ≥ 0.5 MHz

NOTE: If selections different from (0,0) are used at XTAL2/CLKIN frequencies higher than specified in this table, the 8-bit precision of the ADC3 is not assured.

BIT 2–4 RESERVED (Read data is indeterminate)



analog-to-digital converter 3 module (continued)

- BIT 5** **AD ESPEN (Emulator Suspend Enable)**
- Normally this bit has no effect. However, when using the XDS emulator to debug a program, this bit determines what happens to the ADC3 when the program is suspended by an action such as a hardware or software breakpoint.
- 0 = When the emulator is suspended, the ADC3 continues to run until the conversion is complete.
- 1 = When the emulator is suspended, the ADC3 is frozen so that its state can be examined at the point that the emulator was suspended. The conversion data is indeterminate upon restart.
- BIT 6** **AD PRIORITY (ADC3 interrupt priority select)**
- This bit selects the priority level of the ADC3 interrupt.
- 0 = ADC3 Interrupt is a higher priority (level 1) request.
- 1 = ADC3 Interrupt is a lower priority (level 2) request.
- BIT 7** **AD STEST (This bit must be cleared to ensure proper operation)**

instruction set overview

Table 21 provides an opcode-to-instruction cross-reference of all 73 instructions and 274 opcodes of the '370Cx9x instruction set. The numbers at the top of this table represent the most significant nibble (MSN) of the opcode while the numbers at the left side of the table represent the least significant nibble (LSN). The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

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Table 21. TMS370 Family Opcode/Instruction Map†

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L	0	JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8			CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
	1	JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7
	2	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7
	3	JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8
	4	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes
	5	JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14	
	6	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6
	7	JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10
	8	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7
	9	JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9
B	A	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12
	B	JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8

† All conditional jumps (opcodes 01 – 0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

Table 21. TMS370 Family Opcode/Instruction Map[†] (Continued)

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L S N	C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
	D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
	E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
	F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):

F4	8	MOVW *n[Rn] 4/15	DIV Rn,A 3/14-63
F4	9	JMPL *n[Rn] 4/16	
F4	A	MOV *n[Rn],A 4/17	
F4	B	MOV A,*n[Rn] 4/16	
F4	C	BR *n[Rn] 4/16	
F4	D	CMP *n[Rn],A 4/18	
F4	E	CALL *n[Rn] 4/20	
F4	F	CALLR *n[Rn] 4/22	

Legend:

- * = Indirect addressing operand prefix
- & = Direct addressing operand prefix
- # = immediate operand
- #16 = immediate 16-bit number
- lab = 16-label
- n = immediate 8-bit number
- Pd = Peripheral register containing destination type
- Pn = Peripheral register
- Ps = Peripheral register containing source byte
- ra = Relative address
- Rd = Register containing destination type
- Rn = Register file
- Rp = Register pair
- Rpd = Destination register pair
- Rps = Source Register pair
- Rs = Register containing source byte

[†] All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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development system support

The TMS370 family development support tools include an assembler, a C compiler, a linker, an in-circuit emulator (XDS22), CDT, and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850-02 for PC)
 - Includes extensive macro capability
 - Provides high-speed operation
 - Provides format conversion utilities for popular formats
- ANSI C compiler (Part No. TMDS3740855-02 for PC, Part No. TMDS3740555-09 for HP700™, Sun-3™, or Sun-4™)
 - Generates assembly code for the TMS370 that can be easily inspected
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables direct referencing of the TMS370's port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (compact development tool) PACT real-time in-circuit emulation
 - Base (Part Number EDSCDT37P – for PC, requires cable)
 - Cable for 40-pin SDIP (Part No. EDSTRG40SDIL05)
 - Cable for 44-pin PLCC (Part No. EDSTRG44PLCC05)
 - Includes EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Uploads/downloads program and data memory
 - Executes programs and software routines
 - Includes 1 024-sample trace buffer
 - Includes single-step executable instructions
 - Uses software breakpoints to halt program execution at selected address
- Microcontroller programmer
 - Base (Part No. TMDS3760500A — for PC, requires programmer head)
 - Single unit head for 44-pin PLCC and 40-pin SDIP (Part No. TMDS3780513A)
 - Includes PC-based, window/function-key oriented user interface for ease of use and rapid learning environment

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device numbering conventions

Figure 13 illustrates the numbering and symbol nomenclature for the TMS370Cx9x family.

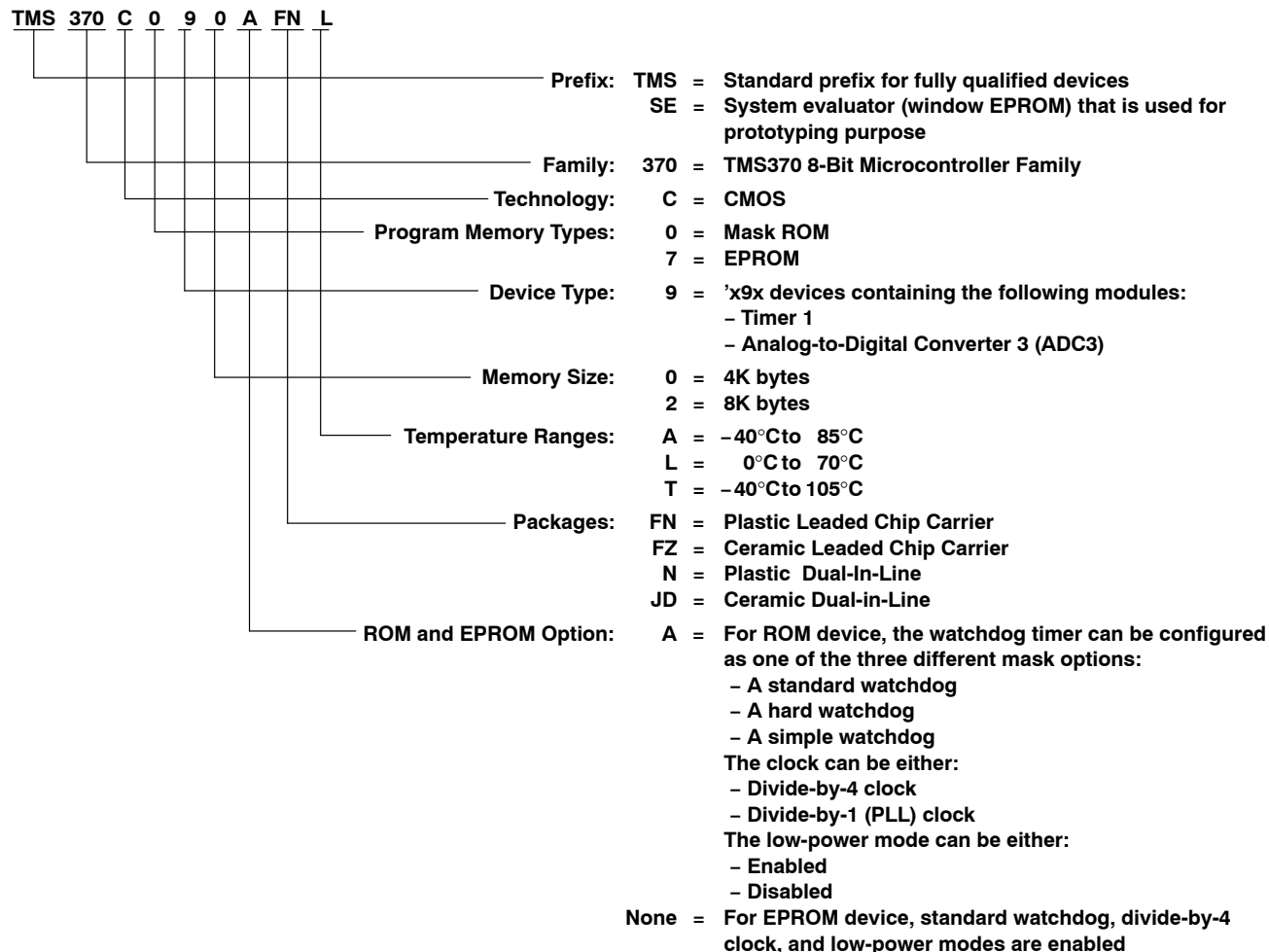


Figure 13. TMS370Cx9x Family Nomenclature

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device part numbers

Table 22 provides all the TMS370Cx9x devices available. The device part-number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog-timer options desired. Each device can only have one of the three possible watchdog-timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 22. Device Part Numbers

DEVICE PART NUMBERS FOR 44 PINS (LCC)	DEVICE PART NUMBERS FOR 40 PINS (SDIP)
TMS370C090AFNA TMS370C090AFNL TMS370C090AFNT	TMS370C090ANJA [†] TMS370C090ANJL [‡] TMS370C090ANJT [‡]
TMS370C792FNT	TMS370C792NJT [‡]
SE370C792FZT [†]	SE370C792JCT [†]

[†] System evaluators are for use only in prototype environment, and their reliability has not been characterized.

[‡] The NJ designator for the 40-pin plastic shrink DIP package was formerly known as N2. The mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

Figure 14 shows a sample of the new code release form.

Figure 14. Sample New Code Release Form

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Table 23. Peripheral File Frame Compilation

Table 23 is a collection of all the peripheral file frames using the 'Cx9x (provided for a quick reference).

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTOWAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018 to P019	Reserved								
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D to P01F	Reserved								
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 [†] (must be 0)					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR
	Modes: Capture/Compare and Dual-Compare								
P040	Bit 15	T1 Counter MSbyte						Bit 8	T1CNTR
P041	Bit 7	T1 Counter LSbyte						Bit 0	
P042	Bit 15	Compare Register MSbyte						Bit 8	T1C
P043	Bit 7	Compare Register LSbyte						Bit 0	
P044	Bit 15	Capture/Compare Register MSbyte						Bit 8	T1CC
P045	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P046	Bit 15	Watchdog Counter MSbyte						Bit 8	WDCNTR
P047	Bit 7	Watchdog Counter LSbyte						Bit 0	
P048	Bit 7	Watchdog Reset Key						Bit 0	WDRST

† To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 23. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Capture/Compare and Dual-Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI
P070	CONVERT START	SAMPLE START	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT3	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SE- LECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A-to-D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	AD RATE SELECT1	AD RATE SELECT0	ADPRI

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to the simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range V_{CC} (see Note 1)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC}) [‡]	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	– 170 mA
Continuous power dissipation	1 W
Operating free-air temperature range, T_A : L version	0°C to 70°C
A version	– 40°C to 85°C
T version	– 40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

NOTE 1: Unless otherwise noted, all voltage values are with respect to V_{SS} .

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)	3		5.5	
V_{CC3}	Analog supply voltage (see Note 1)	3		5.5	V
V_{SS3}	Analog supply ground	– 0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC		0.8	V
		MC, normal operation		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET		V_{CC}	V
		XTAL2/CLKIN		$0.8 V_{CC}$	
		RESET		$0.7 V_{CC}$	
V_{MC}	MC (mode control) voltage	EEPROM write protect override (WPO)		13	V
		EPROM programming voltage (V_{PP})		13.5	
		Microcomputer		0.3	
T_A	Operating free-air temperature	L version		70	°C
		A version		85	
		T version		105	

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS} .

2. RESET must be externally activated when V_{CC} or SYSCLK is out of the recommended operating range.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

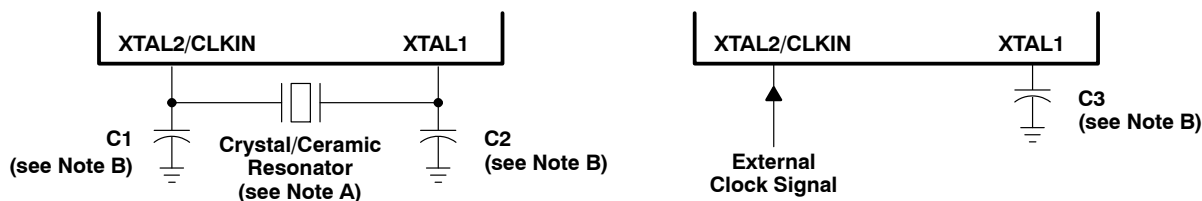
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{OL}	Low-level output voltage		I _{OL} = 1.4 mA		0.4			V
V _{OH}	High-level output voltage		I _{OH} = −50 μA		0.9 V _{CC}			V
			I _{OH} = −2 mA		2.4			
I _I	Input current	MC	0 V < V _I ≤ 0.3 V		10			μA
			0.3 V < V _I ≤ 13 V		650			
			12 V ≤ V _I ≤ 13 V		See Note 3		50	
	I/O pins	0 V ≤ V _I ≤ V _{CC}		± 10			μA	
I _{OL}	Low-level output current		V _{OL} = 0.4 V		1.4			mA
I _{OH}	High-level output current		V _{OH} = 0.9 V _{CC}		− 50			μA
			V _{OH} = 2.4 V		− 2			mA
I _{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 6)		SYSCLK = 5 MHz	See Notes 4 and 5	30		45	mA
			SYSCLK = 3 MHz	See Notes 4 and 5	20		30	
			SYSCLK = 0.5 MHz	See Notes 4 and 5	7		11	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 7)		SYSCLK = 5 MHz	See Notes 4 and 5	10		17	mA
			SYSCLK = 3 MHz	See Notes 4 and 5	8		11	
			SYSCLK = 0.5 MHz	See Notes 4 and 5	2		3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 8)		SYSCLK = 3 MHz	See Notes 4 and 5	6		8.6	mA
			SYSCLK = 0.5 MHz	See Notes 4 and 5	2		3	
Supply current (HALT mode)		XTAL2/CLKIN < 0.2 V	See Note 4	2		30	μA	

- NOTES: 3. Input current I_{PP} is a maximum of 50 mA only when programming EPROM.
4. In single chip mode, ports are configured as inputs or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} – 0.2V.
5. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLOCK, this extra current = 0.01 mA x (total load capacitance + crystal capacitance in pF).
6. Maximum operating current for TMS370Cx9x = 7.6 (SYSCLOCK) + 7 mA.
7. Maximum standby current for TMS370Cx9x = 3 (SYSCLOCK) + 2 mA. (OSC POWER bit = 0).
8. Maximum standby current for TMS370Cx9x = 2.24 (SYSCLOCK) + 1.9 mA. (OSC POWER bit = 1, only valid up to 3-MHz SYSCLOCK).

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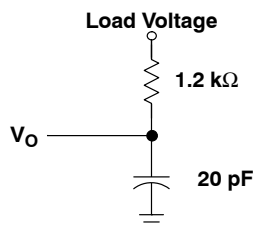
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PARAMETER MEASUREMENT INFORMATION



NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
B. The values of C1 and C2 are typically 15 pF and C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 15. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4 \text{ V}$; Load Voltage = 0 V
Case 2: $V_O = V_{OL} = 0.4 \text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 16. Typical Output Load Circuit (see Note A)

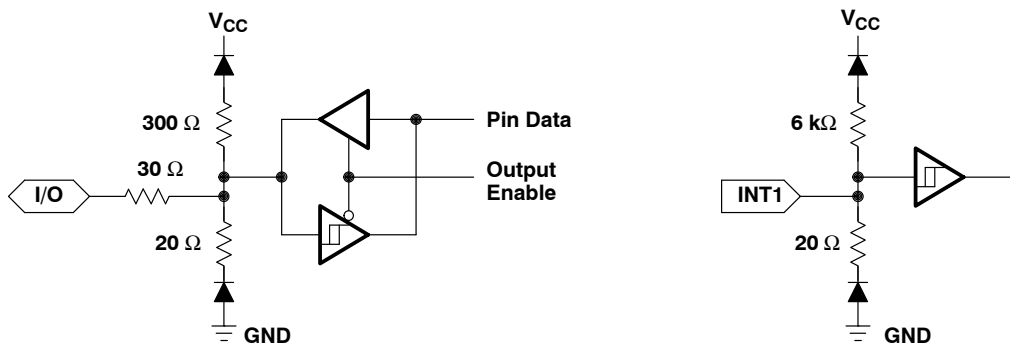


Figure 17. Typical Buffer Circuitry

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

A	Address	IE	Initial
AR	Array	PGM	Program
B	Byte	R	Read
CI	XTAL2/CLKIN	SC	SYSCLK
D	Data	W	Write
E	$\overline{EDS}$	WT	$\overline{WAIT}$
FE	Final		

Lowercase subscripts and their meanings are:

c	cycle time (period)	r	rise time
d	delay time	su	setup time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid
Z	High impedance

All timings are measured between high and low measurement points as indicated in Figure 18 and Figure 19.

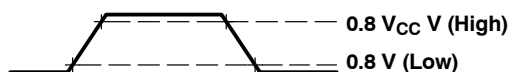


Figure 18. XTAL2/CLKIN Measurement Points

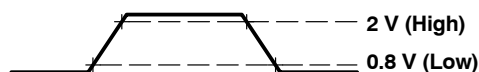


Figure 19. General Measurement Points

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external clocking requirements for clock divided by 4[†] (see Figure 20)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CK)}$ Pulse duration, XTAL2/CLKIN (see Note 9)	20		ns
2	$t_{r(CK)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CK)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN Crystal operating frequency	2	20	MHz
	SYSCLK System clock [‡]	0.5	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions.

[‡] SYSCLK = CLKIN/4

NOTE 9: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

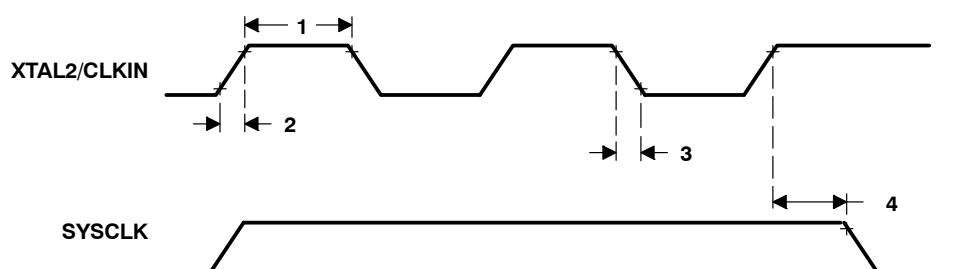


Figure 20. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL)[†] (see Figure 21)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CK)}$ Pulse duration, XTAL2/CLKIN (see Note 9)	20		ns
2	$t_{r(CK)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CK)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN Crystal operating frequency	2	5	MHz
	SYSCLK System clock [§]	2	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions.

[§] SYSCLK = CLKIN/1

NOTE 9: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

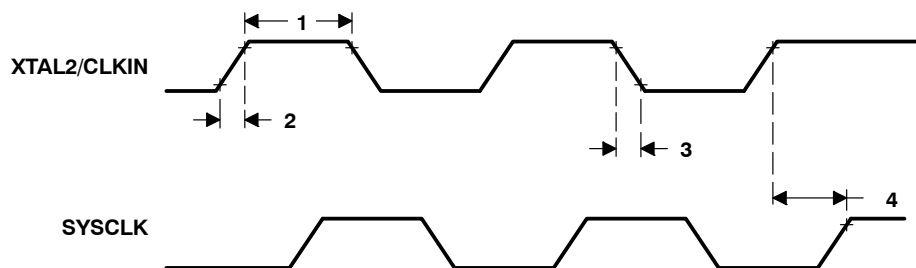


Figure 21. External Clock Timing for Divide-by-1

switching characteristics and timing requirements[†]

NO.	PARAMETER		MIN	MAX	UNIT
5	t_c	Cycle time, SYSCLK			
		Divide-by-4	200	2 000	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low	$0.5t_c - 20$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high	$0.5t_c$	$0.5t_c + 20$	ns

[†] t_c = system-clock cycle time = 1 / SYSCLK

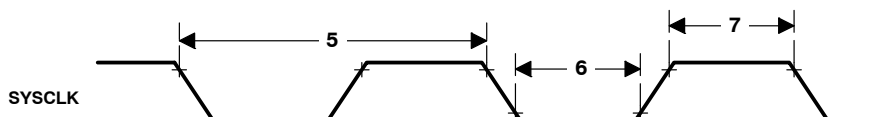


Figure 22. Switching Characteristics

general purpose output signal switching time requirements

	MIN	NOM	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns

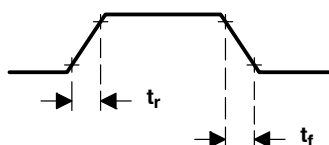


Figure 23. Signal Switching Timing

recommended EEPROM timing requirements for programming

	MIN	MAX	UNIT
$t_{w(PGM)B}$	10		ms
$t_{w(PGM)AR}$	20		ms

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recommended EPROM operating conditions for programming

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.75	5.5	6	V
V _{PP}	Supply voltage at MC pin	13	13.2	13.5	V
I _{PP}	Supply current at MC pin during programming (V _{PP} = 13 V)		30	50	mA
SYSCLK	System clock	Divide-by-4	0.5	5	MHz
		Divide-by-1	2	5	

recommended EPROM timing requirements for programming

		MIN	NOM	MAX	UNIT
t _w (EPGM)	Pulse duration, programming signal (see Note 10)	0.40	0.50	3	ms

NOTE 10: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.



analog-to-digital converter 3

The ADC3 has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3} . The purpose is to enhance ADC3 performance by preventing digital switching noise of the logic circuitry that can be present on V_{SS} and V_{CC} from coupling into the ADC3 analog stage. All ADC3 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution 8-bits (256 values)
 Monotonic Yes
 Output conversion mode 00h to FFh (00 for $V_I \leq V_{SS3}$; FF for $V_I \leq V_{ref}$)
 Conversion time (excluding sample time) $164 t_c$

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC3} Analog supply voltage	4.5	5	5.5	V
	$V_{CC3}-0.3$		$V_{CC3}+0.3$	
V_{SS3} Analog ground	$V_{SS3}-0.3$		$V_{SS3}+0.3$	V
V_{ref} Non- V_{CC3} reference [†]	2.5	V_{CC3}	$V_{CC3} + 0.1$	V
Analog input for conversion	V_{SS3}		V_{ref}	V

[†] V_{ref} must be stable, within $\pm 1/2$ LSB of the required resolution, during the entire conversion time.

operating characteristics over recommended ranges operating conditions

PARAMETER		MIN	MAX	UNIT
Absolute accuracy [†]	$V_{CC3} = 5.5 \text{ V}$ $V_{ref} = 5.1 \text{ V}$	± 1.5		LSB
Differential/integral linearity error ^{†‡}	$V_{CC3} = 5.5 \text{ V}$ $V_{ref} = 5.1 \text{ V}$	± 0.9		LSB
I_{CC3} Analog supply current	Converting	2		mA
	Nonconverting	5		μA
I_I Input current, AN0 – AN14	$0 \text{ V} \leq V_I \leq 5.5 \text{ V}$	2		μA
I_{ref} Input charge current		1		mA
Z_{ref} Source impedance of V_{ref}	$\text{SYSCLK} \leq 3 \text{ MHz}$	24		$\text{k}\Omega$
	$3 \text{ MHz} < \text{SYSCLK} \leq 5 \text{ MHz}$	10		$\text{k}\Omega$

[†] Absolute resolution = 20 mV. At $V_{ref} = 5 \text{ V}$, this is one LSB. As V_{ref} decreases, LSB size decreases; therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

[‡] Excluding quantization error of $1/2$ LSB

analog-to-digital converter 3 (continued)

The ADC3 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined so that the high-impedance sources can be accommodated without penalty to the low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC3 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter will reset the SAMPLE START and CONVERT START bits, signaling that a conversion has started and that the analog signal can be removed.

analog timing requirements†

		MIN	MAX	UNIT
$t_{su(S)}$	Setup time, analog to sample command	0		ns
$t_{h(AN)}$	Hold time, analog input from start of conversion†	$(N+2) t_c$		ns
$t_{w(C)}$	Conversion time†	$(10N + 4) t_c$		ns
$t_{w(S)}$	Pulse duration, sample time per kilohm of source impedance‡	1		$\mu s/k\Omega$

† N = 16, 8, 4, or 2 upon selected conversion rate.

‡ The value given is valid for a signal with a source impedance > 1 k Ω . If the source impedance is < 1 k Ω , use a minimum sampling time of 1 μs .

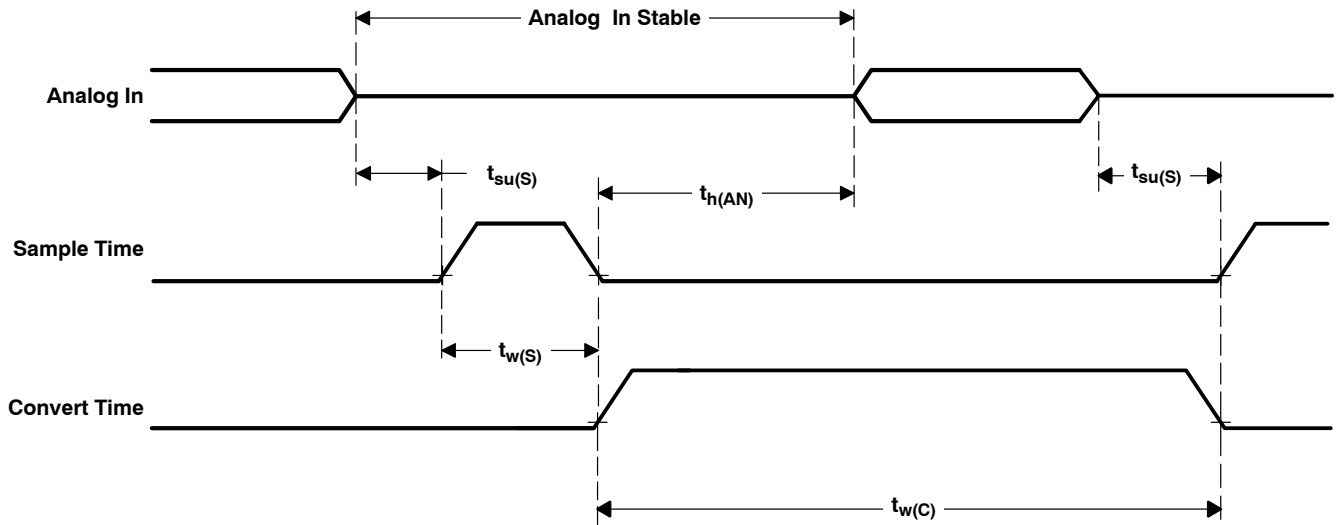


Figure 24. Analog Timing

Table 24 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

Table 24. TMS370Cx9x Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 44 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C090AFNA TMS370C090AFNL TMS370C090AFNT TMS370C792FNT
FZ – 44 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C792FZT
JC – 40 pin (70-mil pin spacing)	CERAMIC SHRINK DUAL-IN-LINE PACKAGE (CSDIP)	JC(R-CDIP-T40) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE	SE370C792JCT
NJ – 40 pin (70-mil pin spacing) [†]	PLASTIC SHRINK DUAL-IN-LINE PACKAGE (PSDIP)	NJ(R-PDIP-T**) PLASTIC SHRINK DUAL-IN-LINE PACKAGE	TMS370C090ANJA TMS370C090ANJL TMS370C090ANJT TMS370C792NJT

[†] NJ formerly known as N2; the mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

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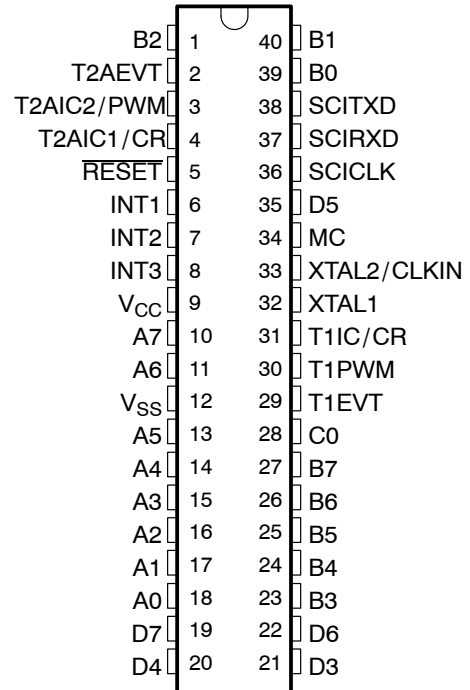
General Information	1
Selection Guide/Tools	2
Ops Cond/Timing/Glossary	3
TMS370Cx0x Data Sheet	4
TMS370Cx1x Data Sheet	5
TMS370Cx2x Data Sheet	6
TMS370Cx32 Data Sheet	7
TMS370Cx36 Data Sheet	8
TMS370Cx4x Data Sheet	9
TMS370Cx5x Data Sheet	10
TMS370Cx6x Data Sheet	11
TMS370Cx7x Data Sheet	12
TMS370Cx8x Data Sheet	13
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Mechanical Data	18
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Electrostatic Discharge Guidelines	20

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- **CMOS/EEPROM/EPROM Technologies on a Single Device**
 - Mask-ROM Devices for High-Volume Production
 - EPROM Devices for Prototyping Purposes (TMS370C758 and SE370C758)
- **Internal System Memory Configurations**
 - On-Chip ROM: 24K Bytes
 - Static RAM: 512 Bytes
- **Flexible Operating Features**
 - Low-Power Modes: STANDBY and HALT
 - Commercial, Industrial, and Automotive Temperature Ranges
 - Clock Options
 - Divide-by-4 (0.5 to 5 MHz SYSCLK)
 - Divide-by-1 (2 to 5 MHz SYSCLK) PLL
 - Supply Voltage (V_{CC}) 5 V $\pm$ 10%
- **Two 16-Bit General-Purpose Timers**
 - Software Configurable as Two 16-Bit Event Counters, or Two 16-Bit Pulse Accumulators, or Three 16-Bit Input Capture Functions, or Four Compare Registers, or Two Self-Contained Pulse-Width-Modulation (PWM) Functions
- **On-Chip 24-Bit Watchdog Timer**
 - Mask-ROM Devices: Hard Watchdog, Simple Counter, or Standard Watchdog
- **Flexible Interrupt Handling**
 - Two S/W Programmable Interrupt Levels
 - Global-and Individual-Interrupt Masking
 - Programmable Rising or Falling Edge Detect
 - Individual Interrupt Vectors
- **Serial Communications Interface 1 (SCI1)**
 - Asynchronous Mode: 156 Kbps Maximum at 5 MHz SYSCLK
 - Isosynchronous[†] Mode: 25 Mbps Maximum at 5 MHz SYSCLK
 - Full Duplex, Double-Buffered Receiver (RX) and Transmitter (TX)
 - Two Multiprocessor Communication Formats

**N PACKAGE
(TOP VIEW)**



- **TMS370 Series Compatibility**
 - Register-to-Register Architecture
 - 256 General-Purpose Registers
 - 14 Powerful Addressing Modes
 - Instructions Upwardly Compatible With All TMS370 Devices
- **CMOS/TTL Compatible I/O Pins/Packages**
 - All Peripheral Function Pins Software Configurable for Digital I/O
 - 33 Bidirectional Pins, One Input Pin
 - 40-Pin Plastic Dual-In-Line Packages
- **Workstation/Personal Computer-Based Development System**
 - C Compiler and C Source Debugger
 - Real-time In-Circuit Emulation
 - Extensive Breakpoint/Trace Capability
 - Multi-Window User Interface
 - Microcontroller Programmer



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[†] Isosynchronous = Isochronous

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TMS370CxAx

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Pin Descriptions

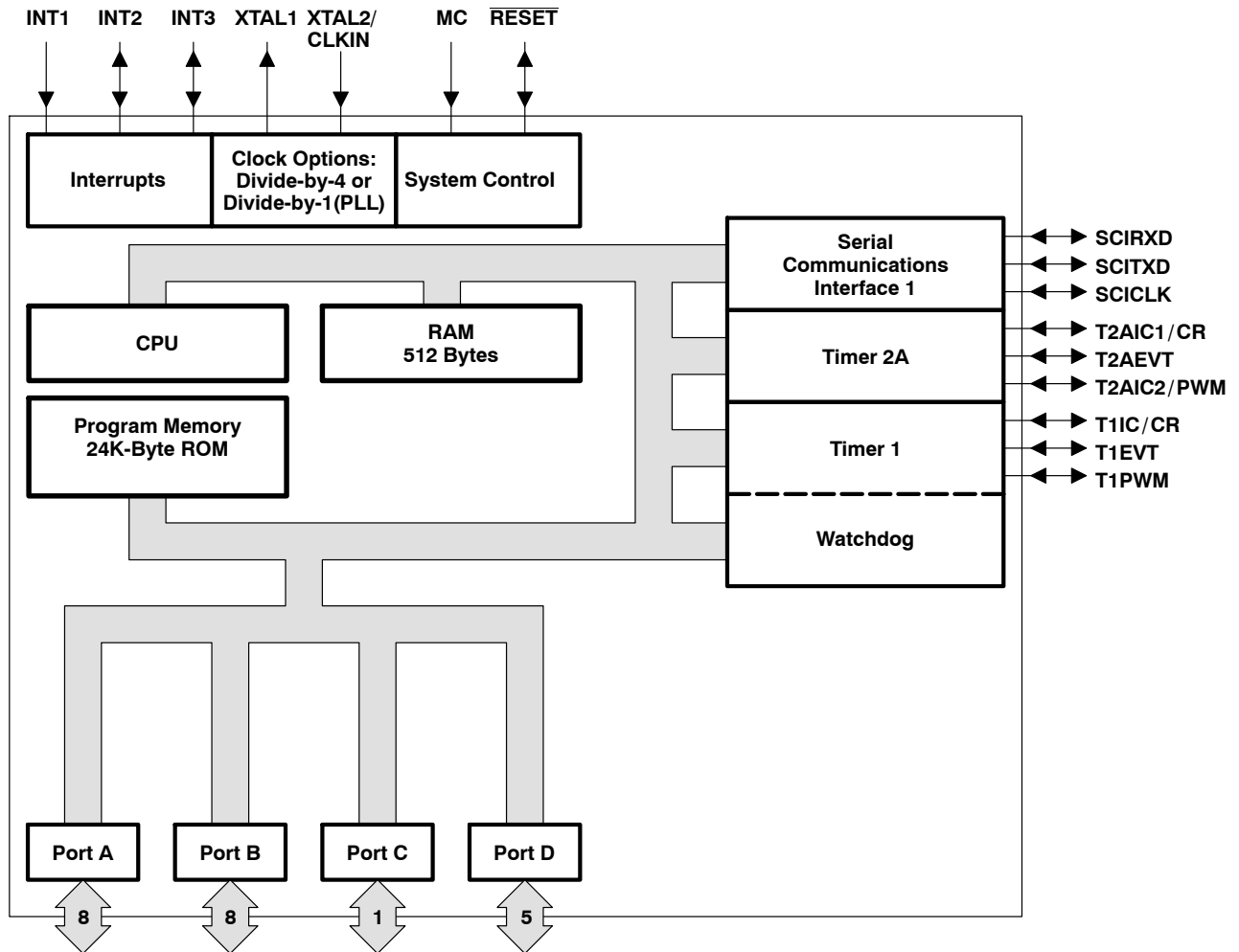
40 PINS PDIP		TYPE†	DESCRIPTION
NAME	NO.		
A0 A1 A2 A3 A4 A5 A6 A7	18 17 16 15 14 13 11 10	I / O	Port A is a general-purpose bidirectional I/O port.
B0 B1 B2 B3 B4 B5 B6 B7	39 40 1 23 24 25 26 27	I / O	Port B is a general-purpose bidirectional I/O port.
C0	28	I / O	Port C is a general-purpose bidirectional I/O port.
D3 D4 D5 D6 D7	21 20 35 22 19	I / O	Port D is a general-purpose bidirectional I/O port. D3 is also configurable as SYSCLK.
INT1 INT2 INT3	6 7 8	I I / O I / O	External interrupt (non-maskable or maskable)/general-purpose input pin. External maskable interrupt input/general-purpose bidirectional pin. External maskable interrupt input/general-purpose bidirectional pin.
T1IC/CR T1PWM T1EVT	31 30 29	I / O	Timer1 input capture/counter reset input pin/general-purpose bidirectional pin. Timer1 PWM output pin/general-purpose bidirectional pin. Timer1 external event input pin/general-purpose bidirectional pin.
SCITXD SCIRXD SCICLK	38 37 36	I / O	SCI transmit data output pin, general-purpose bidirectional pin (see Note 1). SCI receive data input pin/general-purpose bidirectional pin. SCI bidirectional serial clock pin/general-purpose bidirectional pin.
RESET	5	I / O	System reset bidirectional pin; as input pin, $\overline{\text{RESET}}$ initializes the microcontroller; as open-drain output, $\overline{\text{RESET}}$ indicates that an internal failure was detected by watchdog or oscillator fault circuit.
T2AIC1/CR T2AIC2/PWM T2AEVT	4 3 2	I / O	Timer2A input capture 1/counter reset input pin/general-purpose bidirectional pin. Timer2A input capture 2/PWM output pin/general-purpose bidirectional pin. Timer2A external event input pin/general-purpose bidirectional pin.
MC	34	I	Mode control input pin; enables EEPROM write protection override (WPO) mode, also EPROM V_{PP} .
XTAL2/CLKIN XTAL1	33 32	I O	Internal oscillator crystal input/External clock source input. Internal oscillator output for crystal.
V _{CC}	9		Positive supply voltage
V _{SS}	12		Ground reference

† I = input, O = output

NOTE 1: The three SCI configuration pins are referred to as SCI1.



functional block diagram



description

The TMS370C3A7 device is a member of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370CxAx refers to this device. The TMS370 family provides cost-effective, real-time system control through integration of advanced peripheral function modules and various on-chip memory configurations.

The TMS370CxAx family of devices is implemented using high-performance silicon-gate CMOS technologies. Low-operating power, wide-operating temperature range, and noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370CxAx device attractive in system designs for automotive electronics, industrial motors, computer peripheral controls, telecommunications, and consumer applications.

All TMS370C3A7A device contains the following on-chip peripheral modules:

- Serial communications interface 1 (SCI1)
- Two 16-bit general-purpose timers (one with an 8-bit prescaler)
- One 24-bit general-purpose watchdog timer

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description (continued)

Table 1 provides a memory configuration overview of the TMS370CxAx device. Also shown in Table 1, the one-time programmable (OTP) (TMS370C758) and the reprogrammable (SE370C758) devices are the two development devices recommended for the TMS370CxAx family.

Table 1. Memory Configurations

DEVICES	PROGRAM MEMORY (BYTES)		OFF-CHIP MEMORY EXP. (BYTES)	DATA MEMORY (BYTES)		40 PIN PDIP or 68 PIN PLCC/CLCC, OR 64 PIN PSDIP/CSDIP
	ROM	EPROM		RAM	EEPROM	
TMS370CxAx						
TMS370C3A7A	24K	—	—	512	—	N – PDIP
TMS370C758						
TMS370C758A	—	32K	64K	1K	256	FN – PLCC/NM – PSDIP
TMS370C758B						
SE370C758A, [†] SE370C758B [†]	—	32K	64K	1K	256	FZ – CLCC/JN – CSDIP

[†] System evaluators and development are for use only in prototype environment, and their reliability has not been characterized.

The suffix letters (A or B) appended to the device name (shown in the first column of Table 1) indicates the configuration of the device. ROM and EPROM devices have different configurations as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 2. Suffix Letter Configuration

DEVICE [‡]	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM A	Standard	Divide-by-4 (Standard oscillator)	Enabled
EPROM B	Hard	Divide-by-1 (PLL)	Enabled
ROM A	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

[‡] Refer to the “device numbering conventions” section for device nomenclature and the “device part numbers” section for ordering.

The 24K bytes of mask-programmable ROM in the TMS370C3A7A device rely on the 68-pin TMS370C758 development devices and an OTP converter socket for (part number TMDX37788OTP) prototyping and programming purposes.

The OTP device (TMS370C758) and the reprogrammable device (SE370C758) offer 32K bytes of EPROM, 256 bytes of EEPROM, off-chip memory expansion, 512 bytes of additional RAM, and two additional on-chip peripheral modules (analog-to-digital converter and serial peripheral interface).

Refer to the TMS370Cx5x data sheet (literature number SPNS010C) or the TMS370 Family User's Guide (literature number SPNU127) for detailed information because the address and the control register manipulations to these associated pins/ports are different between the 'xAx and 'x5x devices.

The SE370C758 has a windowed ceramic package to allow reprogramming of the program EPROM memory during the development-prototyping phase of design. The SE370C758 device allows quick updates to breadboards and prototype systems while iterating initial designs. The TMS370C758 OTP device is available in plastic packages.



description (continued)

The TMS370CxAx family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all CPU activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370CxAx features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370CxAx family is fully instruction-set-compatible, providing easy transition between members of the TMS370 8-bit microcontroller family.

The TMS370CxAx family provides the system designer with an economical, efficient solution to real-time control applications. The TMS370 family extended development system (XDS™) and compact development tool (CDT™) solve the challenge of efficiently developing the software and hardware required to design the TMS370CxAx into an ever-increasing number of complex applications. The application source code can be written in assembly and C-language, and the output code can be generated by the linker. The TMS370 family XDS development tool communicates through a standard RS-232-C interface with an existing personal computer. This allows the use of the personal computer editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes ease-of-use through extensive menus and screen windowing so that a system designer can begin developing software with minimal training. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as a reduced time-to-market cycle.

The TMS370CxAx family together with the TMS370 family XDS22, CDT370, starter kit, software tools, the SE370C758 reprogrammable devices, comprehensive product documentation, and customer support provide a complete solution to the needs of the system designer.

central processing unit (CPU)

The CPU used on the TMS370CxAx device is the high-performance 8-bit TMS370 CPU module. The 'xAx implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'xAx instruction map is shown in NO TAG in the TMS370CxAx instruction set overview section.

The '370CxAx CPU architecture provides the following components:

- CPU registers:
 - A stack pointer that points to the last entry in the memory stack
 - A status register that monitors the operation of the instructions and contains the global interrupt enable bit.
 - A program counter (PC) that points to the memory location of the next instruction to be executed
- A memory map that includes:
 - 512-byte general-purpose RAM that can be used for data memory storage, program instructions, general-purpose register, or the stack (can be located only in the first 256 bytes)
 - A peripheral file that provides access to all internal peripheral modules and system-wide control functions
 - 24K-byte ROM of program memory

XDS and CDT are trademarks of Texas Instruments Incorporated.

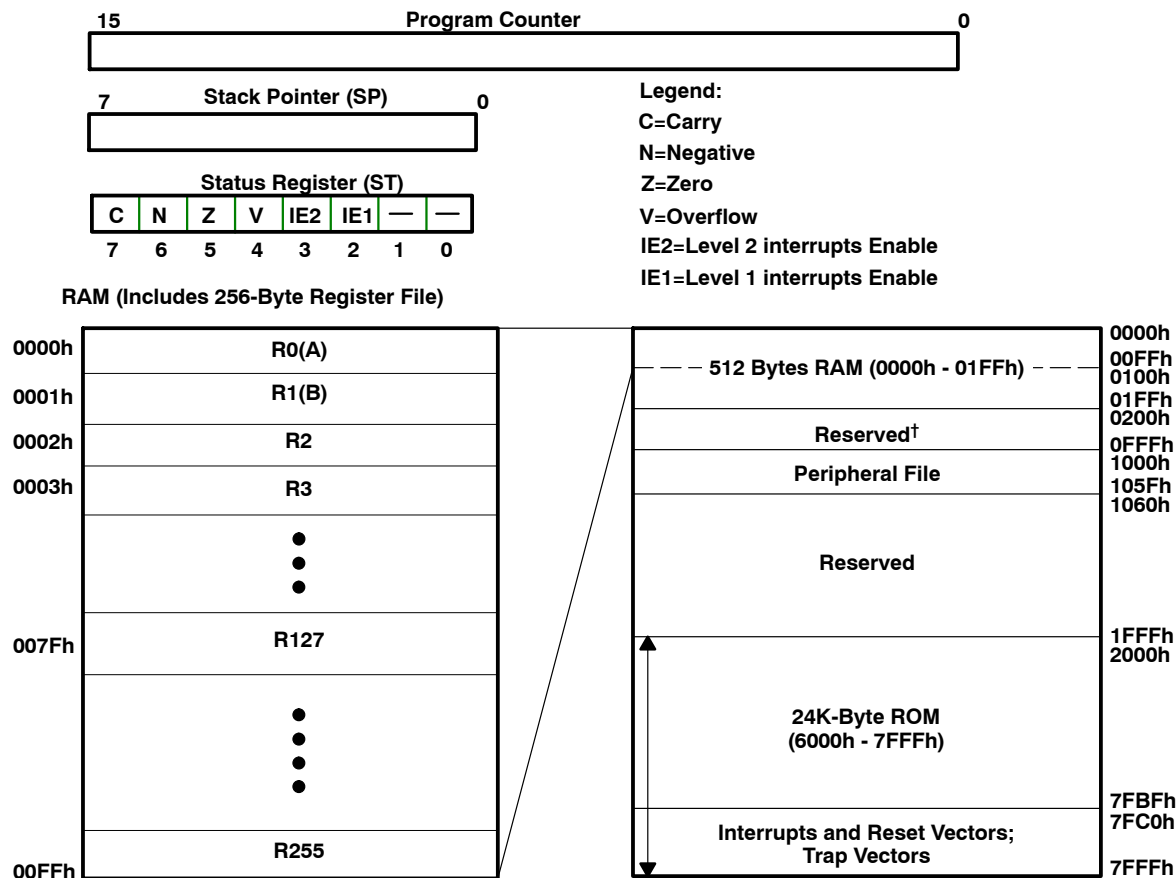


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central processing unit (CPU) (continued)

Figure 1 Illustrates the CPU registers and memory blocks.



[†] Reserved means the address space is reserved for future expansion.

Figure 1. Programmer's Model

stack pointer (SP)

The SP is an 8-bit CPU register. Stack operates as a last-in, first-out, read/write memory. The stack is used typically to store the return address on subroutine calls as well as the status-register contents during interrupt sequences.

The SP points to the last entry or top of the stack. The SP is incremented automatically before data is pushed onto the stack and decremented after data is popped from the stack. The stack can be placed anywhere in the on-chip RAM memory.

status (ST) register

The ST register monitors the operation of the instructions and contains the global interrupt enable bits. The ST register includes four status bits (condition flags) and two interrupt-enable bits:

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional jump instructions) use the status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

central processing unit (CPU) (continued)

The ST register, status-bit notation, and status-bit definitions are shown in Table 3.

Table 3. Status Registers (ST)

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most significant byte and least significant byte of a 16-bit address.

During reset, the contents of the reset vector (7FFEh, 7FFFh) are loaded into the program counter. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 2000h as the contents of the reset vector.

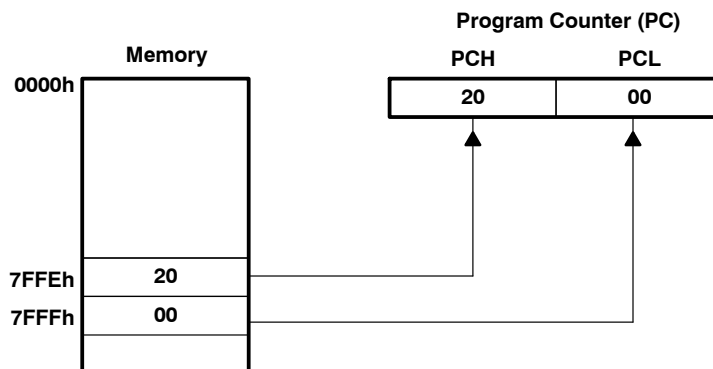


Figure 2. Program Counter After Reset

memory map

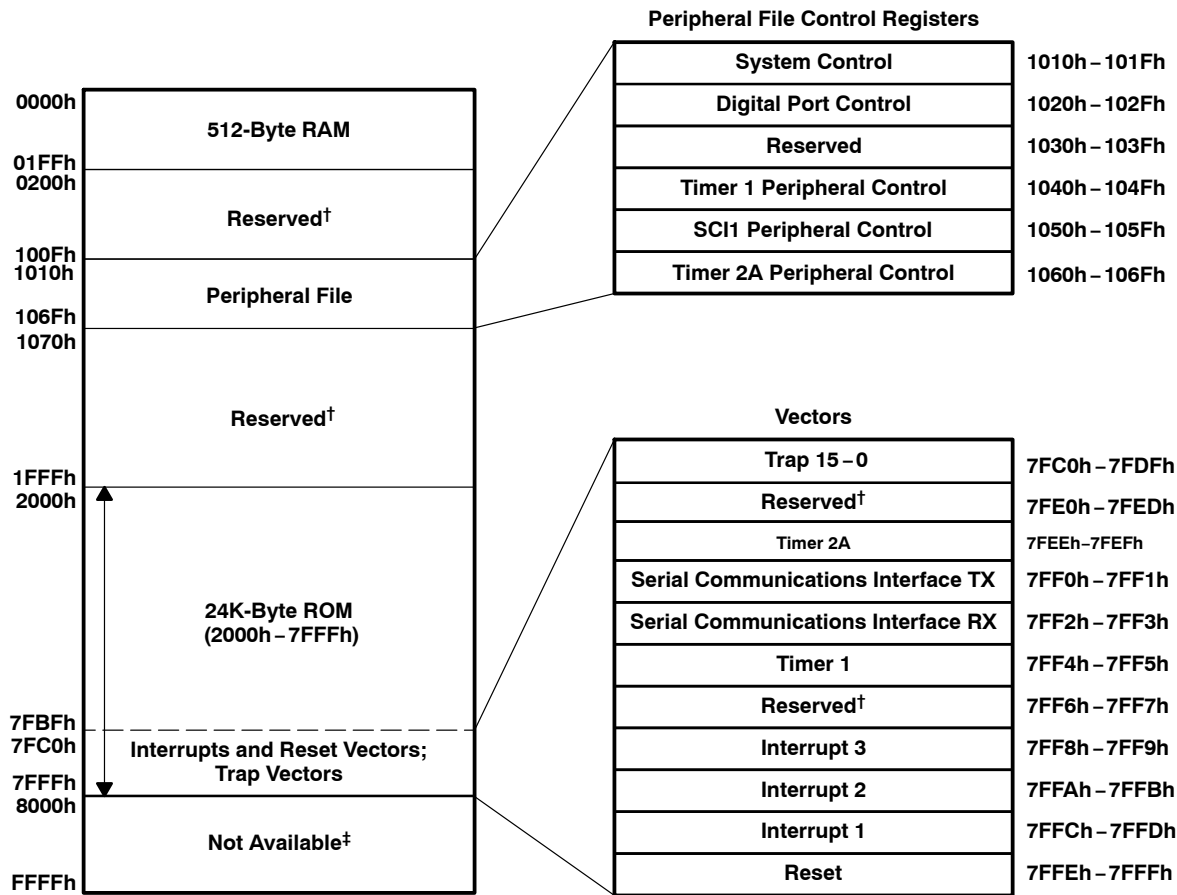
The TMS370C3A7 architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. As shown in Figure 3, the TMS370C3A7 provides memory-mapped RAM, ROM, input/output pins, peripheral functions, and system-interrupt vectors.

The peripheral file contains all input/output port control, peripheral status and control, and system-wide control functions. The peripheral file is located between 1010h to 106Fh and is logically divided into six peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information are passed.

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central processing unit (CPU) (continued)



† Reserved means the address space is reserved for future expansion.

‡ Not available means the address space is not accessible.

Figure 3. TMS370CxAx Memory Map

RAM/register file (RF)

Locations within the RAM address space can serve as the RF, general-purpose read/write memory, program memory, or the stack instructions. The TMS370C3A7 device contains 512 bytes of internal RAM mapped beginning at location 0000h and continuing through location 01FFh which is shown in Figure 1. The first 256 bytes of RAM (0000h–00FFh) are register files, R0 through R255.

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370C3A7 control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or P for a decimal designator. For example, the system control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 4 shows the TMS370C3A7 PF address map.

central processing unit (CPU) (continued)

Table 4. TMS370C3A7 Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h – 100Fh	P000 – P00F	Reserved
1010h – 101Fh	P010 – P01F	System control
1020h – 102Fh	P020 – P02F	Digital I/O port control registers
1030h – 103Fh	P030 – P03F	Reserved
1040h – 104Fh	P040 – P04F	T1 peripheral control
1050h – 105Fh	P050 – P05F	Serial communications interface 1 peripheral control registers
1060h – 106Fh	P060 – P06F	Timer 2A peripheral control registers

program ROM

The program ROM consists of 24K bytes of mask-programmable read-only memory. The program ROM is used for permanent storage of data or instructions. Memory addresses 7FE0h through 7FEBh are reserved for TI, and 7FEEh through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions are located between addresses 7FC0h and 7FDFh. Programming of the mask ROM is performed at the time of device fabrication. Refer to Figure 3 for the ROM memory map.

system reset

The system reset operation ensures an orderly start-up sequence for the TMS370C3A7 CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are internally generated, while one (**RESET** pin) is controlled externally. These actions are as follows:

- External **RESET** pin. A low level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 User's Guide* (literature number SPNU127) for more information.
- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register or if the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 User's Guide* (literature number SPNU127) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside of the recommended operating range. See the *TMS370 User's Guide* (literature number SPNU127) for more information.

Once a reset source is activated, the external **RESET** pin is driven low (active) for a minimum of eight SYSCLK cycles. This allows the '3A7 device to reset external system components. Additionally, if a cold start (V_{CC} is off for several hundred milliseconds) condition or oscillator failure occurs or the **RESET** pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator fault flag (OSC FLT FLAG, SCCR0.4), the cold start flag (COLD START, SCCR0.7) and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 5 lists the reset sources.

Table 5. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

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system reset (continued)

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Registers A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to by the PC.

The reset sequence takes 20 SYSClk cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

When an external reset circuit is connected to the $\overline{\text{RESET}}$ pin, the pin must be held low until the clock signal is valid and V_{CC} is within the operating range. Figure 4 shows a typical reset circuit.

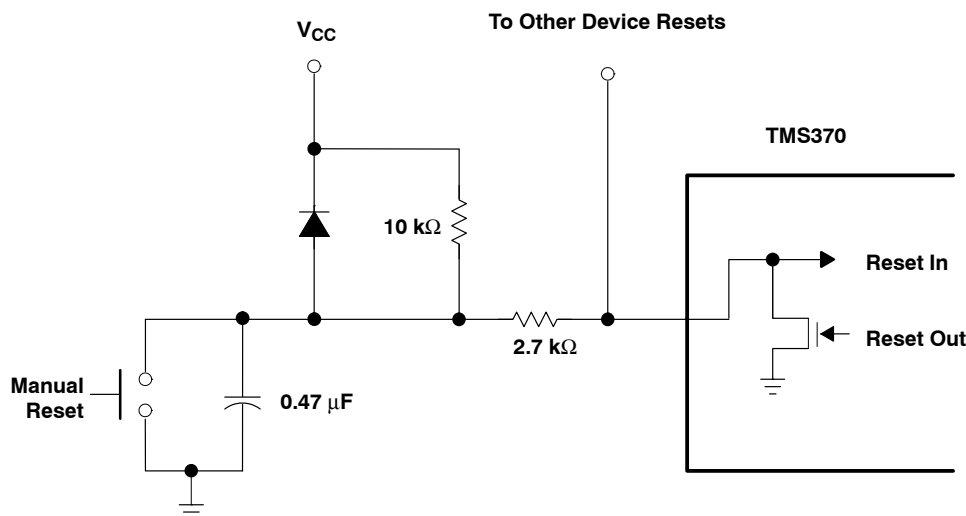


Figure 4. Typical Reset Circuit

interrupts

The TMS370 family software programmable interrupt structure permits flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global-interrupt mask bits (IE1 and IE2) of the status register.

interrupts (continued)

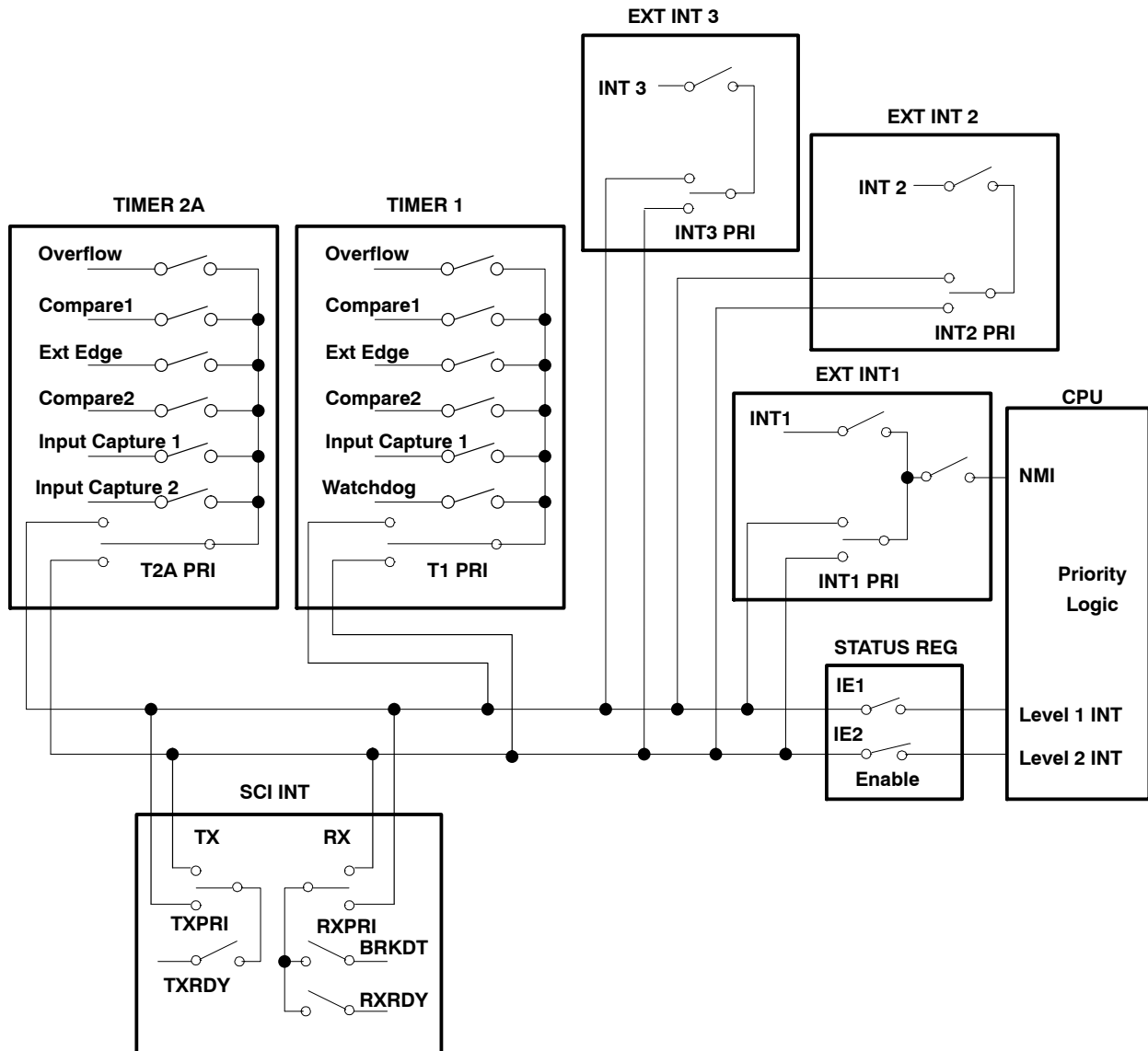


Figure 5. Interrupt Control

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is configured selectively on either the high- or low-priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending-interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370C3A7 has seven hardware system interrupts (plus RESET) as shown in Table 6. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. A system interrupt may have multiple interrupt sources. All of the interrupt sources are

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interrupts (continued)

individually maskable by local interrupt enable control bits in the associated peripheral file. Each interrupt source FLAG bit is individually readable for software polling or for determining which interrupt source generated the associated system interrupt.

Three of the system interrupts are generated by on-chip peripheral functions, and three external interrupts are supported. Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in peripheral file frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt (NMI). When INT1 is configured as NMI, it cannot be masked by the individual or global enable mask bits. The INT1 NMI bit is protected during non-privileged operation and, therefore, should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software-configured as general-purpose input/output pins if the interrupt function is not required (INT1 can be similarly configured as an input pin).

Table 6. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY†
External RESET Watchdog Overflow Oscillator Fault Detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	RESET‡	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1‡	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2‡	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3‡	7FF8h, 7FF9h	4
Timer 1 Overflow Timer 1 Compare 1 Timer 1 Compare 2 Timer 1 External Edge Timer 1 Input Capture 1 Watchdog Overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT§	7FF4h, 7FF5h	5
SCI RX Data Register Full SCI RX Break Detect	RXRDY FLAG BRKDT FLAG	RXINT‡	7FF2h, 7FF3h	6
SCI TX Data Register Empty	TXRDY FLAG	TXINT	7FF0h, 7FF1h	7
Timer 2A Overflow Timer 2A Compare 1 Timer 2A Compare 2 Timer 2A External Edge Timer 2A Input Capture 1 Timer 2A Input Capture 2	T2A OVRFL INT FLAG T2AC1 INT FLAG T2AC2 INT FLAG T2AEDGE INT FLAG T2AIC1 INT FLAG T2AIC2 INT FLAG	T2AINT	7FEEh, 7FEFh	8

† Relative priority within an interrupt level.

‡ Release microcontroller from STANDBY and HALT low-power modes.

§ Release microcontroller from STANDBY low-power mode.

privileged operation

The TMS370C3A7 family has significant flexibility to enable the designer to software configure the system and peripherals to meet the requirements of a variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370C3A7 operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) is set to 1 to enter the



privileged operation (continued)

nonprivileged mode, thus, disabling write operations to specific configuration control bits within the peripheral file. Table 7 displays the system configuration bits which are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

Table 7. Privilege Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCR0	P010.5 P010.6	PF AUTO WAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
SCIPRI	P05F.4 P05F.5 P05F.6 P05F.7	SCI ESPEN SCIRX PRIORITY SCITX PRIORITY SCI STEST
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST
T2APRI	P06F.6 P06F.7	T2A PRIORITY T2A STEST

† The privilege bits are shown in a bold typeface in the peripheral file frame 1 section.

low-power and IDLE modes

The TMS370C3A7 devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time when the mask is manufactured.

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls the low-power mode selection.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity stops; however, the oscillator, internal clocks, T1, and the receive-start bit detection circuit of the serial communications interface 1 remain active. System processing is suspended until a qualified interrupt (hardware RESET, external interrupt on INT1, INT2, INT3, T1 interrupt, or low level on the receive pin of the SCI1) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370C3A7 is placed in its lowest power-consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware RESET, external interrupt on the INT1, INT2, INT3 or low level on the receive pin of the SCI1) is detected. The power-down mode selection bits are summarized in Table 8.

low-power and IDLE modes (continued)

Table 8. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X [†]	IDLE

[†] Don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6-7 bits are ignored. In addition, if an idle instruction executes when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method of always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a NMI during low-power modes when the hard watchdog mode is selected. This means that the NMI is generated always, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing stops during the STANDBY and HALT modes, the clocking of the watchdog timer is inhibited.

clock modules

The TMS370C3A7 provides two clock options that are referred to as divide-by-1 (phase-locked loop) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The '3A7 ROM-masked devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 clock module option provides a one-to-one match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency, whereas the divide-by-4 option produces a SYSCLK which is one-fourth of the frequency of the external resonator. Inside of the divide-by-1 module, the frequency of the external resonator is multiplied by four, and the clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency.

These are formulated as follows:

$$\text{Divide-by-4 : SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 : SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the reduction in EMI. The harmonics of low-speed resonators extend through less of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 option provides the capability of reducing the resonator speed by four times, resulting in a steeper decay of emissions produced by the oscillator.

system configuration registers

Table 9 contains system configuration and control functions. The privileged bits are shown in bold typeface and shaded areas.

Table 9. Peripheral File Frame 1: System Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTO-WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A to P01F	Reserved								

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digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 10 shows the specific addresses, registers, and control bits within this peripheral file frame.

Table 10. Peripheral File Frame 2: Digital Port Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	Port B Control Register 2 (must be 0)								BPORT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPORT1
P029	—	—	—	—	—	—	—	Port C Control Register 2 (must be 0)	CPORT2
P02A	—	—	—	—	—	—	—	Port C Data	CDATA
P02B	—	—	—	—	—	—	—	Port C Direction	CDIR
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0) [†]					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 11. Port Configuration Register Set-up

PORT	PIN	abcd 00q1	abcd 00y0
A	0 – 7	Data Out q	Data In y
B	0 – 7	Data Out q	Data In y
C	0	Data Out q	Data In y
D	3 – 7	Data Out q	Data In y
a = Port x Control Register 1 b = Port x Control Register 2 c = Data d = Direction			

timer 1 module

The programmable timer 1 (T1) module of the TMS370CxAx provides the designer with the enhanced timer resources required to perform real-time system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers, T1 and WD, allow program selection of input clock sources (real-time, external event, or pulse accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The T1 module includes three external device pins that can be used for multiple counter functions (operation mode dependent) or used as general-purpose I/O pins. The T1 module block diagram is shown in Figure 6.

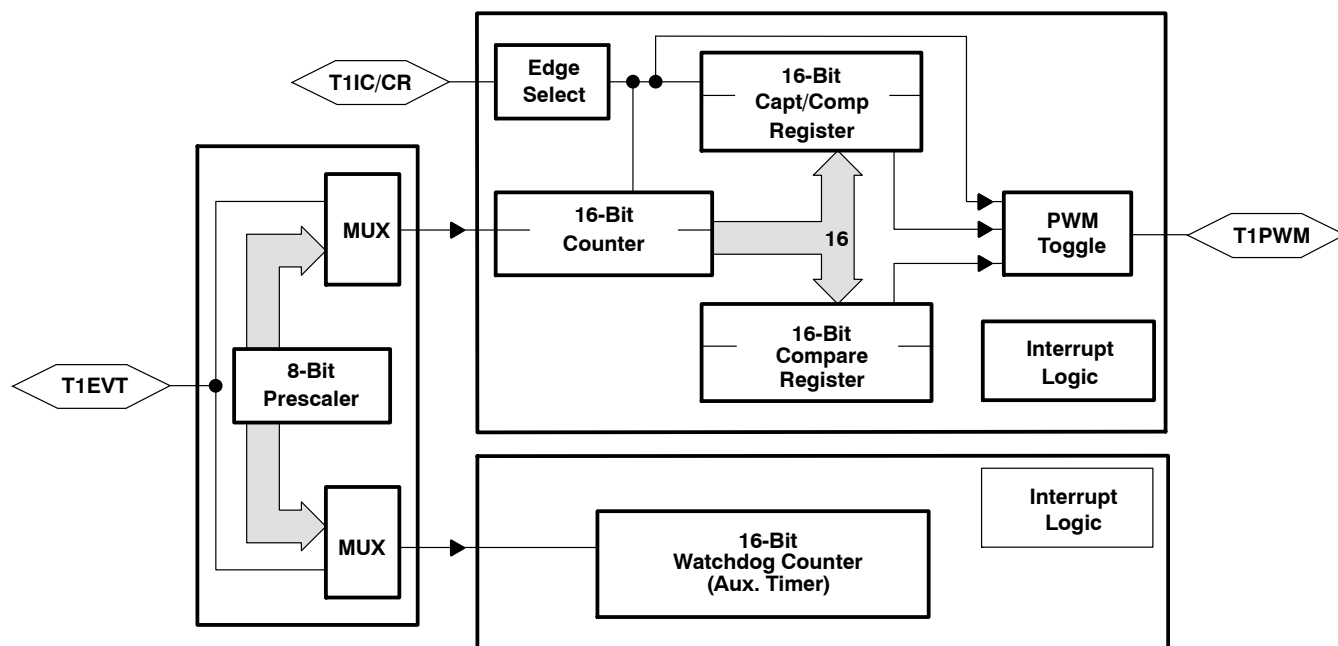


Figure 6. Timer 1 Block Diagram

- Three T1 I/O pins
 - T1IC/CR: T1 input capture / counter reset input pin, or general-purpose bidirectional I/O pin
 - T1PWM: T1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T1EVT: T1 event input pin, or general-purpose bidirectional I/O pin
- Two operation modes:
 - Dual-compare mode: Provides PWM signal
 - Capture/compare mode: Provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register.
- One 16-bit watchdog counter can be used as an event counter, a pulse accumulator, or an interval timer if watchdog feature is not needed.
- Prescaler/clock sources that determine one of eight clock sources for general-purpose timer

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timer 1 module (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR)
- Interrupts that can be generated on the occurrence of:
 - A capture
 - A compare equal
 - A counter overflow
 - An external edge detection
- Sixteen T1 module control registers located in the PF frame beginning at address P040.

The T1 module control registers are illustrated in Table 12.



timer 1 module (continued)

Table 12. Timer 1 Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Mode: Dual Compare and Capture/Compare									
P040	T1 Counter MSbyte							Bit 8	T1CNTR
P041	T1 Counter LSbyte							Bit 0	
P042	Compare Register MSbyte							Bit 8	T1C
P043	Compare Register LSbyte							Bit 0	
P044	Capture/Compare Register MSbyte							Bit 8	T1CC
P045	Capture/Compare Register LSbyte							Bit 0	
P046	Watchdog Counter MSbyte							Bit 8	WDCNTR
P047	Watchdog Counter LSbyte							Bit 0	
P048	Watchdog Reset Key							Bit 0	WDRST
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE=0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Mode: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

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timer 1 module (continued)

Figure 7 shows the T1 capture/compare mode block diagram. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

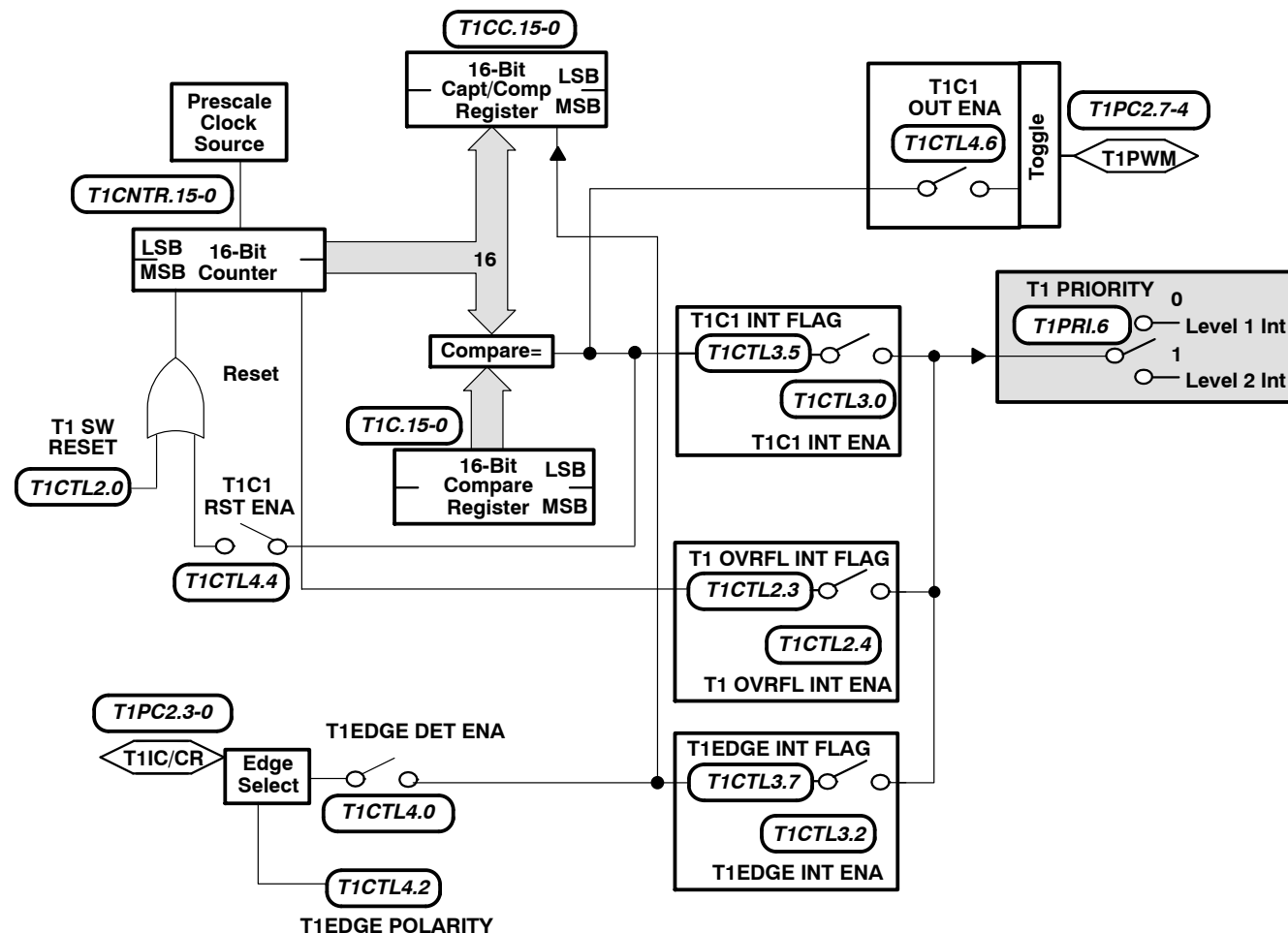


Figure 7. Capture/Compare Mode

timer 1 module (continued)

Figure 8 shows the T1 dual-compare mode block diagram. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

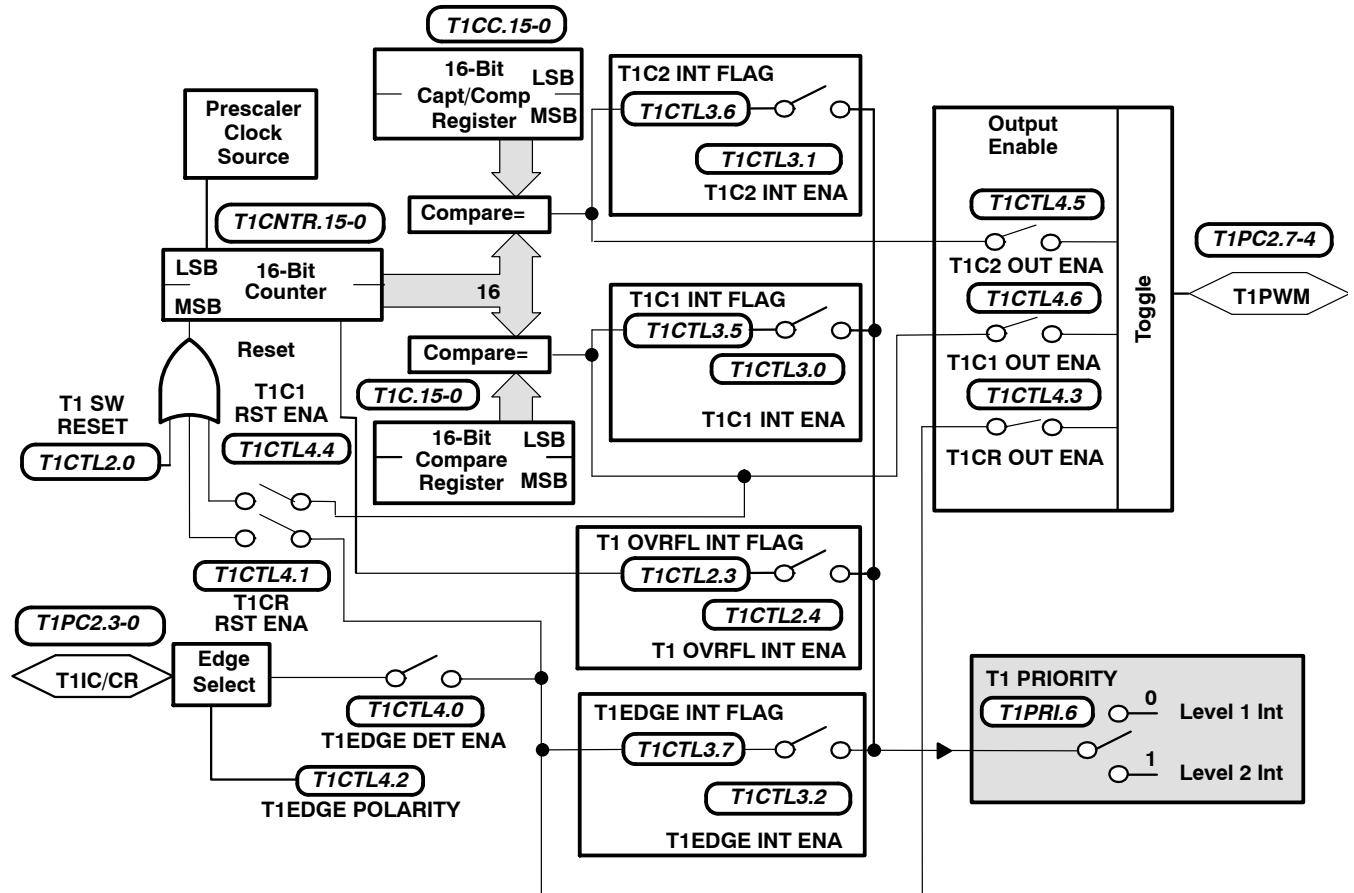


Figure 8. Dual-Compare Mode

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timer 1 module (continued)

The TMS370CxAx device includes a 24-bit WD timer, contained in the T1 module, which can be programmed as an event counter, pulse accumulator, or interval timer if the watchdog function is not used. The WD function is to monitor software and hardware operation, and implements a system reset when the WD counter is not properly serviced (WD counter overflow or WD counter is re-initialized by an incorrect value). The WD can be configured as one of the three mask options as follows:

- Standard watchdog configuration (see Figure 9) for mask-ROM devices:
 - Watchdog mode
 - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5 MHz SYSCCLK.
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows.
 - A watchdog overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset.
 - Non-watchdog mode
 - Watchdog timer can be configured as an event counter, pulse accumulator or an interval timer

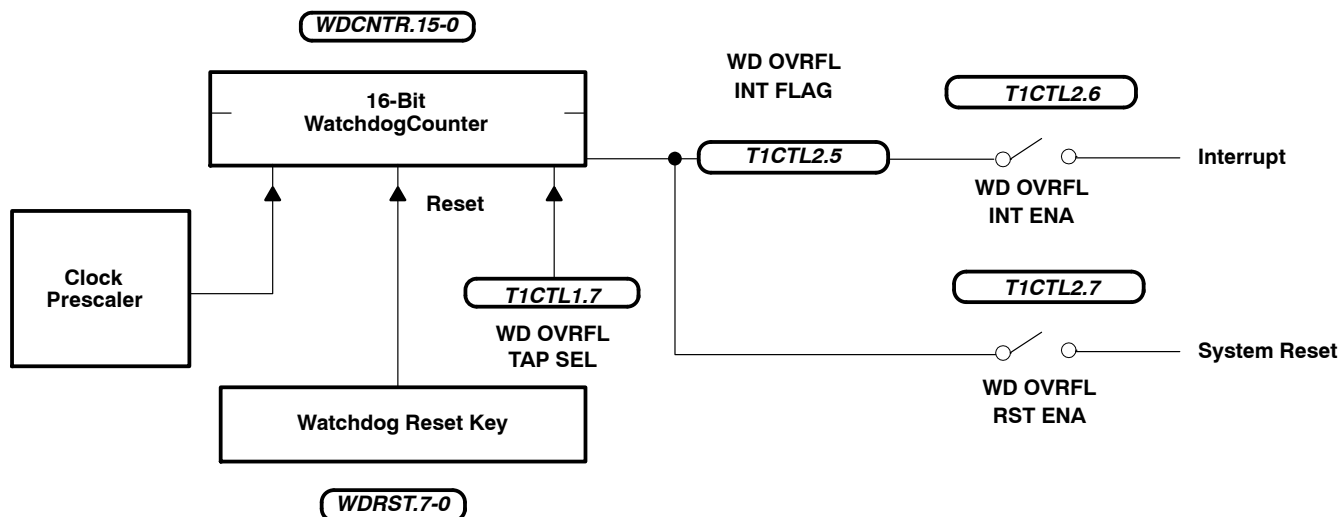


Figure 9. Standard watchdog

timer 1 module (continued)

- Hard watchdog configuration (see Figure 10) for mask-ROM devices:
 - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5 MHz SYSCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows.
 - Automatic activation of the WD timer upon power-up reset
 - INT1 is enabled as a nonmaskable interrupt during low-power modes.
 - A watchdog overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset

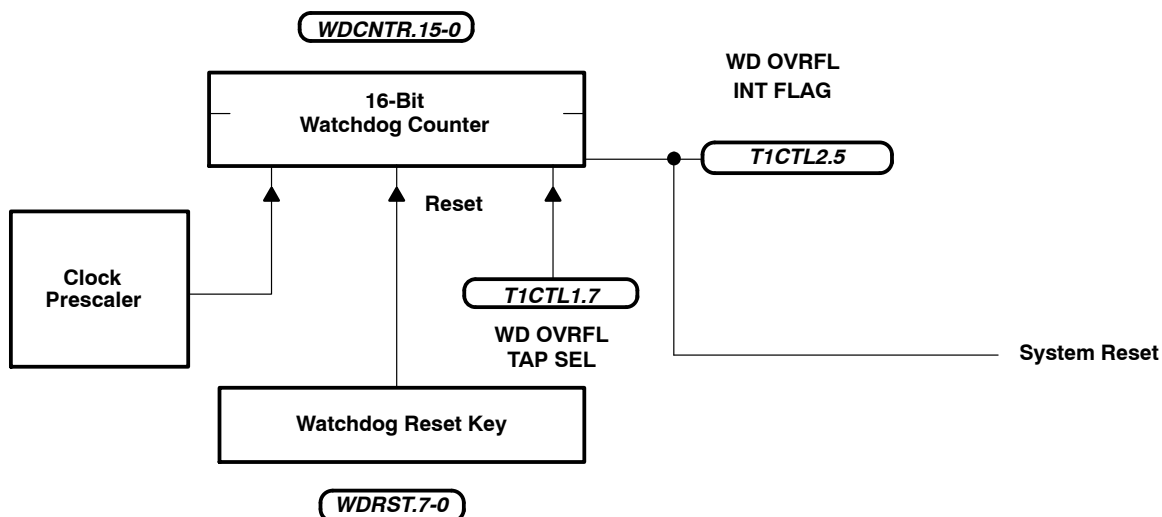


Figure 10. Hard Watchdog

- Simple counter configuration – for mask-ROM devices only (see Figure 11)
 - Simple counter can be configured as an event counter, pulse accumulator or an internal timer.

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timer 1 module (continued)

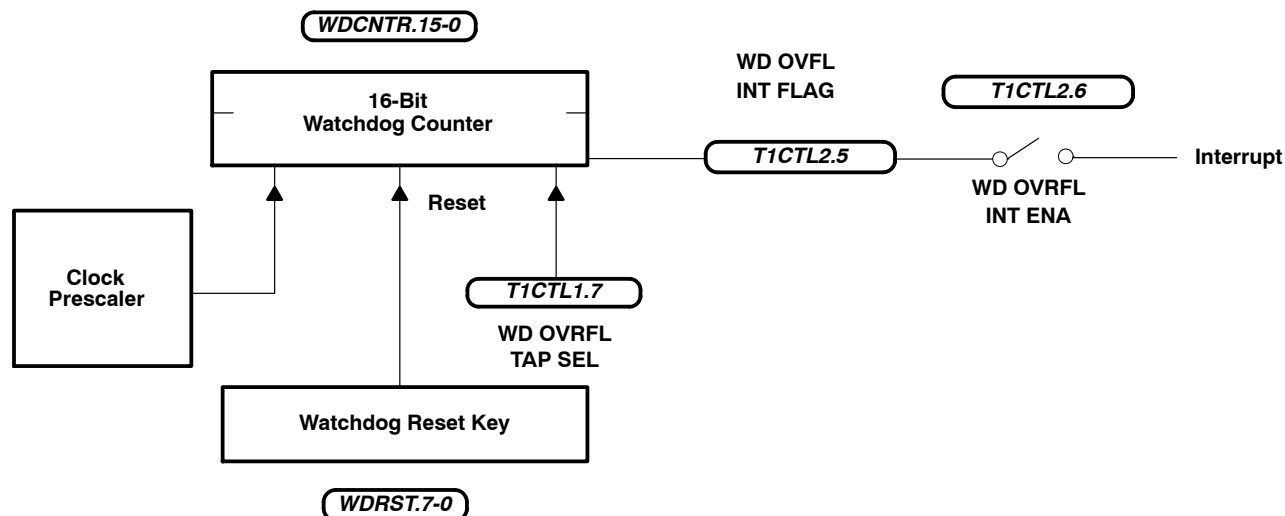


Figure 11. Simple Counter

timer 2A module

The 16-bit general-purpose timer 2A (T2A) module is composed of a 16-bit resettable counter, 16 bit compare register with associated compare logic, 16-bit capture register, and a 16-bit register that functions as a capture register in one mode and as a compare register in the other mode. The T2A module adds an additional timer that provides event count, input capture, and compare functions. The T2A module includes three external device pins that can be dedicated as timer functions or used as general-purpose I/O pins. The T2A module is shown in Figure 12.

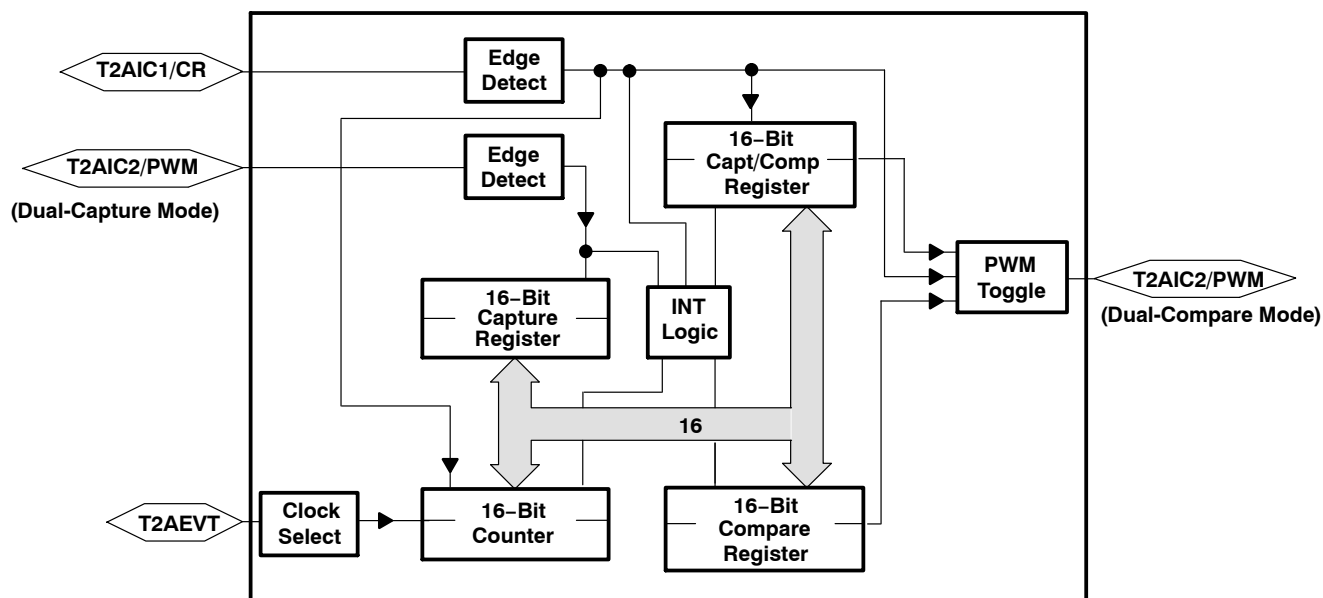


Figure 12. Timer 2A Block Diagram

timer 2A module (continued)

The T2A module features include the following:

- Three I/O pins:
 - T2AIC1/CR: T2A input-capture 1/counter-reset input pin, or general-purpose bidirectional I/O pin
 - T2AIC2/PWM: T2A input-capture 2/pulse-width-modulation (PWM) output pin, or general-purpose bidirection I/O pin
 - T2AEVT: Timer 2A event-input pin, or general-purpose bidirection I/O pin
- Two operational modes:
 - Dual-compare mode: Provides PWM signal
 - Dual-capture mode: Provides input-capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture register with associated capture logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register
- T2A clock sources can be any of the following:
 - System clock
 - No clock (the counter is stopped)
 - External clock synchronized to the system clock (event counter)
 - System clock while external input is high (pulse accumulation)
- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T2AIC1/CR)
- Interrupts that can be generated on the occurrence of:
 - A compare equal to dedicated compare register
 - A compare equal to capture-compare register
 - A counter overflow
 - An external edge 1 detection
 - An external edge 2 detection
- Fourteen T2A module-control registers: Located in the PF frame beginning at address P060

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timer 2A module (continued)

The T2A module-control registers are illustrated in Table 13.

Table 13. Timer 2A Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	Mode: Dual-Compare and Dual-Capture								
P060	Bit 15			T2A Counter MSbyte				Bit 8	T2ACNTR
P061	Bit 7			T2A Counter LSbyte				Bit 0	
P062	Bit 15			Compare Register MSbyte				Bit 8	T2AC
P063	Bit 7			Compare Register LSbyte				Bit 0	
P064	Bit 15			Capture/Compare Register MSbyte				Bit 8	T2ACC
P065	Bit 7			Capture/Compare Register LSbyte				Bit 0	
P066	Bit 15			Capture Register 2 MSbyte				Bit 8	T2AIC
P067	Bit 7			Capture Register 2 LSbyte				Bit 0	
P06A	—	—	—	T2A OVRFL INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1
	Mode: Dual-Compare								
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC2 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
	Mode: Dual-Capture								
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
	Mode: Dual-Compare and Dual-Capture								
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2/PWM DATA IN	T2AIC2/PWM DATA OUT	T2AIC2/PWM FUNCTION	T2AIC2/PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC1/CR DATA DIR	T2APC2
P06F	T2A STEST	T2A PRIORITY	—	—	—	—	—	—	T2APRI

timer 2A module (continued)

The T2A dual-compare mode block diagram is illustrated in Figure 13. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2ACTL2.0 is 106Bh, bit 0, in the T2ACTL2 register.

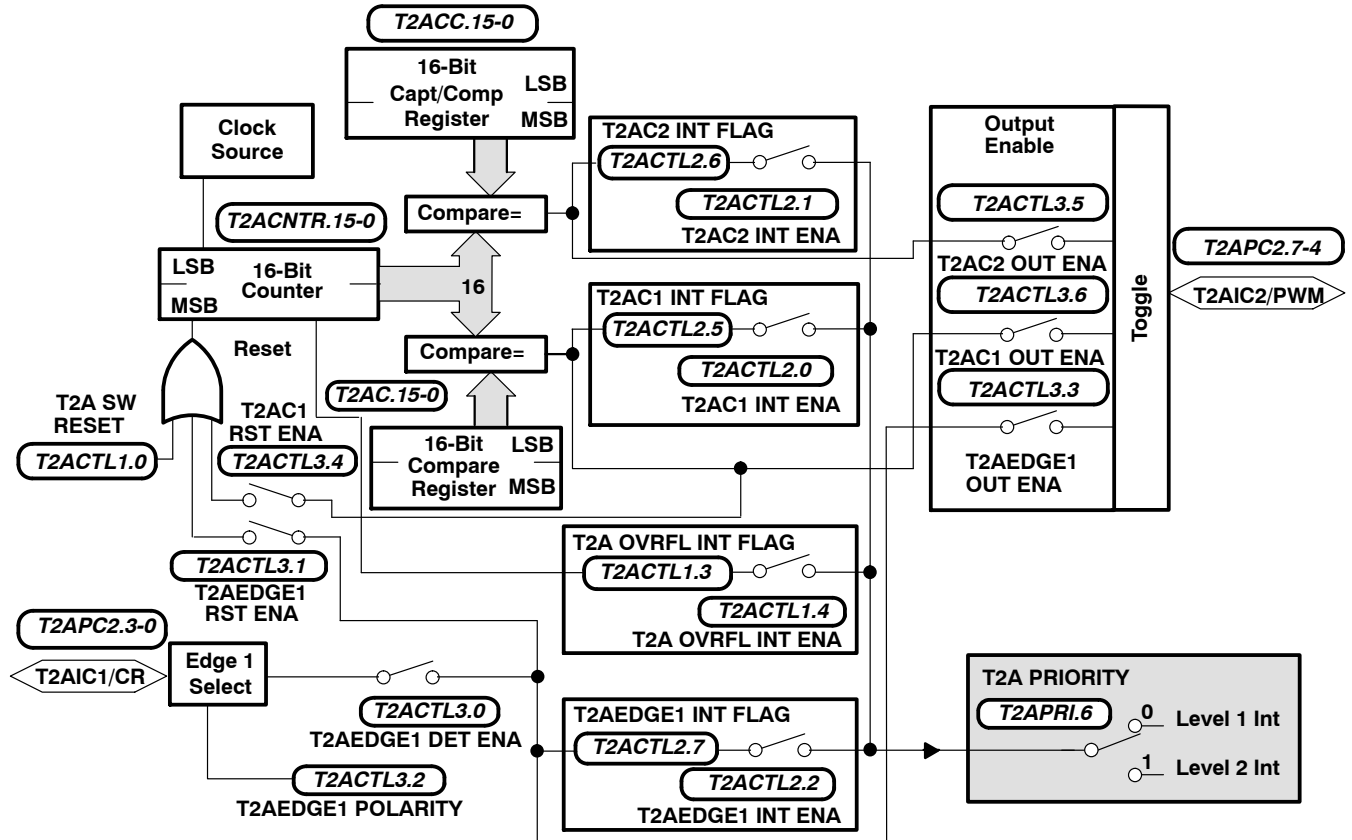


Figure 13. Dual-Compare Mode

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The T2A dual-capture mode block diagram is illustrated in Figure 14. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2ACTL2.0 is 106Bh, bit 0, in the T2ACTL2 register.



The TMS370C3A7 device includes a serial communications interface 1 (SCI1) module. The SCI1 module supports digital communications between the TMS370 devices and other asynchronous peripherals and uses the standard non return-to-zero (NRZ) format. The SCI1 receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full duplex mode. To ensure data integrity, the SCI1 checks received data for break detection, parity, overrun, and framing errors. The speed of bit rate (baud) is programmable to over 65,000 different speeds through a 16-bit baud-select register. Features of the SCI1 module include:

- Three external pins:
 - SCITXD: SCI transmit-output pin or general-purpose bidirectional I/O pin.
 - SCIRXD: SCI receive-input pin or general-purpose bidirectional I/O pin.
 - SCICLK: SCI bidirectional serial-clock pin, or general-purpose bidirectional I/O pin.
- Two communications modes: asynchronous and isosynchronous[†]

† Isosynchronous = Isochronous

serial communications interface 1 module (continued)

- Baud rate: 64K different programmable rates
 - Asynchronous mode: 3 bps to 156K bps at 5 MHz SYSCLK
$$\text{Asynchronous Baud} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 32}$$
 - Isosynchronous mode: 39 bps to 2.5 Mbps at 5 MHz SYSCLK
$$\text{Isosynchronous Baud} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 2}$$
- Data word format:
 - One start bit
 - Data word length programmable from one to eight bits
 - Optional even/odd/no parity bit
 - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: Idle-line and address bit
- Half or full-duplex operation
- Double-buffered receiver and transmitter operations
- Transmitter and receiver operations can be accomplished through either interrupt-driven or polled-algorithms with status flags:
 - Transmitter: TXRDY flag (transmitter buffer register is ready to receive another character) and TX EMPTY flag (Transmitter shift register is empty)
 - Receiver: RXRDY flag (receive buffer register ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR monitoring four interrupt conditions
 - Separate enable bits for transmitter and receiver interrupts
 - NRZ (non return-to-zero) format
- Eleven SCI1 module control registers, located in control register frame beginning at address P050h

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serial communications interface 1 module (continued)

The SCI1 module control registers are illustrated in Table 14.

Table 14. SCI1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNC/ ISOSYNC	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	Reserved								
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF
P05A P05B P05C	Reserved								
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	SCI STEST	SCITX PRIORITY	SCIRX PRIORITY	SCI ESPEN	—	—	—	—	SCIPRI

The SCI1 module block diagram is illustrated in Figure 15.



NO TAG provides an opcode-to-instruction cross-reference of all 73 instructions and 274 opcodes of the '370CxAx instruction set. The numbers at the top of this table represent the most significant nibble (MSN) of the opcode while the numbers at the left side of the table represent the least significant nibble (LSN). The instructions for these two opcode nibbles contain the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

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Table 15. TMS370 Family Opcode/Instruction Map[†]

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	L	JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8			CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
		JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7
2	S	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7
		JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8
4	N	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes
		JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14	
6	I	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6
		JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10
8	O	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7
		JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9
A	P	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12
		JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

Table 15. TMS370 Family Opcode/Instruction Map[†] (Continued)

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L S N	C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
	D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
	E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
	F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):

F4	8	MOVW *n[Rn] 4/15	DIV Rn,A 3/14-63
F4	9	JMPL *n[Rn] 4/16	
F4	A	MOV *n[Rn],A 4/17	
F4	B	MOV A,*n[Rn] 4/16	
F4	C	BR *n[Rn] 4/16	
F4	D	CMP *n[Rn],A 4/18	
F4	E	CALL *n[Rn] 4/20	
F4	F	CALLR *n[Rn] 4/22	

Legend:

* = Indirect addressing operand prefix
 & = Direct addressing operand prefix
 # = immediate operand
 #16 = immediate 16-bit number
 lab = 16-label
 n = immediate 8-bit number
 Pd = Peripheral register containing destination type
 Pn = Peripheral register
 Ps = Peripheral register containing source byte
 ra = Relative address
 Rd = Register containing destination type
 Rn = Register file
 Rp = Register pair
 Rpd = Destination register pair
 Rps = Source Register pair
 Rs = Register containing source byte

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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development system support

The TMS370 family development support tools include an assembler, a C-compiler, a linker, an in-circuit emulator (XDS22 – extended development support), and compact development tool, and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
 - Includes extensive macro capability
 - Allows high-speed operation
 - Provides format conversion utilities for popular formats.
- ANSI C-compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, Sun-3™ or Sun-4™).
 - Generates assembly code for the TMS370 that can be inspected easily.
 - Improves code execution speed and reduces code size with optional optimizer pass.
 - Enables direct reference to the TMS370's port registers by using a naming convention.
 - Provides flexibility in specifying the storage for data objects.
 - Interfaces C functions and assembly functions easily.
 - Includes assembler and linker.
- CDT370 (compact development tool) real-time in-circuit emulation
 - Base (Part Number EDSCDT370 – for PC, requires cable)
 - Cable for 40-pin DIP (Part No. EDSTRG40DILAX).
 - Includes EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Allows uploading/downloading program and data memory
 - Executes programs and software routines
 - Includes 1 024-sample trace buffer
 - Provides single-step executable instructions
 - Uses software breakpoints to halt program execution at selected address.
- XDS/22 (extended development support) in-circuit emulator
 - Base (Part Number TMDS3762210 for PC, requires cable)
 - Cable for 40-pin DIP (Part No. TMDS3788844).
 - Contains all of the features of the CDT370 described previously but does not have the capability to program the data EEPROM and program EPROM.
 - Contains sophisticated breakpoint trace and timing hardware that provides up to 2047 qualified trace samples with symbolic disassembly.
 - Allows qualification of breakpoints by address and/or data on any type of memory acquisition. Up to four levels of events can be combined to cause a breakpoint.

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Sun-3 and Sun-4 are trademarks of Sun Microsystems, Inc.



development system support (continued)

- Provides timers for analyzing total and average time in routines.
- Contains an eight-line logic probe for adding visibility of external signals to the breakpoint qualifier and for tracing display.
- Microcontroller programmer
 - Base (Part No. TMDS3760500A – for PC, requires programmer head)
 - Single unit head for 40-pin PDIP (Part No. TMDS3780511A)
 - Personal computer based, window/function-key-oriented user interface for ease of use and rapid learning environment
- Starter kit (Part No. TMDX37000 – For PC)
 - Includes TMS370 Assembler diskette and documentation.
 - Includes TMS370 Simulator.
 - Includes programming adapter board and programming software.
 - Does not include (to be supplied by the user):
 - + 5 V power supply
 - ZIF sockets
 - Nine-pin RS232 cable
- Converter socket (Part No. TMDS37788OTP)

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device numbering conventions

Figure 16 illustrates the numbering and symbol nomenclature for the TMS370CxAx family.

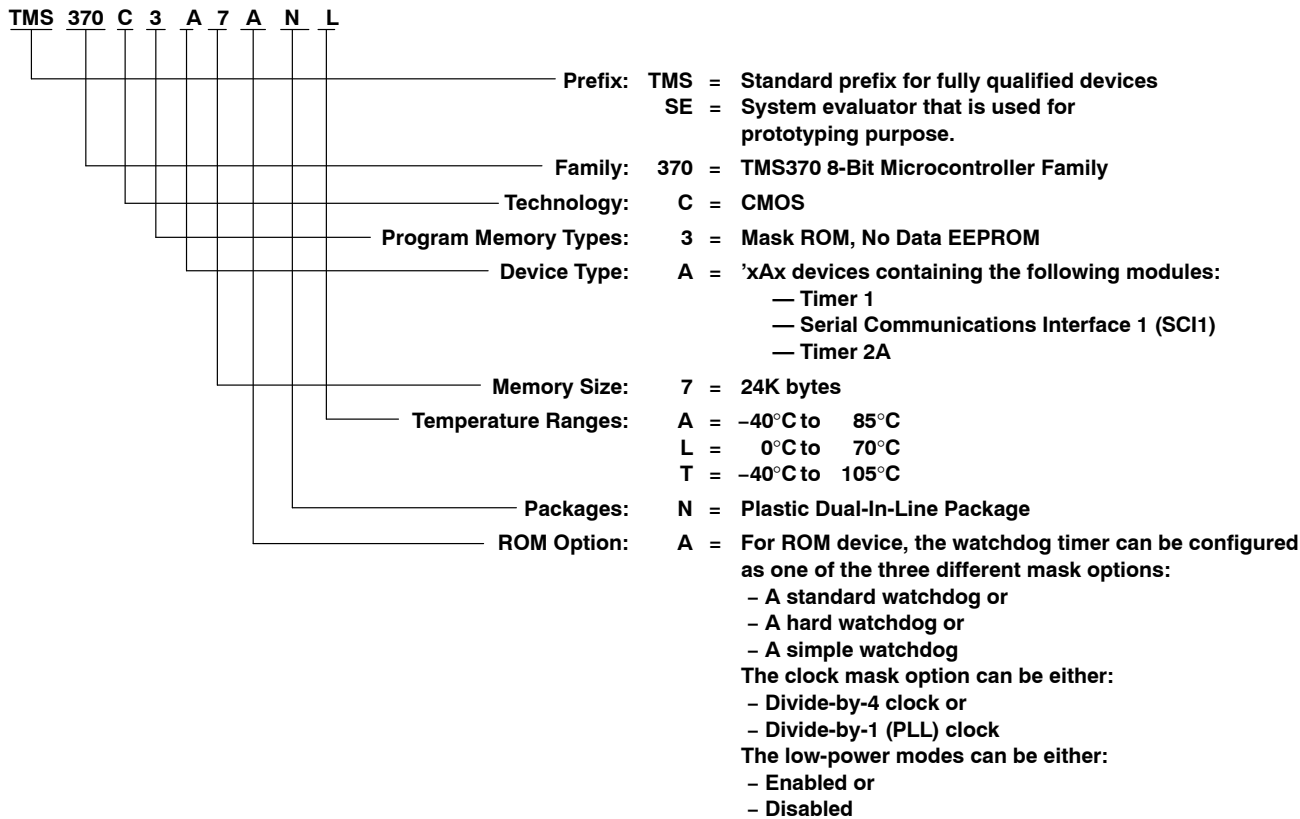


Figure 16. TMS370CxAx Family Nomenclature

device part numbers

Table 16 provides a listing of the '3A7 devices available. The device part number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock, watchdog timer options, and whether or not a low-power mode is desired. Each device can have only one of the three possible watchdog timer options, and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 16. Device Part Numbers

DEVICE PART NUMBERS FOR 40 PINS (PDIP)
TMS370C3A7ANA
TMS370C3A7ANL
TMS370C3A7ANT

new code release form

Figure 17 shows a sample of the new code release form.

NEW CODE RELEASE FORM TEXAS INSTRUMENTS TMS370 MICROCONTROLLER PRODUCTS		DATE: _____	
To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information:			
1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media) 2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.			
Company Name: _____ Street Address: _____ Street Address: _____ City: _____ State _____ Zip _____ Customer Part Number: _____ Customer Application: _____		Contact Mr./Ms.: _____ Phone: (_____) _____ Ext.: _____ Customer Purchase Order Number: _____ Customer Print Number *Yes: _____ # _____ No: _____ (Std. spec to be followed) *If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.	
TMS370 Device: _____ TI Customer ROM Number: _____ (provided by Texas Instruments)			
OSCILLATOR FREQUENCY			
	MIN	TYP	MAX
☐ External Drive (CLKIN)	_____	_____	_____
☐ Crystal	_____	_____	_____
☐ Ceramic Resonator	_____	_____	_____
☐ Supply Voltage MIN: _____ MAX: _____ (std range: 4.5V to 5.5V)			
TEMPERATURE RANGE			
☐ 'L':	0° to 70°C (standard)		
☐ 'A':	-40° to 85°C		
☐ 'T':	-40° to 105°C		
SYMBOLIZATION			
☐ TI standard symbolization ☐ TI standard w/customer part number ☐ Customer symbolization (per attached spec, subject to approval)			
NON-STANDARD SPECIFICATIONS: ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.			
RELEASE AUTHORIZATION: This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cyclotime commences when this document is signed off and the verification code is approved by the customer.			
1. Customer: _____ Date: _____		2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____	

CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS

Low Power Modes ☐ Enabled ☐ Disabled	Watchdog counter ☐ Standard ☐ Hard Enabled ☐ Simple Counter	Clock Type ☐ Standard (/4) ☐ PLL (/1)

NOTE:
 Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B).

PACKAGE TYPE

☐ 'N' 28-pin PDIP ☐ "FN" 28-pin PLCC ☐ 'N' 40-pin PDIP ☐ "NJ" 40-pin PSDIP (formerly known as N2)	☐ "FN" 44-pin PLCC ☐ "FN" 68-pin PLCC ☐ "NM" 64-pin PSDIP

BUS EXPANSION

☐ YES
 ☐ NO

Figure 17. Sample New Code Release Form

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Table 17 is a collection of all the peripheral file frames used in the 'CxAx (provided for a quick reference).

Table 17. Peripheral File Frame Compilation

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	System Configuration Registers								
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTO-WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT / STANDBY	PWRDWN / IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A to P01F	Reserved								
	Digital Port Control Registers								
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	Port B Control Register 2 (must be 0)								BPORT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPORT1
P029	—	—	—	—	—	—	—	Port C Control Register 2 (must be 0)	CPORT2
P02A	—	—	—	—	—	—	—	Port C Data	CDATA
P02B	—	—	—	—	—	—	—	Port C Direction	CDIR
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0) [†]					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

[†] To configure pin D3 as SYSCLK, set port D control 2 = 08h.



Table 17. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Timer1 Module Register Memory Map									
Mode: Dual-Compare and Capture/Compare									
P040	Bit 15	T1 Counter MSbyte						Bit 8	T1CNTR
P041	Bit 7	T1 Counter LSbyte						Bit 0	
P042	Bit 15	Compare Register MSbyte						Bit 8	T1C
P043	Bit 7	Compare Register LSbyte						Bit 0	
P044	Bit 15	Capture/Compare Register MSbyte						Bit 8	T1CC
P045	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P046	Bit 15	Watchdog Counter MSbyte						Bit 8	WDCNTR
P047	Bit 7	Watchdog Counter LSbyte						Bit 0	
P048	Bit 7	Watchdog Reset Key						Bit 0	WDRST
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE=0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture / Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Mode: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI
SCI1 Module Control Memory Map									
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNC/ ISOSYNC	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

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Table 17. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P056	Reserved								RXBUF
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	
P058	Reserved								TXBUF
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	
P05A P05B P05C	Reserved								SCIPC1
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	SCI STEST	SCITX PRIORITY	SCIRX PRIORITY	SCI ESPEN	—	—	—	—	SCIPRI
T2A MODULE REGISTER									
Mode: Dual-Compare and Dual-Capture									
P060	Bit 15 T2A Counter MSbyte Bit 8								T2ACNR
P061	Bit 7 T2A Counter LSbyte Bit 0								
P062	Bit 15 Compare Register MSbyte Bit 8								T2AC
P063	Bit 7 Compare Register LSbyte Bit 0								
P064	Bit 15 Capture/Compare Register MSbyte Bit 8								T2ACC
P065	Bit 7 Capture/Compare Register LSbyte Bit 0								
P066	Bit 15 Capture Register 2 MSbyte Bit 8								T2AIC
P067	Bit 7 Capture Register 2 LSbyte Bit 0								
P06A	—	—	—	T2A OVRFL- INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1
Mode: Dual-Compare									
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC2 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
Mode: Dual-Capture									
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
Mode: Dual-Compare and Dual-Capture									
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2/PWM DATA IN	T2AIC2/PWM DATA OUT	T2AIC2/PWM FUNCTION	T2AIC2/PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC1/CR DATA DIR	T2APC2
P06F	T2A STEST	T2A PRIORITY	—	—	—	—	—	—	T2APRI

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 2)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC}) (see Note 3)	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	1 W
Operating free-air temperature, T_A :	
L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. Unless otherwise noted, all voltage values are with respect to V_{SS} .

3. Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage (see Note 2)		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 4)		3		5.5	V
V _{IL}	Low-level input voltage	All pins except MC	V _{SS}		0.8	V
		MC, normal operation	V _{SS}		0.3	
V _{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET	2		V _{CC}	V
		XTAL2/CLKIN	0.8 V _{CC}		V _{CC}	
		RESET	0.7 V _{CC}		V _{CC}	
V _{MC}	MC (mode control) voltage	Microcomputer	V _{SS}		0.3	V
T _A	Operating free-air temperature	L version	0		70	°C
		A version	– 40		85	
		T version	– 40		105	

NOTES: 2. Unless otherwise noted, all voltage values are with respect to V_{SS} .

4. RESET must be activated externally when V_{CC} or SYSCLK is out of the recommended operating range.

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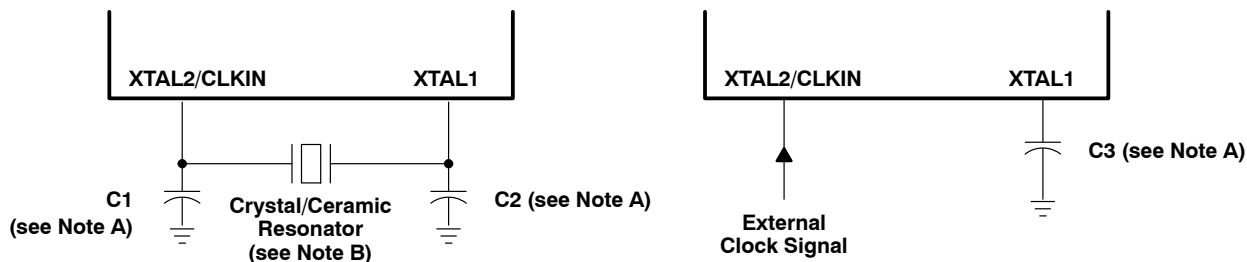
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OL}	Low-level output voltage	I _{OL} = 1.4 mA			0.4	V
V _{OH}	High-level output voltage	I _{OH} = -50 µA	0.9 V _{CC}			V
		I _{OH} = -2 mA	2.4			
I _I	Input current	MC	0 V < V _I ≤ 0.3 V		10	µA
			0.3 V < V _I ≤ 13 V		650	
		I/O pins	0 V ≤ V _I ≤ V _{CC}		± 10	µA
I _{OL}	Low-level output current	V _{OL} = 0.4 V	1.4			mA
I _{OH}	High-level output current	V _{OH} = 0.9 V _{CC}	- 50			µA
		V _{OH} = 2.4 V	- 2			mA
I _{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 7)	See Notes 5 and 6 SYSCLK = 5 MHz		30	45	mA
		See Notes 5 and 6 SYSCLK = 3 MHz		20	30	
		See Notes 5 and 6 SYSCLK = 0.5 MHz		7	11	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 8)	See Notes 5 and 6 SYSCLK = 5 MHz		10	17	mA
		See Notes 5 and 6 SYSCLK = 3 MHz		8	11	
		See Notes 5 and 6 SYSCLK = 0.5 MHz		2	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 9)	See Notes 5 and 6 SYSCLK = 3 MHz		6	8.6	mA
		See Notes 5 and 6 SYSCLK = 0.5 MHz		2	3.0	
	Supply current (HALT mode)	See Note 5 XTAL2/CLKIN < 0.2 V		2	30	µA

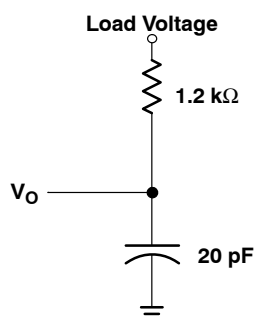
- NOTES: 5. Single chip mode, ports configured as inputs or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} - 0.2 V.
6. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = 0.01 mA x (total load capacitance + crystal capacitance in pF).
7. Maximum operating current = 7.6 (SYSCLK) + 7 mA.
8. Maximum standby current = 3 (SYSCLK) + 2 mA. (OSC POWER bit = 0).
9. Maximum standby current = 2.24 (SYSCLK) + 1.9 mA. (OSC POWER bit = 1, only valid up to 3 MHz of SYSCLK).





NOTES: A. The values of C1 and C2 are typically 15 pF and the value of C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.
B. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.

Figure 18. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4 \text{ V}$; Load Voltage = 0 V

Case 2: $V_O = V_{OL} = 0.4 \text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 19. Typical Output Load Circuit (See Note A)

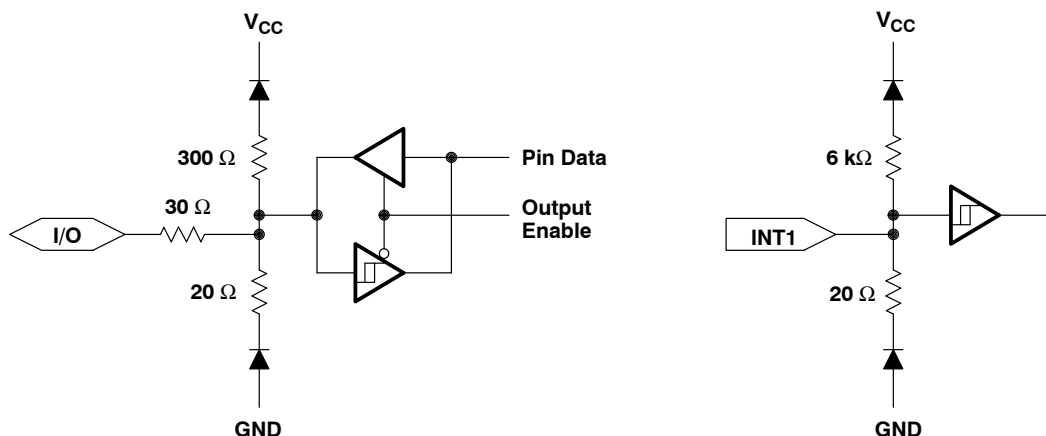


Figure 20. Typical Buffer Circuitry

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PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

AR	Array	SC	SYSCLK
B	Byte	SCC	SCICLK
CI	XTAL2/CLKIN	TXD	SCITXD
RXD	SCIRXD		

Lowercase subscripts and their meanings are:

c	cycle time (period)	su	setup time
d	delay time	v	valid time
f	fall time	w	pulse duration (width)
r	rise time		

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid

All timings are measured between high and low measurement points as indicated in Figure 21 and Figure 22.

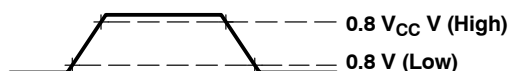


Figure 21. XTAL2/CLKIN Measurement Points

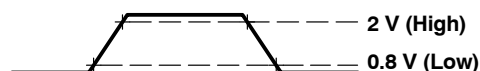


Figure 22. General Measurement Points

external clocking requirements for divide-by-4 clock (see Note 10 and Figure 23)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 11)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN Crystal operating frequency	2	20	MHz
	SYSCLK Internal system clock operating frequency [†]	0.5	5	MHz

[†] SYSCLK = CLKIN/4

NOTES: 10. For V_{IL} and V_{IH} , refer to recommended operating conditions.

11. This pulse can be either a high pulse which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

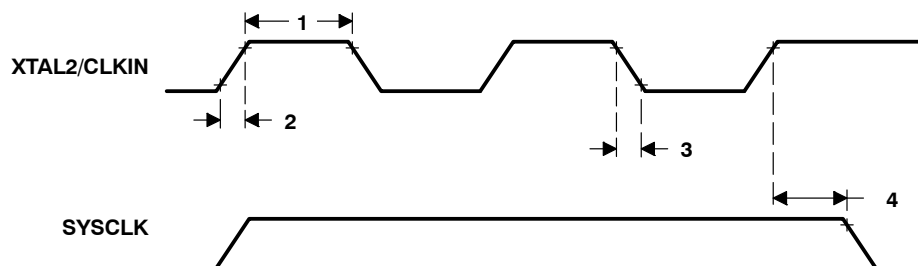


Figure 23. External Clock Timing for Divide-by-4

external clocking requirements for divide-by-1 clock (PLL) (see Note 10 and Figure 24)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 11)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN Crystal operating frequency	2	5	MHz
	SYSCLK Internal system clock operating frequency [‡]	2	5	MHz

[‡] SYSCLK = CLKIN/1

NOTES: 10. For V_{IL} and V_{IH} , refer to recommended operating conditions.

11. This pulse can be either a high pulse which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

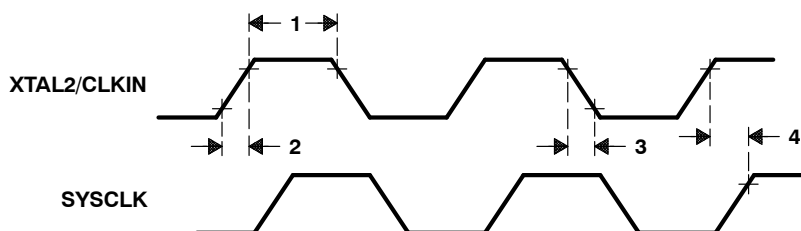


Figure 24. External Clock Timing for Divide-by-1

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switching characteristics and timing requirements (see Note 12 and Figure 25)

NO.	PARAMETER		MIN	MAX	UNIT
5	t_c	Cycle time, SYSCLK (system clock)	200	2000	ns
		Divide-by-4	200	500	
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low	$0.5 t_c - 20$	$0.5 t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high	$0.5 t_c$	$0.5 t_c + 20$	ns

NOTE 12: t_c = system-clock cycle time = 1 / SYSCLK

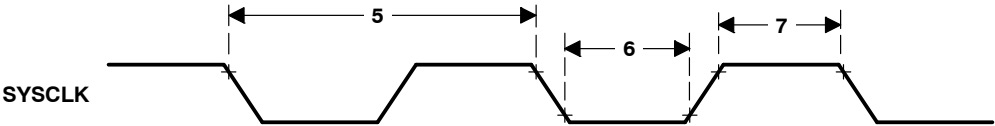


Figure 25. SYSCLK Timing

general purpose output signal switching time requirements

		MIN	TYP	MAX	UNIT
t_r	Rise time		30		ns
t_f	Fall time		30		ns

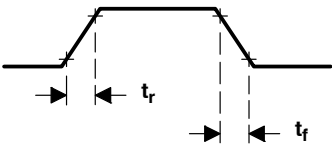


Figure 26. Signal Switching Time

SCI1 isosynchronous mode timing characteristics and requirements for internal clock
(see Note 12 and Figure 27)

NO.		MIN	MAX	UNIT
24	$t_c(\text{SCC})$ Cycle time, SCICLK	$2t_c$	$131\,072t_c$	ns
25	$t_w(\text{SCCL})$ Pulse duration, SCICLK low	$t_c - 45$	$0.5t_c(\text{SCC}) + 45$	ns
26	$t_w(\text{SCCH})$ Pulse duration, SCICLK high	$t_c - 45$	$0.5t_c(\text{SCC}) + 45$	ns
27	$t_d(\text{SCCL-TXDV})$ Delay time, SCITXD valid after SCICLK low	- 50	60	ns
28	$t_v(\text{SCCH-TXD})$ Valid time, SCITXD data valid after SCICLK high	$t_w(\text{SCCH}) - 50$		ns
29	$t_{su}(\text{RXD-SCCH})$ Setup time, SCIRXD to SCICLK high	$0.25 t_c + 145$		ns
30	$t_v(\text{SCCH-RXD})$ Valid time, SCIRXD data valid after SCICLK high	0		ns

NOTE 12: t_c = system-clock cycle time = $1/\text{SYSCLK}$

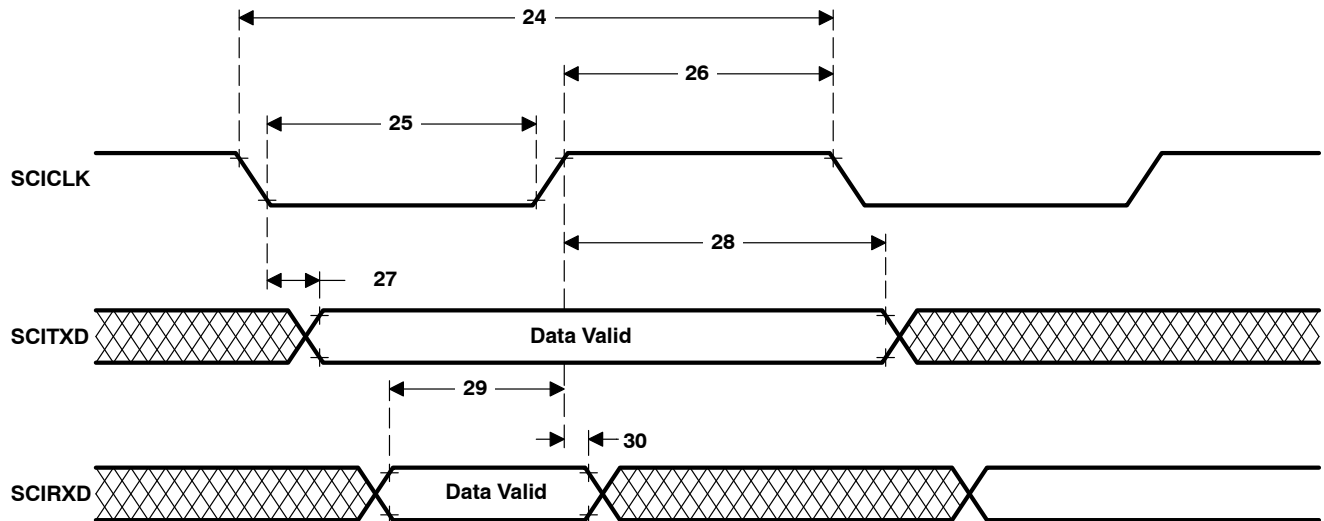


Figure 27. SCI1 Isosynchronous Mode Timing for Internal Clock

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SCI1 isosynchronous mode timing characteristics and requirements for external clock
(see Note 12 and Figure 28)

NO.		MIN	MAX	UNIT
31	$t_c(SCC)$ Cycle time, SCICLK	$10t_c$		ns
32	$t_w(SCCL)$ Pulse duration, SCICLK low	$4.25t_c + 120$		ns
33	$t_w(SCCH)$ Pulse duration, SCICLK high	$t_c + 120$		ns
34	$t_d(SCCL-TXDV)$ Delay time, SCITXD valid after SCICLK low		$4.25t_c + 145$	ns
35	$t_v(SCCH-TXD)$ Valid time, SCITXD data valid after SCICLK high	$t_w(SCCH)$		ns
36	$t_{su}(RXD-SCCH)$ Setup time, SCIRXD to SCICLK high	40		ns
37	$t_v(SCCH-RXD)$ Valid time, SCIRXD data after SCICLK high	$2t_c$		ns

NOTE 12: t_c = system-clock cycle time = 1 / SYSCLK

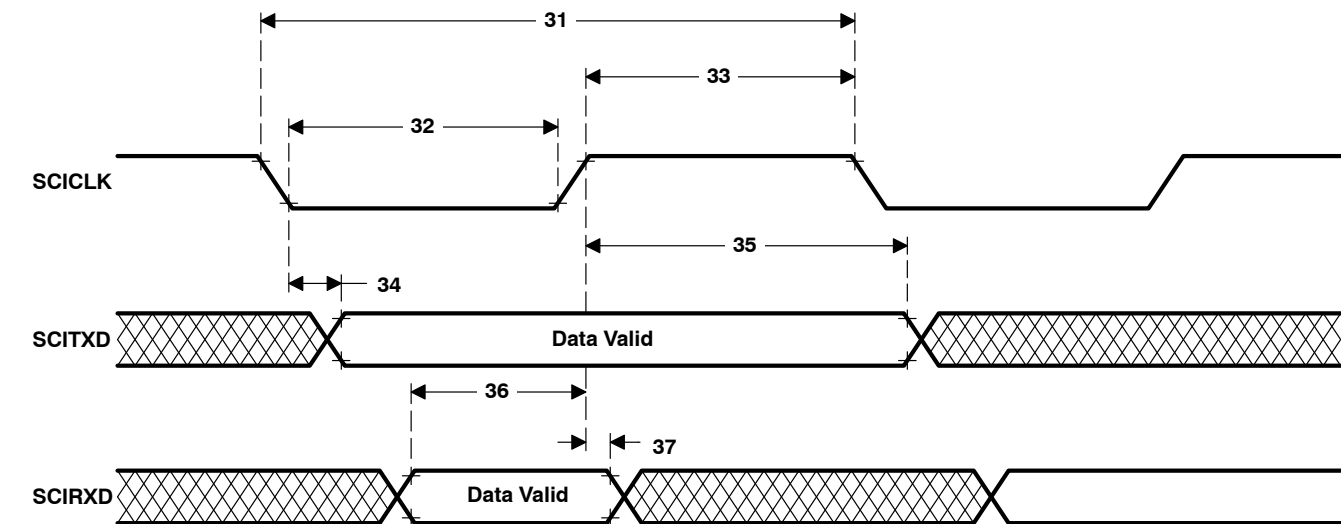


Figure 28. SCI1 Isosynchronous Timing for External Clock

Table 18 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

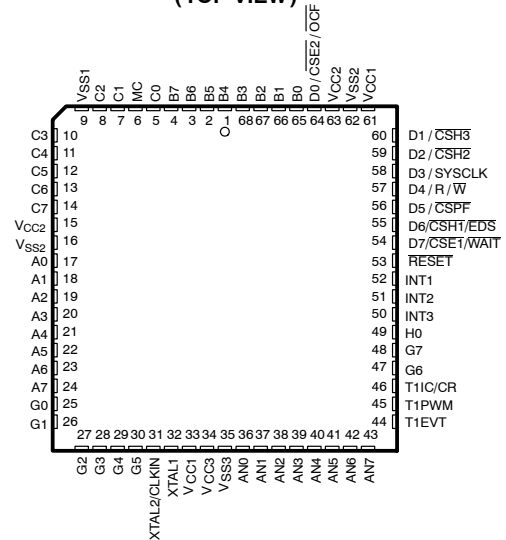
Table 18. TMS370CxAx Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
N – 40 pin (100-mil pin spacing)	PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	N(R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE	TMS370C3A7ANL TMS370C3A7ANA TMS370C3A7ANT

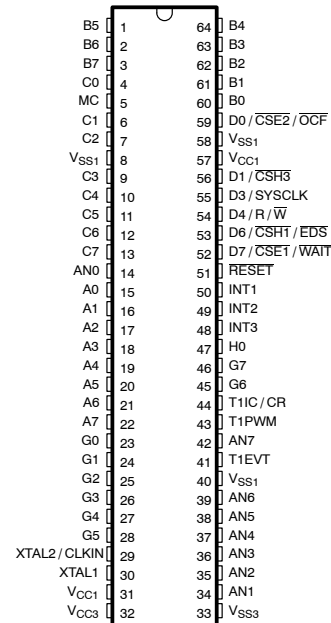
General Information	1
Selection Guide/Tools	2
Ops Cond/Timing/Glossary	3
TMS370Cx0x Data Sheet	4
TMS370Cx1x Data Sheet	5
TMS370Cx2x Data Sheet	6
TMS370Cx32 Data Sheet	7
TMS370Cx36 Data Sheet	8
TMS370Cx4x Data Sheet	9
TMS370Cx5x Data Sheet	10
TMS370Cx6x Data Sheet	11
TMS370Cx7x Data Sheet	12
TMS370Cx8x Data Sheet	13
TMS370Cx9x Data Sheet	14
TMS370CxAx Data Sheet	15
TMS370CxBx Data Sheet	16
TMS370CxCx Data Sheet	17
Mechanical Data	18
Quality and Reliability	19
Electrostatic Discharge Guidelines	20

- **CMOS/EEPROM/EPROM Technologies on a Single Device**
 - Mask-ROM Devices for High-Volume Production
 - EPROM Devices for Prototyping Purposes (TMS370C758 and SE370C758)
- **Internal System Memory Configurations**
 - On-Chip ROM: 16K Bytes
 - Data EEPROM: 256 Bytes
 - Static RAM: 384 Bytes
 - External Memory/Peripheral Wait States
 - Precoded External Chip-Select Outputs in Microcomputer Mode
- **Flexible Operating Features**
 - Low-Power Modes: STANDBY and HALT
 - Commercial, Industrial, and Automotive Temperature Ranges
 - Clock Options:
 - Divide-by-4 (0.5-MHz – 5-MHz SYSCLK)
 - Divide-by-1 (2-MHz – 5-MHz SYSCLK) Phase-Locked Loop (PLL)
 - Supply Voltage (V_{CC}): $5\text{ V} \pm 10\%$
- **16-Bit General-Purpose Timer**
 - Software Configurable as a 16-Bit Event Counter, or a 16-Bit Pulse Accumulator, or a 16-Bit Input Capture Function, or a Two Compare Registers, or a Self-Contained Pulse-Width-Modulation (PWM) Function
- **TMS370 Series Compatibility**
 - Instructions Upwardly Compatible With All TMS370 Devices
 - Register-to-Register Architecture
 - 256 General-Purpose Registers
 - 14 Powerful Addressing Modes
- **On-Chip 24-Bit Watchdog Timer**
 - Mask-ROM Devices: Hard Watchdog, Simple Counter, or Standard Watchdog
- **CMOS/Package/TTL-Compatible I/O Pins**
 - 64-Pin Plastic Shrink Dual-In-Line Package / 44 Bidirectional, 9 Input Pins
 - 68-Pin Plastic Chip Carrier Package / 46 Bidirectional, 9 Input Pins
 - All Peripheral Function Pins Are Software Configurable for Digital I/O
- **Eight-Channel 8-Bit Analog-to-Digital Converter 1 (ADC1)**

FN PACKAGE
(TOP VIEW)



NM PACKAGE
(TOP VIEW)



- **Flexible Interrupt Handling**
- **Workstation/PC-Based Software Development System**
 - C Compiler and C Source Debugger
 - Real-Time In-Circuit Emulation
 - Extensive Breakpoint/Trace Capability
 - Software Performance Analysis
 - Multi-Window User Interface
 - Microcontroller Programmer



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Pin Descriptions

PIN				I/O†	DESCRIPTION‡
NAME	ALTERNATE FUNCTION	PSDIP (64)	PLCC (68)		
A0 A1 A2 A3 A4 A5 A6 A7	DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7	15 16 17 18 19 20 21 22	17 18 19 20 21 22 23 24	I/O	Single-chip mode: Port A is a general-purpose bidirectional I/O port. Expansion mode: Port A can be individually programmed as the external bidirectional data bus (DATA0 – DATA7).
B0 B1 B2 B3 B4 B5 B6 B7	ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7	60 61 62 63 64 1 2 3	65 66 67 68 1 2 3 4	I/O	Single-chip mode: Port B is a general-purpose bidirectional I/O port. Expansion mode: Port B can be individually programmed as the low-order address output bus (ADDR0 – ADDR7).
C0 C1 C2 C3 C4 C5 C6 C7	ADDR8 ADDR9 ADDR10 ADDR11 ADDR12 ADDR13 ADDR14 ADDR15	4 6 7 9 10 11 12 13	5 7 8 10 11 12 13 14	I/O	Single-chip mode: Port C is a general-purpose bidirectional I/O port. Expansion mode: Port C can be individually programmed as the high-order address output bus (ADDR8 – ADDR15).
INT1 INT2 INT3	NMI — —	50 49 48	52 51 50	I I/O I/O	External (nonmaskable or maskable) interrupt/general-purpose input pin External maskable interrupt input/general-purpose bidirectional pin External maskable interrupt input/general-purpose bidirectional pin
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	E0 E1 E2 E3 E4 E5 E6 E7	14 34 35 36 37 38 39 42	36 37 38 39 40 41 42 43	I	ADC1 analog input (AN0 – AN7) or positive reference pins (AN1 – AN7) Port E can be individually programmed as general-purpose input pins if not used as ADC1 analog input or positive reference input.
V _{CC3} V _{SS3}		32 33	34 35		ADC1 positive-supply voltage and optional positive-reference input pin ADC1 ground reference pin
RESET		51	53	I/O	System reset bidirectional pin. RESET, as an input, initializes the microcontroller; as an open-drain output, RESET indicates an internal failure was detected by the watchdog or oscillator fault circuit.
MC		5	6	I	Mode control (MC) pin. MC enables EEPROM write-protection-override (WPO) mode, also EPROM V _{PP} .
XTAL2/CLKIN XTAL1		29 30	31 32	I O	Internal oscillator crystal input/external clock source input Internal oscillator output for crystal
V _{CC1}		31, 57	33, 61		Positive supply voltage
V _{CC2}		—	15, 63		Positive supply voltage for digital I/O

† I = input, O = output

‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Also, port D3 can be configured as SYSCLK.



Pin Descriptions (Continued)

PIN				I/O†	DESCRIPTION‡
NAME	ALTERNATE FUNCTION	PSDIP (64)	PLCC (68)		
V _{SS1}		8, 58,40	9		Ground reference for digital logic
V _{SS2}		—	16,62		Ground reference for digital I/O logic
	FUNCTION				Single-chip mode: Port D is a general-purpose bidirectional I/O port. Each of the port D pins can be individually configured as a general-purpose I/O pin, primary memory control signal (function A), or secondary memory control signal (function B). All chip selects are independent and can be used for memory bank switching. Refer to Table 1 for function A memory accesses.
	A	B			
D0	$\overline{\text{CSE}}_2$	$\overline{\text{OCF}}$	59	64	I/O I/O pin A: Chip-select eighth output 2 goes low during memory accesses. I/O pin B: Opcode fetch goes low during the opcode fetch memory cycle.
D1	$\overline{\text{CSH}}_3$	—	56	60	I/O I/O pin A: Chip-select half output 3 goes low during memory accesses. I/O pin B: Reserved
D2	$\overline{\text{CSH}}_2$	—	—	59	I/O I/O pin A: Chip-select half output 2 goes low during memory accesses. I/O pin B: Reserved
D3	SYSCLK	SYSCLK	55	58	I/O I/O pin A, B: Internal clock signal is 1/1 (PLL) or 1/4 XTAL2/CLKIN frequency.
D4	R/W	R/ $\overline{\text{W}}$	54	57	I/O I/O pin A, B: Read/write output pin
D5	$\overline{\text{CSPF}}$	—	—	56	I/O I/O pin A: Chip-select peripheral output for peripheral file goes low during memory accesses. I/O pin B: Reserved
D6	$\overline{\text{CSH}}_1$	$\overline{\text{EDS}}$	53	55	I/O I/O pin A: Chip-select half output 1 goes low during memory accesses. I/O pin B: External data strobe output goes low during memory accesses from external memory and has the same timings as the five chip selects.
D7	$\overline{\text{CSE}}_1$	WAIT	52	54	I/O I/O pin A: Chip-select eighth output goes low during memory accesses. I/O pin B: Wait input pin extends bus signals.
G0 G1 G2 G3 G4 G5 G6 G7		23 24 25 26 27 28 45 46	25 26 27 28 29 30 47 48	I/O	Port G is a general-purpose bidirectional port.
H0		47	49	I/O	Port H is a general-purpose bidirectional pin.
T1IC/CR	T1IO1	44	46	I/O	Timer1 input capture/counter reset input pin/general-purpose bidirectional pin
T1PWM	T1IO2	43	45	I/O	Timer1 pulse-width-modulation (PWM) output pin/general-purpose bidirectional pin
T1EVT	T1IO3	41	44	I/O	Timer1 external event input pin/general-purpose bidirectional pin

† I = input, O = output

‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Port D3 also can be configured as SYSCLK.

Table 1. Function A: Memory Access Locations for 'xBx Devices

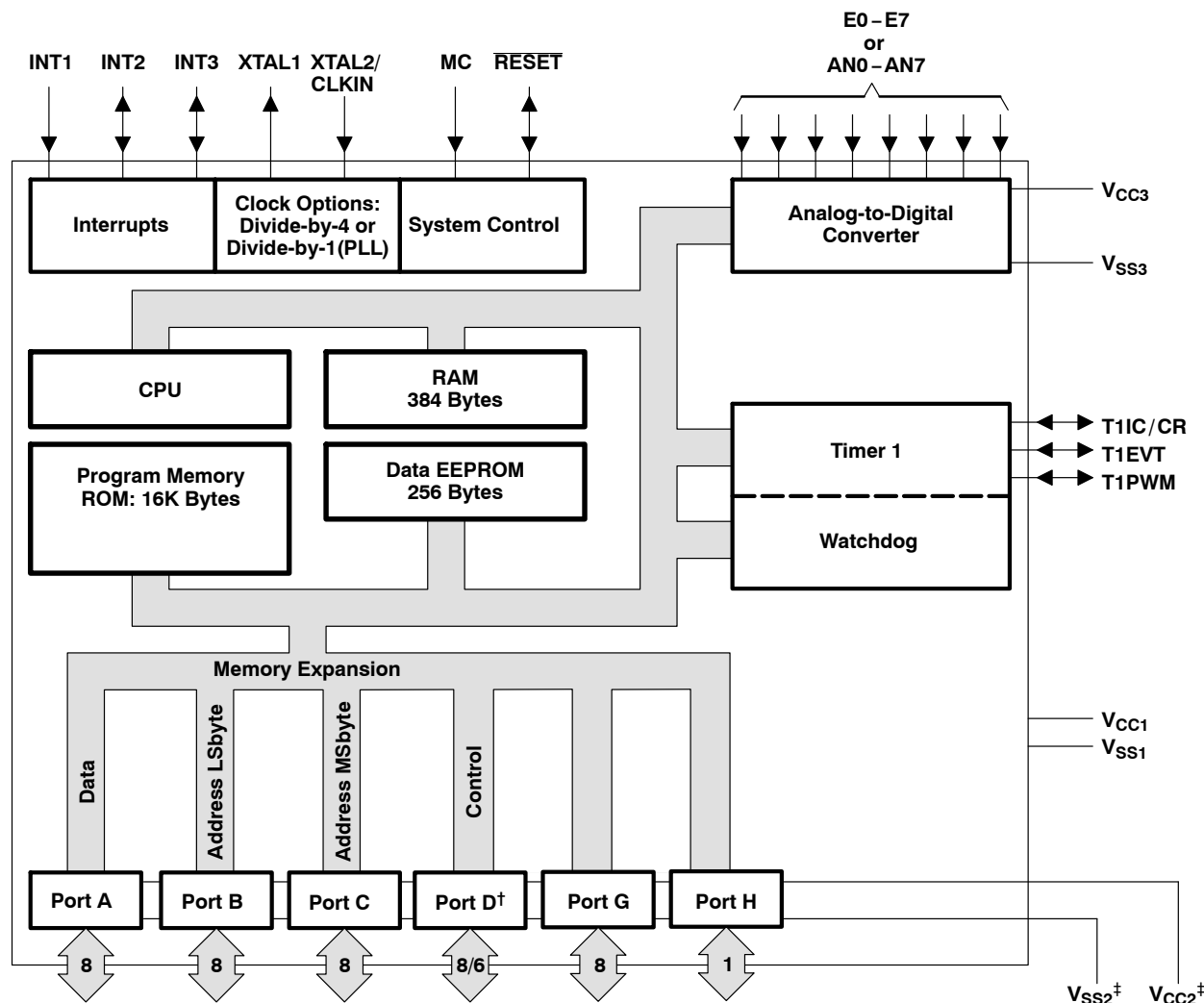
FUNCTION A	TMS370C0B6
$\overline{\text{CSE}}_x$	2000h – 3FFFh (8K bytes)
$\overline{\text{CSH}}_x$	8000h – FFFFh (32K bytes)
$\overline{\text{CSPF}}$	10C0h – 10FFh (64 bytes)

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functional block diagram



† For the 64-pin devices, there are only six pins for port D.

‡ These pins are not available for the 64-pin devices.

description

The TMS370C0B6 is a member of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370CxBx refers to this device. The TMS370 family provides cost-effective real-time system control through integration of advanced peripheral function modules and various on-chip memory configurations.

The TMS370CxBx family is implemented using high-performance silicon-gate CMOS EEPROM technology. The low-operating power, wide-operating temperature range, and noise immunity of CMOS technology, coupled with the high performance and extensive on-chip peripheral functions make the TMS370CxBx devices attractive in system designs for automotive electronics, industrial motor control, computer peripheral control, telecommunications, and consumer application.

description (continued)

All TMS370CxBx devices contain the following on-chip peripheral modules:

- Eight-channel, 8-bit analog-to-digital converter 1 (ADC1)
- One 24-bit general-purpose watchdog timer
- One 16-bit general-purpose timer with an 8-bit prescaler

Table 2 provides a memory configuration overview of the TMS370CxBx device. Also shown are the two recommended development devices – the TMS370C758 (one-time programmable) and SE370C758 (reprogrammable).

Table 2. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		OFF-CHIP MEMORY EXPANSION (BYTES)	DATA MEMORY (BYTES)		OPERATING MODES		PACKAGES 68-PIN PLCC/CLCC, OR 64-PIN PSDIP/CSDIP
	ROM	EPROM		RAM	EEPROM	μC†	μP‡	
TMS370CxBx								
TMS370C0B6A	16K	—	112K	384	256	√	√	FN – PLCC / NM – PSDIP
TMS370C758								
TMS370C758A TMS370C758B	—	32K	112K	1K	256	√	√	FN – PLCC / NM – PSDIP
SE370C758A§, SE370C758B§	—	32K	112K	1K	256	√	√	FZ – CLCC / JN – CSDIP

† μC – Microcomputer mode

‡ μP – Microprocessor mode

§ System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.

The suffix letter A appended to the device names shown in the device column of Table 2 indicates the configuration of the device. ROM and EPROM devices have a different configuration as indicated in Table 3. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 3. Suffix Letter Configuration

DEVICE†	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM A	Standard	Divide-by-4 (Standard oscillator)	Enabled
EPROM B	Hard	Divide-by-1 (PLL)	Enabled
ROM	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

† Refer to the “device numbering conventions” section for device nomenclature and the “device part numbers” section for ordering.

The 16K bytes of mask-programmable ROM in the associated TMS370C0B6 device is replaced in the '370C758 with 32K bytes of EPROM. One-time programmable device (TMS370C758) and the reprogrammable device (SE370C758) offer an additional 640 bytes of RAM and three on-chip peripheral modules (serial communications interface 1, serial peripheral interface, and timer 2A), while having the same EEPROM and off-chip memory expansion size. The 'xBx and 'x5x devices have similar pinouts, except for nine of the pins. Nevertheless, these pins on the 'x5x are configurable as general-purpose I/O as required by the 'xBx device and shown in Table 4.

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description (continued)

Table 4. Conversion Table

PINS		TMS370C0B6A		TMS370C758	
PSDIP (64)	PLCC (68)	NAME	DESCRIPTION	NAME	DESCRIPTION
23	25	G0	Port G general-purpose bidirectional port	T2AEVT	Timer2A external event input pin/general-purpose bidirectional pin
24	26	G1		T2AIC2/PWM	Timer2A input capture 2/PWM output pin/general-purpose bidirectional pin
25	27	G2		T2AIC1/CR	Timer2A input capture 1/counter reset input pin/general-purpose bidirectional pin
26	28	G3		SCICLK	SCI bidirectional serial clock pin/general-purpose bidirectional pin
27	29	G4		SCIRXD	SCI receive data input pin/general-purpose bidirectional pin
28	30	G5		SCITXD	SCI transmit data output pin/general-purpose bidirectional pin
45	47	G6		SPICLK	SPI bidirectional serial clock pin/general-purpose bidirectional pin
46	48	G7		SPISIMO	SPI slave input pin, master output pin/general-purpose bidirectional pin
47	49	H0	Port H general-purpose bidirectional port	SPISOMI	SPI slave output pin, master input pin/general-purpose bidirectional pin

Refer to the TMS370Cx5x data sheet (literature number SPNS010) or the *TMS370 Family User's Guide* (literature number SPNU127) for detailed information because the addresses and the control register manipulators to these associated pins/ports are different between the 'xBx and the 'x5x devices.

TMS370C758 OTP devices are available in plastic packages. This microcontroller is effective for use in immediate production updates for the TMS370C0B6 device or for low-volume production runs when the mask charge or cycle time for the low-cost mask ROM devices is not practical.

The SE370C758 has a windowed ceramic package to allow reprogramming of the program EPROM memory during the development/prototyping phase of design. The SE370C758 devices allow quick updates to breadboards and prototype systems while iterating initial designs.

The TMS370CxBx family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all CPU activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370CxBx features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370CxBx family is fully instruction-set-compatible, providing easy transition between members of the TMS370 8-bit microcontroller family.

For large memory applications, the TMS370CxBx family provides an external bus with non-multiplexed address and data. Precoded memory chip select outputs can be enabled, which allows minimum-chip-count system implementations. Wait state support facilitates performance matching between the CPU and external memory and the peripherals. All pins associated with memory expansion interface are individually software configurable for general-purpose digital input/output pins when operating in the microcomputer mode.



description (continued)

The TMS370CxBx family provides the system designer with very economical, efficient solutions to real-time control applications. The TMS370 family extended development system (XDS™) and compact development tool (CDT™) solve the challenge of efficiently developing the software and hardware required to design the TMS370CxBx into an ever-increasing number of complex applications. The application source code can be written in assembly and C language, and the output code can be generated by the linker. The TMS370 family XDS development tools communicate through a standard RS-232-C interface with an existing personal computer. This allows the designer to use familiar personal-computer editors and software utilities. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as reduced time-to-market cycle.

The TMS370CxBx family together with the TMS370 family XDS/22, CDT370, starter kit, software tools, the SE370C758 reprogrammable device, comprehensive product documentation, and customer support provide a complete solution to the needs of the system designer.

modes

The TMS370CxBx has four operating modes, two basic modes with each mode having two memory configurations. The basic operating modes are the microcomputer and microprocessor modes, which are selected by the voltage level applied to the dedicated MC pin two cycles before the $\overline{\text{RESET}}$ pin goes inactive. The two memory configurations are then selected through software programming of the internal system configuration registers. The four operating modes are the microcomputer single chip, microcomputer with external expansion, microprocessor without internal program memory, and microprocessor with internal program memory. These modes are described in the following list.

- Microcomputer single chip mode:
 - Operates as a self-contained microcomputer with all memory and peripherals on chip
 - Maximizes the general-purpose I/O capability for real-time control applications
- Microcomputer with external expansion mode:
 - Supports bus expansion to external memory or peripherals, while all on-chip memory (RAM, ROM, and data EEPROM) remains active
 - Configures digital I/O ports (ports A, B, C, and D) through software, under control of the associated port control, to become external memory as follows:
 - Port A: 8-bit data memory
 - Port B and Port C: 16-bit address memory
 - Port D: 8-bit control memory (pin not used as function A or B can be configured as I/O)
 - Utilizes the pins available (not used for address, data, or control memory) as general-purpose input/output by programming them individually
 - Lowers the system cost by not requiring an external address/data latch (address memory and data memory are nonmultiplexed)
 - Reduces external interface decode logic by using the precoded chip-select outputs that provide direct memory/peripheral chip-select or chip-enable functions
 - Function A maps up to 112K bytes of external memory into the address space by using $\overline{\text{CSE1}}$, $\overline{\text{CSE2}}$, $\overline{\text{CSH1}}$, $\overline{\text{CSH2}}$, and $\overline{\text{CSH3}}$ as memory-bank selects under software control

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modes (continued)

- Function B maps up to 40K bytes of external memory into the address space by using $\overline{EDS}$ under software control
- Microprocessor without internal program memory mode:
 - Ports A, B, C, and D (these ports are not programmable) become the address, data, and control buses for interface to external memory and peripherals.
 - On-chip RAM and data EEPROM remain active, while the on-chip ROM is disabled.
 - Program area and the reset, interrupt, and trap vectors are located in off-chip memory locations.
- Microprocessor with internal program memory mode:
 - Configured as the microprocessor without internal program-memory mode with respect to the external bus interface
 - Application program in external memory enables the internal program ROM to be active in the system. (Writing a zero to the MEMORY DISABLED control bit (SCCR1.2) of the SCCR1 control register accomplishes this.)

memory/peripheral wait operation

The TMS370CxBx enhances interface flexibility by providing $\overline{WAIT}$ -state support, decoupling the cycle time of the CPU from the read/write access of the external memory or peripherals. External devices can extend the read/write accesses indefinitely by placing an active low on the $\overline{WAIT}$ input pin. The CPU continues to wait as long as $\overline{WAIT}$ remains active.

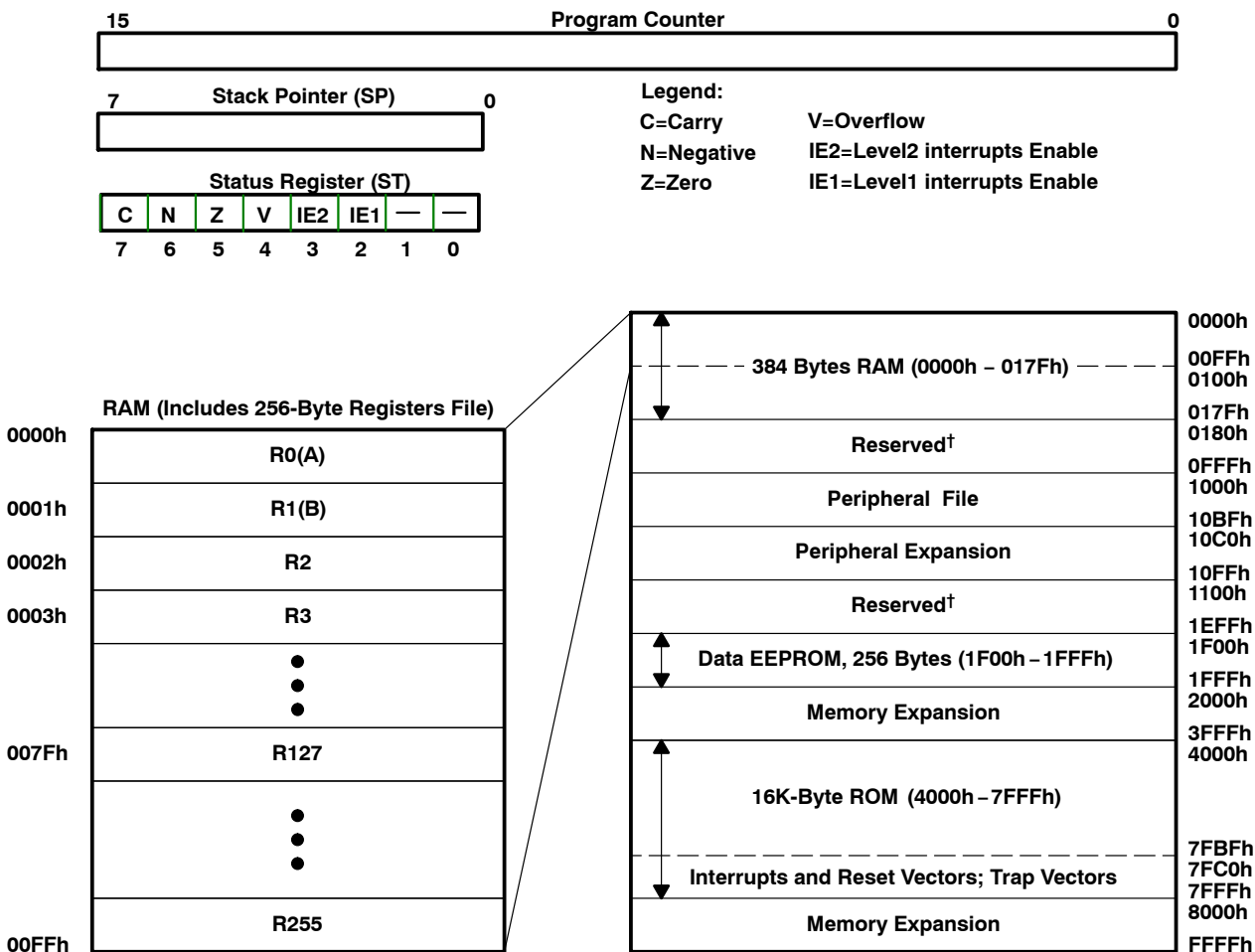
Programmable automatic wait-state generation is provided also by the TMS370CxBx on-chip bus controller. Following a hardware reset, the TMS370CxBx is configured to automatically add one wait state to all external bus transactions, and memory and peripheral accesses, making every external access a minimum of three system clock cycles. The designer can disable the automatic wait-state generation if the AUTOWAIT DISABLE bit in SCCR1 is set to 1. Also, all accesses to the upper four frames of the peripheral file can be extended independently to four system clock cycles if the PF AUTO WAIT bit in SCCR0 is set to 1. Programmable wait states can be used in conjunction with the external $\overline{WAIT}$ pin. In applications where the external device read/write access can interface with the TMS370CxBx CPU using one wait state, the automatic wait-state generation can eliminate external $\overline{WAIT}$ interface logic, lowering system cost.

central processing unit (CPU)

The CPU used on the TMS370CxBx device is the high-performance 8-bit TMS370 CPU module. The 'xBx implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'xBx instruction set is summarized in Table 17. Figure 1 illustrates the CPU registers and memory blocks.



central processing unit (CPU) (continued)



† Reserved means that the address space is reserved for future expansion.

Figure 1. Programmer's Model

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central processing unit (CPU) (continued)

The 'xBx CPU architecture provides the following components:

- CPU registers:
 - A stack pointer that points to the last entry in the memory stack
 - A status register that monitors the operation of the instructions and contains the global-interrupt-enable bits
 - A program counter (PC) that points to the memory location of the next instruction to be executed
- A memory map that includes:
 - 384 bytes of general-purpose RAM that can be used for data memory storage, program instructions, a general-purpose register, or the stack (can be located only in the first 256 bytes)
 - A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM programming control
 - A 256-byte EEPROM module that provides in-circuit programmability and data retention in power-off conditions
 - 16K bytes of ROM program memory

stack pointer (SP)

The SP is an 8-bit CPU register. The stack operates as a last-in, first-out, read/write memory and is typically used to store the return address on subroutine calls as well as the status register contents during interrupt sequences.

The SP points to the last entry or to the top of the stack. The SP increments automatically before data is pushed onto the stack and decrements after data is popped from the stack. The stack can be located only in the first 256 bytes of the on-chip RAM memory.

status register (ST)

The ST monitors the operation of the instructions and contains the global-interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits:

- The four status bits indicate the outcome of the previous instruction. Conditional instructions (for example, the conditional jump instructions) use these status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

The ST register and status bit notation are shown in Table 5.

Table 5. Status Register

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset



central processing unit (CPU) (continued)

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most-significant byte (MSbyte) and least-significant byte (LSbyte) of a 16-bit address.

The contents of the reset vector (7FFEh, 7FFFh) are loaded into the program counter during reset. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 4000h as the contents of memory locations 7FFEh and 7FFFh (reset vector).

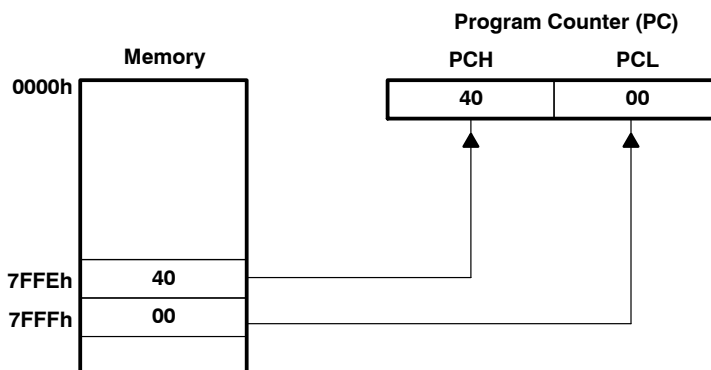


Figure 2. Program Counter After Reset

memory map

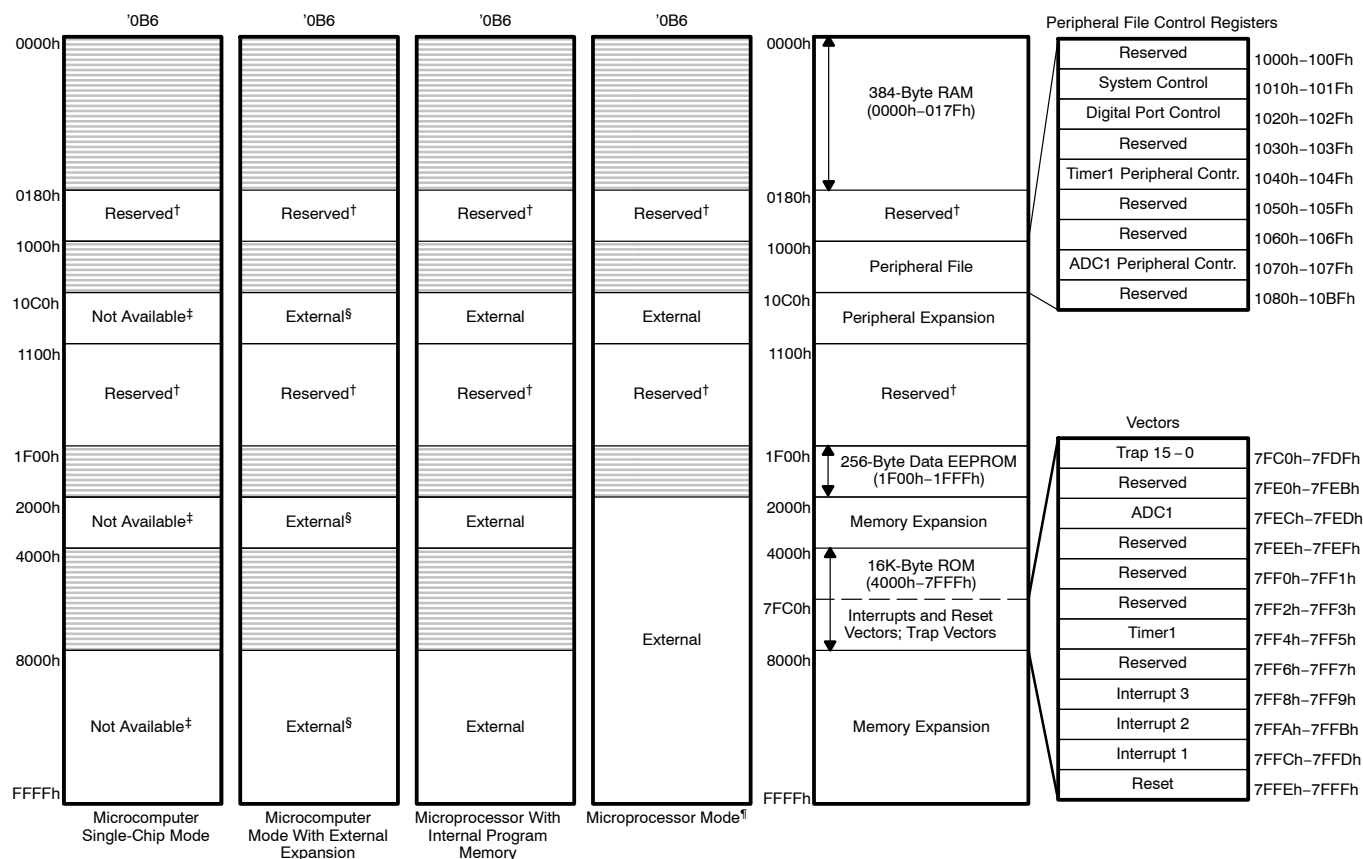
The TMS370CxBx architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. In the expansion mode, external memory peripherals are also memory-mapped into this common address. As shown in Figure 3, the TMS370CxBx provides a 16-bit address range to access internal or external RAM, ROM, data EEPROM, peripheral functions, and system-interrupt vectors.

The peripheral file contains all input/output port control, on- and off-chip peripheral status and control, EEPROM programming, and system-wide control functions. The peripheral file consists of 256 contiguous addresses located from 1000h to 10FFh. The 256 contiguous addresses are logically divided into 16 peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed. The TMS370CxBx has its on-chip peripherals and system control assigned to peripheral file frames 1 through 7, addresses 1010h through 107Fh.

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memory map (continued)



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[†] Reserved = the address space is reserved for future expansion.

[‡] Not available = address space is unavailable in the particular mode illustrated by that block.

[§] Precoded chip-select outputs available on external expansion bus.

[¶] Microprocessor mode is designed for ROMless device, ROM and EPROM devices also can be used in this mode but all on-chip memory is ignored.

Figure 3. TMS370CxBx Memory Map

RAM/register file (RF)

Locations within RAM address space can serve as either register file or general-purpose read/write memory, program memory, or stack instructions. The TMS370CxBx device contains 384 bytes of internal RAM mapped beginning at location 0000h and continuing through location 017Fh, as shown in Figure 3. The first 256 bytes of RAM (0000h – 00FFh) are the register files, R0 through R255.

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370CxBx control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the peripheral file (PF) directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or by P for a decimal designator. For example, the system control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 6 shows the TMS370CxBx peripheral files.

Table 6. TMS370CxBx Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h – 100Fh	P000 – P00F	Reserved for factory test
1010h – 101Fh	P010 – P01F	System and EEPROM/EPROM control registers
1020h – 102Fh	P020 – P02F	Digital I/O port control registers
1030h – 103Fh	P030 – P03F	Reserved
1040h – 104Fh	P040 – P04F	Timer 1 registers
1050h – 105Fh	P050 – P05F	Reserved
1060h – 106Fh	P060 – P06F	Reserved
1070h – 107Fh	P070 – P07F	Analog-to-digital converter 1 registers
1080h – 10BFh	P080 – P0BF	Reserved
10C0h – 10FFh	P0C0 – P0FF	External peripheral control

data EEPROM

The TMS370CxBx devices contain 256 bytes of data EEPROM beginning at location 1F00h, and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127), or the *TMS370 Family Data Manual* (SPNS014B). The data EEPROM features include the following:

- Programming:
 - Bit, byte, and block write/erase modes
 - Internal charge pump circuitry: No external EEPROM programming voltage supply is needed.
 - Control register: Data EEPROM programming is controlled by the data EEPROM control register (DEECTL) located in the PF frame beginning at location P01A.
 - In-circuit programming capability: There is no need to remove the device to program.
- Write-protection: Writes to the data EEPROM are disabled during the following conditions:
 - Reset: All programming of the data EEPROM module is halted.
 - Write protection active: there is one write-protect bit per 32-byte EEPROM block.
 - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 7 shows the memory map of the control registers.

Table 7. Data EEPROM Control Register Memory Map

ADDRESS	SYMBOL	NAME
101Ah (P01A)	DEECTL	Data EEPROM control register

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program ROM

The program ROM consists of 16K bytes of mask-programmable ROM. The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication. Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments (TI™), and addresses 7FECh through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh.

system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370CxBx CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are internally generated, while one ($\overline{\text{RESET}}$) is controlled externally. These actions are as follows:

- External $\overline{\text{RESET}}$ pin. A low level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle (it is possible, however, that a signal of less than one SYSCLK could cause a reset). See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.
- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside of the recommended operating range. See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'xBx device to reset external system components. Additionally, if a cold-start condition (V_{CC} is off for several hundred milliseconds), oscillator failure occurs, or $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator fault flag (OSC FLT FLAG, SCCR0.4), the cold start flag (COLD START, SCCR0.7), and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 8 depicts the reset sources.

Table 8. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT NAME	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Registers A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to by the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state. During $\overline{\text{RESET}}$ the two basic operating modes, which are the

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system reset (continued)

microcomputer and microprocessor modes, can be selected by applying the desired voltage level to the dedicated MC pin two cycles before $\overline{\text{RESET}}$ goes inactive (refer to the operating modes description).

$\overline{\text{RESET}}$ must be held low until the clock signal is valid and V_{CC1} is within the operating range, when an external reset circuit is connected to $\overline{\text{RESET}}$. Figure 4 shows a typical reset circuit.

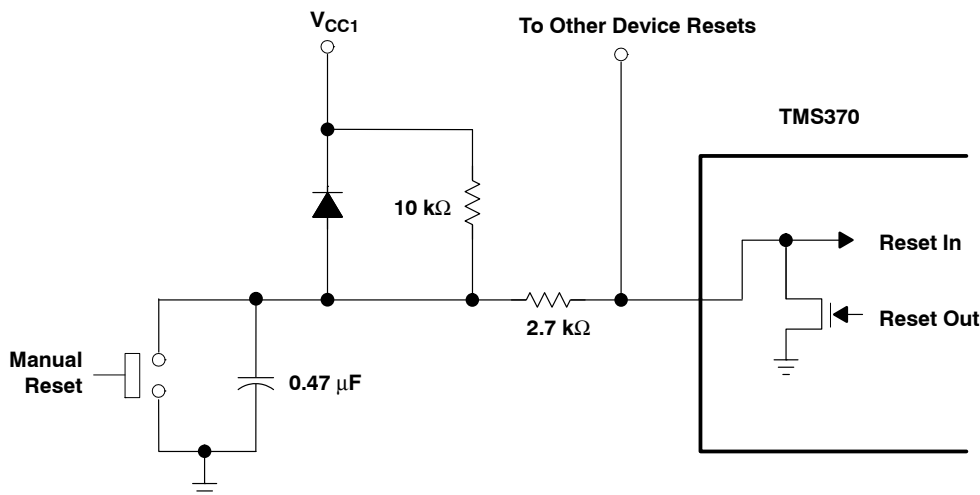


Figure 4. Typical Reset Circuit

interrupts

The TMS370 family software programmable interrupt structure permits flexible on-chip and external-interrupt configurations to meet real-time interrupt-driven application requirements. The hardware-interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global-interrupt mask bits (IE1 and IE2) of the status register.

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is configured selectively on either the high- or low-priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370CxBx has five hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 9. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. All of the interrupt sources are individually maskable by local interrupt-enable control bits in the associated PF. Each interrupt source FLAG bit is individually readable for software polling or determining which interrupt source generated the associated system interrupt. The interrupt control block diagram is illustrated in Figure 5.

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interrupts (continued)

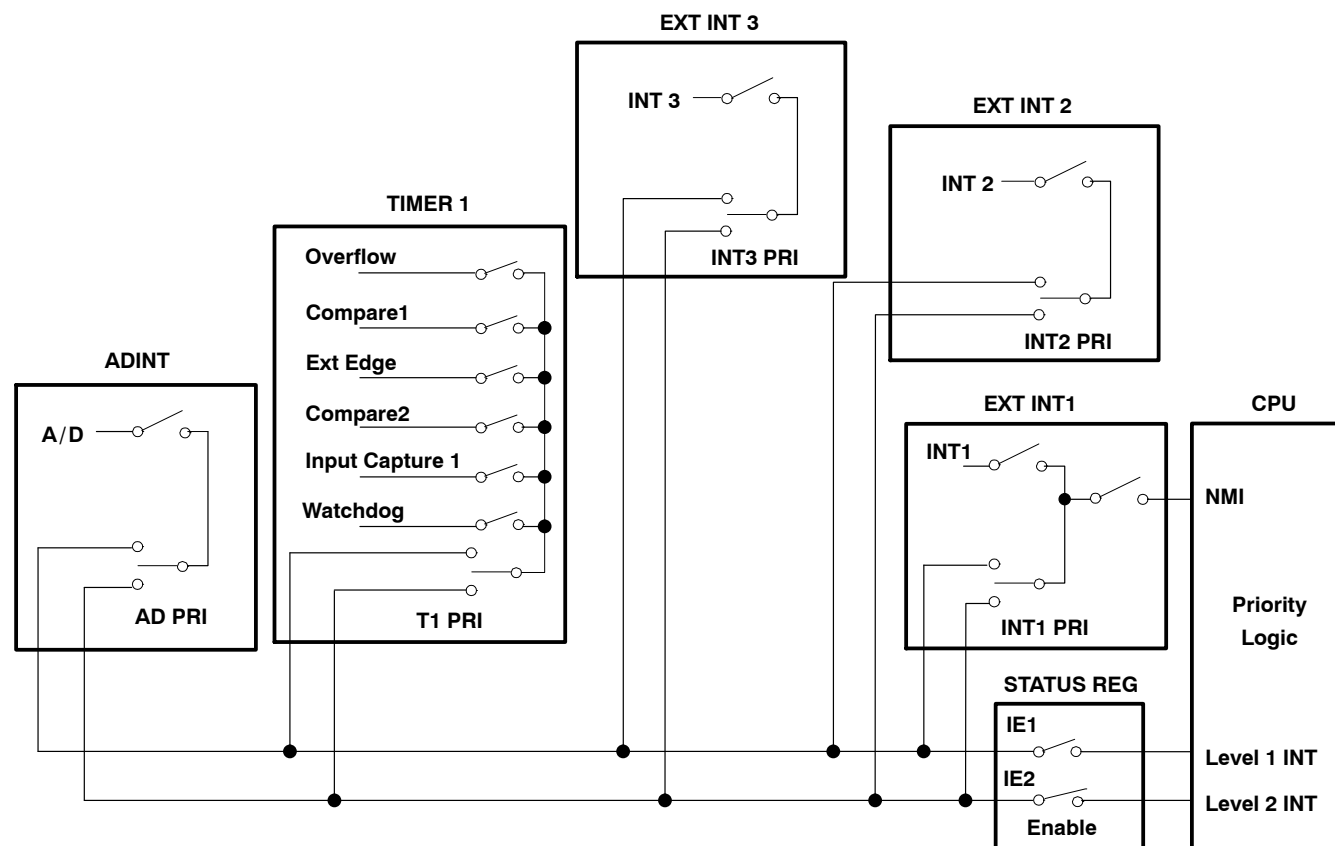


Figure 5. Interrupt Control

Of the five system interrupts, two are generated by on-chip peripherals (T1INT and ADINT) and three are external interrupts (INT1 – INT3). Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in PF frame 1.

Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual- or global-enable mask bits. The INT1 NMI bit is protected during non-privileged operation and therefore should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software configured as general-purpose input/output pins if the interrupt function is not required (INT1 can be similarly configured as an input pin). Table 9 shows the interrupt vector sources, corresponding addresses, and hardware priorities.

interrupts (continued)

Table 9. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY [†]
External RESET Watchdog overflow Oscillator fault detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	RESET [‡]	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1 [‡]	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2 [‡]	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3 [‡]	7FF8h, 7FF9h	4
Timer 1 overflow Timer 1 compare 1 Timer 1 compare 2 Timer 1 external edge Timer 1 input capture 1 Watchdog overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT [§]	7FF4h, 7FF5h	5
A/D conversion complete	AD INT FLAG	ADINT	7FECh, 7FEDh	6

[†] Relative priority within an interrupt level.

[‡] Releases microcontroller from STANDBY and HALT low-power modes.

[§] Releases microcontroller from STANDBY low-power mode.

privileged operation and EEPROM write-protection override

The TMS370CxBx family has significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a broad variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370CxBx operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) should be set to 1 to enter the nonprivileged mode, thus disabling write operations to specific configuration control bits within the peripheral file. Table 10 displays the system configuration bits that are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

Table 10. Privileged Bits

REGISTER [¶]		CONTROL BIT
NAME	LOCATION	
SCCRO	P010.5 P010.6	PF AUTOWAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST
ADPRI	P07F.5 P07F.6 P07F.7	AD ESPEN AD PRIORITY AD STEST

[¶] The privileged bits are shown in a bold typeface in Table 12.

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privileged operation and EEPROM write-protection override (continued)

The write-protect-override (WPO) mode provides an external hardware method of overriding the write-protection registers of data EEPROM on the TMS370CxBx. Applying a 12-V input to the MC pin after the **RESET** input goes high (logic 1) enters the WPO mode. The high voltage on MC during the WPO mode is not the programming voltage for the data EEPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware system level capability to modify the content of the data EEPROM while the device remains in the application but only while requiring a 12-V external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power and IDLE modes

The TMS370C0B6 device has two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time the mask is manufactured.

The STANDBY and HALT low power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the idle instruction when the PWRDWN/IDLE bit in register SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls which low-power mode is entered.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, and timer 1 remain active. System processing is suspended until a qualified interrupt (hardware **RESET**, external interrupt on INT1, INT2, INT3, or Timer 1 interrupt) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370C0B6 is placed in its lowest power-consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware **RESET** or an external interrupt on INT1, INT2, INT3) is detected. The low-power mode selection bits are summarized in Table 11.

Table 11. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X	IDLE

X = don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6–7 bits is ignored. In addition, if an IDLE instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method of always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI always is generated, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the watchdog timer is inhibited.

clock modules

The '370CxBx family provides two clock options which are referred to as divide-by-1 (PLL) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The '370CxBx ROM-masked devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on the ROM device.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a 1-to-1 match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency. The divide-by-4 produces a SYSCLK which is one-fourth the frequency of the external resonator. Inside the divide-by-1 module, the frequency of the external resonator is multiplied by four. The clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. The frequencies are formulated as follows:

$$\text{Divide-by-4 option : SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option : SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the reduction of EMI. The harmonics of low-speed resonators extend through less of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 provides the capability of reducing the resonator speed by four times, and this results in a steeper decay of emissions produced by the oscillator.

system configuration registers

Table 12 contains system configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in a bold typeface and shaded.

Table 12. Peripheral File Frame 1: System Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTOWAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B to P01F	Reserved								

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digital port control registers

Peripheral file frames 2 and 3 contain the digital I/O pin configuration and control registers. Table 13 displays the specific addresses, registers, and control bits within this peripheral file frame.

Table 13. Peripheral File Frames 2 and 3: Digital Port Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P020	Reserved								APOINT1
P021	Port A Control Register 2								APOINT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPOINT1
P025	Port B Control Register 2								BPOINT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPOINT1
P029	Port C Control Register 2								CPOINT2
P02A	Port C Data								CDATA
P02B	Port C Direction								CDIR
P02C	Port D Control Register 1								DPOINT1
P02D	Port D Control Register 2†								DPOINT2
P02E	Port D Data								DDATA
P02F	Port D Direction								DDIR
P030 to P035	Reserved								
P036	Port G Data								GDATA
P037	Port G Direction								GDIR
P038	Reserved								
P039	Reserved								
P03A	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Port H Data	HDATA
P03B	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Port H Direction	HDIR

† To configure pin D3 as SYSCLK, set port D control register 2 = 08h.



digital port control registers (continued)

Table 14. Port Configuration Register Setup

PORT	PIN	INPUT	OUTPUT	FUNCTION A	FUNCTION B (μ P MODE)
		XPORT1 = 0 [†] XPORT2 = 0 XDATA = y XDIR = 0	XPORT1 = 0 [†] XPORT2 = 0 XDATA = q XDIR = 1	XPORT1 = 0 [†] XPORT2 = 1 XDATA = x XDIR = x	XPORT1 = 1 [†] XPORT2 = 1 XDATA = x XDIR = x
A	0–7	Data In y	Data Out q	Data Bus	Reserved
B	0–7	Data In y	Data Out q	Low ADDR	Reserved
C	0–7	Data In y	Data Out q	Hi ADDR	Reserved
D	0	Data In y	Data Out q	$\overline{\text{CSE2}}$	$\overline{\text{OCF}}$
	1			$\overline{\text{CSH3}}$	—
	2			$\overline{\text{CSH2}}$	—
	3			SYSCLK	SYSCLK
	4			R/W	R/W
	5			$\overline{\text{CSPF}}$	—
	6			$\overline{\text{CSH1}}$	$\overline{\text{EDS}}$
	7			$\overline{\text{CSE1}}$	WAIT
G	0–7	Data In y	Data Out q	Reserved	Reserved
H	0	Data In y	Data Out q	Reserved	Reserved
XPORT1 = 1 XPORT2 = 0 XDATA = x XDIR = x } Not defined					

[†] DPORT only

timer 1 module

The programmable timer 1 (T1) module of the TMS370CxBx provides the designer with the enhanced timer resources required to perform real-time system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers, T1 and WD, allow program selection of input clock sources (real-time, external event, or pulse-accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The T1 module includes three external device pins that can be used for multiple counter functions (operation-mode dependent) or used as general-purpose I/O pins. T1 module is shown in Figure 6.

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timer 1 module (continued)

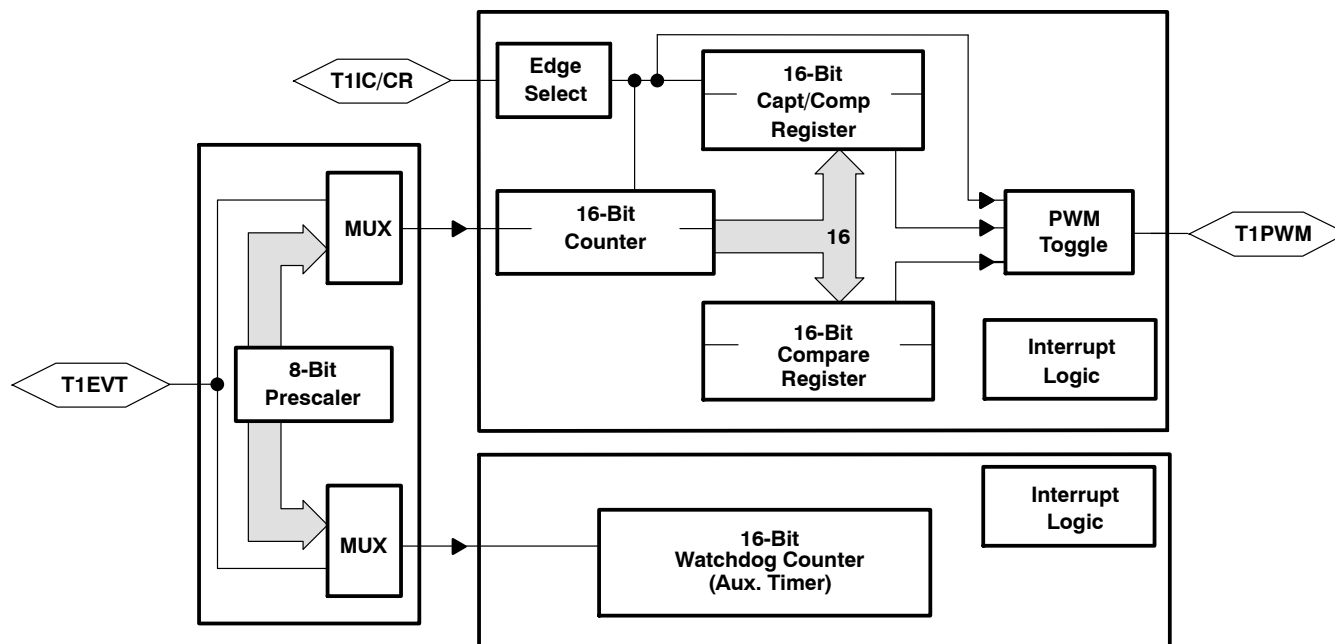


Figure 6. Timer 1 Block Diagram

- Three T1 I/O pins:
 - T1IC/CR: Timer 1 input capture / counter reset input pin, or general-purpose bidirectional I/O pin
 - T1PWM: Timer 1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T1EVT: Timer 1 event input pin, or general-purpose bidirectional I/O pin
- Two operational modes:
 - Dual-compare mode: provides PWM signal
 - Capture/compare mode: provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register.
- One 16-bit watchdog counter that can be used as an event counter, a pulse accumulator, or an interval timer if watchdog feature is not needed.
- Prescaler/clock sources that determines one of eight clock sources for general-purpose timer
- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR).

timer 1 module (continued)

- Interrupts that can be generated on the occurrence of:
 - A capture
 - A compare equal
 - A counter overflow
 - An external edge detection
- Sixteen T1 module control registers: Located in the PF frame beginning at address P040.

Table 15 shows the T1 module control register.

Table 15. Timer 1 Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Modes: Capture/Compare and Dual-Compare									
P040	T1 Counter MSbyte							Bit 8	T1CNTR
P041	T1 Counter LSbyte							Bit 0	
P042	Compare Register MSbyte							Bit 8	T1C
P043	Compare Register LSbyte							Bit 0	
P044	Capture/Compare Register MSbyte							Bit 8	T1CC
P045	Capture/Compare Register LSbyte							Bit 0	
P046	Watchdog Counter MSbyte							Bit 8	WDCNTR
P047	Watchdog Counter LSbyte							Bit 0	
P048	Watchdog Reset Key							Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Capture/Compare and Dual-Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

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timer 1 module (continued)

The T1 capture/compare mode block diagram is illustrated in Figure 7. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

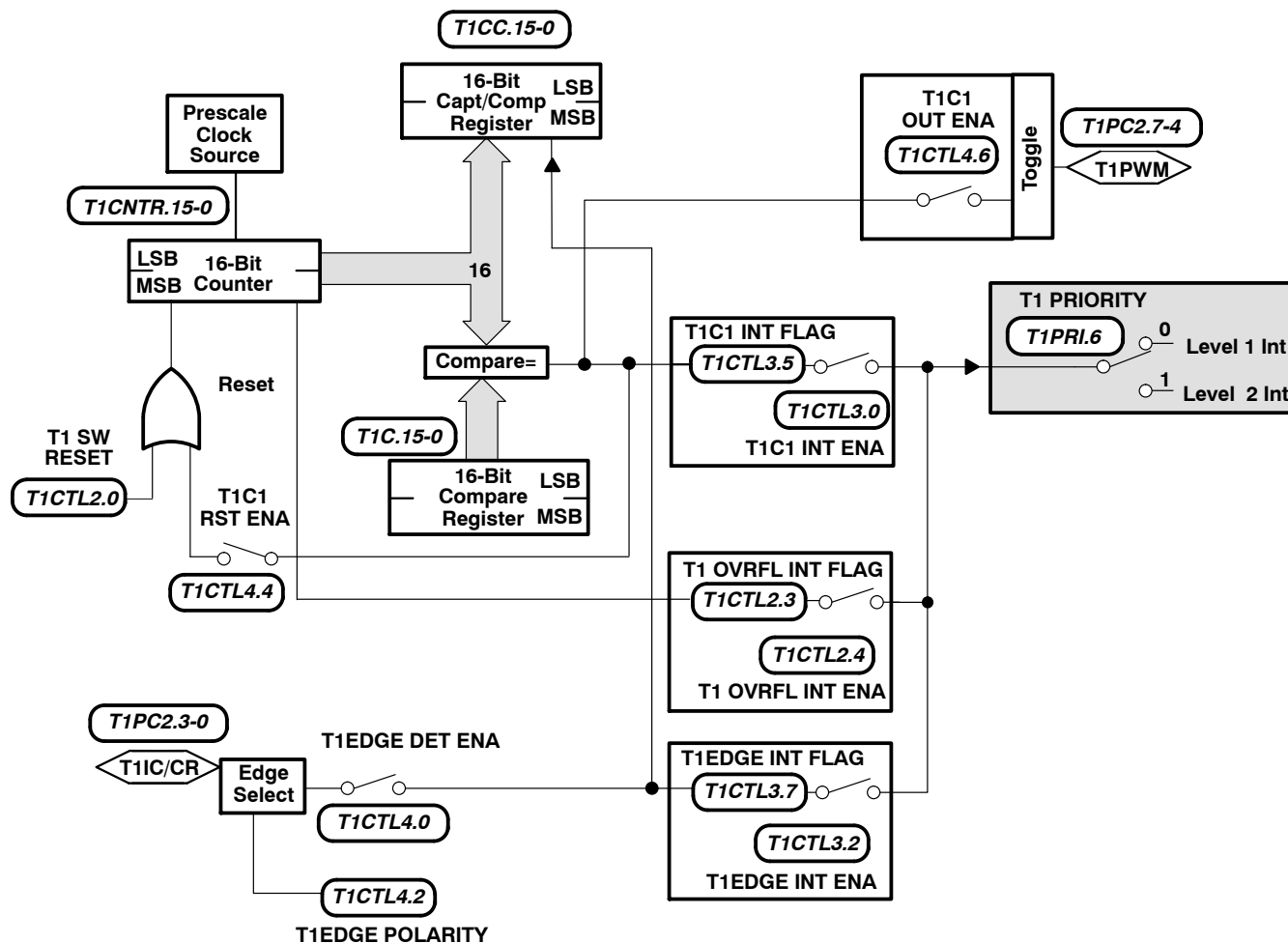


Figure 7. Capture/Compare Mode

timer 1 module (continued)

The T1 dual-compare mode block diagram is illustrated in Figure 8. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

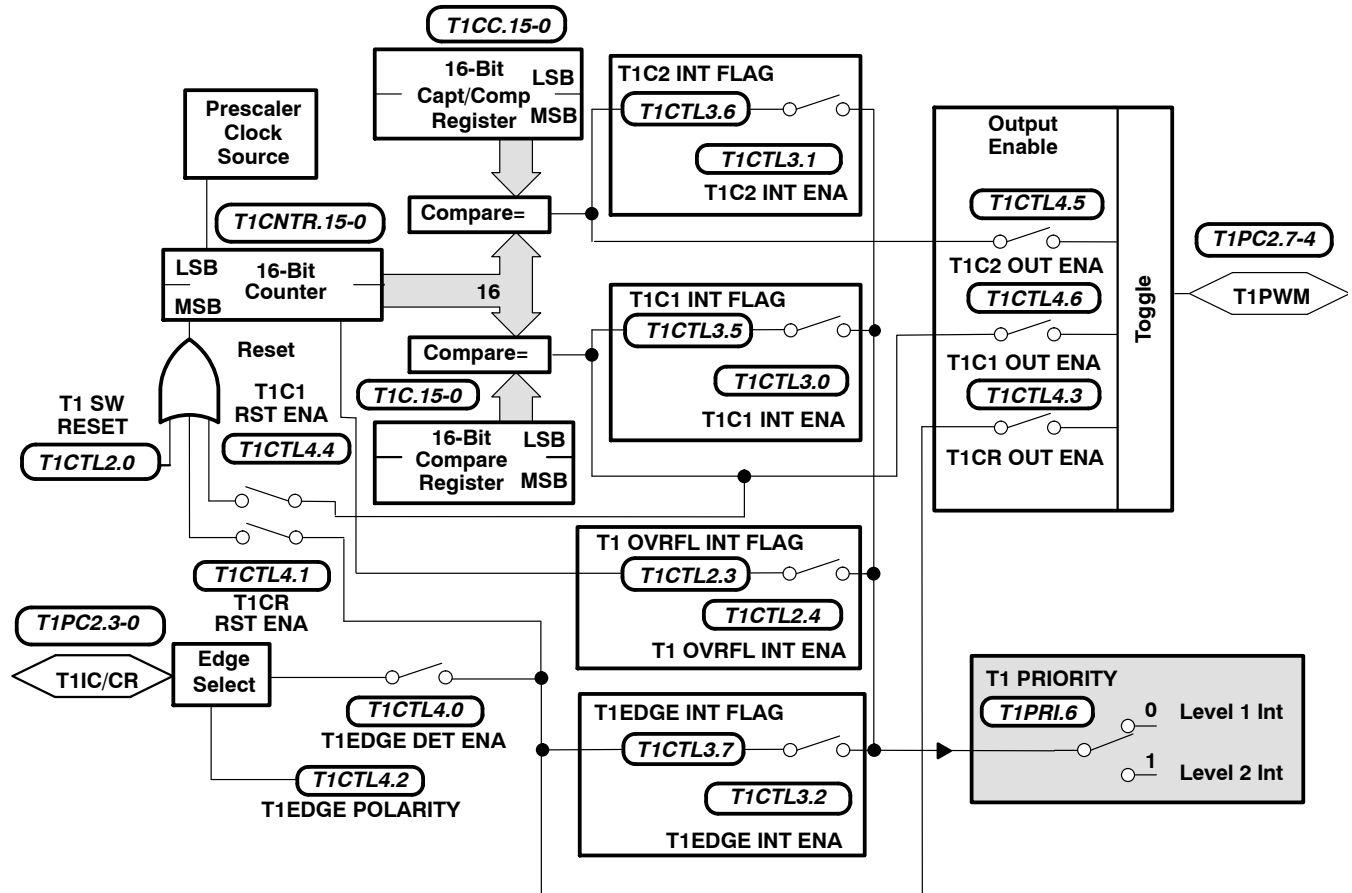


Figure 8. Dual-Compare Mode

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timer 1 module (continued)

The TMS370CxBx device includes a 24-bit watchdog (WD) timer, contained in the T1 module, which can be software programmed as an event counter, pulse accumulator, or interval timer if the WD function is not used. The WD function is to monitor software and hardware operation, and it implements a system reset when the WD counter is not serviced properly (WD counter overflow or WD counter is reinitialized by an incorrect value). The WD can be configured as one of the three mask options: standard WD, hard WD, or simple counter.

- Standard watchdog configuration for mask-ROM devices only (see Figure 9)
 - Watchdog mode
 - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the WD reset key or if the counter overflows
 - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
 - Non-watchdog mode
 - Watchdog timer can be configured as an event counter, pulse accumulator, or an interval timer

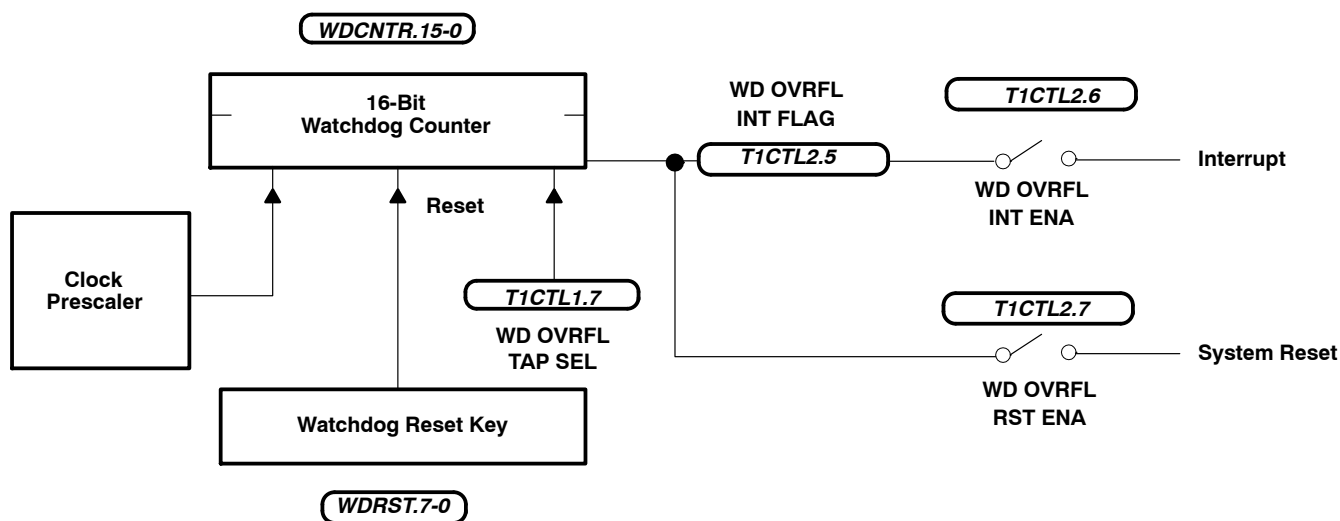


Figure 9. Standard Watchdog

timer 1 module (continued)

- Hard watchdog configuration for mask-ROM device only (see Figure 10)
 - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows
 - Automatic activation of the WD timer upon power-up reset
 - INT1 is enabled as nonmaskable interrupt during low-power modes
 - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset

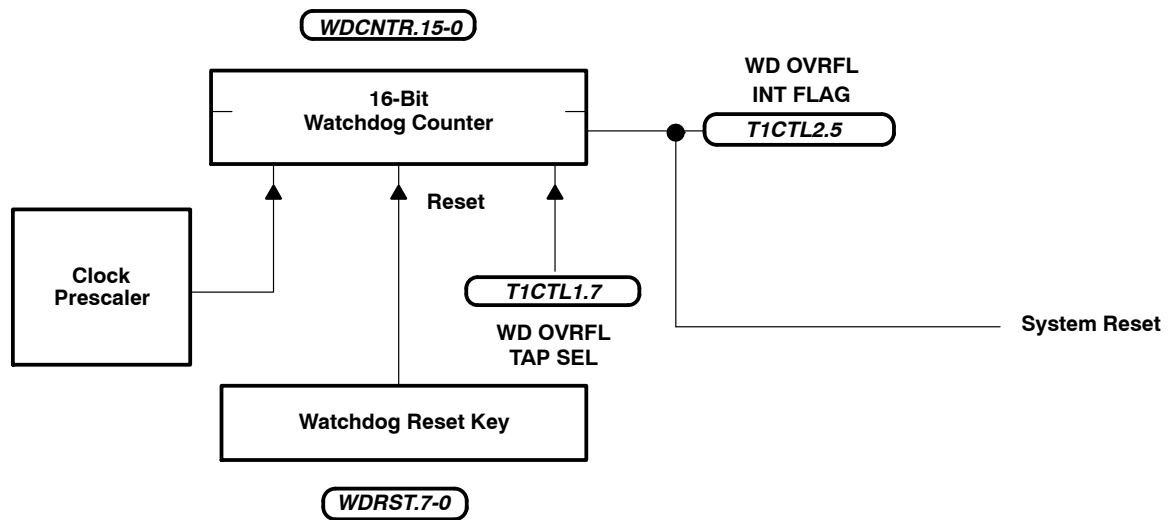


Figure 10. Hard Watchdog

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timer 1 module (continued)

- Simple-counter configuration for mask-ROM devices only (see Figure 11)
 - Simple counter can be configured as an event counter, pulse accumulator, or an interval timer.

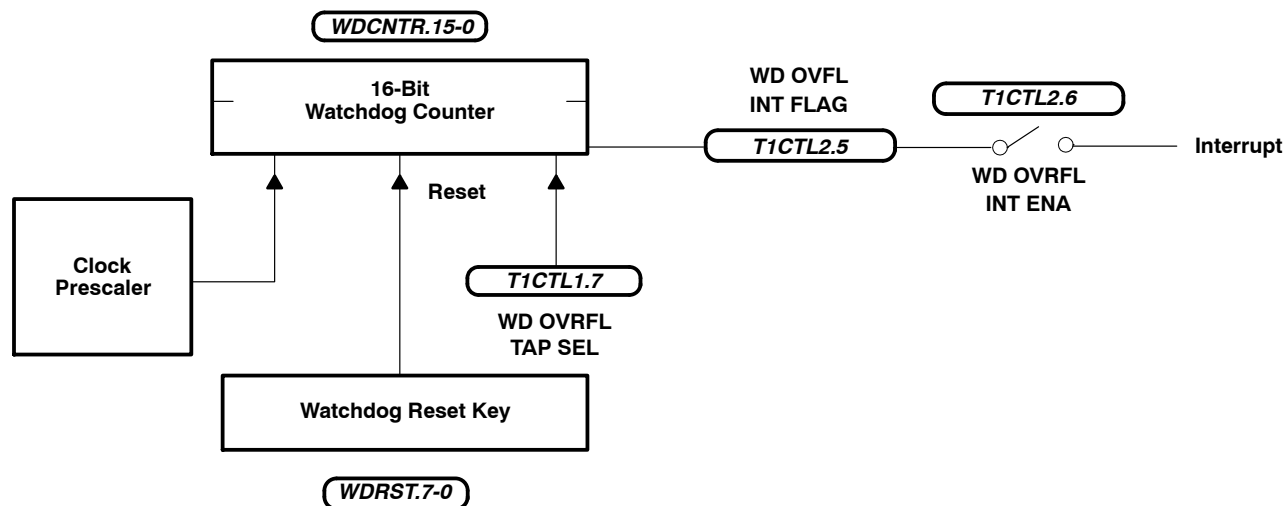


Figure 11. Simple Counter

analog-to-digital converter 1 (ADC1) module

The analog-to-digital converter 1 (ADC1) module is an 8-bit, successive approximation converter with internal sample-and-hold circuitry. The module has eight multiplexed analog input channels that allow the processor to convert the voltage levels from up to eight different sources. The ADC1 module features include the following:

- Minimum conversion time: 32.8 μ s at 5-MHz SYSCLK
- Ten external pins:
 - Eight analog input channels (AN0–AN7), any of which can be software configured as digital inputs (E0–E7) if not needed as analog channels. AN1–AN7 can also be configured as positive input voltage reference.
 - V_{CC3}: ADC1 module high-voltage reference input
 - V_{SS3}: ADC1 module low-voltage reference input
- The ADDATA register, which contains the digital result of the last A/D conversion
- ADC1 operations can be accomplished through either interrupt driven or polled algorithms.
- Six ADC1 module control registers are located in the control register frame beginning at address 1070h.

analog-to-digital converter 1 (ADC1) module (continued)

The ADC1 module control registers are illustrated in Table 16.

Table 16. ADC1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A-to-D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI

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analog-to-digital converter 1 (ADC1) module (continued)

The ADC1 module block diagram is illustrated in Figure 12.

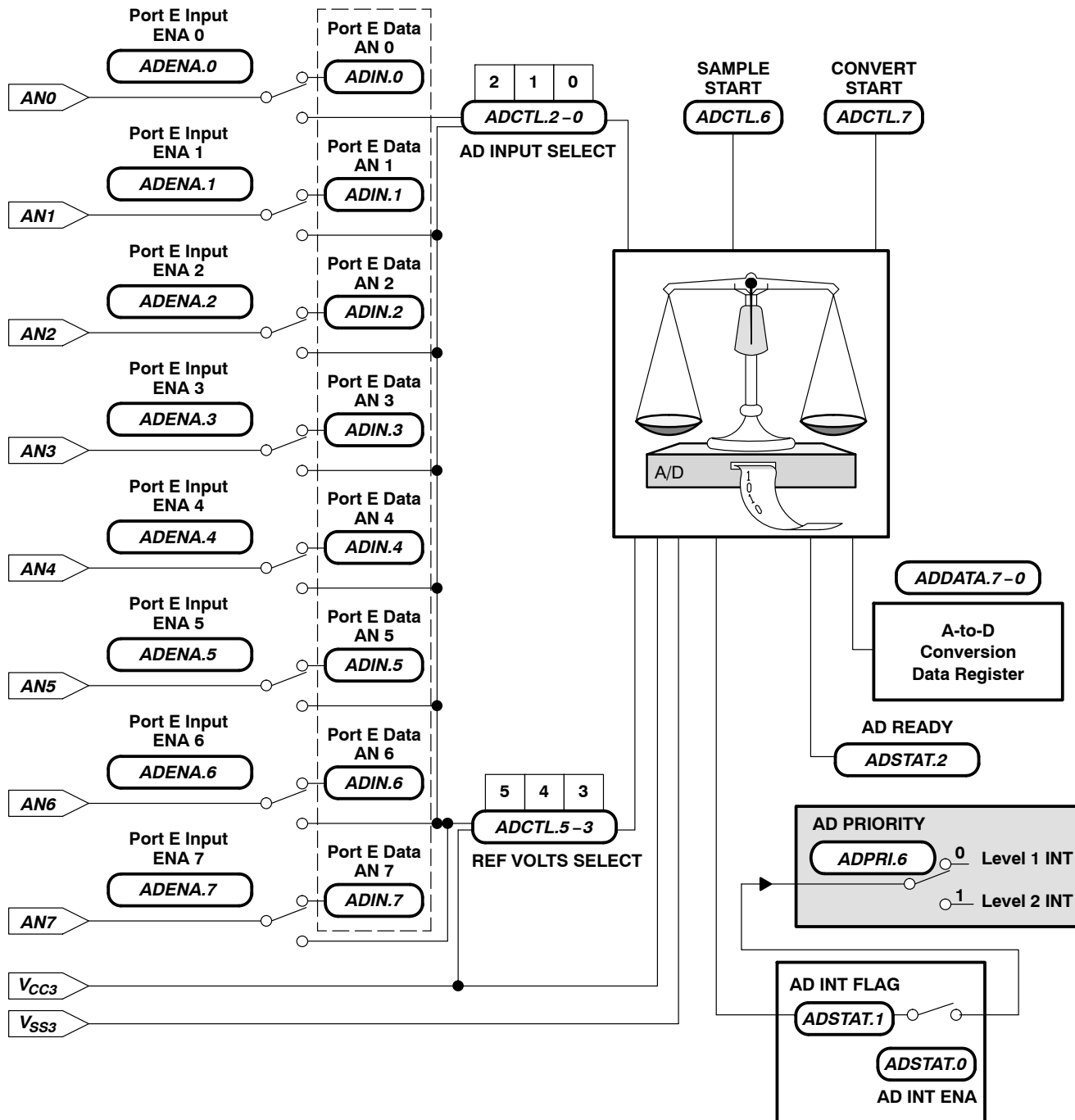


Figure 12. ADC1 Block Diagram

instruction set overview

Table 17 provides an opcode-to-instruction cross-reference of all 73 instructions and 274 opcodes of the '370CxBx instruction set. The numbers at the top of this table represent the most significant nibble (MSN) of the opcode while the numbers at the left side of the table represent the least significant nibble (LSN). The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

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Table 17. TMS370 Family Opcode/Instruction Map[†]

		MSN																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	L	JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8				CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
		JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7	
2	S	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10		DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7
		JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8	
4	N	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes	
		JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14		
6	Z	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6	
		JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10	
8	N	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7	
		JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9	
A	B	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12	
		JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8	

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

Table 17. TMS370 Family Opcode/Instruction Map[†] (Continued)

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L S N	C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
	D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
	E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
	F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):

F4	8	MOVW *n[Rn] 4/15	DIV Rn,A 3/14-63
F4	9	JMPL *n[Rn] 4/16	
F4	A	MOV *n[Rn],A 4/17	
F4	B	MOV A,*n[Rn] 4/16	
F4	C	BR *n[Rn] 4/16	
F4	D	CMP *n[Rn],A 4/18	
F4	E	CALL *n[Rn] 4/20	
F4	F	CALLR *n[Rn] 4/22	

Legend:

* = Indirect addressing operand prefix
 & = Direct addressing operand prefix
 # = immediate operand
 #16 = immediate 16-bit number
 lab = 16-label
 n = immediate 8-bit number
 Pd = Peripheral register containing destination type
 Pn = Peripheral register
 Ps = Peripheral register containing source byte
 ra = Relative address
 Rd = Register containing destination type
 Rn = Register file
 Rp = Register pair
 Rpd = Destination register pair
 Rps = Source Register pair
 Rs = Register containing source byte

[†] All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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development system support

The TMS370 family development support tools include an assembler, a C compiler, a linker, an in-circuit emulator (XDS/22), CDT, and an EEPROM/UVEEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
 - Includes extensive macro capability
 - Provides high-speed operation
 - Provides format conversion utilities for popular formats
- ANSI C compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, Sun-3™, or Sun-4™)
 - Generates assembly code for the TMS370 that can be easily inspected
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables direct referencing of the TMS370's port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (compact development tool) Timer real-time in-circuit emulation
 - Base (Part Number EDSCDT370T – for PC, requires cable)
 - Cable for 68-pin PLCC (Part No. EDSTRG68PLCC)
 - Cable for 64-pin SDIP (Part No. EDSTRG64SDIL)
 - Includes EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Uploads/downloads program and data memory
 - Executes programs and software routines
 - Includes 1 024 samples trace buffer
 - Includes single-step executable instructions
 - Uses software breakpoints to halt program execution at selected address
- Microcontroller programmer
 - Base (Part No. TMDS3760500A — for PC, requires programmer head)
 - Single unit head for 68-pin PLCC (Part No. TMDS3780510A)
 - Single unit head for 64-pin SDIP (Part No. TMDS3780511A)
 - Includes PC-based, window/function-key oriented user interface for ease of use and rapid learning environment

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development system support (continued)

- Starter Kit (Part No. TMDX37000 — for PC)
 - Includes TMS370 assembler diskette and documentation
 - Includes TMS370 simulator
 - Includes programming adapter board and programming software
 - Not included (to be supplied by the user):
 - + 5 V power supply
 - ZIF sockets
 - 9-pin RS232 cable

device numbering conventions

Figure 13 illustrates the numbering and symbol nomenclature for the TMS370CxBx family.

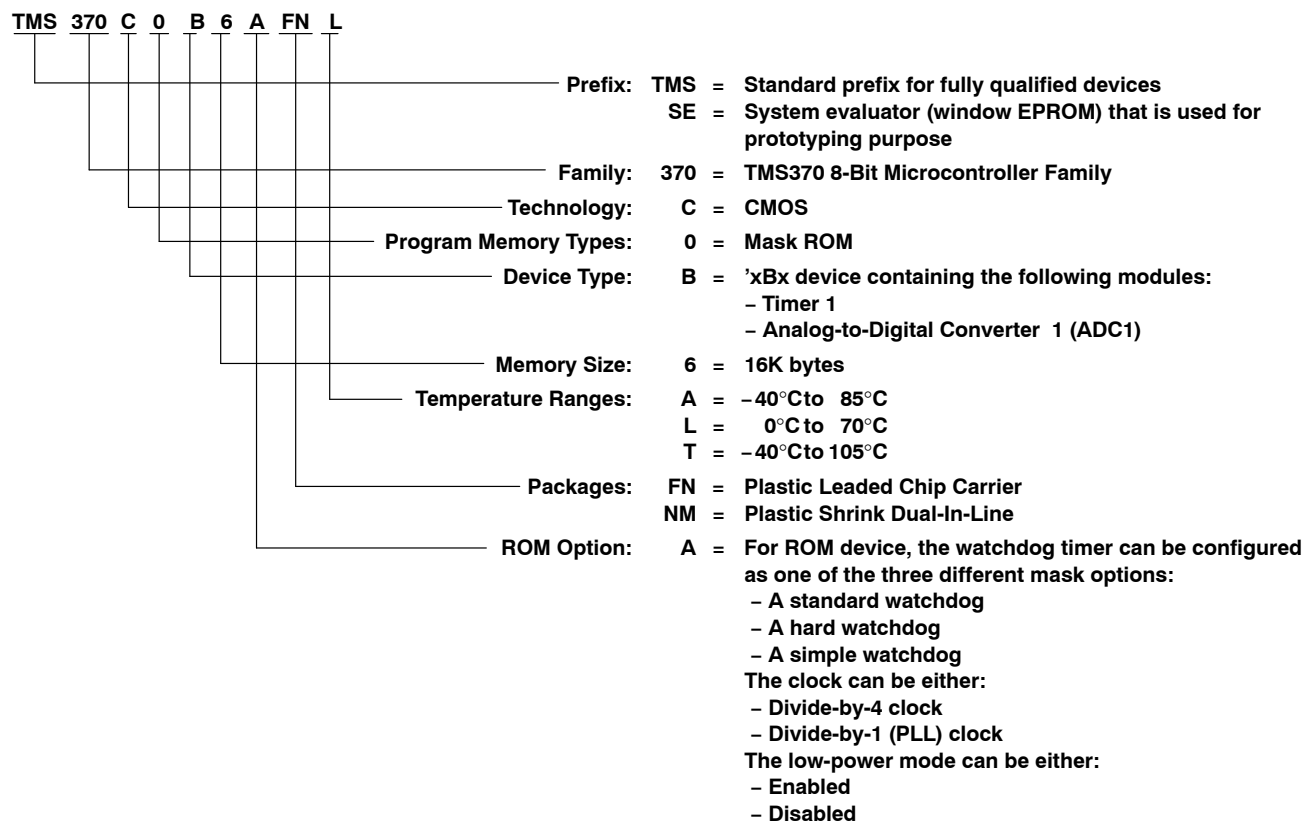


Figure 13. TMS370CxBx Family Nomenclature

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device part numbers

Table 18 provides a listing of all the TMS370CxBx devices available. The device part-number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog-timer options desired. Each device can only have one of the three possible watchdog-timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 18. Device Part Numbers

DEVICE PART NUMBERS FOR 68 PINS (PLCC)	DEVICE PART NUMBERS FOR 64 PINS (PSDIP)
TMS370C0B6AFNA TMS370C0B6AFNL TMS370C0B6AFNT	TMS370C0B6ANMA TMS370C0B6ANML TMS370C0B6ANMT

new code release form

Figure 14 shows a sample of the new code release form.

NEW CODE RELEASE FORM TEXAS INSTRUMENTS TMS370 MICROCONTROLLER PRODUCTS		DATE: _____																												
To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information:																														
1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media) 2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.																														
Company Name: _____ Street Address: _____ Street Address: _____ City: _____ State _____ Zip _____ Customer Part Number: _____ Customer Application: _____		Contact Mr./Ms.: _____ Phone: (_____) _____ Ext.: _____ Customer Purchase Order Number: _____ Customer Print Number *Yes: _____ # _____ No: _____ (Std. spec to be followed) *If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.																												
TMS370 Device: _____ TI Customer ROM Number: _____ (provided by Texas Instruments) OSCILLATOR FREQUENCY <table border="0" style="width: 100%;"> <tr> <td style="width: 30%;"></td> <td style="width: 10%; text-align: center;">MIN</td> <td style="width: 10%; text-align: center;">TYP</td> <td style="width: 10%; text-align: center;">MAX</td> </tr> <tr> <td>☐ External Drive (CLKIN)</td> <td>_____</td> <td>_____</td> <td>_____</td> </tr> <tr> <td>☐ Crystal</td> <td>_____</td> <td>_____</td> <td>_____</td> </tr> <tr> <td>☐ Ceramic Resonator</td> <td>_____</td> <td>_____</td> <td>_____</td> </tr> </table> ☐ Supply Voltage MIN: _____ MAX: _____ (std range: 4.5V to 5.5V)			MIN	TYP	MAX	☐ External Drive (CLKIN)	_____	_____	_____	☐ Crystal	_____	_____	_____	☐ Ceramic Resonator	_____	_____	_____	CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS <table border="0" style="width: 100%;"> <tr> <td style="width: 33%;">Low Power Modes</td> <td style="width: 33%;">Watchdog counter</td> <td style="width: 33%;">Clock Type</td> </tr> <tr> <td>☐ Enabled</td> <td>☐ Standard</td> <td>☐ Standard (/4)</td> </tr> <tr> <td>☐ Disabled</td> <td>☐ Hard Enabled</td> <td>☐ PLL (/1)</td> </tr> <tr> <td></td> <td>☐ Simple Counter</td> <td></td> </tr> </table> NOTE: Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the <i>TMS370 Family User's Guide</i> (literature number SPNU127) or the <i>TMS370 Family Data Manual</i> (literature number SPNS014B).	Low Power Modes	Watchdog counter	Clock Type	☐ Enabled	☐ Standard	☐ Standard (/4)	☐ Disabled	☐ Hard Enabled	☐ PLL (/1)		☐ Simple Counter	
	MIN	TYP	MAX																											
☐ External Drive (CLKIN)	_____	_____	_____																											
☐ Crystal	_____	_____	_____																											
☐ Ceramic Resonator	_____	_____	_____																											
Low Power Modes	Watchdog counter	Clock Type																												
☐ Enabled	☐ Standard	☐ Standard (/4)																												
☐ Disabled	☐ Hard Enabled	☐ PLL (/1)																												
	☐ Simple Counter																													
TEMPERATURE RANGE ☐ 'L': 0° to 70°C (standard) ☐ 'A': -40° to 85°C ☐ 'T': -40° to 105°C		PACKAGE TYPE <table border="0" style="width: 100%;"> <tr> <td>☐ 'N' 28-pin PDIP</td> <td>☐ "FN" 44-pin PLCC</td> </tr> <tr> <td>☐ "FN" 28-pin PLCC</td> <td>☐ "FN" 68-pin PLCC</td> </tr> <tr> <td>☐ "N" 40-pin PDIP</td> <td>☐ "NM" 64-pin PSDIP</td> </tr> <tr> <td>☐ "NJ" 40-pin PSDIP (formerly known as N2)</td> <td></td> </tr> </table> BUS EXPANSION ☐ YES ☐ NO	☐ 'N' 28-pin PDIP	☐ "FN" 44-pin PLCC	☐ "FN" 28-pin PLCC	☐ "FN" 68-pin PLCC	☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP	☐ "NJ" 40-pin PSDIP (formerly known as N2)																					
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☐ "N" 40-pin PDIP	☐ "NM" 64-pin PSDIP																													
☐ "NJ" 40-pin PSDIP (formerly known as N2)																														
SYMBOLIZATION ☐ TI standard symbolization ☐ TI standard w/customer part number ☐ Customer symbolization (per attached spec, subject to approval)																														
NON-STANDARD SPECIFICATIONS: ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.																														
RELEASE AUTHORIZATION: This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cyclotime commences when this document is signed off and the verification code is approved by the customer.																														
1. Customer: _____ Date: _____		2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____																												

Figure 14. Sample New Code Release Form

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range V_{CC1} , V_{CC2} , V_{CC3} (see Note 1)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC1}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC1}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC1}) [‡]	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	1 W
Operating free-air temperature range, T_A : L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

NOTE 1: Unless otherwise noted, all voltage values are with respect to V_{SS1} . $V_{CC1} = V_{CC}$.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage (see Note 1)	4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)	3		5.5	
V_{CC2}	Digital I/O supply voltage (see Note 1)	4.5	5	5.5	V
V_{CC3}	Analog supply voltage (see Note 1)	4.5	5	5.5	
V_{SS2}	Digital I/O supply ground	–0.3	0	0.3	V
V_{SS3}	Analog supply ground	–0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC		V_{SS1}	V
		MC, normal operation		V_{SS1}	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET		2	V
		MC (non-WPO mode)		$V_{CC1} - 0.3$	
		XTAL2/CLKIN		$0.8 V_{CC1}$	
		RESET		$0.7 V_{CC1}$	
V_{MC}	MC (mode control) voltage (see Note 3)	EEPROM write protect override (WPO)		11.7	V
		Microprocessor		$V_{CC1} - 0.3$	
		Microcomputer		V_{SS1}	
T_A	Operating free-air temperature	L version		0	°C
		A version		–40	
		T version		–40	

NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS1} . $V_{CC1} = V_{CC}$.

2. RESET must be externally activated when V_{CC1} or SYSCLK is out of the recommended operating range.

3. The basic microcomputer and microprocessor operating modes are selected by the voltage level applied to the dedicated MC pin two system clock cycles (t_c) before RESET goes inactive (high). The WPO mode can be selected anytime a sufficient voltage is present on MC pin.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

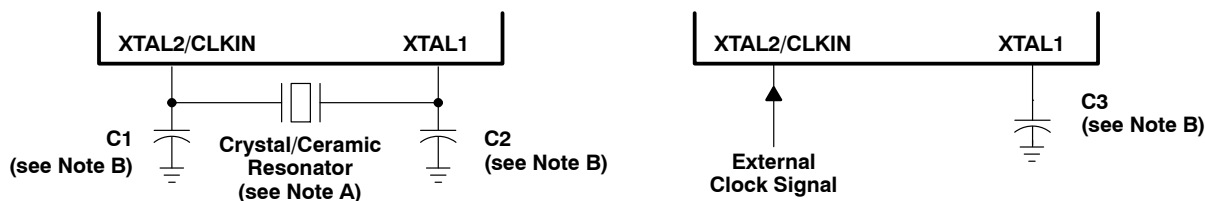
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OL}	Low-level output voltage	I _{OL} = 1.4 mA			0.4	V
V _{OH}	High-level output voltage	I _{OH} = -50 µA	0.9 V _{CC1}			V
		I _{OH} = -2 mA	2.4			
I _I	Input current	MC	0 V < V _I ≤ 0.3 V		10	µA
			0.3 V < V _I < V _{CC1} - 0.3 V		50	
			V _{CC1} - 0.3 V ≤ V _I ≤ V _{CC1} + 0.3 V		10	
			V _{CC1} + 0.3 V < V _I ≤ 13 V		650	
	I/O pins	0 V ≤ V _I ≤ V _{CC1}			± 10	
I _{OL}	Low-level output current	V _{OL} = 0.4 V	1.4			mA
I _{OH}	High-level output current	V _{OH} = 0.9 V _{CC1}	- 50			µA
		V _{OH} = 2.4 V	- 2			mA
I _{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 6)	SYSCLK = 5 MHz See Notes 4 and 5		35	56	mA
		SYSCLK = 3 MHz See Notes 4 and 5		25	36	
		SYSCLK = 0.5 MHz See Notes 4 and 5		13	18	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 7)	SYSCLK = 5 MHz See Notes 4 and 5		12	17	mA
		SYSCLK = 3 MHz See Notes 4 and 5		8	11	
		SYSCLK = 0.5 MHz See Notes 4 and 5		2.5	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 8)	SYSCLK = 3 MHz See Notes 4 and 5		6	8.6	mA
		SYSCLK = 0.5 MHz See Notes 4 and 5		2	3	
	Supply current (HALT mode)	XTAL2/CLKIN < 0.2 V See Note 4		2	30	µA

- NOTES: 4. In single chip mode, ports are configured as inputs or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC1} - 0.2V.
5. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = 0.01 mA x (total load capacitance + crystal capacitance in pF).
6. Maximum operating current for TMS370CxBx = 10 (SYSCLK) + 5.8 mA.
7. Maximum standby current for TMS370CxBx = 3 (SYSCLK) + 2 mA. (OSC POWER bit = 0).
8. Maximum standby current for TMS370CxBx = 2.24 (SYSCLK) + 1.9 mA. (OSC POWER bit =1, only valid up to 3 MHz SYSCLK).

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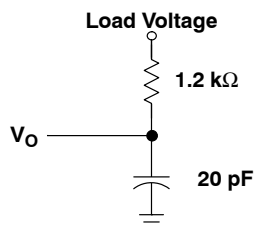
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PARAMETER MEASUREMENT INFORMATION



NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
B. The values of C1 and C2 are typically 15 pF and the value of C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 15. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4 \text{ V}$; Load Voltage = 0 V
Case 2: $V_O = V_{OL} = 0.4 \text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 16. Typical Output Load Circuit (see Note A)

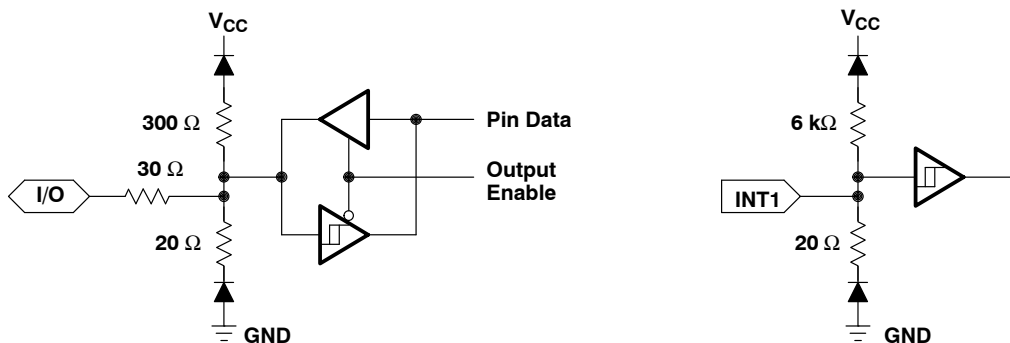


Figure 17. Typical Buffer Circuitry

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

A	Address	IE	Initial
AR	Array	PGM	Program
B	Byte	R	Read
CI	XTAL2/CLKIN	SC	SYSCLK
D	Data	W	Write
E	EDS	WT	WAIT
FE	Final		

Lowercase subscripts and their meanings are:

c	cycle time (period)	r	rise time
d	delay time	su	setup time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid
Z	High impedance

All timings are measured between high and low measurement points as indicated in Figure 18 and Figure 19.

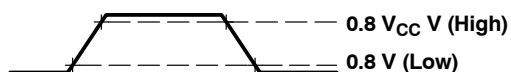


Figure 18. XTAL2/CLKIN Measurement Points

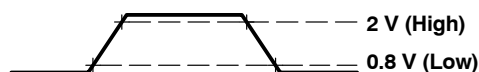


Figure 19. General Measurement Points

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external clocking requirements for clock divided by 4[†] (see Figure 20)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 9)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN Crystal operating frequency	2	20	MHz
	SYSCLK System clock [‡]	0.5	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions.

[‡] SYSCLK = CLKIN/4

NOTE 9: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

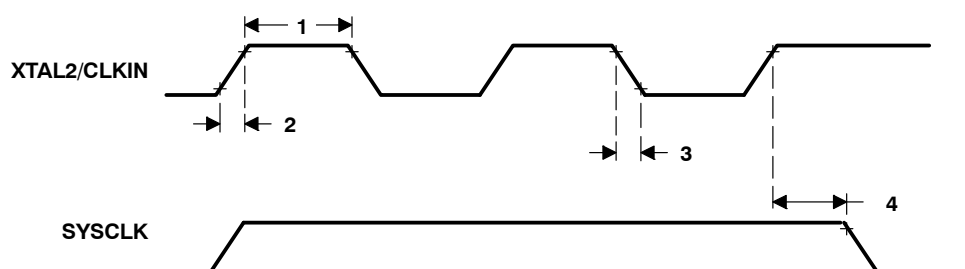


Figure 20. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL)[†] (see Figure 21)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 9)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN Crystal operating frequency	2	5	MHz
	SYSCLK System clock [§]	2	5	MHz

[†] For V_{IL} and V_{IH} , refer to recommended operating conditions.

[§] SYSCLK = CLKIN/1

NOTE 9: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

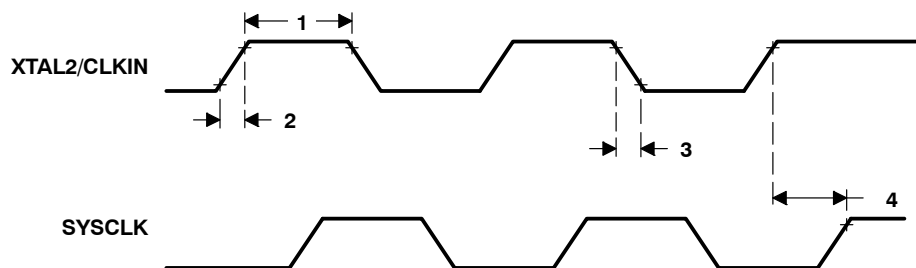


Figure 21. External Clock Timing for Divide-by-1

general purpose output signal switching time requirements (see Figure 22)

	MIN	NOM	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns

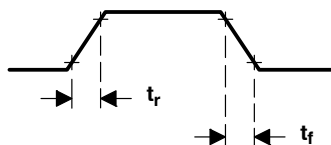


Figure 22. Signal Switching Timing

recommended EEPROM timing requirements for programming

	MIN	MAX	UNIT
$t_{w(PGM)B}$ Pulse duration, programming signal to ensure valid data is stored (byte mode)	10		ms
$t_{w(PGM)AR}$ Pulse duration, programming signal to ensure valid data is stored (array mode)	20		ms

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switching characteristics and timing requirements for external read and write[†] (see Figure 23 and Figure 24)

NO.	PARAMETER		MIN	MAX	UNIT	
5	t _c	Cycle time, SYSCLK (system clock)	Divide-by-4 clock	200	2000	ns
			Divide-by-1-(PLL)	200	500	
6	t _{w(SCL)}	Pulse duration, SYSCLK low	0.5t _c –25	0.5t _c	ns	
7	t _{w(SCH)}	Pulse duration, SYSCLK high	0.5t _c	0.5t _c +20	ns	
8	t _{d(SCL-A)}	Delay time, SYSCLK low to address R/ $\overline{W}$ and $\overline{OCF}$ valid		0.25t _c +75	ns	
9	t _{v(A)}	Valid time, address to $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ low	0.5t _c –90		ns	
10	t _{su(D)}	Setup time, write data time to $\overline{EDS}$ high	0.75t _c –80 [‡]		ns	
11	t _{h(EH-A)}	Hold time, address, R/ $\overline{W}$ and $\overline{OCF}$ from $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ high	0.5t _c –60		ns	
12	t _{h(EH-D)W}	Hold time, write data time from $\overline{EDS}$ high	0.75t _c +15		ns	
13	t _{d(DZ-EL)}	Delay time, data bus high impedance to $\overline{EDS}$ low (read cycle)	0.25t _c –35		ns	
14	t _{d(EH-D)}	Delay time, $\overline{EDS}$ high to data bus enable (read cycle)	1.25t _c –40		ns	
15	t _{d(EL-DV)R}	Delay time, $\overline{EDS}$ low to read data valid		t _c –95 [‡]	ns	
16	t _{h(EH-D)R}	Hold time, read time from $\overline{EDS}$ high	0		ns	
17	t _{su(WT-SCH)}	Setup time, $\overline{WAIT}$ time to SYSCLK high	0.25t _c +70 [§]		ns	
18	t _{h(SCH-WT)}	Hold time, $\overline{WAIT}$ time from SYSCLK high	0		ns	
19	t _{d(ED-WTV)}	Delay time, $\overline{EDS}$ low to $\overline{WAIT}$ valid		0.5t _c –60	ns	
20	t _w	Pulse duration, $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ low	t _c –80 [‡]	t _c +40 [‡]	ns	
21	t _{d(AV-DV)R}	Delay time, address valid to read data valid		1.5t _c –115 [‡]	ns	
22	t _{d(AV-WTV)}	Delay time, address valid to $\overline{WAIT}$ valid		t _c –115	ns	
23	t _{d(AV-EH)}	Delay time, address valid to $\overline{EDS}$ high (end of write)	1.5t _c –85 [‡]		ns	

[†] t_c = system clock cycle time = $1/\text{SYSCLK}$

[‡] If wait states, PFWait, or the autowait feature is used, add t_c to this value for each wait state invoked.

[§] If the autowait feature is enabled, the WAIT input can assume a don't care condition until the third cycle of the access. The WAIT signal must be synchronized with the high pulse of the SYSCLK signal while still conforming to the minimum set-up time.



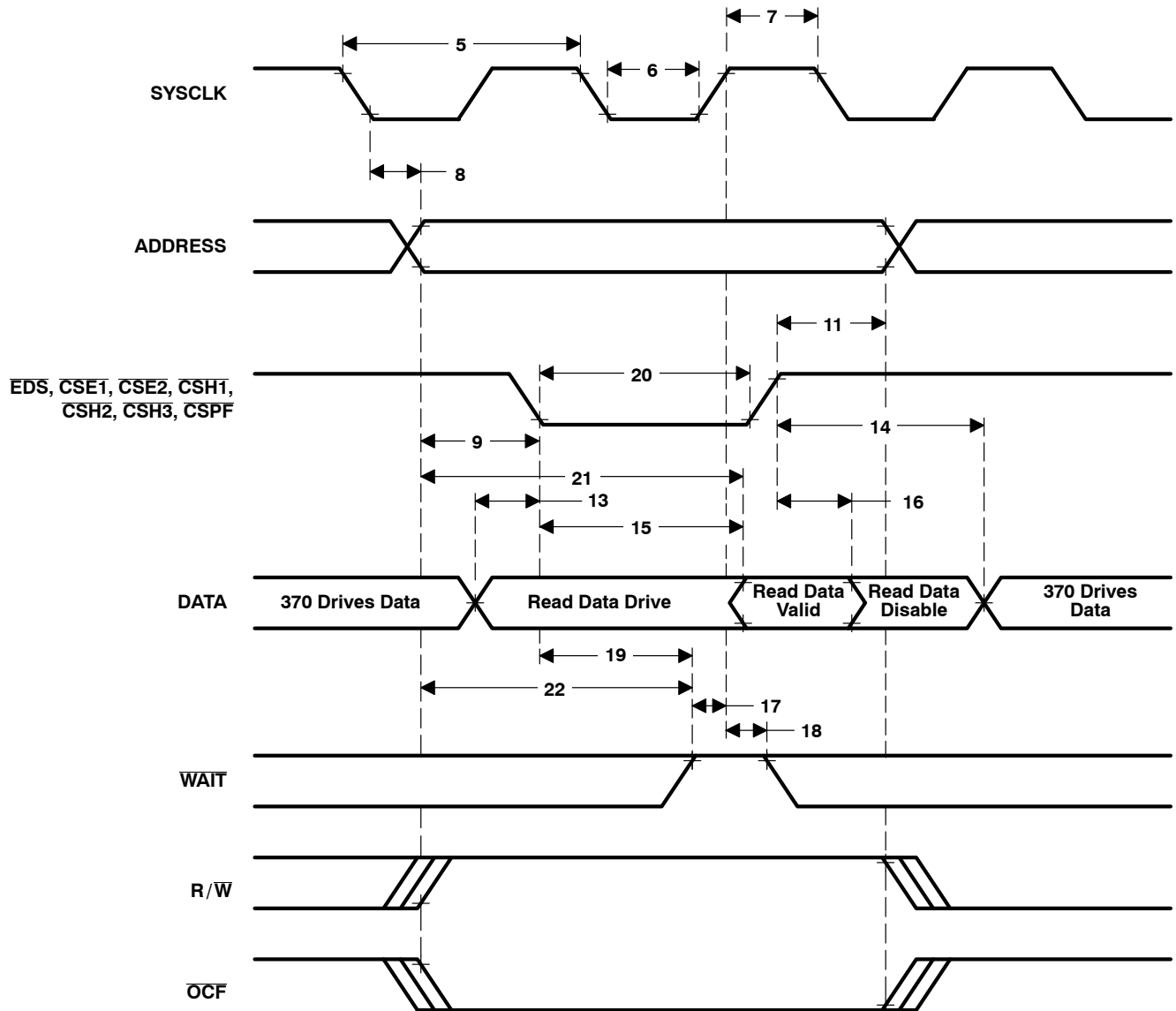


Figure 23. External-Read Timing

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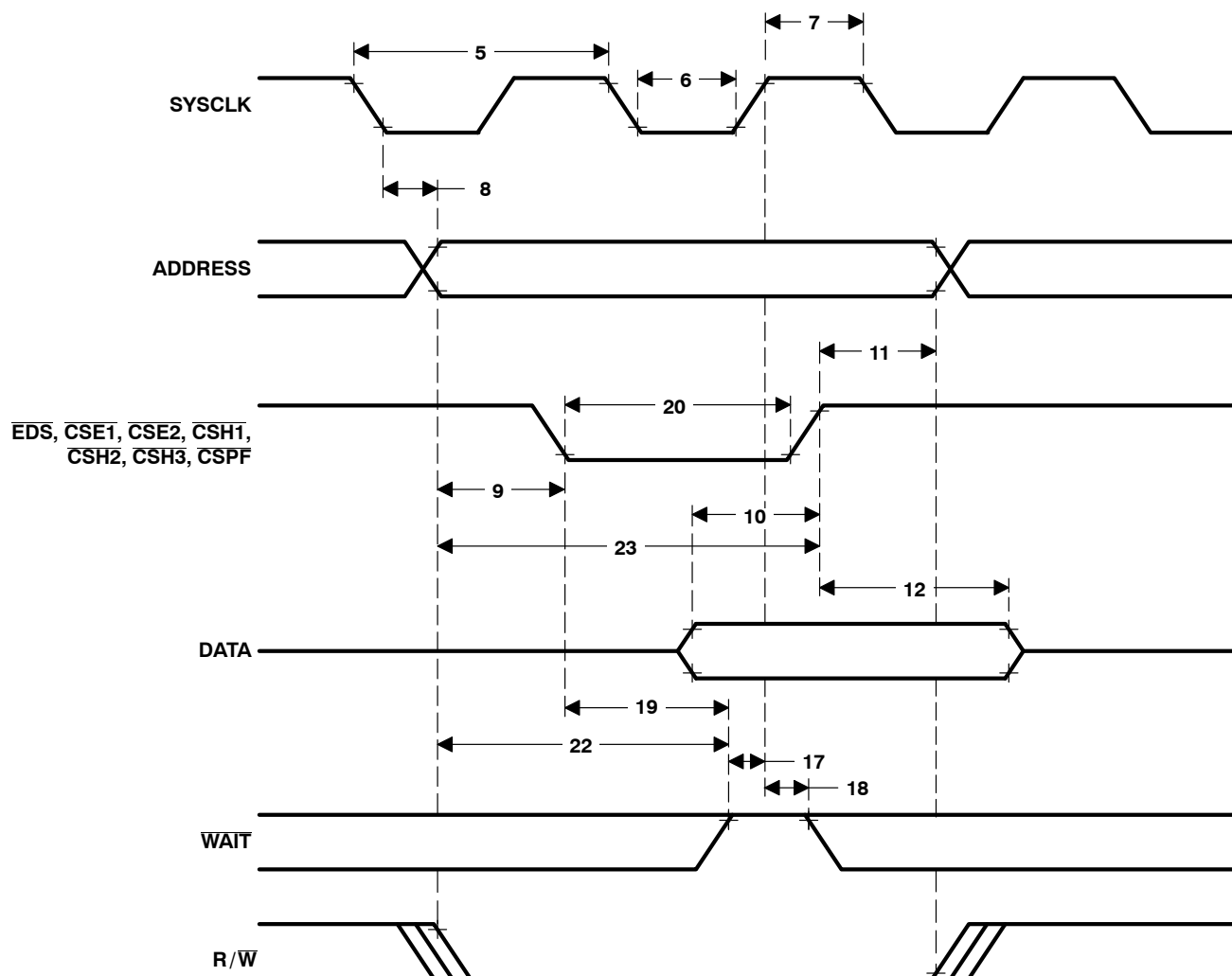


Figure 24. External-Write Timing

analog-to-digital converter 1 (ADC1)

The ADC1 has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3} . The purpose of these pins is to enhance ADC1 performance by preventing digital switching noise of the logic circuitry that can be present on V_{SS1} and V_{CC1} from coupling into the ADC1 analog stage. All ADC1 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution 8-bits (256 values)
 Monotonic Yes
 Output conversion mode 00h to FFh (00 for $V_I \leq V_{SS3}$; FF for $V_I \leq V_{ref}$)
 Conversion time (excluding sample time) $164 t_c$

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC3} Analog supply voltage	4.5	5	5.5	V
	$V_{CC3}-3$		$V_{CC3}+0.3$	
V_{SS3} Analog ground	$V_{SS3}-3$		$V_{SS3}+0.3$	V
V_{ref} Non- V_{CC3} reference [†]	2.5	V_{CC3}	$V_{CC3} + 0.1$	V
Analog input for conversion	V_{SS3}		V_{ref}	V

[†] V_{ref} must be stable, within $\pm 1/2$ LSB of the required resolution, during the entire conversion time.

operating characteristics over recommended ranges operating conditions

PARAMETER		MIN	MAX	UNIT
Absolute accuracy [‡]	$V_{CC3} = 5.5$ V $V_{ref} = 5.1$ V	± 1.5		LSB
Differential/integral linearity error ^{‡§}	$V_{CC3} = 5.5$ V $V_{ref} = 5.1$ V	± 0.9		LSB
I_{CC3} Analog supply current	Converting	2		mA
	Nonconverting	5		μ A
I_I Input current, AN0 – AN7	$0 \text{ V} \leq V_I \leq 5.5 \text{ V}$	2		μ A
I_{ref} Input charge current		1		mA
Z_{ref} Source impedance of V_{ref}	$SYSCLK \leq 3 \text{ MHz}$	24		k Ω
	$3 \text{ MHz} < SYSCLK \leq 5 \text{ MHz}$	10		k Ω

[‡] Absolute resolution = 20 mV. At $V_{ref} = 5$ V, this is one LSB. As V_{ref} decreases, LSB size decreases; therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

[§] Excluding quantization error of 1/2 LSB

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analog-to-digital converter 1 (ADC1) (continued)

The ADC1 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined so that the high-impedance can be accommodated without penalty to the low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC1 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter resets the SAMPLE START and CONVERT START bits, signaling that a conversion has started and that the analog signal can be removed.

analog timing requirements (see Figure 25)

Table with 4 columns: PARAMETERS, MIN, MAX, UNIT. Rows include t_su(S) Setup time, t_h(AN) Hold time, and t_w(S) Pulse duration.

† The value given is valid for a signal with a source impedance > 1 kΩ. If the source impedance is < 1 kΩ, use a minimum sampling time of 1μs.

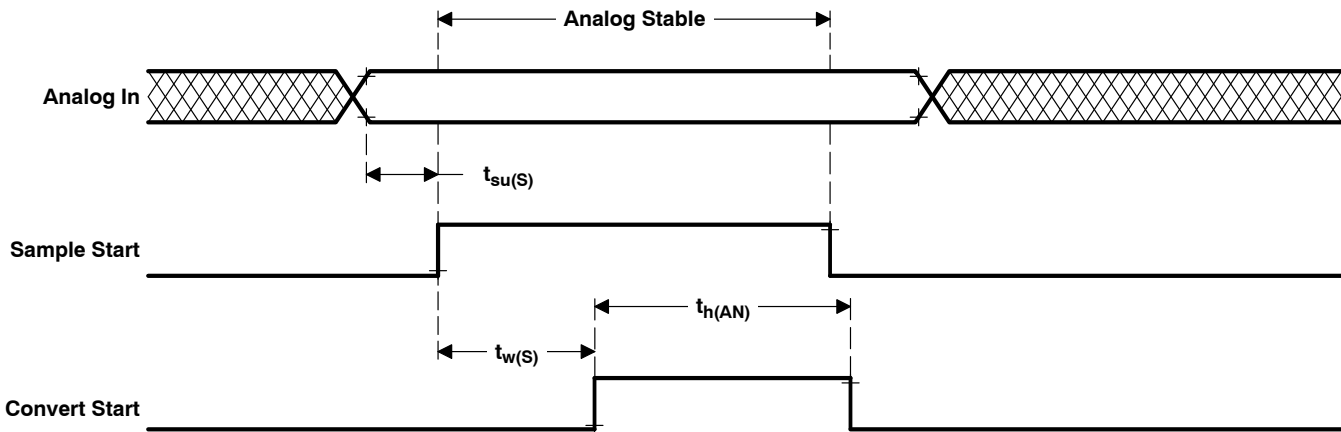


Figure 25. Analog Timing

Table 19 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

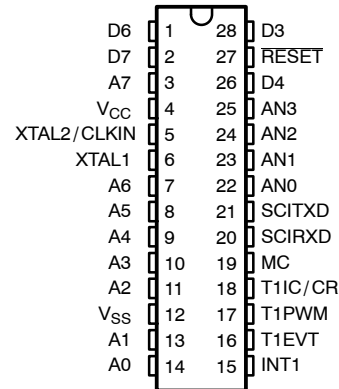
Table 19. TMS370CxBx Family Package Type and Mechanical Cross-Reference

Table with 4 columns: PKG TYPE (mil pin spacing), TMS370 GENERIC NAME, PKG TYPE NO. AND MECHANICAL NAME, and DEVICE PART NUMBERS. Rows describe FN and NM package types.

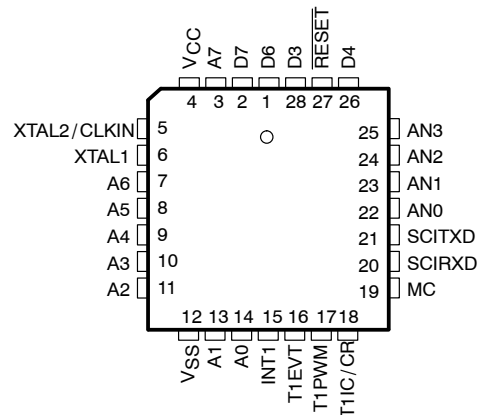
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- **CMOS/EEPROM/EPROM Technologies on a Single Device**
 - Mask-ROM Devices for High-Volume Production
 - One-Time-Programmable (OTP) EPROM Devices for Low Volume Production
 - Reprogrammable EPROM Devices for Prototyping Purposes
- **Internal System Memory Configurations**
 - On-Chip Program Memory Versions
 - ROM: 4K Bytes
 - EPROM: 8K Bytes
 - Static RAM: 128 Bytes
- **Flexible Operating Features**
 - Low-Power Modes: STANDBY and HALT
 - Commercial, Industrial, and Automotive Temperature Ranges
 - Clock Options
 - Divide-by-4 (0.5 to 5 MHz SYSCLK)
 - Divide-by-1 (2 to 5 MHz SYSCLK) PLL
 - Supply Voltage (V_{CC}) 5 V $\pm$ 10%
- **Four-Channel 8-Bit Analog-to-Digital Converter 2 (ADC2)**
- **16-Bit General-Purpose Timer**
 - Software Configurable as a 16-Bit Event Counter, or a 16-Bit Pulse Accumulator, or a 16-Bit Input Capture Function, or Two Compare Registers, or a Self-Contained Pulse-Width-Modulation (PWM) Function
- **On-Chip 24-Bit Watchdog Timer**
 - EPROM/OTP Devices: Standard Watchdog
 - Mask-ROM Devices: Hard Watchdog, Simple Counter, or Standard Watchdog
- **Flexible Interrupt Handling**
- **Workstation/Personal Computer-Based Development System**
 - C Compiler and C Source Debugger
 - Real-Time In-Circuit Emulation
 - Extensive Breakpoint/Trace Capability
 - Software Performance Analysis
 - Multi-Window User Interface
 - Microcontroller Programmer

**JD AND N PACKAGES
(TOP VIEW)**



**FZ AND FN PACKAGES
(TOP VIEW)**



- **Serial Communications Interface 2 (SCI2)**
 - Asynchronous Mode: 156 Kbps Maximum at 5 MHz SYSCLK
 - Full Duplex, Double-Buffered Receiver (RX) and Transmitter (TX)
- **TMS370 Series Compatibility**
 - Register-to-Register Architecture
 - 256 General-Purpose Registers
 - 14 Powerful Addressing Modes
 - Instructions Upwardly Compatible With All TMS370 Devices
- **CMOS/TTL Compatible I/O Pins/Packages**
 - All Peripheral Function Pins Software Configurable for Digital I/O
 - 17 Bidirectional Pins, 5 Input Pins
 - 28-Pin Plastic and Ceramic Dual-In-Line, or Leaded Chip Carrier Packages



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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TMS370CxCx

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Pin Descriptions

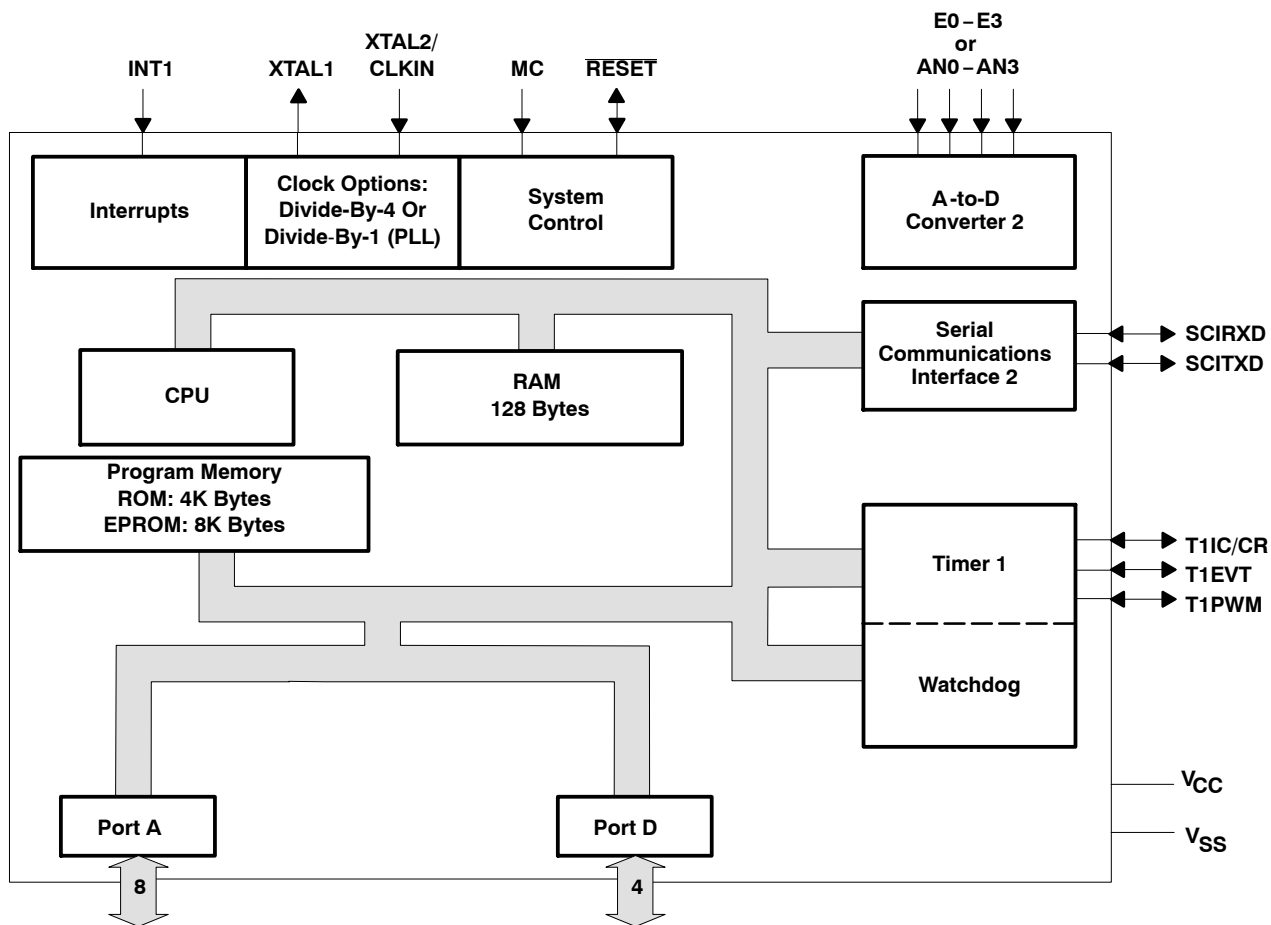
28 PINS DIP and LCC		I/O†	DESCRIPTION
NAME	NO.		
A0 A1 A2 A3 A4 A5 A6 A7	14 13 11 10 9 8 7 3	I / O	Port A is a general-purpose bidirectional I/O port.
D3 D4 D6 D7	28 26 1 2	I / O	Port D is a general-purpose bidirectional I/O port. D3 is also configurable as SYSCLK.
INT1	15	I	External interrupt (non-maskable or maskable)/general-purpose input pin.
AN0/E0 AN1/E1 AN2/E2 AN3/E3	22 23 24 25	I	ADC2 module analog input (AN0 – AN3) or positive reference pins (AN1 – AN3). Port E can be individually programmed as general-purpose input pins if not used as ADC2 analog input.
T1IC/CR T1PWM T1EVT	18 17 16	I / O	Timer1 input capture/counter reset input pin /general-purpose bidirectional pin. Timer1 PWM output pin/general-purpose bidirectional pin. Timer1 external event input pin/general-purpose bidirectional pin.
SCITXD SCIRXD	21 20	I / O	SCI module transmit data output/general-purpose bidirectional pin. (See Note 1) SCI module receive data input pin/general-purpose bidirectional pin.
RESET	27	I / O	System reset bidirectional pin; as input pin, RESET initializes the microcontroller; as open-drain output, RESET indicates that an internal failure was detected by watchdog or oscillator fault circuit.
MC	19	I	Mode control input pin; programming EPROM when V _{PP} is applied to MC pin.
XTAL2/CLKIN XTAL1	5 6	I O	Internal oscillator crystal input/External clock source input. Internal oscillator output for crystal.
V _{CC}	4		Positive supply voltage
V _{SS}	12		Ground reference

† I = input, O = output

NOTE 1: The two SCI configuration pins are referenced to as SCI2.



functional block diagram



description

The TMS370C3C0, TMS370C6C2, and SE370C6C2 devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370CxCx refers to these devices. The TMS370 family provides cost-effective real-time system control through integration of advanced peripheral function modules and various on-chip memory configurations.

The TMS370CxCx family of devices is implemented using high-performance silicon-gate CMOS EPROM technologies. Low-operating power, wide-operating temperature range, and noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370CxCx devices attractive in system designs for automotive electronics, industrial motors, computer peripheral controls, telecommunications, and consumer applications.

All TMS370CxCx devices contain the following on-chip peripheral modules:

- Four-channel, 8-bit analog to digital converter 2 (ADC2)
- Serial communications interface 2 (SCI2)
- One 24-bit general-purpose watchdog timer
- One 16-bit general-purpose timer with an 8-bit prescaler

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description (continued)

Table 1 provides a memory configuration overview of the TMS370CxTx devices.

Table 1. Memory Configurations

DEVICES	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		PACKAGES 28-PIN LCC OR DIP
	ROM	EPROM	RAM	EEPROM	
TMS370C3C0A	4K	—	128	—	FN – PLCC N – PDIP
TMS370C6C2A	—	8K	128	—	FN – PLCC N – PDIP
SE370C6C2A [†]	—	8K	128	—	FZ – CLCC JD – CDIP

[†] System evaluators and development are for use only in prototype environment, and their reliability has not been characterized.

The suffix letter (A) appended to the device name (shown in Table 1) indicates configuration of the device. ROM or EPROM devices have different configurations as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 2. Suffix Letter Configuration

DEVICE	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM A	Standard	Divide-by-4 (standard oscillator)	Enabled
ROM A	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

The 4K bytes of mask-programmable ROM in the associated TMS370C3C0A device are replaced in the TMS370C6C2A with 8K bytes of EPROM while all other available memory and on-chip peripherals are identical. The one-time programmable (OTP) (TMS370C6C2A) and reprogrammable (SE370C6C2A) devices are available.

TMS370C6C2A OTP devices are available in plastic packages. This microcontroller is effective to use for immediate production updates for other members of the TMS370C3C0A or for low-volume production runs when the mask charge or cycle time for the low-cost mask ROM devices is not practical.

The SE370C6C2A has a windowed ceramic package to allow reprogramming of the program EPROM memory during the development-prototyping phase of design. The SE370C6C2A devices allow quick updates to breadboards and prototype systems during initial design iterations.

The TMS370CxTx family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all CPU activity, that is, no instructions are executed. In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370CxTx features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370CxTx family is fully instruction-set compatible, providing easy transition between members of the TMS370 8-bit microcontroller family.



description (continued)

The TMS370CxCx device has one operational mode of serial communications provided by the SCI2 module. The SCI2 allows standard RS-232-C communications with other common data transmission equipment.

The TMS370CxCx family provides the system designer with economical, efficient solutions to real-time control applications. The TMS370 family extended development system (XDS™) and compact development tool (CDT™) solve the challenge of efficiently developing the software and hardware required to design the TMS370CxCx into an ever-increasing number of complex applications. The application source code can be written in assembly and C-language, and the output code can be generated by the linker. The TMS370 family XDS development tool communicates through a standard RS-232-C interface with an existing personal computer. This allows the use of the personal computer editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes ease-of-use through extensive menus and screen windowing so that a system designer can begin developing software with minimal training. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as reduced time-to-market cycle.

The TMS370CxCx family together with the TMS370 family XDS22, CDT370, design kit, starter kit, software tools, the SE370C6C2A reprogrammable devices, comprehensive product documentation, and customer support provide a complete solution to the needs of the system designer.

central processing unit (CPU)

The CPU used on the TMS370CxCx device is the high-performance 8-bit TMS370 CPU module. The 'xCx implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete 'xCx instruction map is shown in Table 36 in the TMS370CxCx instruction set overview section.

The '370CxCx CPU architecture provides the following components:

CPU registers:

- A stack pointer that points to the last entry in the memory stack.
- A status register that monitors the operation of the instructions and contains the global-interrupt enable bits.
- A program counter (PC) that points to the memory location of the next instruction to be executed.

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central processing unit (CPU) (continued)

Figure 1 illustrates the CPU registers and memory blocks.

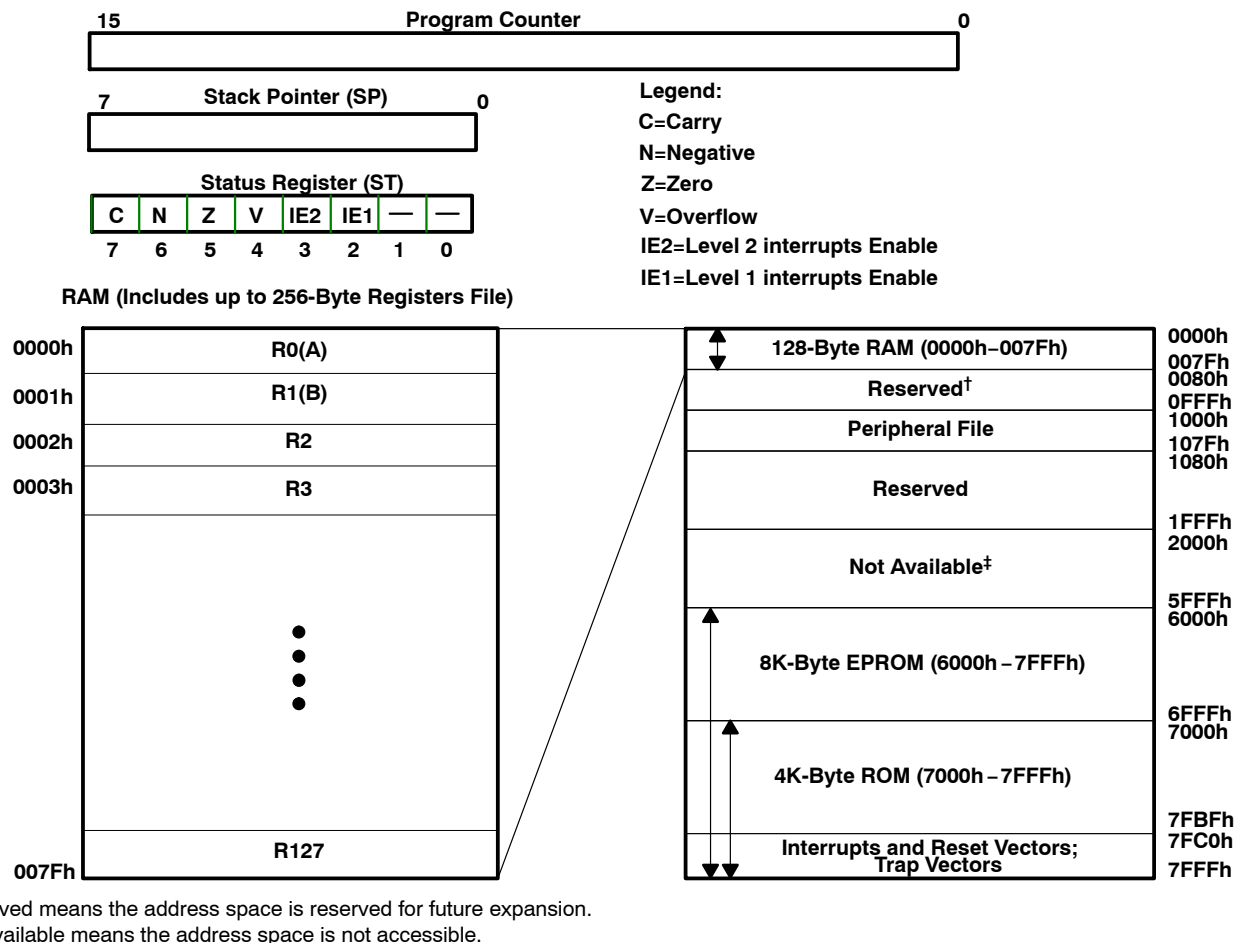


Figure 1. Programmer's Model

A memory map that includes:

- 128-byte general-purpose RAM that can be used for data memory storage, program instructions, general-purpose register, or the stack
- A peripheral file that provides access to all internal peripheral modules, system-wide control functions and EPROM programming control
- 4K-byte ROM or 8K-byte EPROM program memory

stack pointer (SP)

The SP is an 8-bit CPU register that operates as a last-in, first-out, read/write memory. Typically, the stack is used to store the return address on subroutine calls as well as the status-register contents during interrupt sequences.

The SP points to the last entry or top of the stack. The SP is incremented automatically before data is pushed onto the stack and decremented after data is popped from the stack. The stack can be placed anywhere in the on-chip RAM.

central processing unit (CPU) (continued)

status register (ST)

The ST monitors the operation of the instructions and contains the global interrupt-enable bits. The ST register includes four status bits (condition flags) and two interrupt-enable bits:

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional jump instructions) use the status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

The ST register, status-bit notation, and status-bit definitions are shown in Table 3.

Table 3. Status Register (ST)

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most significant byte (MSbyte) and least significant byte (LSbyte) of a 16-bit address.

During reset, the contents of the reset vector (7FFEh, 7FFFh) are loaded into the program counter. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 7000h as the contents of the reset vector.

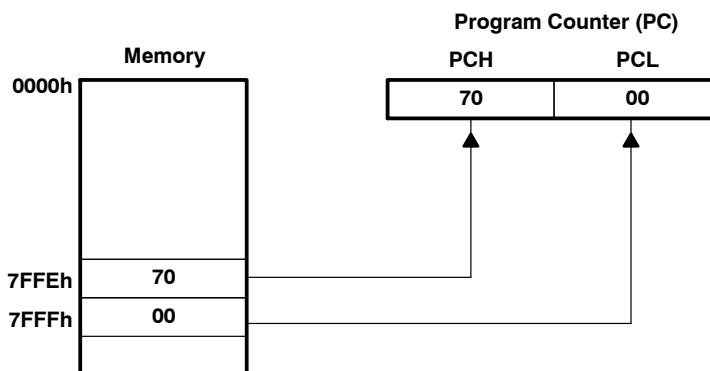


Figure 2. Program Counter After Reset

memory map

The TMS370CxCx architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. As shown in Figure 3, the TMS370CxCx provides memory-mapped RAM, ROM, input/output pins, peripheral functions, and system interrupt vectors.

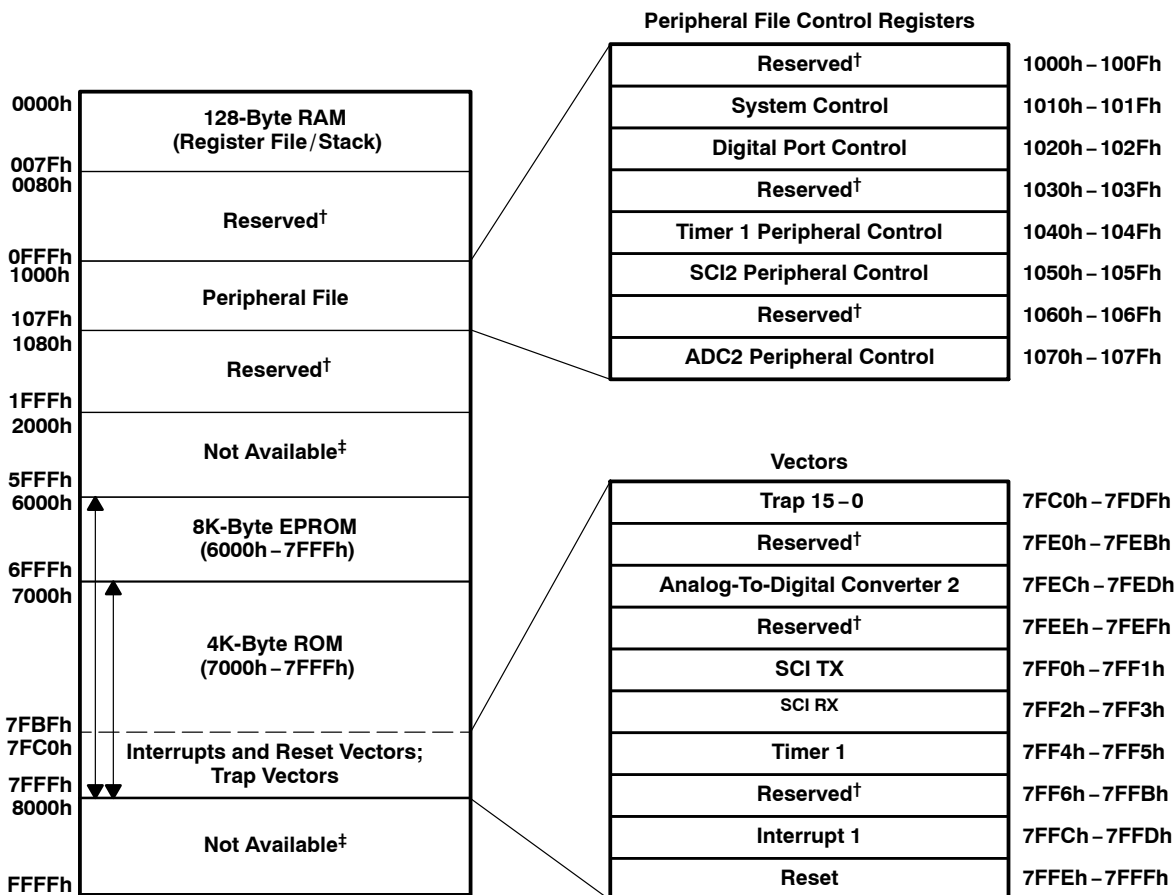
The peripheral file contains all input/output port control, peripheral status and control, EPROM, and system-wide control functions. The peripheral file is located from 1000h to 107Fh and is logically divided into seven peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed.

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memory map (continued)



† Reserved means the address space is reserved for future expansion.

‡ Not available means the address space is not accessible.

Figure 3. TMS370CxTx Memory Map

RAM/register file (RF)

Locations within the RAM address space can serve as the RF, general-purpose read/write memory, program memory, or the stack instructions. The TMS370CxTx devices contain 128 bytes of internal RAM mapped beginning at location 0000h (R0) and continuing through location 007Fh (R127) which is shown in Figure 1.

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the SP is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370CxTx control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or P for a decimal designator. For example, the system control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 4 shows the TMS370CxTx PF address map.

peripheral file (PF) (continued)

Table 4. TMS370CxCx Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h – 100Fh	P000 – P00F	Reserved
1010h – 101Fh	P010 – P01F	System and EPROM control registers
1020h – 102Fh	P020 – P02F	Digital I/O port control registers
1030h – 103Fh	P030 – P03F	Reserved
1040h – 104Fh	P040 – P04F	Timer 1 registers
1050h – 105Fh	P050 – P05F	Serial communications interface 2 registers
1060h – 106Fh	P060 – P06F	Reserved
1070h – 107Fh	P070 – P07F	Analog-to-digital converter 2 registers
1080h – 1FFFh	P080 – P0FF	Reserved

program EPROM[†]

The TMS370C6C2 device contains 8K bytes of EPROM mapped at location 6000h and continuing through location 7FFFh as shown in Figure 3. Reading the program EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the EPROM control register (EPCTL). The program EPROM module features include:

- Programming
 - In-circuit programming capability if V_{PP} is applied to MC
 - Control register: EPROM programming is controlled by the EPROM control register (EPCTL) located in the peripheral file (PF) frame at location P01Ch as shown in Table 5.
- Write protection: Writes to the program EPROM are disabled under the following conditions:
 - Reset halts all programming to the EPROM module.
 - Low-power modes
 - 13 V not applied to MC

Table 5. Data EEPROM and Program EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME
P01A to P01B	—	Reserved
P01C	EPCTL	Program EPROM Control Register

program ROM[†]

The program read-only memory (ROM) consists of 4K bytes of mask-programmable ROM. The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication. Refer to Figure 3 for ROM memory map.

[†] Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments, and addresses 7FECb through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh.

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system reset

The system reset operation ensures an orderly start-up sequence for the TMS370CxTx CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are internally generated, while one ($\overline{\text{RESET}}$ pin) is controlled externally. These actions are as follows:

- External $\overline{\text{RESET}}$ pin. A low level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 User's Guide* (literature number SPNU127) for more information.
- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 User's Guide* (literature number SPNU127) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside of the recommended operating range. See the *TMS370 User's Guide* (literature number SPNU127) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven low (active) for a minimum of eight SYSCLK cycles. This allows the 'xCx device to reset external system components. Additionally, if a cold start (V_{CC} is off for several hundred milliseconds) condition or oscillator failure occurs or the $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator fault flag (OSC FLT FLAG, SCCR0.4), the cold start flag (COLD START, SCCR0.7) and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 6 lists the reset sources.

Table 6. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Registers A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

When an external reset circuit is connected to the $\overline{\text{RESET}}$ pin, the pin must be held low until the clock signal is valid and V_{CC} is within the operating range. Figure 4 shows a typical reset circuit.

system reset (continued)

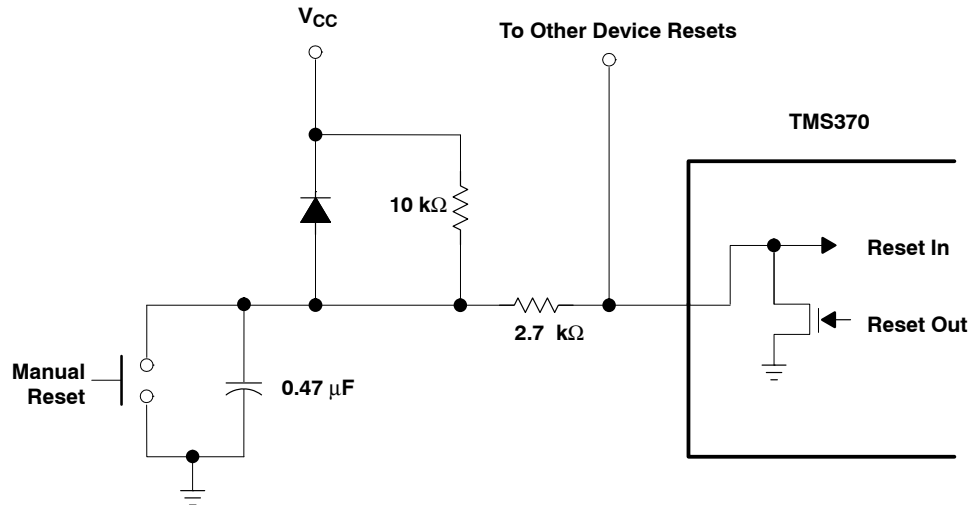


Figure 4. Typical Reset Circuit

interrupts

The TMS370 family software programmable interrupt structure permits flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 5. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global-interrupt mask bits (IE1 and IE2) of the status register.

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interrupts (continued)

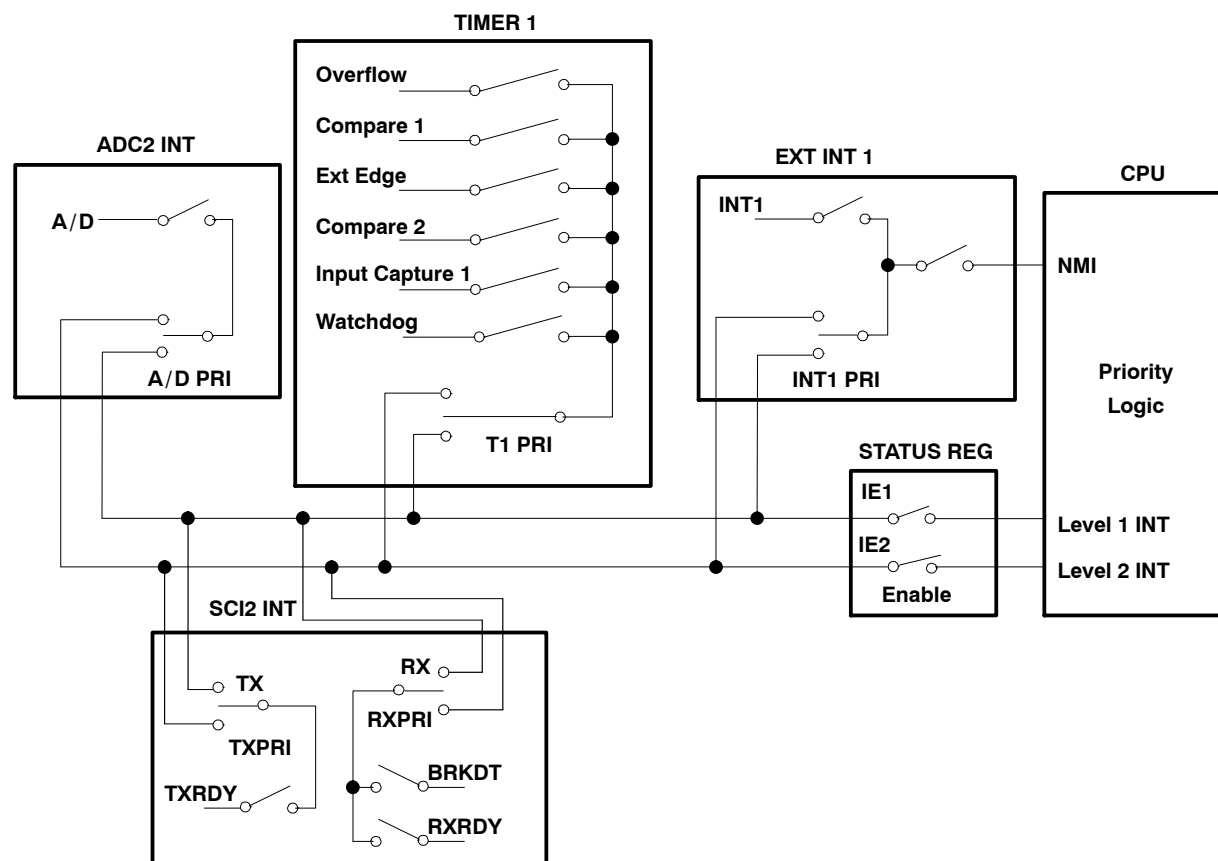


Figure 5. Interrupt Control

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is selectively configured on either the high- or low-priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending-interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370CxTx has five hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 7. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. A system interrupt may have multiple interrupt sources (for example, SCI RXINT has two interrupt sources). All of the interrupt sources are individually maskable by local interrupt-enable control bits in the associated peripheral file. Each interrupt source FLAG bit is readable individually for software polling or for determining which interrupt source generated the associated system interrupt.

Four of the system interrupts are generated by on-chip peripheral functions, and one external interrupt is supported. Software configuration of the external interrupts is performed through the INT1 control register in peripheral file frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual-

interrupts (continued)

or global-enable mask bits. The INT1 NMI bit is protected during non-privileged operation and therefore should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupt INT1 can be software-configured as a general-purpose input pin if the interrupt function is not required.

Table 7. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY [†]
External RESETW Watchdog Overflow Oscillator Fault Detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	RESET [‡]	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1 [‡]	7FFCh, 7FFDh	2
Timer 1 Overflow Timer 1 Compare 1 Timer 1 Compare 2 Timer 1 External Edge Timer 1 Input Capture 1 Watchdog Overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT [§]	7FF4h, 7FF5h	3
SCI RX Data Register Full SCI RX Break Detect	RXRDY FLAG BRKDT FLAG	RXINT [‡]	7FF2h, 7FF3h	4
SCI TX Data Register Empty	TXRDY FLAG	TXINT	7FF0h, 7FF1h	5
A/D Conversion Complete	AD INT FLAG	ADINT	7FECh, 7FEDh	6

[†] Relative priority within an interrupt level.

[‡] Release microcontroller from STANDBY and HALT low-power modes.

[§] Release microcontroller from STANDBY low-power mode.

privileged operation and EEPROM write-protection override

The TMS370Cx family has significant flexibility to enable the designer to software configure the system and peripherals to meet the requirements of a variety of applications. The non-privileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) is set to 1 to enter the non-privileged mode; thus, disabling write operations to specific configuration control bits within the peripheral file. Table 8 displays the system configuration bits which are write-protected during the non-privileged mode and must be configured by software prior to exiting the privileged mode.

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privileged operation and EEPROM write-protection override (continued)

Table 8. Privilege Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCR0	P010.5 P010.6	PF AUTO WAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
T1PRI	P04F.6 P04F.7	T1 PRIORITY TI STEST
SCIPRI	P05F.4 P05F.5 P05F.6 P05F.7	SCI ESPEN SCIRX PRIORITY SCITX PRIORITY SCI STEST
ADPRI	P07F.5 P07F.6 P07F.7	AD ESPEN AD PRIORITY AD STEST

† The privilege bits are shown in a bold typeface in the peripheral file frame 1 section.

low-power and IDLE modes

The TMS370CxCx devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time when the mask is manufactured.

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls the low-power mode selection.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity stops; however, the oscillator, internal clocks, timer 1, and the receive-start bit detection circuit of the serial communications interface 2 remain active. System processing is suspended until a qualified interrupt (hardware RESET, external interrupt on INT1, timer 1 interrupt, or low level in the receive pin of the SCI2) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370CxCx is placed in its lowest power-consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware RESET, external interrupt on the INT1, or low level on the receive pin of the serial communications interface 2) is detected. The power-down mode selection bits are summarized in Table 9.



low-power and IDLE modes (continued)

Table 9. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X †	IDLE

† Don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6-7 bits are ignored. In addition, if an idle instruction executes when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method of always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI always is generated, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing stops during the STANDBY and HALT modes, the clocking of the watchdog timer is inhibited.

clock modules

The 'xCx family provides two clock options that are referred to as divide-by-1 (phase-locked loop) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The 'xCx ROM-masked devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device. The '6C2A EPROM has only the divide-by-4.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 clock module option provides a one-to-one match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency, whereas the divide-by-4 option produces a SYSCLK which is one-fourth of the frequency of the external resonator. Inside of the divide-by-1 module, the frequency of the external resonator is multiplied by four, and the clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency.

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clock modules (continued)

These are formulated as follows:

$$\text{Divide-by-4 : SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 : SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is to reduce EMI. The harmonics of low-speed resonators extend through less of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 option provides the capability of reducing the resonator speed by four times, resulting in a steeper decay of emissions produced by the oscillator.

system configuration registers

Table 10 contains system configuration and control functions. The privileged bits are shown in bold typeface and shaded areas.

Table 10. System Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	AUTO WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1
P012	HALT/STANDBY	PWRDWN/IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2
P013 to P016	RESERVED								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018 to P01B	RESERVED								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D P01E P01F	RESERVED								

digital I/O port configuration registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 11 shows the specific addresses, registers, and control bits within this peripheral file frame. Table 12 shows the port-configuration register setup.

Table 11. Peripheral File Frame 2: Digital Port-Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
P020	Reserved								APOINT1
P021	Port A Control Register 2 (must be 0)								APOINT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)	—		Port D Control Register 1 (must be 0)	—	—	—	—	DPOINT1
P02D	Port D Control Register 2 (must be 0) [†]	—		Port D Control Register 2 (must be 0) [†]	—	—	—	—	DPOINT2
P02E	Port D Data	—		Port D Data	—	—	—	—	DDATA
P02F	Port D Direction	—		Port D Direction	—	—	—	—	DDIR

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 12. Port Configuration Register Set-up

PORT	PIN	abcd 00q1	abcd 00y0
A	0 – 7	Data Out q	Data In y
D	3, 4, 6, 7	Data Out q	Data In y
a = Port x Control Register 1 b = Port x Control Register 2 c = Data d = Direction			

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programmable timer 1

The programmable Timer 1 (T1) module of the TMS370CxTx provides the designer with the enhanced timer resources required to perform real-time system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers allow program selection of input clock sources (real-time, external event, or pulse accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The T1 module includes three external device pins that can be used for multiple counter functions (operation mode dependent) or used as general-purpose I/O pins. The T1 module is shown in Figure 6.

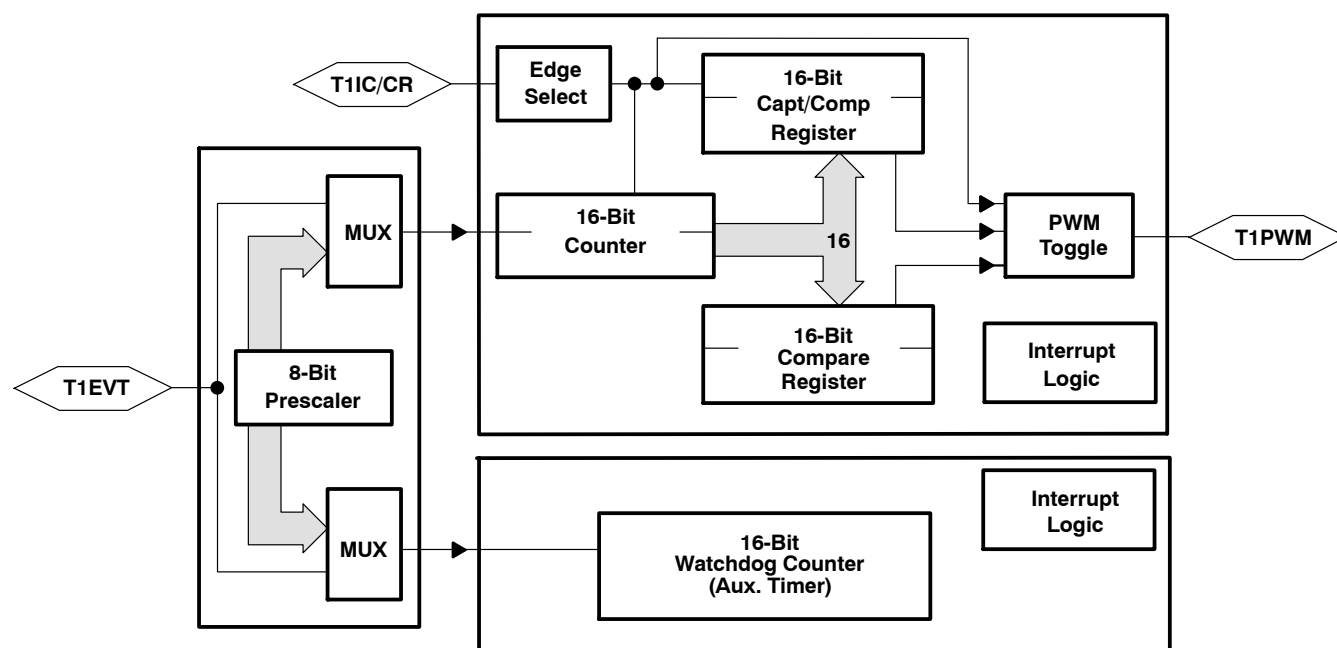


Figure 6. Timer 1 Block Diagram

- Three T1 I/O pins
 - T1IC/CR: Timer 1 input capture / counter reset input pin, or general-purpose bidirectional I/O pin
 - T1PWM: Timer 1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
 - T1EVT: Timer 1 event input pin, or general-purpose bidirectional I/O pin
- Two operation modes:
 - Dual-compare mode: Provides PWM signal
 - Capture/compare mode: Provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register.
- One 16-bit watchdog counter can be used as an event counter, a pulse accumulator, or an interval timer if watchdog feature is not needed.
- Prescaler/clock sources that determine one of eight clock sources for general-purpose timer

programmable timer 1 (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR)
- Interrupts that can be generated on the occurrence of:
 - A capture
 - A compare equal
 - A counter overflow
 - An external edge detection
- Sixteen T1 module control registers located in the PF frame beginning at address P040.

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programmable timer 1 (continued)

The T1 module control registers are listed in Table 13. Privilege bits are shown in bold typeface and shaded.

Table 13. Timer Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Mode: Dual-Compare and Capture/Compare									
P040	T1 Counter MSbyte							Bit 8	T1CNTR
P041	T1 Counter LSbyte							Bit 0	
P042	Compare Register MSbyte							Bit 8	T1C
P043	Compare Register LSbyte							Bit 0	
P044	Capture/Compare Register MSbyte							Bit 8	T1CC
P045	Capture/Compare Register LSbyte							Bit 0	
P046	Watchdog Counter MSbyte							Bit 8	WDCNTR
P047	Watchdog Counter LSbyte							Bit 0	
P048	Watchdog Reset Key							Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE=0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Mode: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

Figure 7 shows the T1 capture/compare mode block diagram. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.



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programmable timer 1 (continued)

Figure 8 shows the T1 dual-compare mode block diagram. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

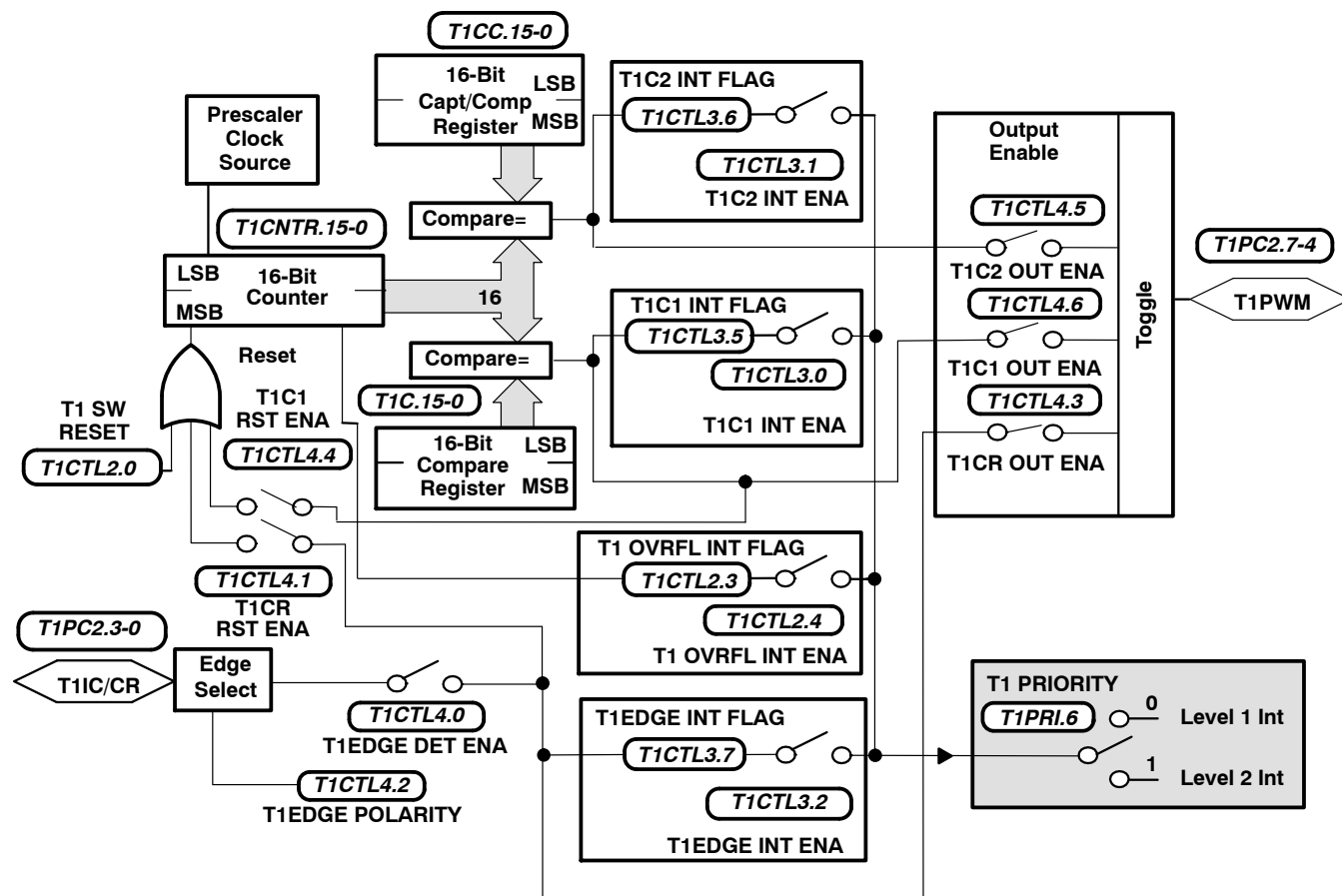


Figure 8. Dual-Compare Mode

programmable timer 1 (continued)

The TMS370Cx device includes a 24-bit WD timer, contained in the T1 module, which can be programmed as an event counter, pulse accumulator, or interval timer if the watchdog function is not used. The WD function is to monitor software and hardware operation and to implement a system reset when the WD counter is not properly serviced (WD counter overflow or WD counter is re-initialized by an incorrect value). The WD can be configured as one of the three mask options as follows:

- Standard watchdog configuration (see Figure 9) – for EPROM and mask-ROM devices:
 - Watchdog mode
 - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5 MHz SYSCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows
 - A watchdog overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
 - Non-watchdog mode
 - Watchdog timer can be configured as an event counter, pulse accumulator, or an interval timer.

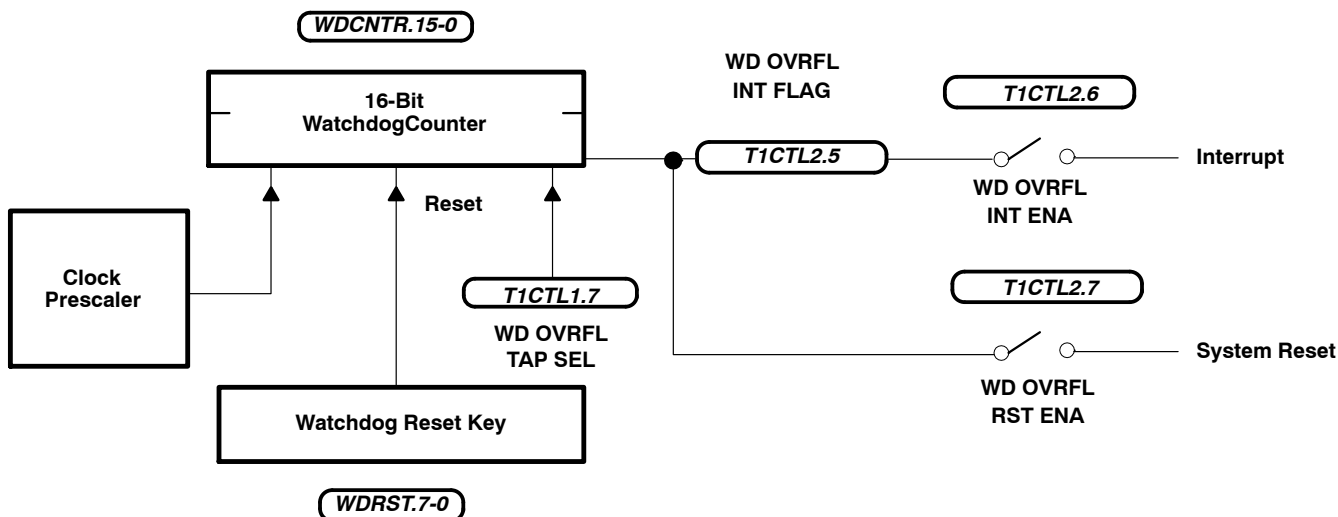


Figure 9. Standard watchdog

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programmable timer 1 (continued)

- Hard watchdog configuration (see Figure 10) – for mask-ROM devices:
 - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5 MHz SYSCCLK
 - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
 - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows.
 - Automatic activation of the WD timer upon power-up reset
 - INT1 is enabled as a nonmaskable interrupt during low-power modes.
 - A watchdog overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset

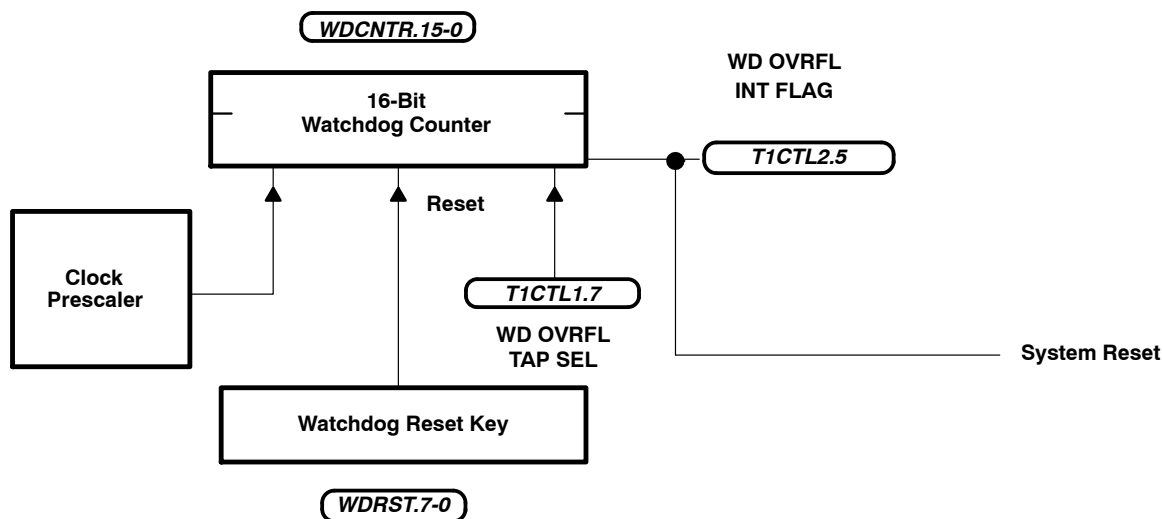


Figure 10. Hard Watchdog

- Simple counter configuration – for mask-ROM devices only (see Figure 11)
 - Simple counter can be configured as an event counter, pulse accumulator, or an internal timer.

programmable timer 1 (continued)

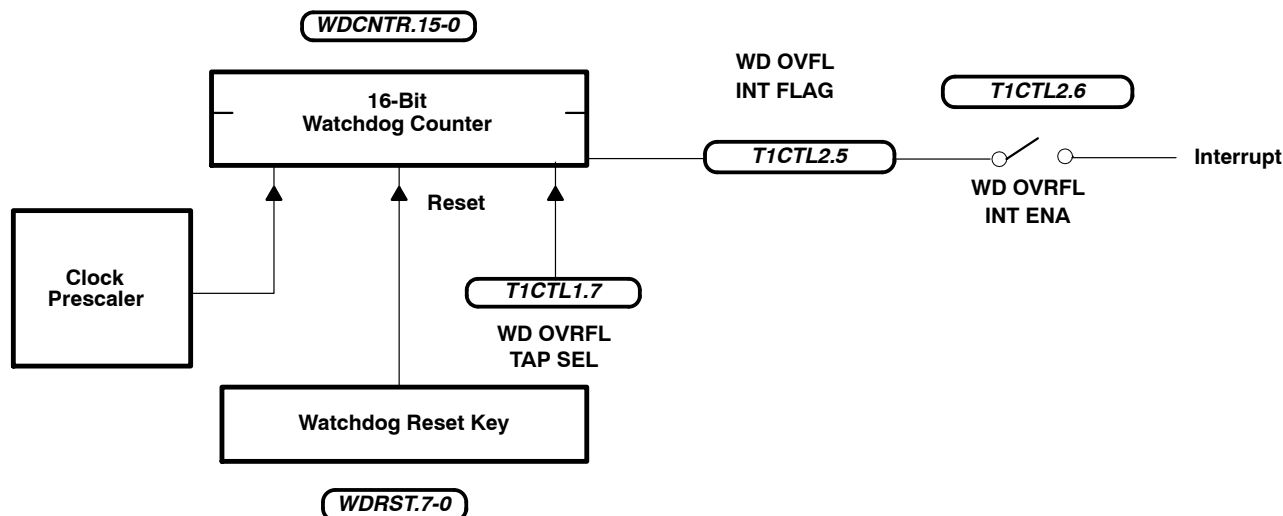


Figure 11. Simple Counter

serial communications interface 2 module

The TMS370Cx devices include a serial communications interface 2 (SCI2) module. The SCI2 module supports digital communications between the TMS370 devices and other asynchronous peripherals and uses the standard non-return-zero (NRZ) format. The SCI2 modules receiver and transmitter are double buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full duplex mode. To ensure data integrity, the SCI2 checks received data for break detection, parity, overrun, and framing errors. The speed of bit rate (baud) is programmable to over 65,000 different speeds through a 16-bit baud-select register. Features of the SCI2 module include:

- Two external pins:
 - SCITXD: SCI2 module transmit-output pin or general-purpose bidirectional I/O pin.
 - SCIRXD: SCI2 module receive-input pin or general-purpose bidirectional I/O pin.
- Asynchronous communications mode
- Baud rate: 64K different programmable rates
 - Asynchronous mode: 3 bps to 156K bps at 5 MHz SYSCLK

$$\text{Asynchronous Baud} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 32}$$

- Data word format:
 - One start bit
 - Data word length programmable from one to eight bits
 - Optional even/odd/no parity bit
 - One or two stop bits

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serial communications interface 2 module (continued)

- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: Idle-line and address bit
- Half or full-duplex operation
- Double-buffered receiver and transmitter operations
- Transmitter and receiver operations can be accomplished through either interrupt-driven or polled-algorithms with status flags:
 - Transmitter: TXRDY flag (transmitter buffer register is ready to receive another character) and TX EMPTY flag (Transmitter shift register is empty)
 - Receiver: RXRDY flag (receive buffer register ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR monitoring four interrupt conditions
 - Separate enable bits for transmitter and receiver interrupts
 - NRZ format
- Ten SCI2 module control registers located in control register frame beginning at address P050

The SCI2 module control registers are listed in Table 14. Privilege bits are shown in bold typeface and shaded.

Table 14. SCI2 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	—	ADDRESS/IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	—	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	RESERVED								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	RESERVED								
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF
P05A to P05D	RESERVED								
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	SCI STEST	SCITX PRIORITY	SCIRX PRIORITY	SCI ESPEN	—	—	—	—	SCIPRI



serial communications interface 2 module (continued)

The SCI2 module block diagram is illustrated in Figure 12.

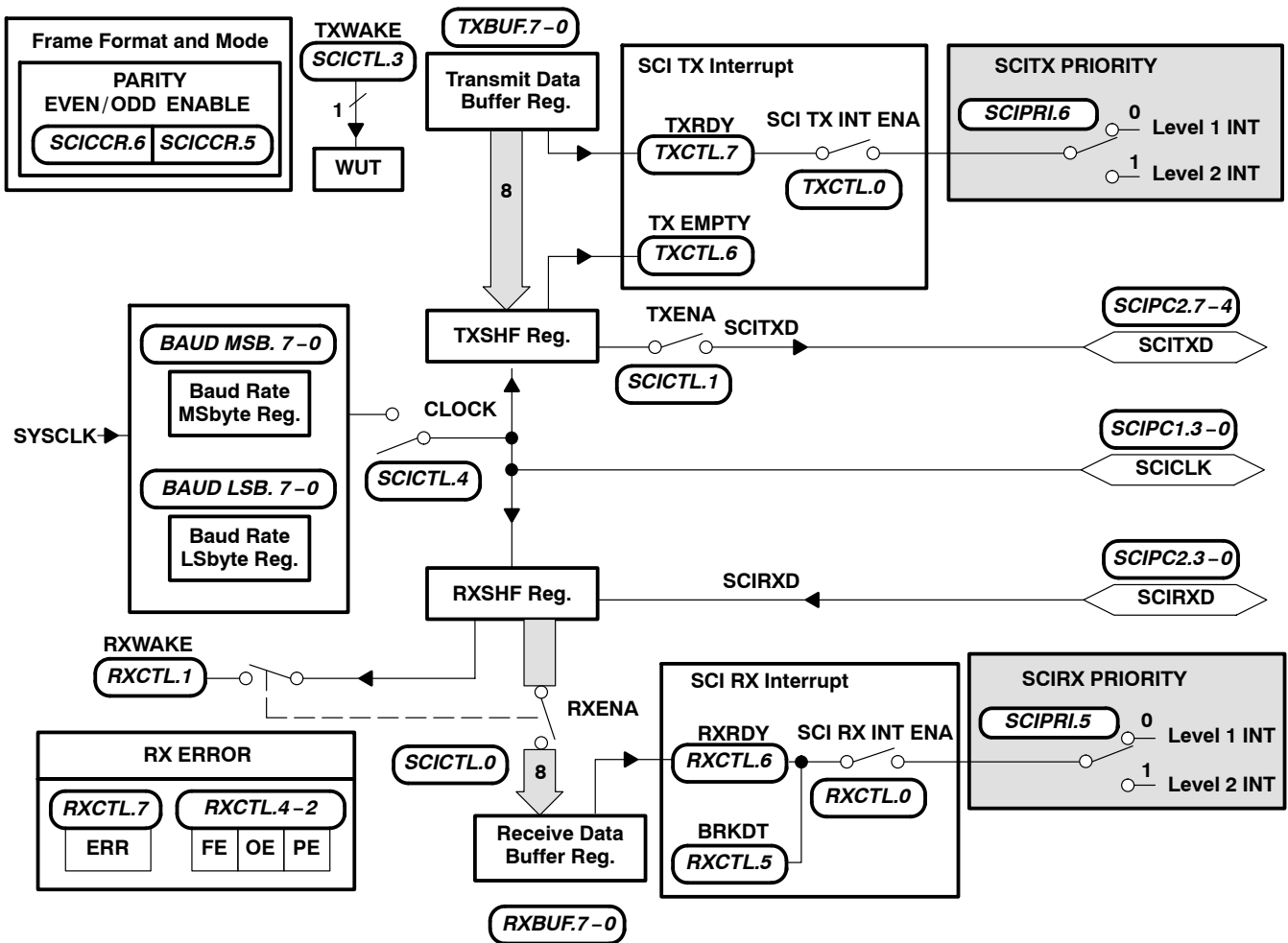


Figure 12. SCI2 Block Diagram

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serial communications interface 2 module (continued)

SCI communication control register (SCICCR)

The SCICCR register defines the character format, protocol, and communications modes used by the SCI2.

Table 15. SCI Communication Control Register (SCICCR) [Memory Address – 1050h]

Bit #	7	6	5	4	3	2	1	0
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	—	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0
	RW–0	RW–0	RW–0			RW–0	RW–0	RW–0

R = read, W = write, –n = value of the bit after the register is reset

Bits 0–2 SCI CHAR0–2 (SCI character length control bits 0–2)

These bits select the SCI character (data) bit length, from 1 to 8 bits. Characters of less than 8 bits are right-justified in RXBUF and TXBUF, and are padded with leading 0s in RXBUF. TXBUF need not be padded with leading 0s.

Table 16. Character Bit Length

SCI CHAR2	SCI CHAR1	SCI CHAR0	Character Length
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Bit 3 ADDRESS/IDLE WUP (SCI multiprocessor mode control bit)

This bit selects the multiprocessor mode.

0 = Selects idle line mode

1 = Selects address bit mode

The idle line mode is usually used for normal communications because the address bit mode adds an extra bit to the frame; the idle line mode does not add this extra bit and is compatible with RS-232-type communications. Multiprocessor communication is different from the other communications modes because it uses TXWAKE and SLEEP functions.

Bit 4 Reserved (read data is indeterminate)

Bit 5 PARITY ENABLE (SCI parity enable)

This bit enables or disables the parity function. When parity is enabled during the address bit multiprocessor mode, the address bit is included in the parity calculation.

0 = Disables parity. No parity bit is generated during transmission or expected during reception.

1 = Enables parity



serial communications interface 2 module (continued)

- Bit 6** **EVEN/ODD PARITY (SCI parity enable)**
- If the PARITY ENABLE bit is set, this bit selects odd or even parity (odd or even number of bits in both transmitted and received characters).
- 0 = Sets odd parity
1 = Sets even parity
- Bit 7** **STOP BITS (SCI number of stop bits)**
- This bit determines the number of stop bits transmitted. The receiver checks for one stop bit only.
- 0 = One stop bit
1 = Two stop bits

SCI control register (SCICTL)

The SCICTL register controls the RX/TX enable, TXWAKE and SLEEP functions, and the SCI software reset.

Table 17. SCI Control Register (SCICTL) [Memory Address – 1051h]

Bit #	7	6	5	4	3	2	1	0
P051	—	—	SCI SW RESET	—	TXWAKE	SLEEP	TXENA	RXENA
			RW–0	RW–0	RS–0	RW–0	RW–0	RW–0

R = read, W = write, S = set only, –n = value of the bit after the register is reset

- Bit 0** **RXENA (SCI receive enable)**
- When this bit is set, received characters are transferred into RXBUF, and the RXRDY flag is set. When cleared, this bit prevents received characters from being transferred into the receiver buffer (RXBUF), and no receiver interrupts are generated. However, the receiver shift register continues to assemble characters. As a result, if RXENA is set during the reception of a character, the complete character is transferred into RXBUF.
- 0 = Disables SCI receiver
1 = Enables SCI receiver
- Bit 1** **TXENA (SCI transmit enable)**
- Data transmission through the SCITXD pin occurs only when this bit is set. If this bit is reset, the transmission is not halted until all the data previously written to TXBUF has been sent.
- 0 = Disables SCI transmitter
1 = Enables SCI transmitter
- Bit 2** **SLEEP (SCI sleep)**
- This bit controls the receive features of the multiprocessor communication modes. This bit must be cleared to bring the SCI out of sleep mode.
- 0 = Disables sleep mode
1 = Enables sleep mode

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serial communications interface 2 module (continued)

Bit 3 TXWAKE (SCI transmitter wake-up)

The TXWAKE bit controls the transmit features of the multiprocessor communication modes. This bit is cleared only by system reset. The SCI hardware clears this bit, once it has been transferred to wake-up temporary (WUT).

Bit 4 Reserved (read data is indeterminate)

Bit 5 SCI SW RESET (SCI software reset—active low)

Writing a 0 to this bit initializes the SCI state machines and operation flags to the reset condition. All affected logic is held in the reset state until a 1 is written to the SCI SW RESET bit. After a system reset, you must re-enable the SCI by writing a 1 to this bit. This bit must be cleared after a receiver break detect.

SCI SW RESET affects the operating flags of the SCI. This bit does not affect the configuration bits, nor does it put in the reset values. The flags listed in Table 18 are set to the values shown when SCI SW RESET is cleared. The operating flags are frozen until the SCI SW RESET bit is set again.

Table 18. Flags Affected by SCI SW RESET

SCI FLAG	DESIGNATION	VALUE AFTER SCI SW RESET
TXRDY	TXCTL.7	1
TXEMPTY	TXCTL.6	1
RXWAKE	RXCTL.1	0
PE	RXCTL.2	0
OE	RXCTL.3	0
FE	RXCTL.4	0
BRKDT	RXCTL.5	0
RXRDY	RXCTL.6	0
RX ERROR	RXCTL.7	0

Bits 6, 7 Reserved (read data is indeterminate)

baud-select registers (BAUD MSB and BAUD LSB)

The BAUD MSB and BAUD LSB registers store the data required to generate the bit rate. The SCI2 uses the combined 16-bit value, BAUD REG, of the baud-select registers to set the internal SCI2 clock frequency.

- For asynchronous-mode communication, data is transmitted and received at the rate of one bit for each 16 internal SCICLK periods.

The asynchronous bit rates are calculated as follows:

$$\text{Asynchronous Baud} = \text{SYSCLK} / [(\text{BAUD REG} + 1) 32]$$

serial communications interface 2 module (continued)

Table 19. Baud-Select Register (BAUD MSB) [Memory Address – 1052h]

Bit #	7	6	5	4	3	2	1	0
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R = read, W = write, -n = value of the bit after the register is reset

Table 20. Baud-Select Register (BAUD LSB) [Memory Address – 1053h]

Bit #	7	6	5	4	3	2	1	0
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R = read, W = write, -n = value of the bit after the register is reset

SCI transmitter interrupt control and status register (TXCTL)

The TXCTL register contains the transmitter interrupt-enable bit, the transmitter-ready flag, and the transmitter-empty flag. The status flags are updated each time a complete character is transmitted.

Table 21. SCI Transmitter Interrupt Control and Status Register (TXCTL) [Memory Address – 1054h]

Bit #	7	6	5	4	3	2	1	0
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA
	R-1	R-1						RW-0

R = read, W = write, -n = value of the bit after the register is reset

Bit 0 SCI TX INT ENA (SCI transmitter ready interrupt enable)

This bit controls the ability of the TXRDY bit to request an interrupt but does not prevent the TXRDY bit from being set. The SCI TX INT ENA bit is set to 0 by a system reset.

0 = Disables SCI TXRDY interrupt

1 = Enables SCI TXRDY interrupt

Bits 1–5 Reserved (read data is indeterminate)

Bit 6 TX EMPTY (SCI transmitter empty)

This bit indicates the status of the transmitter-shift register and the TXBUF register. TX EMPTY is set to 1 by an SCI SW RESET or by a system reset.

0 = The CPU has written data to the TXBUF register; the data has not been completely transmitted.

1 = TXBUF and TXSHF registers are empty.

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serial communications interface 2 module (continued)

Bit 7 TXRDY (SCI transmitter ready)

The TXRDY bit is set by the transmitter to indicate that TXBUF is ready to receive another character. The bit is automatically cleared when a character is loaded into TXBUF. This flag asserts a transmitter interrupt if the interrupt-enable bit SCI TX INT ENA (TXCTL.0) is set. TXRDY is a read-only flag. It is set to 1 by an SCI SW RESET or by a system reset.

0 = TXBUF is full.

1 = TXBUF is ready to receive a character.

SCI receiver interrupt control and status register (RXCTL)

The RXCTL register contains one interrupt-enable bit and seven receiver-status flags (two of which can generate interrupt requests). The status flags are updated each time a complete character is transferred to the RXBUF. They are cleared each time RXBUF is read.

Table 22. SCI Receiver Interrupt Control and Status Register (RXCTL) [Memory Address – 1055h]

Bit #	7	6	5	4	3	2	1	0
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA
	R-0	R-0	R-0	R-0	R-0	R-0	R-0	RW-0

R = read, W = write, -n = value of the bit after the register is reset

Bit 0 SCI RX INT ENA (SCI receiver interrupt enable)

The SCI RX INT ENA bit controls the ability of the RXRDY and the BRKDT bits to request an interrupt but does not prevent these flags from being set.

0 = Disables RXRDY/BRKDT interrupt

1 = Enables RXRDY/BRKDT interrupt

Bit 1 RXWAKE (receiver wake-up detect)

The SCI sets this bit when a receiver wake-up condition is detected. In the address bit multiprocessor mode, RXWAKE reflects the value of the address bit for the character contained in RXBUF. In the idle line multiprocessor mode, RXWAKE is set if an idle SCIRXD line is detected. RXWAKE is a read-only flag. It is cleared by transfer of the first byte after the address byte to RXBUF, by reading the address character in RXBUF, by an SCI SW RESET, or by a system reset.

Bit 2 PE (SCI parity error flag)

This flag bit is set when a character is received with a mismatch between the number of 1s and its parity bit. The parity checker includes the address bit in the calculation. If parity generation and detection are not enabled, the PE flag is disabled and read as 0. The PE bit is reset by an SCI SW RESET, by a system reset, or by reading RXBUF.

0 = No parity error or parity is disabled

1 = Parity error detected



serial communications interface 2 module (continued)

- Bit 3 OE (SCI overrun error flag)
- The SCI sets this bit when a character is transferred into RXBUF before the previous character has been read out. The previous character is overwritten and lost. The OE flag is reset by an SCI SW RESET, by a system reset, or by reading RXBUF.
- 0 = No overrun error detected
1 = Overrun error detected
- Bit 4 FE (SCI framing error flag)
- The SCI sets this bit when it does not find a stop bit that it expects. Only the first stop bit is checked. The missing stop bit indicates that synchronization with the start bit has been lost and that the character is incorrectly framed. It is reset by an SCI SW RESET, by a system reset, or by reading RXBUF.
- 0 = No framing error detected
1 = Framing error detected
- Bit 5 BRKDT (SCI break detect flag)
- The SCI sets this bit when a break condition occurs. A break condition occurs when the SCIRXD line remains continuously low for at least 10 bits, beginning after a missing first stop bit. The occurrence of a break causes a receiver interrupt to be generated if the SCI RX INT ENA bit is a 1, but it does not cause the receiver buffer to be loaded. A BRKDT interrupt can occur, even if the receiver SLEEP bit is set to 1.
- BRKDT is cleared by an SCI SW RESET or by a system reset. It is not cleared by receipt of a character after the break is detected. In order to receive more characters, the SCI must be reset by toggling the SCI SW RESET bit or by a system reset.
- Bit 6 RXRDY (SCI receiver ready)
- The receiver sets this bit to indicate that RXBUF is ready with a new character and clears the bit when the character is read. A receiver interrupt is generated if the SCI RX INT ENA bit is a 1. RXRDY is reset by an SCI SW RESET or by a system reset.
- Bit 7 RX ERROR (SCI receiver error flag)
- The RX ERROR flag indicates that one of the error flags in the receiver status register is set. It is a logical OR of the parity, overrun, framing error, and break detect flags. The bit can be used for fast error condition checking during the interrupt service routine because a negative value of the status register indicates that an error condition has occurred. This error flag cannot be cleared directly but is cleared if no individual error flags are set. This bit is cleared by an SCI SW RESET, by a system reset, or by reading RXBUF.

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serial communications interface 2 module (continued)

SCI receiver data buffer register (RXBUF)

The RXBUF register contains current data from the receiver shift register. RXBUF is cleared by a system reset.

Table 23. SCI Receiver Data Buffer Register (RXBUF) [Memory Address – 1057h]

Bit #	7	6	5	4	3	2	1	0
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0
	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R = read, W = write, -n = value of the bit after the register is reset

SCI transmitter data buffer register (TXBUF)

The TXBUF register is a read/write register that stores data bits to be transmitted by SCITX. Data written to TXBUF must be right-justified because the left-most bits are ignored for characters less than eight bits long.

Table 24. SCI Transmit Data Buffer Register (TXBUF) [Memory Address – 1059h]

Bit #	7	6	5	4	3	2	1	0
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R = read, W = write, -n = value of the bit after the register is reset

SCI port control register 2 (SCIPC2)

The SCIPC2 register controls the SCIRXD and SCITXD pin functions.

Table 25. SCI Port Control Register 2 (SCIPC2) [Memory Address – 105Eh]

Bit #	7	6	5	4	3	2	1	0
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR
	R-0	RW-0	RW-0	RW-0	R-0	RW-0	RW-0	RW-0

R = read, W = write, -n = value of the bit after the register is reset

Bit 0 SCIRXD DATA DIR (SCIRXD data direction)

This bit determines the data direction on the SCIRXD pin if SCIRXD has been defined as a general-purpose I/O pin.

0 = SCIRXD pin is a general-purpose input pin.

1 = SCIRXD pin is a general-purpose output pin.

Bit 1 SCIRXD FUNCTION

This bit defines the function of the SCIRXD pin.

0 = SCIRXD pin is a general-purpose digital I/O pin.

1 = SCIRXD pin is the SCI receiver pin.



serial communications interface 2 module (continued)

- Bit 2** **SCIRXD DATA OUT**
- This bit contains the data to be output on the SCIRXD pin if the following conditions are met:
- SCIRXD pin has been defined as a general-purpose I/O pin.
 - SCIRXD pin data direction has been defined as output.
- Bit 3** **SCIRXD DATA IN**
- This bit contains the current value on the SCIRXD pin.
- Bit 4** **SCITXD DATA DIR (SCITXD data direction)**
- This bit determines the data direction on the SCITXD pin if SCITXD has been defined as a general-purpose I/O pin.
- 0 = SCITXD pin is a general-purpose input pin.
1 = SCITXD pin is a general-purpose output pin.
- Bit 5** **SCITXD FUNCTION**
- This bit defines the function of the SCITXD pin.
- 0 = SCITXD pin is a general-purpose digital I/O pin.
1 = SCITXD pin is the SCI transmit pin.
- Bit 6** **SCITXD DATA OUT**
- This bit contains the data to be output on the SCITXD pin if the following conditions are met:
- SCITXD pin has been defined as a general-purpose I/O pin.
 - SCITXD pin data direction has been defined as output.
- Bit 7** **SCITXD DATA IN**
- This bit contains the current value on the SCITXD pin.

SCI priority control register (SCIPRI)

The SCIPRI register contains the receiver and transmitter interrupt-priority select bits. This register is read-only during normal operation but can be written to in the privileged mode.

Table 26. SCI Priority Control Register (SCIPRI) [Memory Address – 105Fh]

Bit #	7	6	5	4	3	2	1	0
P05F	SCI STEST	SCITX PRIORITY	SCIRX PRIORITY	SCI ESPEN	—	—	—	—
	RP-0	RP-0	RP-0	RP-0				

R = read, P = privilege write only, -n = value of the bit after the register is reset

Bits 0–3 Reserved (read data is indeterminate)

serial communications interface 2 module (continued)

- Bit 4 SCI ESPEN (SCI emulator suspend enable)
- This bit has no effect except when you are using the XDS emulator to debug a program. Then, this bit determines how the SCI operates when the program is suspended by an action such as a hardware or software breakpoint.
- 0 = When the emulator is suspended, the SCI continues to work until the current transmit or receive sequence is complete.
- 1 = When the emulator is suspended, the SCI state machine is frozen so that the state of the SCI can be examined at the point that the emulator was suspended.
- Bit 5 SCI RX PRIORITY (SCI receiver interrupt priority select)
- This bit assigns the interrupt-priority level of the SCI receiver interrupts.
- 0 = Receiver interrupts are level 1 (high-priority) requests.
- 1 = Receiver interrupts are level 2 (low-priority) requests.
- Bit 6 SCI TX PRIORITY (SCI transmitter interrupt priority select)
- This bit assigns the interrupt-priority level of the SCI transmitter interrupts.
- 0 = Transmitter interrupts are level 1 (high-priority) requests.
- 1 = Transmitter interrupts are level 2 (low-priority) requests.
- Bit 7 SCI STEST (SCI STEST)

analog-to-digital converter 2 module

The analog-to-digital converter 2 (ADC2) module is an 8-bit, successive approximation converter with internal sample-and-hold circuitry. The module has four multiplexed analog input channels that allow the processor to convert the voltage levels from up to four different sources. The ADC2 module features include the following:

- Minimum conversion time: 32.8 μ s at 5 MHz SYSCLK
- Four external pins:
 - Four analog input channels (AN0–AN3), any of which can be software configured as digital inputs (E0–E3) if not needed as analog channels
 - AN1–AN3 also can be configured as positive-input voltage reference.
- The ADDATA register, which contains the digital result of the last analog-to-digital (A/D) conversion
- A/D operations can be accomplished through either interrupt-driven or polled algorithms.
- Six ADC2 module control registers located in the control register frame beginning at address 1070h

analog-to-digital converter 2 module (continued)

The ADC2 module control registers are listed in Table 27.

Table 27. ADC2 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P070	CONVERT START	SAMPLE START	—	REF VOLT SELECT1	REF VOLT SELECT0	—	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A/D Conversion Data Register								ADDATA
P073 to P07C	RESERVED								
P07D	—	—	—	—	Port E Data Input Register				ADIN
P07E	—	—	—	—	Port E Input Enable Register				ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI

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analog-to-digital converter 2 module (continued)

The ADC2 module block diagram is illustrated in Figure 13.

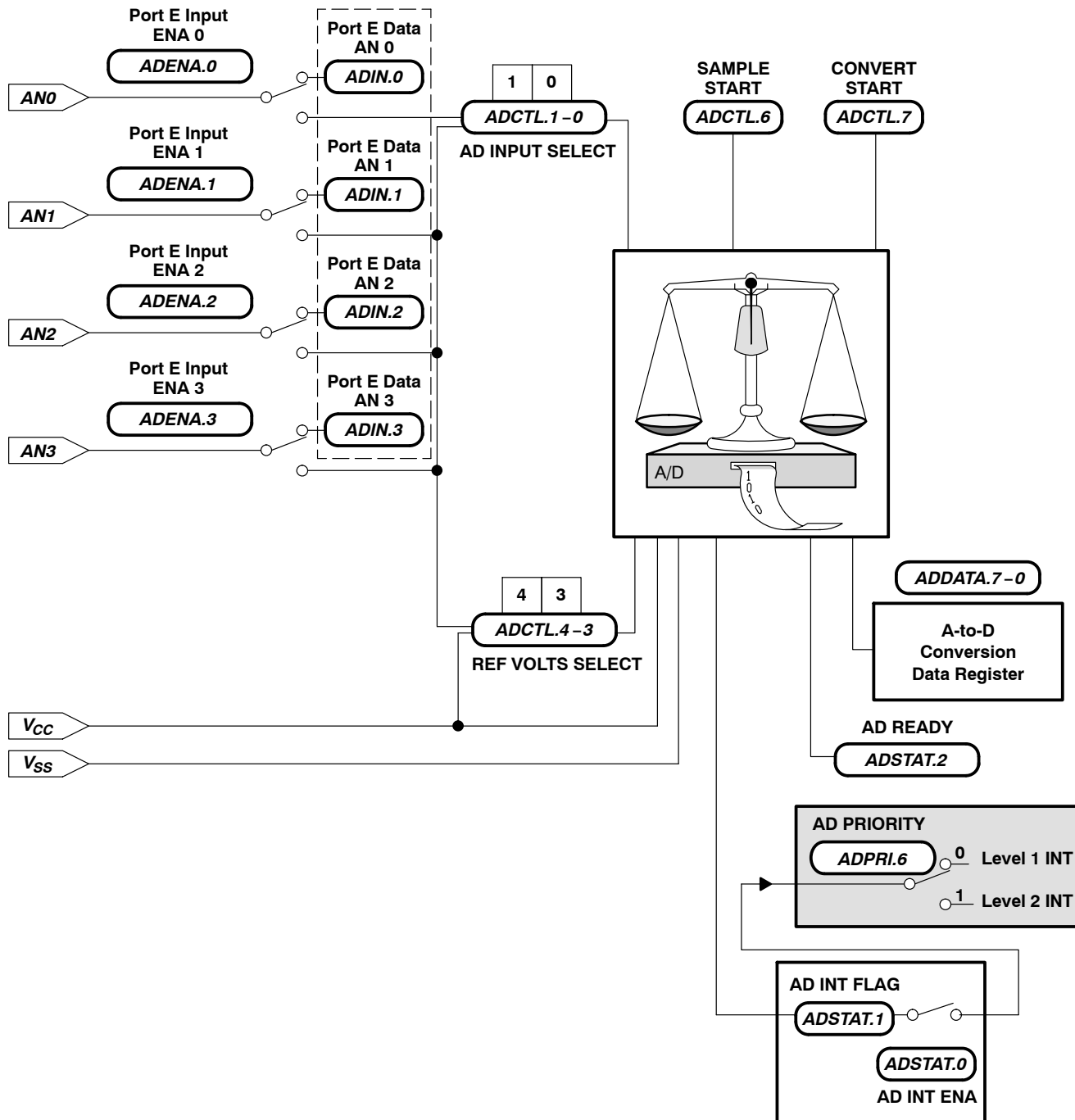


Figure 13. ADC2 Block Diagram

analog-to-digital converter 2 module (continued)

Table 28. A/D CONTROL REGISTER (ADCTL)

Bit #	7	6	5	4	3	2	1	0
P070	CONVERT START	SAMPLE START	—	REF VOLT SELECT1	REF VOLT SELECT0	—	AD INPUT SELECT1	AD INPUT SELECT0
	RW-0	RW-0		RW-0	RW-0	RW-0	RW-0	RW-0

R = read, W = write, -n = value of the bit after the register is reset

Bits 0–1 AD INPUT SELECT 0–1 (analog input channel select bits 0–1)

These bits select the channel used for conversion. Channels should be changed only after the ADC2 module has cleared the SAMPLE START and CONVERT START bits. Changing the channel while either SAMPLE START or CONVERT START is 1 invalidates the conversion in progress.

Table 29. Analog-Input Channel Selection

AD INPUT SELECT 1	AD INPUT SELECT 0	AD INPUT CHANNEL
0	0	AN0
0	1	AN1
1	0	AN2
1	1	AN3

Bit 2 Reserved (read data is indeterminate)

Bits 3–4 REF VOLT SELECT 3–4 (reference voltage (+V_{REF}) select bits 3–4)

These bits select the channel the ADC2 module uses for the positive voltage reference. These bits must not change during the entire conversion.

Table 30. Voltage-Channel Selection

REF VOLT SELECT 1	REF VOLT SELECT 0	+V _{REF} SOURCE
0	0	V _{CC}
0	1	AN1
1	0	AN2
1	1	AN3

Bit 5 Reserved (read data is indeterminate)

Bit 6 SAMPLE START (sample start)

Setting this bit stops any ongoing conversion and starts sampling the selected input channel to begin a new conversion. This bit is cleared by the ADC2 module. Entering HALT or STANDBY mode clears this bit and aborts any sampling in progress.

Bit 7 CONVERT START (conversion start)

Setting this bit starts the conversion. This bit is cleared by the ADC2 module. Entering HALT or STANDBY mode clears this bit and aborts any conversion in progress.

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analog-to-digital converter 2 module (continued)

Table 31. A/D Control Register (ADSTAT)

Bit #	7	6	5	4	3	2	1	0
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA
						R-0	RC-0	RW-0

R = read, W = write, C = clear only, -n = value of the bit after the register is reset

Bit 0 AD INT ENA (A/D interrupt enable)

This bit controls the ADC2 module's ability to generate an interrupt.

0 = Disable A/D interrupt

1 = Enable A/D interrupt

Bit 1 AD INT FLAG (A/D interrupt flag)

The ADC2 module sets this bit at the end of an ADC2 conversion. If this bit is set while the A/D INT ENA bit is set, an interrupt request is generated. Clearing this flag clears pending A/D interrupt requests. This bit is cleared by the system reset or by entering HALT or STANDBY mode. Software cannot set this bit.

Bit 2 AD READY (A/D converter ready)

The ADC2 module sets this bit whenever a conversion is not in progress and the ADC2 is ready for a new conversion to start. Writing to this bit has no effect on its state.

0 = Conversion is in process

1 = Converter is ready

Bits 3–7 Reserved (read data is indeterminate)

Table 32. A/D Conversion Data Register (DATA)

Bit #	7	6	5	4	3	2	1	0
P072	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

R = read, -n = value of the bit after the register is reset

The analog-to-digital conversion data is loaded into this register at the end of a conversion and remains until replaced by another conversion.

Table 33. AN0–AN3 Port E0–E3 Data Input Register (ADIN)

Bit #	7	6	5	4	3	2	1	0
P07D	—	—	—	—	DATA IN AN3	DATA IN AN2	DATA IN AN1	DATA IN AN0
					R-0	R-0	R-0	R-0

R = read, -n = value of the bit after the register is reset



analog-to-digital converter 2 module (continued)

Bits 0–3 PORT E DATA AN0–AN3 (Analog port E data in)

The ADIN register shows the data present at the pins configured for general-purpose input instead of ADC2 channels. A bit is configured as general-purpose input if the corresponding bit of the port enable register is a 1. Pins configured as ADC2 channels are read as 0s. Writing to this address has no effect.

Bits 4–7 Reserved (read data is indeterminate)

Table 34. AN0–AN3 Port E0–E3 Data Input-Enable Register (ADENA)

Bit #	7	6	5	4	3	2	1	0
P07E	—	—	—	—	INPUT ENA 3	INPUT ENA 2	INPUT ENA 1	INPUT ENA 0
					RW–0	RW–0	RW–0	RW–0

R = read, W = write, –n = value of the bit after the register is reset

Bits 0–3 INPUT ENA 0–3 (Analog port E input enable)

The ADENA register individually configures the pins AN0–AN3 as either analog-input channels or as general-purpose input pins.

0 = The pin becomes an analog-input channel for the ADC2. When the bit is 0, the corresponding bit in the ADIN register reads 0.

1 = Enables the pin as a general-purpose input pin and its digital value can be read from the corresponding bit in the ADIN register.

Bits 4–7 Reserved (read data is indeterminate)

Table 35. Analog Interrupt Priority/Conversion Rate Register (ADPRI)

Bit #	7	6	5	4	3	2	1	0
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—
	RP–0	RP–0	RP–0				RW–0	RW–0

R = read, W = write, P = privileged write, –n = value of the bit after the register is reset

Bits 0–4 Reserved (read data is indeterminate)

Bit 5 AD ESPEN (emulator suspend enable)

Normally this bit has no effect. However, when using the XDS emulator to debug a program, this bit determines what happens to the ADC2 when the program is suspended by an action such as a hardware or software breakpoint.

0 = When the emulator is suspended, the ADC2 continues to run until the conversion is complete

1 = When the emulator is suspended, the ADC2 is frozen so that its state can be examined at the point that the emulator was suspended. The conversion data is indeterminate upon restart.

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analog-to-digital converter 2 module (continued)

- Bit 6 AD PRIORITY (A/D interrupt priority select)
- This bit selects the priority level of the A/D interrupt.
- 0 = A/D Interrupt is a higher priority (level 1) request.
- 1 = A/D Interrupt is a lower priority (level 2) request.
- Bit 7 AD STEST (this bit must be cleared to ensure proper operation)

instruction set overview

Table 36 provides an opcode-to-instruction cross-reference of all 73 instructions and 274 opcodes of the '370CxCx instruction set. The numbers at the top of this table represent the most significant nibble of the opcode while the numbers at the left side of the table represent the least significant nibble. The instructions for these two opcode nibbles contain the mnemonic, operands, and byte/cycle specific to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.



Table 36. TMS370 Family Opcode/Instruction Map[†]

		MSN															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L S N	0	JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8			CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
	1	JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7
	2	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7
	3	JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8
	4	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes
	5	JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14	
	6	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6
	7	JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10
	8	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7
	9	JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9
A		JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12
B		JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A, *lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8

[†] All conditional jumps (opcodes 01-0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

development system support

The TMS370 family development support tools include an assembler, a C compiler, a linker, an in-circuit emulator (XDS22 – extended development support), compact development tool, and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
 - Includes extensive macro capability
 - Allows high-speed operation
 - Provides format conversion utilities for popular formats.
- ANSI C Compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, Sun-3™ or Sun-4™)
 - Generates assembly code for the TMS370 that can be inspected easily
 - Improves code execution speed and reduces code size with optional optimizer pass
 - Enables direct reference to the TMS370's port registers by using a naming convention
 - Provides flexibility in specifying the storage for data objects
 - Interfaces C functions and assembly functions easily
 - Includes assembler and linker
- CDT370 (compact development tool) real-time in-circuit emulation
 - Base (Part Number EDSCDT370 – for PC, requires cable)
 - Cable for 28-pin PLCC (Part No. EDSTRG28PLCCCX)
 - Cable for 28-pin DIP (Part No. EDSTRG28DILCX)
 - Includes EEPROM and EPROM programming support
 - Allows inspection and modification of memory locations
 - Allows uploading/downloading program and data memory
 - Executes programs and software routines
 - Includes 1024 samples trace buffer
 - Provides single-step executable instructions
 - Uses software breakpoints to halt program execution at selected address
- XDS/22 (extended development support) in-circuit emulator
 - Base (Part Number TMDS3762210 for PC, requires cable)
 - Cable for 28-pin DIP/ PLCC (Part No. TMDS3788828)
 - Contains all of the features of the CDT370 described previously but does not have the capability to program the data EEPROM and program EPROM
 - Contains sophisticated breakpoint trace and timing hardware that provides up to 2047 qualified trace samples with symbolic disassembly
 - Allows qualification of breakpoints by address and/or data on any type of memory acquisition. Up to four levels of events can be combined to cause a breakpoint

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development system support (continued)

- Provides timers for analyzing total and average time in routines
- Contains an eight-line logic probe for adding visibility of external signals to the breakpoint qualifier and for tracing display
- Microcontroller programmer
 - Base (Part No. TMDS3760500A – for PC, requires programmer head)
 - Single unit head for 28-pin PLCC (Part No. TMDS3780510A)
 - Single unit head for 28-pin DIP (Part No. TMDS3780511A)
 - Personal computer based, window/function-key-oriented user interface for ease of use and rapid learning environment
- Design kit (Part No. TMDS3770110 – for PC)
 - Includes TMS370 Application Board and TMS370 Assembler diskette and documentation
 - Supports quick evaluation of TMS370 functionality
 - Provides capability to upload and download code
 - Provides capability to execute programs and software routines and to single-step executable instructions
 - Provides software breakpoints to halt program execution at selected addresses
 - Includes wire-wrap prototype area
 - Includes reverse assembler
- Starter Kit (Part No. TMDX37000 – For PC)
 - Includes TMS370 Assembler diskette and documentation
 - Includes TMS370 Simulator
 - Includes programming adapter board and programming software
 - Does not include (to be supplied by the user):
 - + 5 V power supply
 - ZIF sockets
 - Nine-pin RS232 cable



device numbering conventions

Figure 14 illustrates the numbering and symbol nomenclature for the TMS370CxCx family.

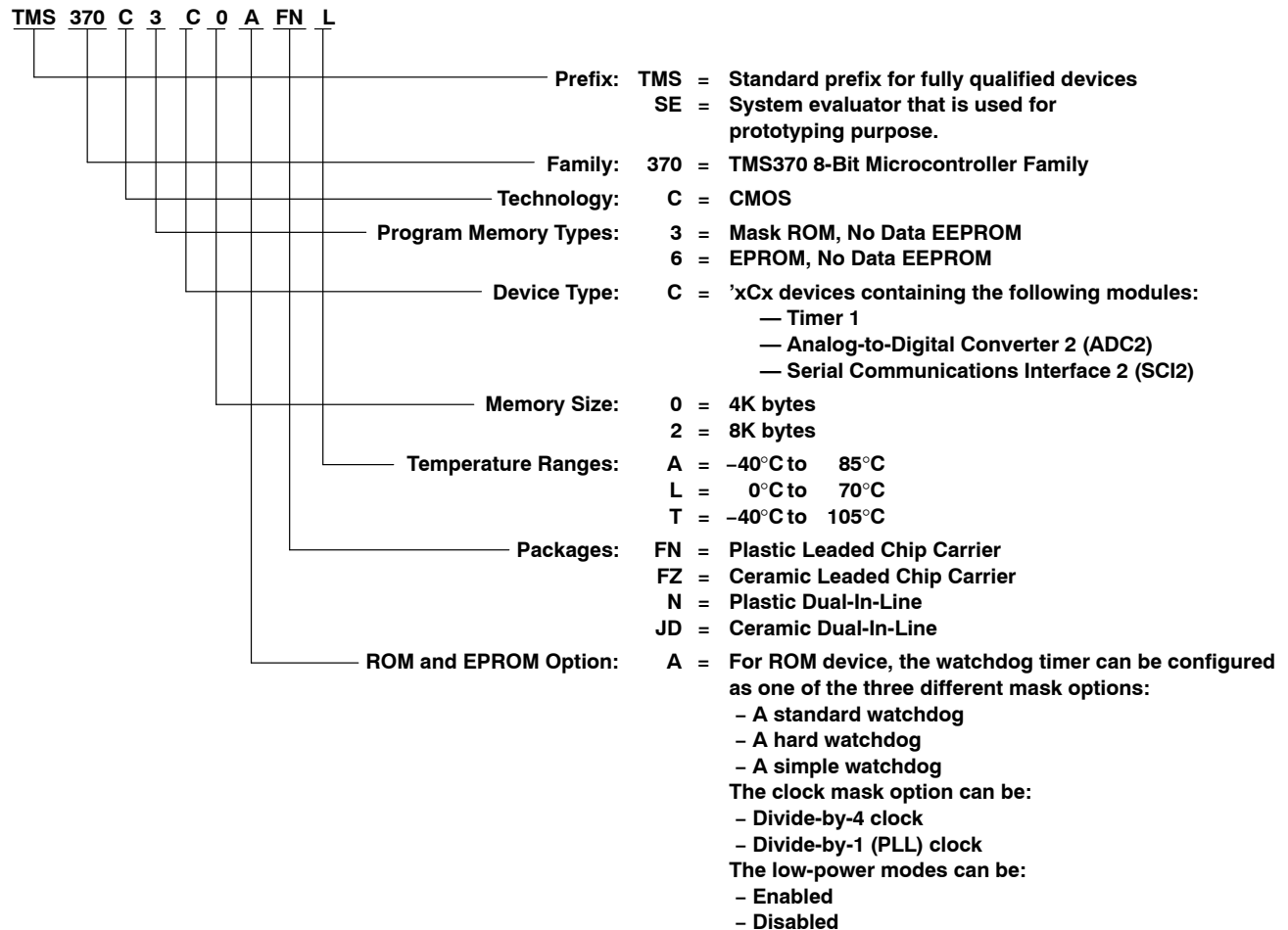


Figure 14. TMS370CxCx Family Nomenclature

TMS370CxCx

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device part numbers

Table 37 lists all of the 'xCx devices available. The devices' part number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog timer options desired. Each device can have only one of the three possible watchdog timer options and one of the two clock options. The required options information pertains solely to orders involving ROM devices.

Table 37. Device Part Numbers

DEVICE PART NUMBERS	
FOR 28 PINS (LCC)	FOR 28 PINS (DIP)
TMS370C3C0AFNA TMS370C3C0AFNL TMS370C3C0AFNT	TMS370C3C0ANA TMS370C3C0ANL TMS370C3C0ANT
TMS370C6C2AFNT	TMS370C6C2ANT
SE370C6C2AFZT [†]	SE370C6C2AJDT [†]

[†] System evaluators are for use in prototype environment and their reliability has not been characterized.

new code release form

Figure 15 shows a sample of the new code release form.

NEW CODE RELEASE FORM TEXAS INSTRUMENTS TMS370 MICROCONTROLLER PRODUCTS		DATE: _____																
To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information:																		
1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media) 2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.																		
Company Name: _____ Street Address: _____ Street Address: _____ City: _____ State _____ Zip _____ Customer Part Number: _____ Customer Application: _____		Contact Mr./Ms.: _____ Phone: (_____) _____ Ext.: _____ Customer Purchase Order Number: _____ Customer Print Number *Yes: _____ # _____ No: _____ (Std. spec to be followed) *If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.																
TMS370 Device: _____ TI Customer ROM Number: _____ (provided by Texas Instruments)																		
OSCILLATOR FREQUENCY <table border="0" style="width: 100%; margin-top: 5px;"> <tr> <td style="width: 30%;"></td> <td style="width: 10%; text-align: center;">MIN</td> <td style="width: 10%; text-align: center;">TYP</td> <td style="width: 10%; text-align: center;">MAX</td> </tr> <tr> <td>☐ External Drive (CLKIN)</td> <td>_____</td> <td>_____</td> <td>_____</td> </tr> <tr> <td>☐ Crystal</td> <td>_____</td> <td>_____</td> <td>_____</td> </tr> <tr> <td>☐ Ceramic Resonator</td> <td>_____</td> <td>_____</td> <td>_____</td> </tr> </table> ☐ Supply Voltage MIN: _____ MAX: _____ (std range: 4.5V to 5.5V)				MIN	TYP	MAX	☐ External Drive (CLKIN)	_____	_____	_____	☐ Crystal	_____	_____	_____	☐ Ceramic Resonator	_____	_____	_____
	MIN	TYP	MAX															
☐ External Drive (CLKIN)	_____	_____	_____															
☐ Crystal	_____	_____	_____															
☐ Ceramic Resonator	_____	_____	_____															
TEMPERATURE RANGE <table border="0" style="width: 100%; margin-top: 5px;"> <tr> <td style="width: 30%;">☐ 'L':</td> <td style="width: 70%;">0° to 70°C (standard)</td> </tr> <tr> <td>☐ 'A':</td> <td>-40° to 85°C</td> </tr> <tr> <td>☐ 'T':</td> <td>-40° to 105°C</td> </tr> </table>			☐ 'L':	0° to 70°C (standard)	☐ 'A':	-40° to 85°C	☐ 'T':	-40° to 105°C										
☐ 'L':	0° to 70°C (standard)																	
☐ 'A':	-40° to 85°C																	
☐ 'T':	-40° to 105°C																	
SYMBOLIZATION <table border="0" style="width: 100%; margin-top: 5px;"> <tr> <td style="width: 30%;">☐ TI standard symbolization</td> <td style="width: 70%;"></td> </tr> <tr> <td>☐ TI standard w/customer part number</td> <td></td> </tr> <tr> <td>☐ Customer symbolization</td> <td></td> </tr> <tr> <td colspan="2">(per attached spec, subject to approval)</td> </tr> </table>			☐ TI standard symbolization		☐ TI standard w/customer part number		☐ Customer symbolization		(per attached spec, subject to approval)									
☐ TI standard symbolization																		
☐ TI standard w/customer part number																		
☐ Customer symbolization																		
(per attached spec, subject to approval)																		
NON-STANDARD SPECIFICATIONS: ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.																		
RELEASE AUTHORIZATION: This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cycletime commences when this document is signed off and the verification code is approved by the customer.																		
<table border="0" style="width: 100%;"> <tr> <td style="width: 50%; vertical-align: top;"> 1. Customer: _____ Date: _____ </td> <td style="width: 50%; vertical-align: top;"> 2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____ </td> </tr> </table>			1. Customer: _____ Date: _____	2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____														
1. Customer: _____ Date: _____	2. TI: Field Sales: _____ Marketing: _____ Prod. Eng.: _____ Proto. Release: _____																	

CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS

Low Power Modes ☐ Enabled ☐ Disabled	Watchdog counter ☐ Standard ☐ Hard Enabled ☐ Simple Counter	Clock Type ☐ Standard (/4) ☐ PLL (/1)

NOTE:
 Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B).

PACKAGE TYPE

☐ 'N' 28-pin PDIP ☐ "FN" 28-pin PLCC ☐ "N" 40-pin PDIP ☐ "NJ" 40-pin PSDIP (formerly known as N2)	☐ "FN" 44-pin PLCC ☐ "FN" 68-pin PLCC ☐ "NM" 64-pin PSDIP

BUS EXPANSION

☐ YES	☐ NO

Figure 15. Sample New Code Release Form

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Table 38 is a collection of all the peripheral file frames used in the 'CxCx (provided for a quick reference).

Table 38. Peripheral File Frame Compilation

		System Configuration Registers								
PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG	
P010	COLD START	OSC POWER	PF AUTO WAIT	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0	
P011	—	—	—	AUTO WAIT DISABLE	—	MEMORY DISABLE	—	—	SCCR1	
P012	HALT / STANDBY	PWRDWN / IDLE	—	BUS STEST	CPU STEST	—	INT1 NMI	PRIVILEGE DISABLE	SCCR2	
P013 to P016	Reserved									
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1	
P018 to P01B	Reserved									
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL	
P01D to P01F	Reserved									
Digital Port-Control Registers										
P020	Reserved									APORT1
P021	Port A Control Register 2 (must be 0)									APORT2
P022	Port A Data									ADATA
P023	Port A Direction									ADIR
P024 to P02B	Reserved									
P02C	Port D Control Register 1 (must be 0)		—	Port D Control Register 1 (must be 0)		—	—	—	DPORT1	
P02D	Port D Control Register 2 (must be 0) [†]		—	Port D Control Register 2 (must be 0) [†]		—	—	—	DPORT2	
P02E	Port D Data		—	Port D Data		—	—	—	DDATA	
P02F	Port D Direction		—	Port D Direction		—	—	—	DDIR	
Timer 1 Module Register Memory Map										
Modes: Dual-Compare and Capture/Compare										
P040	Bit 15			T1Counter MSbyte				Bit 8		T1CNTR
P041	Bit 7			T1 Counter LSbyte				Bit 0		
P042	Bit 15			Compare Register MSbyte				Bit 8		T1C
P043	Bit 7			Compare Register LSbyte				Bit 0		
P044	Bit 15			Capture/Compare Register MSbyte				Bit 8		T1CC
P045	Bit 7			Capture/Compare Register LSbyte				Bit 0		
P046	Bit 15			Watchdog Counter MSbyte				Bit 8		WDCNTR
P047	Bit 7			Watchdog Counter LSbyte				Bit 0		
P048	Bit 7			Watchdog Reset Key				Bit 0		WDRST

[†] To configure pin D3 as SYSCLK, set port D control register 2 = 08h.



Table 38. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
Mode: Dual-Compare and Capture/Compare (Continued)									
P049	WD OVRFL TAP SEL [†]	WD INPUT SELECT2 [†]	WD INPUT SELECT1 [†]	WD INPUT SELECT0 [†]	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA [†]	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
Mode: Dual-Compare									
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE=0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
Mode: Capture/Compare									
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
Modes: Dual-Compare and Capture/Compare									
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	T1 STEST	T1 PRIORITY	—	—	—	—	—	—	T1PRI
SCI2 Module Control Memory Map									
P050	STOP BITS	EVEN/ODD PARITY	PARITY EN- ABLE	—	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RE- SET	—	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	Reserved								
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF
P05A to P05D	Reserved								
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	SCI STEST	SCITX PRIORITY	SCIRX PRIORITY	SCI ESPEN	—	—	—	—	SCIPRI

[†] Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

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Table 38. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
ADC2 Module Control Registers									
P070	CONVERT START	SAMPLE START	—	REF VOLT SELECT1	REF VOLT SELECT0	—	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A-to-D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	—	—	—	—	Port E Data Input Register				ADIN
P07E	—	—	—	—	Port E Input Enable Register				ADENA
P07F	AD STEST	AD PRIORITY	AD ESPEN	—	—	—	—	—	ADPRI

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 2)	–0.6 V to 7 V
Input voltage range, All pins except MC	–0.6 V to 7 V
MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC}) (see Note 3)	±10 mA
Maximum I_{CC} current	170 mA
Maximum I_{SS} current	–170 mA
Continuous power dissipation	500 mW
Operating free-air temperature range, T_A : L version	0°C to 70°C
A version	–40°C to 85°C
T version	–40°C to 105°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. Unless otherwise noted, all voltage values are with respect to V_{SS} .

3. Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 2)		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 4)		3		5.5	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and RESET	2		V_{CC}	V
		XTAL2/CLKIN	0.8 V_{CC}		V_{CC}	
		RESET	0.7 V_{CC}		V_{CC}	
V_{MC}	MC (mode control) voltage	EPROM programming voltage (V_{PP})	13	13.2	13.5	V
		Microcomputer	V_{SS}		0.3	
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	
		T version	–40		105	

NOTES: 2. Unless otherwise noted, all voltage values are with respect to V_{SS} .

4. RESET must be activated externally when V_{CC} or SYSCLK is out of the recommended operating range.

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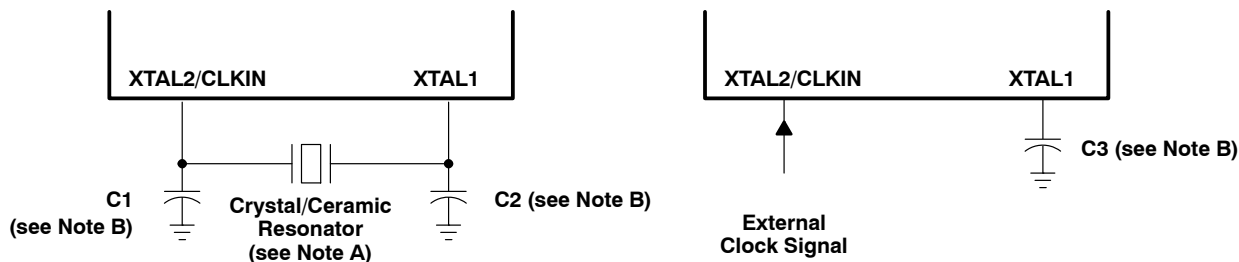
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OL}	Low-level output voltage	I _{OL} = 1.4 mA			0.4	V
V _{OH}	High-level output voltage	I _{OH} = -50 µA	0.9 V _{CC}			V
		I _{OH} = -2 mA	2.4			
I _I	Input current	0 V ≤ V _I ≤ 0.3 V			10	µA
		0.3 V < V _I ≤ 13 V			650	
		12 V ≤ V _I ≤ 13 V See Note 5			50	mA
	I/O pins	0 V ≤ V _I ≤ V _{CC}			± 10	µA
I _{OL}	Low-level output current	V _{OL} = 0.4 V	1.4			mA
I _{OH}	High-level output current	V _{OH} = 0.9 V _{CC}	- 50			µA
		V _{OH} = 2.4 V	- 2			mA
I _{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 8)	See Notes 6 and 7 SYSCLK = 5 MHz		20	36	mA
		See Notes 6 and 7 SYSCLK = 3 MHz		13	25	
		See Notes 6 and 7 SYSCLK = 0.5 MHz		5	11	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 9)	See Notes 6 and 7 SYSCLK = 5 MHz		10	17	mA
		See Notes 6 and 7 SYSCLK = 3 MHz		6.5	11	
		See Notes 6 and 7 SYSCLK = 0.5 MHz		2	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 10)	See Notes 6 and 7 SYSCLK = 3 MHz		4.5	8.6	mA
		See Notes 6 and 7 SYSCLK = 0.5 MHz		1.5	3.0	
	Supply current (HALT mode)	See Note 6 XTAL2/CLKIN < 0.2 V		1	30	µA

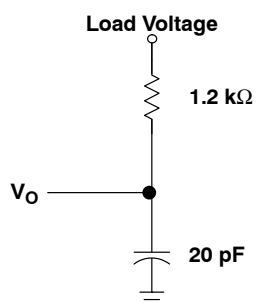
- NOTES: 5. Input current I_{pp} is a maximum of 50 mA only when you are programming EPROM.
6. Single chip mode, ports configured as inputs or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} - 0.2 V.
7. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = 0.01 mA x (total load capacitance + crystal capacitance in pF).
8. Maximum operating current = 5.6 (SYSCLK) + 8 mA.
9. Maximum standby current = 3 (SYSCLK) + 2 mA. (OSC POWER bit = 0).
10. Maximum standby current = 2.24 (SYSCLK) + 1.9 mA. (OSC POWER bit = 1, only valid up to 3 MHz (SYSCLK)).





NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
B. The values of C1 and C2 are typically 15 pF and the value of C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 16. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH} = 2.4 \text{ V}$; Load Voltage = 0 V
Case 2: $V_O = V_{OL} = 0.4 \text{ V}$; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 17. Typical Output Load Circuit (See Note A)

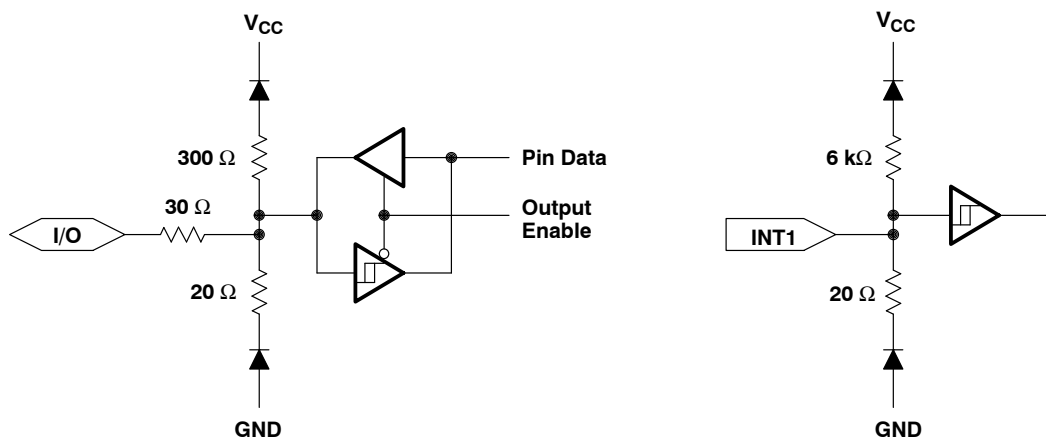


Figure 18. Typical Buffer Circuitry

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PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

AR	Array	RXD	SCIRXD
B	Byte	SC	SYSCLK
CI	XTAL2/CLKIN	TXD	SCITXD

Lowercase subscripts and their meanings are:

c	cycle time (period)	su	setup time
d	delay time	v	valid time
f	fall time	w	pulse duration (width)
r	rise time		

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid

All timings are measured between high and low measurement points as indicated in Figure 19 and Figure 20.

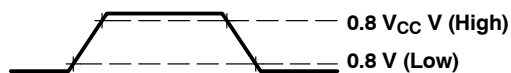


Figure 19. XTAL2/CLKIN Measurement Points

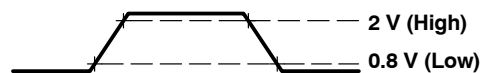


Figure 20. General Measurement Points

external clocking requirements for divide-by-4 clock (see Note 11 and Figure 21)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 12)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$ Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN Crystal operating frequency	2	20	MHz
	SYSCLK Internal system clock operating frequency [†]	0.5	5	MHz

[†] SYSCLK = CLKIN/4

NOTES: 11. For V_{IL} and V_{IH} , refer to recommended operating conditions.

12. This pulse can be either a high pulse which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

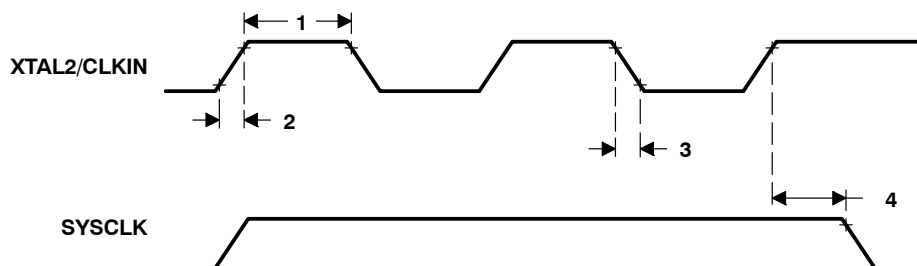


Figure 21. External Clock Timing for Divide-by-4

external clocking requirements for divide-by-1 clock (PLL) (see Note 11 and Figure 22)

NO.	PARAMETER	MIN	MAX	UNIT
1	$t_{w(CI)}$ Pulse duration, XTAL2/CLKIN (see Note 12)	20		ns
2	$t_{r(CI)}$ Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$ Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$ Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN Crystal operating frequency	2	5	MHz
	SYSCLK Internal system clock operating frequency [‡]	2	5	MHz

[‡] SYSCLK = CLKIN/1

NOTES: 11. For V_{IL} and V_{IH} , refer to recommended operating conditions.

12. This pulse can be either a high pulse which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

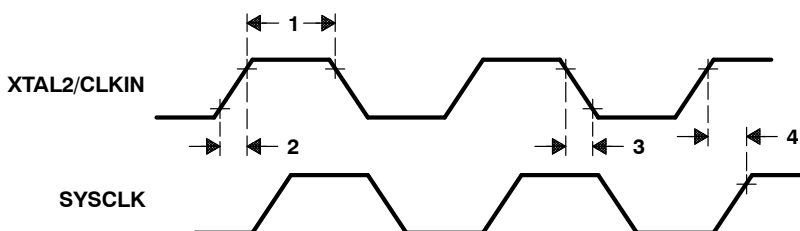


Figure 22. External Clock Timing for Divide-by-1

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switching characteristics and timing requirements (see Note 13 and Figure 23)

NO.	PARAMETER		MIN	MAX	UNIT
5	t_c	Cycle time, SYSCLK (system clock)	200	2000	ns
			200	500	
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low	$0.5 t_c - 20$	$0.5 t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high	$0.5 t_c$	$0.5 t_c + 20$	ns

NOTE 13: t_c = system clock cycle time = $1 / \text{SYSCLK}$

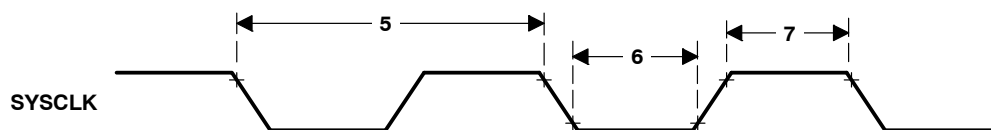


Figure 23. SYSCLK Timing

general purpose output signal switching time requirements (see Figure 24)

	MIN	NOM	MAX	UNIT
t_r Rise time		30		ns
t_f Fall time		30		ns

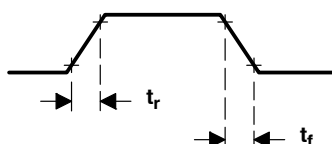


Figure 24. Signal Switching Time

recommended EPROM operating conditions for programming

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5.5	6	V
V_{PP} Supply voltage at MC pin	13	13.2	13.5	V
I_{PP} Supply current at MC pin during programming ($V_{PP} = 13 \text{ V}$)		30	50	mA
SYSCLK System clock operating frequency	Divide-by-4	0.5	5	MHz
	Divide-by-1	2	5	

recommended EPROM timing requirements for programming

	MIN	NOM	MAX	UNIT
$t_{w(EPGM)}$ Pulse duration, programming signal (see Note 14)	0.40	0.50	3	ms

NOTE 14: Programming pulse is active when both EXE (EPCTL.0) and VPPS (EPCTL.6) are set.



ADC2

The ADC2 share the V_{CC} power bus for its analog and digital circuitry. All ADC2 specifications are given with respect to V_{SS} unless otherwise noted.

Resolution 8 bits (256 values)
 Monotonic Yes
 Output conversion code 00h to FFh (00h for $V_I \leq V_{SS}$; FFh for $V_I \geq V_{ref}$)
 Conversion time (excluding sample time) $164t_c$

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Analog supply voltage	4.5	5	5.5	V
V_{ref} Non- V_{CC} reference [†]	2.5	V_{CC}	$V_{CC} + 0.1$	V
Analog input for conversion	V_{SS}		V_{ref}	V

[†] V_{ref} must be stable, within $\pm 1/2$ LSB of the required resolution, during the entire conversion time.

operating characteristics over full ranges of recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Absolute accuracy (see Note 15)	$V_{CC} = 5.5$ V, $V_{ref} = 5.1$ V		+1.5	LSB
Differential/integral linearity error (see Notes 15 and 16)	$V_{CC} = 5.5$ V, $V_{ref} = 5.1$ V		± 0.9	LSB
I_{CC} Analog supply current	Converting		2	mA
	Not Converting		5	μ A
I_I Input current, AN0-AN3	$0 \text{ V} \leq V_I \leq 5.5 \text{ V}$		2	μ A
I_{ref} Input charge current			1	mA
Z_{ref} Source impedance V_{ref}	$\text{SYSCLK} \leq 3 \text{ MHz}$		24	k Ω
	$3 \text{ MHz} < \text{SYSCLK} \leq 5 \text{ MHz}$		10	k Ω

NOTES: 15. Absolute resolution = 20 mV. At $V_{ref} = 5$ V, this is 1 LSB. As V_{ref} decreases, LSB size decreases and thus absolute accuracy and differential / integral linearity errors in terms of LSBs increases.

16. Excluding quantization error of $1/2$ LSB.

TMS370CxTx

8-BIT MICROCONTROLLER

SPNS040A – NOVEMBER 1995 – REVISED MARCH 1996

ADC2 (continued)

The ADC2 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined such that high-impedance sources can be accommodated without penalty to low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC2 control register (ADCTL) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START) of the ADCTL is set to 1. After a hold time, the converter resets the SAMPLE START and CONVERT START bits, signaling that a conversion has started and the analog signal can be removed.

analog timing requirements

		MIN	MAX	UNIT
$t_{su(S)}$	Setup time, analog input to sample command	0		ns
$t_{h(AN)}$	Hold time, analog input from start of conversion	$18t_c$		ns
$t_w(S)$	Pulse duration, sample time per kilohm of source impedance (see Note 17)	1		$\mu s/k\Omega$

NOTE 17: The value given is valid for a signal with a source impedance $> 1\text{ k}\Omega$. If the source impedance is $< 1\text{ k}\Omega$, use a minimum sampling time of $1\text{ }\mu s$.

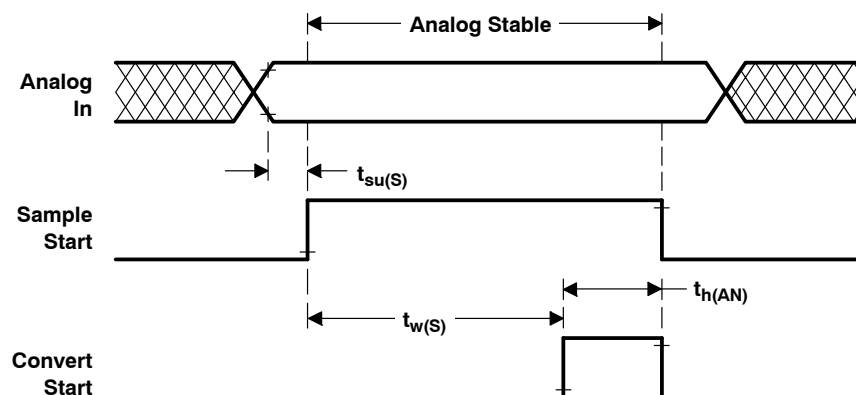


Figure 25. Analog Timing

Table 39 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

Table 39. TMS370CxTx Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 28 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C3C0AFNA TMS370C3C0AFNL TMS370C3C0AFNT TMS370C6C2AFNT
FZ – 28 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C6C2AFZT
JD – 28 pin (70-mil pin spacing)	CERAMIC SHRINK DUAL-IN-LINE PACKAGE (CSDIP)	JD(R-CDIP-T**) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE	SE370C6C2AJDT
N – 28 pin (100-mil pin spacing)	PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	N(R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE	TMS370C3C0ANA TMS370C3C0ANL TMS370C3C0ANT TMS370C6C2ANT

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TMS370Cx5x Data Sheet	10
TMS370Cx6x Data Sheet	11
TMS370Cx7x Data Sheet	12
TMS370Cx8x Data Sheet	13
TMS370Cx9x Data Sheet	14
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introduction to mechanical drawings

Table 1 is designed to aid the user when referencing a device family to the mechanical data section. The table shows a cross-reference of the device family to the TMS370 generic package names and the associated mechanical drawing(s) by drawing number and name.

Table 1. TMS370 Family Package Type and Mechanical Cross-Reference

PACAKGE TYPE (mil pin spacing)	TMS370 GENERIC NAME	PACAKGE TYPE NUMBER AND MECHANICAL NAME	FAMILY MEMBERS†
FN – 28 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370Cx0x, TMS370Cx1x, and TMS370CxCx
FN – 44 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370Cx2x, TMS370Cx32, TMS370Cx36, TMS370Cx4x, TMS370Cx8x, and TMS370Cx9x
FN – 68 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370Cx5x, TMS370Cx6x, TMS370Cx7x, and TMS370CxBx
FZ – 28 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370Cx0x, SE370Cx1x, and SE370CxCx
FZ – 44 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370Cx2x, SE370Cx32, SE370Cx36, SE370Cx4x, SE370Cx8x, and SE370Cx9x
FZ – 68 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370Cx5x, SE370Cx6x, and SE370Cx7x
JD – 28 pin (100-mil pin spacing)	CERAMIC DUAL-IN-LINE PACKAGE (CDIP)	JD(R-CDIP-T**) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE	SE370Cx1x and SE370CxCx
JD – 40 pin (100-mil pin spacing)	CERAMIC DUAL-IN-LINE PACKAGE (CDIP)	JD(R-CDIP-T**) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE	SE370Cx2x and SE370Cx4x
N – 28 pin (100-mil pin spacing)	PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	N(R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE	TMS370Cx1x and TMS370CxCx
N – 40 pin (100-mil pin spacing)	PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	N(R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE	TMS370Cx2x, TMS370Cx4x, TMS370Cx8x, and TMS370CxAx
JC – 40 pin (70-mil pin spacing)	CERAMIC SHRINK DUAL-IN-LINE PACKAGE (CSDIP)	JC(R-CDIP-T40) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE	SE370Cx2x, SE370Cx4x, and SE370Cx9x
NJ – 40 pin (70-mil pin spacing)‡	PLASTIC SHRINK DUAL-IN-LINE PACKAGE (PSDIP)	NJ(R-PDIP-T**) PLASTIC SHRINK DUAL-IN-LINE PACKAGE	TMS370Cx2x, TMS370Cx4x, and TMS370Cx9x
JN – 64 pin (70-mil pin spacing)	CERAMIC SHRINK DUAL-IN-LINE PACKAGE (CSDIP)	JN(R-CDIP-T64) CERAMIC DUAL-IN-LINE PACKAGE	SE370Cx5x and SE370Cx7x
NM – 64 pin (70-mil pin spacing)	PLASTIC SHRINK DUAL-IN-LINE PACKAGE (PSDIP)	NM(R-PDIP-T64) PLASTIC SHRINK DUAL-IN-LINE PACKAGE	TMS370Cx5x, TMS370Cx7x, and TMS370CxBx

† TMS370Cxxx refers to ROM and OTP devices; SE370Cxxx refers to UV-EPROM devices

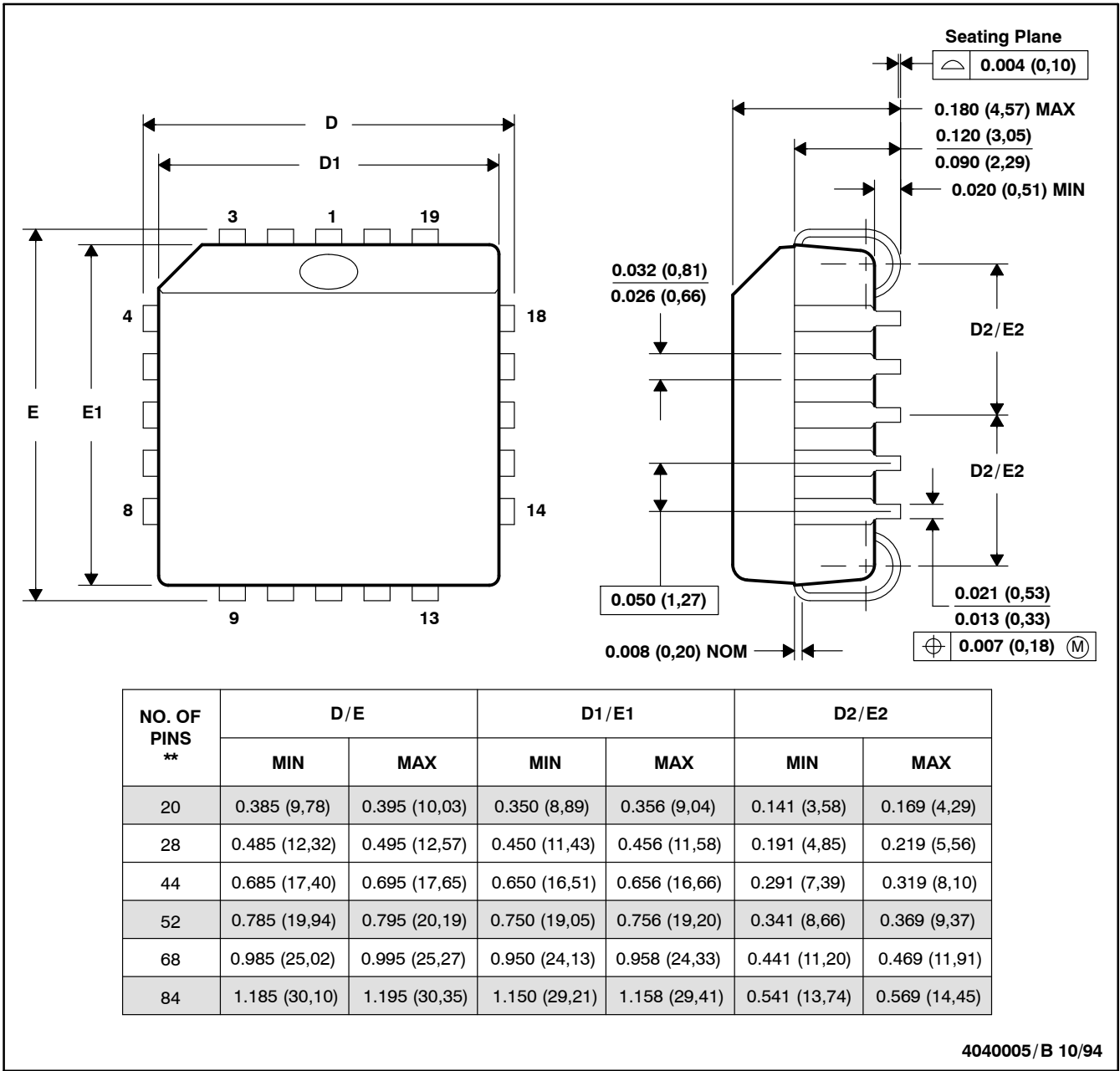
‡ NJ formerly known as N2; the mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

FN 28-, 44-, and 68-pin plastic leaded chip carrier (PLCC)

FN (S-PQCC-J**)

20 PIN SHOWN

PLASTIC J-LEADED CHIP CARRIER



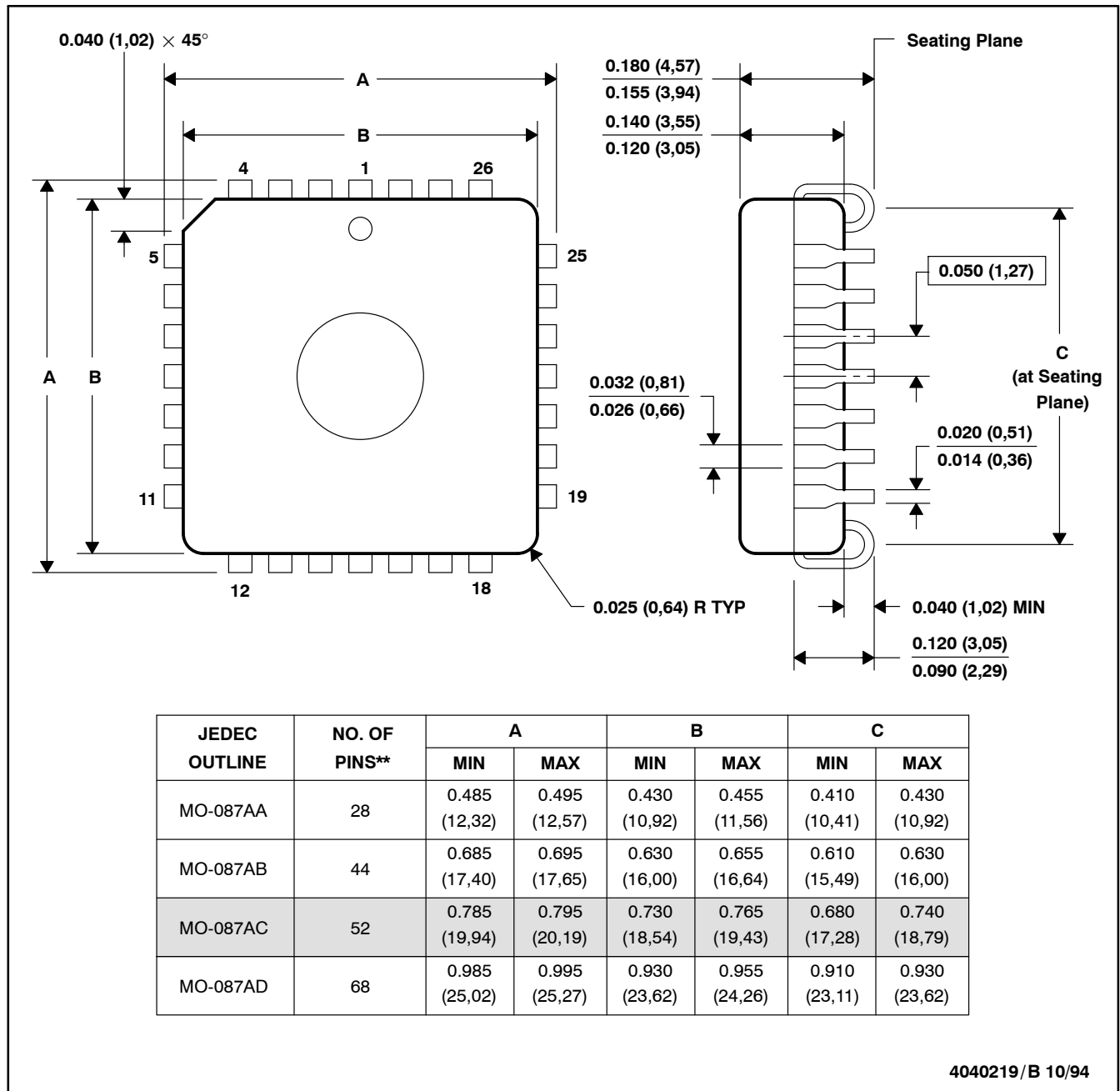
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

FZ 28-, 44-, and 68-pin ceramic leaded chip carrier (CLCC)

FZ (S-CQCC-J**)

J-LEADED CERAMIC CHIP CARRIER

28 LEAD SHOWN



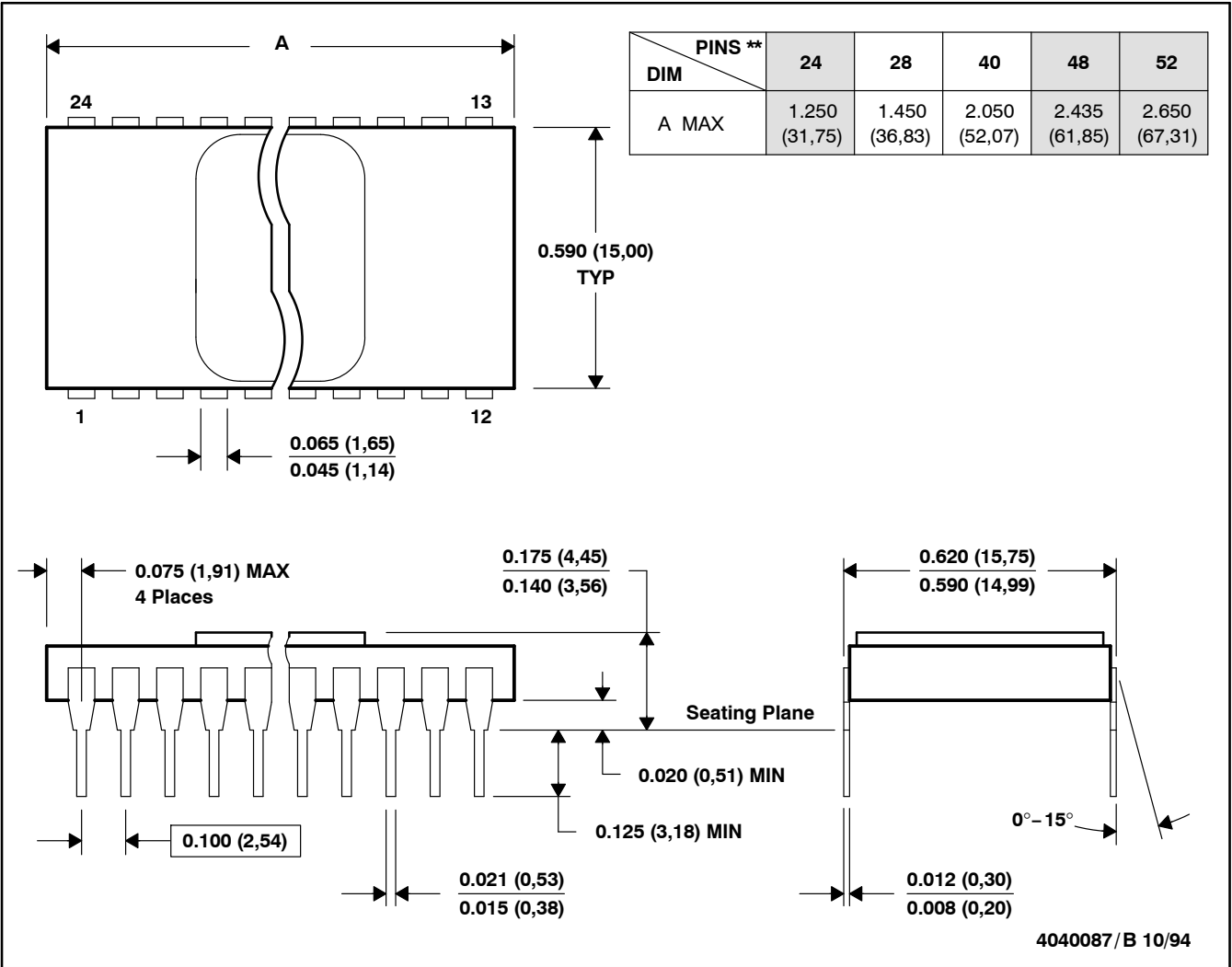
NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.

JD 28- and 40-pin ceramic dual-in-line package (CDIP)

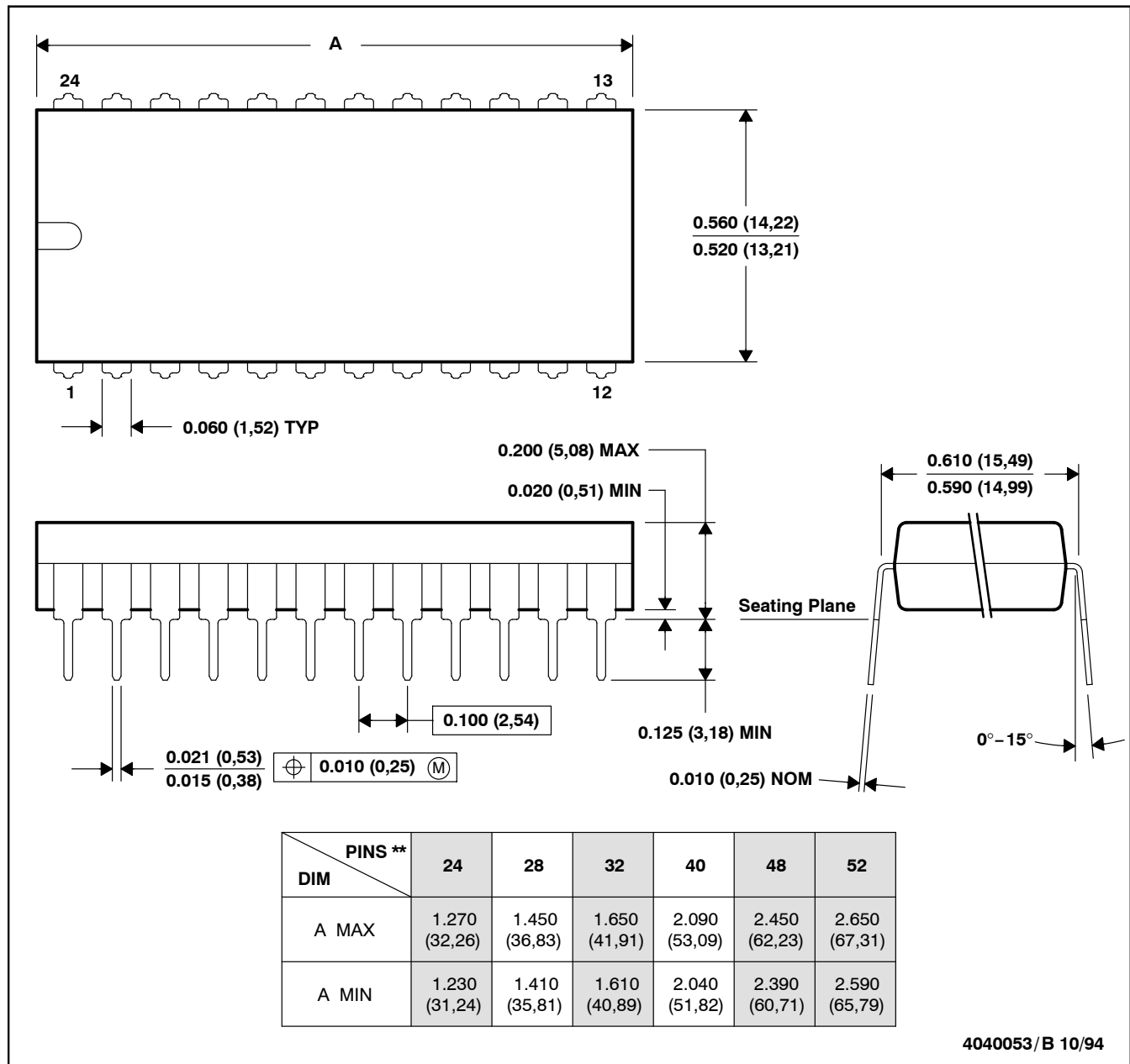
JD (R-CDIP-T**)

CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

24 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

N 28- and 40-pin plastic dual-in-line package (PDIP)**N (R-PDIP-T**)****PLASTIC DUAL-IN-LINE PACKAGE****24 PIN SHOWN**

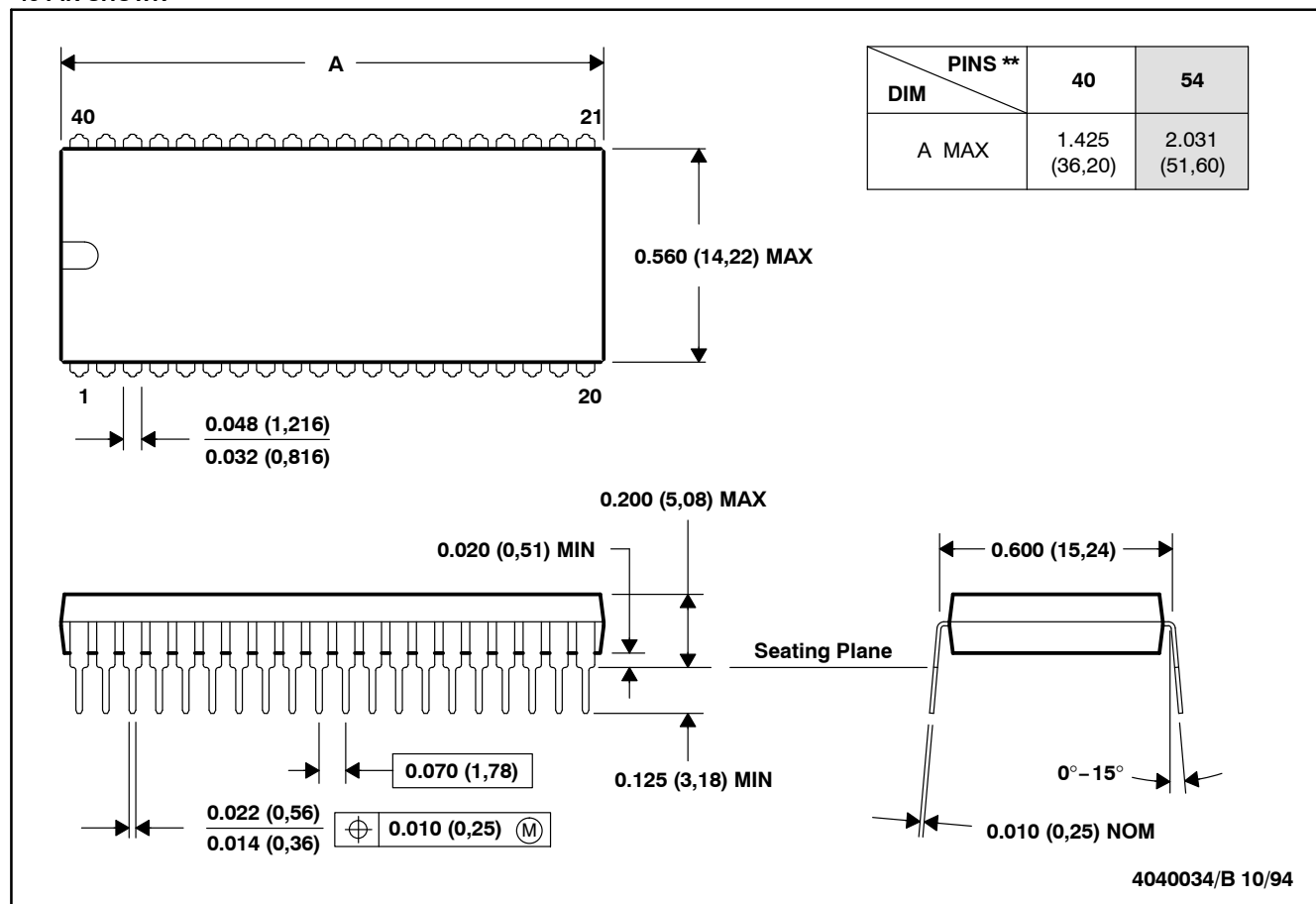
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-011
 D. Falls within JEDEC MS-015 (32 pin only)

NJ 40-pin plastic shrink dual-in-line package (PSDIP)

NJ (R-PDIP-T**)

PLASTIC SHRINK DUAL-IN-LINE PACKAGE

40 PIN SHOWN

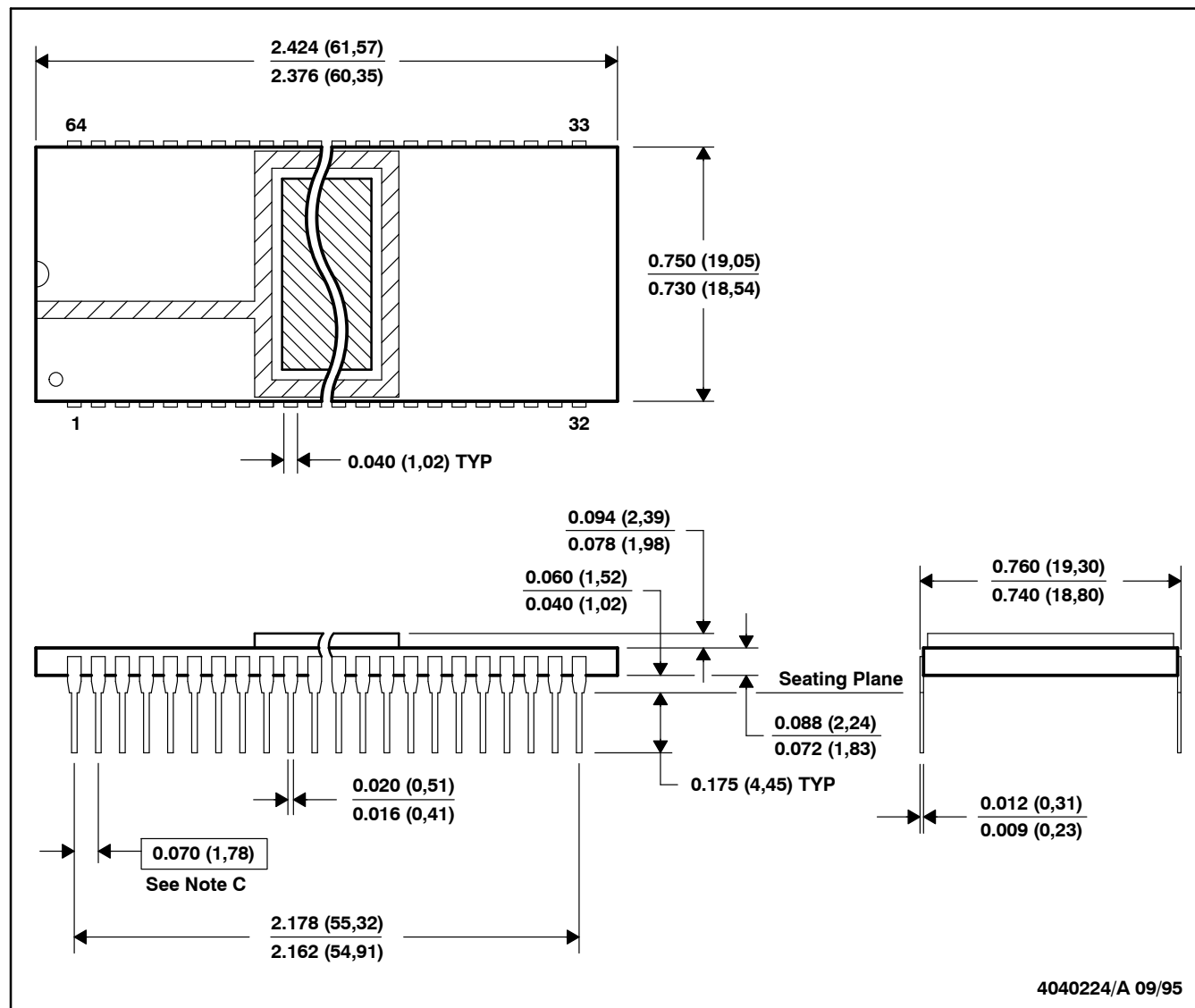


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

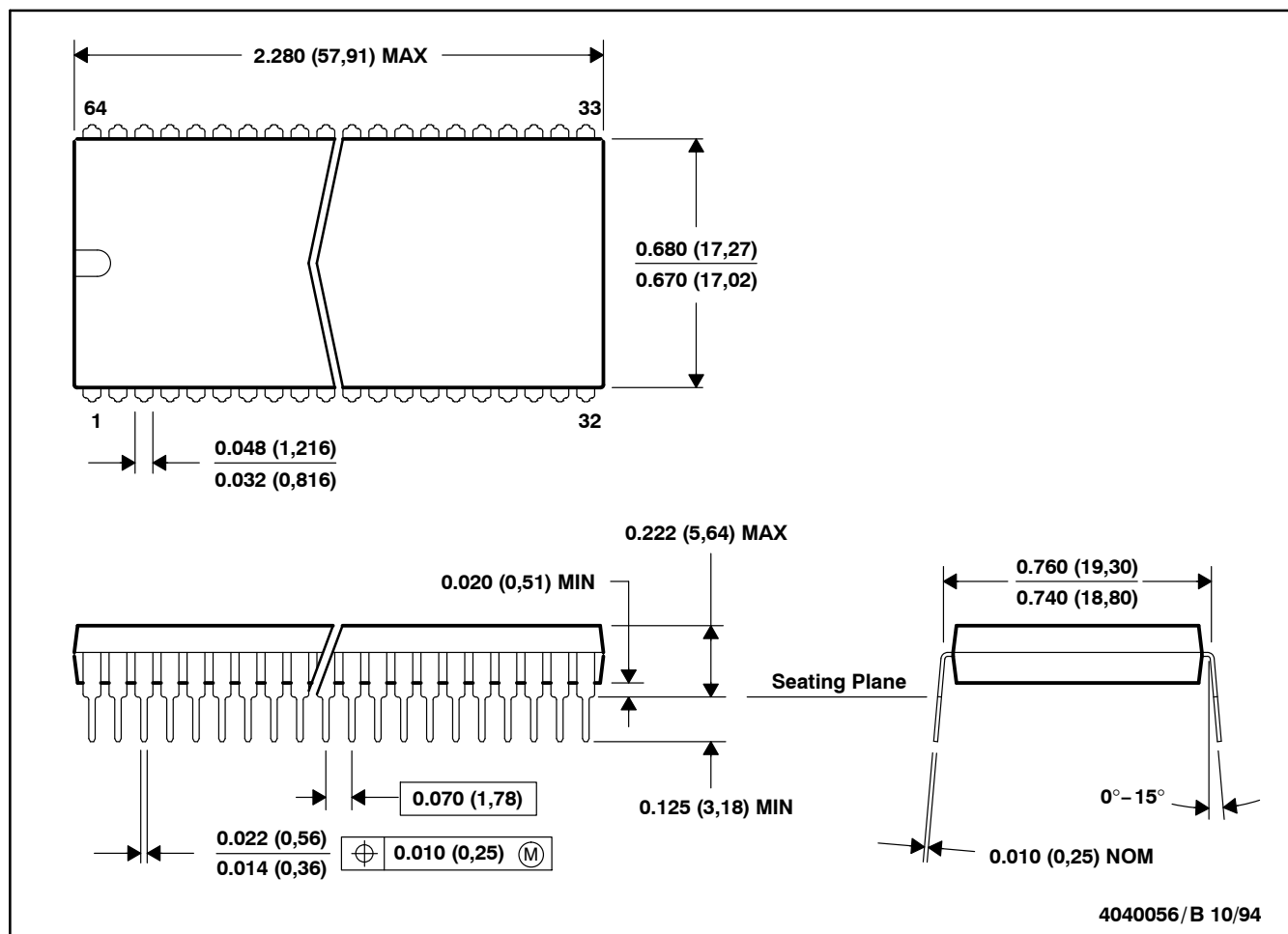
JN 64-pin ceramic shrink dual-in-line package (CSDIP)

JN (R-CDIP-T64)

CERAMIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Each pin centerline located within 0.010 (0,26) of its true longitudinal position.

NM 64-pin plastic shrink dual-in-line package (PSDIP)**NM (R-PDIP-T64)****PLASTIC SHRINK DUAL-IN-LINE PACKAGE**

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

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introduction to quality and reliability

The quality and reliability of Texas Instruments (TI) microprocessor and microcontroller products, which include the TMS370 8-bit microcontrollers and the TMS320 digital signal processors, rely on the following:

- Feedback from customers
- Total manufacturing operation from front-end wafer fabrication to final shipping inspection
- Monitoring of product quality and reliability

The customer's perception of quality is the governing criterion for judging performance. This concept is the basis for TI Corporate Quality Policy, which is as follows:

"For every product or service we offer, we shall define the requirements that solve the customer's problems, and we shall conform to those requirements without exception."

Texas Instruments has developed a leadership reliability qualification system, based on years of experience with leading-edge memory technology and years of research into customer requirements. To achieve constant improvement, programs that support that system respond to customer input and internal information.

This chapter discusses the following major topic: reliability stress tests.

reliability stress tests

Accelerated stress tests are performed on new semiconductor products and process changes to qualify them and to ensure excellence in product reliability. The following test environments are typical:

- High-temperature operating life
- Storage life
- Temperature cycling
- Biased humidity
- Autoclave
- Electrostatic discharge
- Package integrity
- Electromigration
- Channel-hot electrons (performed on geometries of less than 2.0 μm)

Typical events or changes that require internal requalification of a product include the following:

- New die design, shrink, or layout
- Wafer process (baseline/control systems, flow, mask, chemicals, gases, dopants, passivation, or metal systems)
- Packaging assembly (baseline control systems or critical assembly equipment)
- Piece parts (such as lead frame, mold compound, mount material, bond wire, or lead finish)
- Manufacturing site

TI reliability control systems extend beyond qualification. Total reliability controls and management include product reliability monitoring as well as final product release controls. Metal oxide semiconductor (MOS) memories, utilizing high-density active elements, serve as the leading indicator in wafer-process integrity at TI MOS fabrication sites, enhancing all MOS-logic device yields and reliability. Monthly, TI places several thousand MOS devices on reliability tests to ensure and sustain built-in product excellence.

Table 1 lists the microprocessor and microcontroller reliability tests, the duration of the tests, and the size of the samples. Table 2 contains definitions and descriptions of the terms used in these tests.

Table 1. Microprocessor and Microcontroller Tests

TEST	DURATION	SAMPLE SIZE	
		PLASTIC	CERAMIC
Operating life, 125°C, 5.0 V	1000 hrs	129	129
Storage life, 150°C	1000 hrs	45 [†]	45
Biased humidity, 85°C/85% RH, 5 V	1000 hrs	77	–
Autoclave, 121°C, 1 ATM	240 hrs	45	–
Temperature cycle, –65°C to 150°C	1000 cyc [‡]	77	77
Temperature cycle, 0°C to 125° C	3000 cyc	77	77
Thermal shock, –65°C to 150° C	200 cyc	77	77
Electrostatic discharge, ± 2 kV		15	15
Latch-up (CMOS devices only)		5	5
Mechanical sequence		–	22
Thermal sequence		–	22
Thermal/mechanical sequence		–	22
Particle Impact Noise Detection (PIND)		–	45
Internal water vapor		–	3
Solderability		22	22
Solder heat		22	22
Resistance to solvents		15	15
Lead integrity		15	15
Lead pull		22	–
Lead finish adhesion		15	15
Salt atmosphere		15	15
Flammability (UL94-V0)		3	–
Thermal impedance		5	5

[†] If junction temperature does not exceed plasticity of package

[‡] For severe environments; reduced cycles for office environments

Table 2. Definitions of Microprocessor Testing Terms

TERM	DEFINITION/DESCRIPTION	REFERENCES
Average Outgoing Quality (AOQ)	Amount of defective product in a population, usually expressed in terms of parts per million (PPM)	
Failure in Time (FIT)	Estimated field failure rate in number of failures per billion power-on device hours; 1000 FITS equal 0.1% failures per 1000 device hours.	
Operating Life	Device dynamically exercised at a high ambient temperature (usually 125°C) to simulate field usage that would expose the device to a much lower ambient temperature (such as 55°C). Using a derived high temperature, a 55°C ambient failure rate can be calculated.	
Storage Life	Device exposed to 150°C unbiased condition. Bond integrity is stressed in this environment.	
Biased Humidity	Moisture and bias used to accelerate corrosion-type failures in plastic packages. Conditions include 85°C ambient temperature with 85% relative humidity (RH). Typical bias voltage is 5 V and is grounded on alternating pins.	
Autoclave (Pressure Cooker)	Plastic-packaged devices exposed to moisture at 121°C using a pressure of one atmosphere above normal pressure. The pressure forces moisture permeation of the package and accelerates corrosion mechanisms (if present) on the device. External package contaminants can also be activated and caused to generate inter-pin current leakage paths.	
Temperature Cycle	Device exposed to severe temperature extremes in an alternating fashion (–65°C for 15 minutes and 150°C for 15 minutes per cycle) for at least 1000 cycles. Package strength, bond quality, and consistency of assembly process are tested in this environment.	
Electrostatic Discharge (ESD)	Device exposed to electrostatic discharge pulses. Calibration is according to MIL STD 883C, method 3015.6. Devices are stressed to determine failure threshold of the design.	

Table 2. Definitions of Microprocessor Testing Terms (Continued)

TERM	DEFINITION/DESCRIPTION	REFERENCES
Thermal Shock	Test similar to the temperature cycle test, but involving a liquid-to-liquid transfer.	MIL-STD-883C, Method 1011
Particle Impact Noise Detection (PIND)	A nondestructive test to detect loose particles inside a device cavity.	
Mechanical Sequence	Fine and gross leak Mechanical shock PIND (optional) Vibration, variable frequency Constant acceleration Fine and gross leak Electrical test	MIL-STD-883C, Method 1014 MIL-STD-883C, Method 2002, 1500 g, 0.5 ms, Condition B MIL-STD-883C, Method 2020 MIL-STD-883C, Method 2007, 20g, Condition A MIL-STD-883C, Method 2001 MIL-STD-883C, Method 1014 To data sheet limits
Thermal Sequence	Fine and gross leak Solder heat (optional) Temperature cycle (10 cycles minimum) Thermal shock (10 cycles minimum) Moisture resistance Fine and gross leak Electrical test	MIL-STD-883C, Method 1014 MIL-STD-750C, Method 1014 MIL-STD-883C, Method 1010, – 65 to + 150°C, Condition C MIL-STD-883C, Method 1011, – 55 to +125°C, Condition B MIL-STD-883C, Method 1004 MIL-STD-883C, Method 1014 To data sheet limits
Thermal/Mechanical Sequence	Fine and gross leak Temperature cycle (10 cycles minimum) Constant acceleration Fine and gross leak Electrical test Electrostatic discharge Solderability Solder heat Salt atmosphere Lead pull Lead integrity Electromigration Resistance to solvents	MIL-STD-883C, Method 1014 MIL-STD-883C, Method 1010, – 65 to +150°C, Condition C MIL-STD-883C, Method 2001, 30 kg, Y1 Plane MIL-STD-883C, Method 1014 To data sheet limits MIL-STD-883C, Method 3015 MIL-STD-883C, Method 2033 MIL-STD-750C, Method 2031, 10 sec MIL-STD-883C, Method 1009, Condition A, 24 hrs min MIL-STD-883C, Method 2004, Condition A MIL-STD-883C, Method 2004, Condition B1 Accelerated stress testing of con- ductor patterns to ensure accept- able lifetime of power-on operation MIL-STD-883C, Method 2015

Texas Instruments reserves the right to make changes in semiconductor test limits, procedures, or processes without notice. Unless prior arrangements for notification have been made, TI advises all customers to verify current test and manufacturing conditions prior to relying on published data.

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Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies

scope

This guideline establishes the requirements for methods and materials used to protect electronic parts, devices, and assemblies (items) that are susceptible to damage or degradation from electrostatic discharge (ESD). The electrostatic charges referred to in this specification are generated and stored on surfaces of ordinary plastics, most common textile garments, ungrounded person's bodies, and many other commonly unnoticed static generators. The passage of these charges through an electrostatic-sensitive part can result in catastrophic failure or performance degradation of the part.

The part types for which these requirements are applicable include, but are not limited to the following:

- All metal-oxide semiconductor (MOS) devices; e.g., CMOS, PMOS, etc.
- Junction field-effect transistors (JFET)
- Bipolar digital and linear circuits
- Op-amps, monolithic microcircuits with MOS compensating networks, on-board MOS capacitors, or other MOS elements
- Hybrid microcircuits and assemblies containing any of the types of devices listed
- Printed circuit boards and other types of assembly containing static-sensitive devices
- Thin-film passive devices

definitions

- Electrostatic discharge (ESD): A transfer of electrostatic charges between bodies at different electrostatic potentials caused by direct contact or electrostatic field induction.
- Conductive material: Material having a surface resistivity of $10^5 \Omega/\text{square}$ maximum.
- Static dissipative material: Material having a surface resistivity between 10^5 and $10^9 \Omega/\text{square}$.
- Antistatic material: Material having a surface resistivity between 10^9 and $10^{14} \Omega/\text{square}$.
- Surface resistivity: An inverse measure of the conductivity of a material and is the resistance of unit length and unit width of a surface. Note: Surface resistivity of a material is numerically equal to the surface resistance between two electrodes forming opposite sides of a square. The size of the square is immaterial. Surface resistivity applies to both surface- and volume-conductive materials and has the dimension of Ω/square .
- Volume resistivity: Also referred to as bulk resistivity, it is normally determined by measuring the resistance (R) of a square of material (surface resistivity) and multiplying this value by the thickness (T).
- Ionizer: A blower that generates positive and negative ions, either by electrostatic means or from a radioactive energy source in an airstream and distributes a layer of low-velocity ionized air over a work area to neutralize static charges.
- Close proximity: For the purpose of this guideline, six inches or less.

device sensitivity per test circuit of Method 3015, MIL-STD-883C

- Devices are categorized according to their susceptibility to damage resulting from electrostatic discharges (ESD).

Category	ESD Sensitivity
Class 1	0 V – 1999 V
Class 2	2000 V – 3999 V
Class 3	4000 V and above

- At TI, devices are to be protected from ESD damage from receipt at incoming inspection through assembly, test, and shipment of completed equipment.



Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies

applicable reference documents

The following reference documents (of latest issue) can provide additional information on ESD controls.

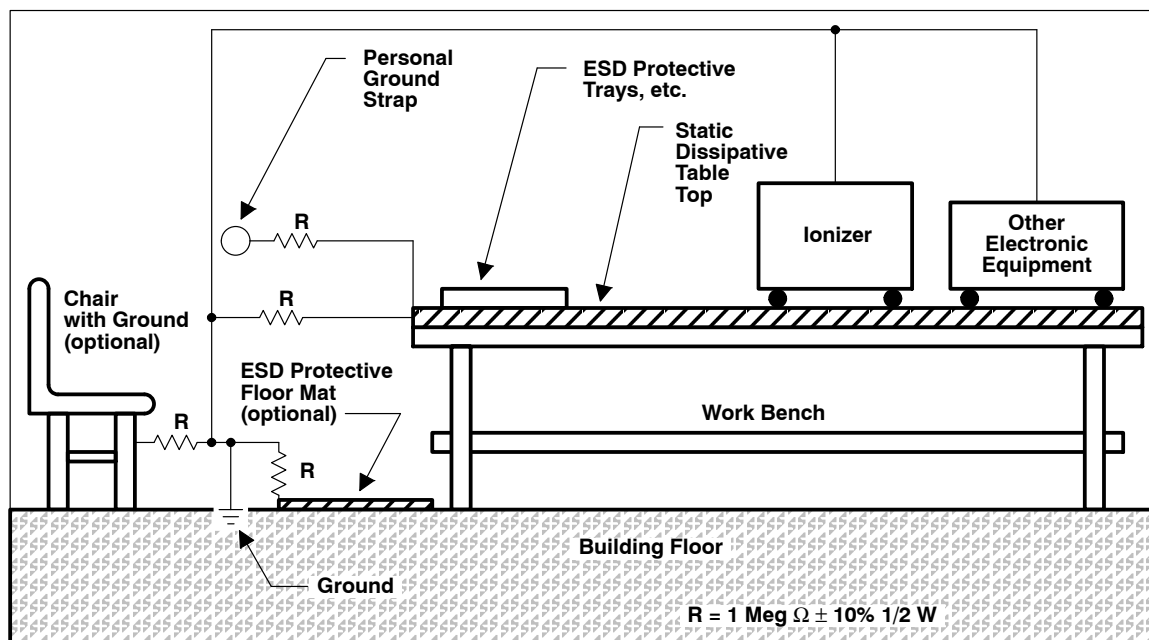
- MIL-M-38510 Microcircuits, General Specification
- MIL-STD-883 Test Methods and Procedures for Microelectronics
- MIL-STD-19491 Semiconductor Devices, Packaging of
- MIL-M-55565 Microcircuits, Packaging of
- DOD-HDBK-263 Electrostatic Discharge Control Handbook for Protection
- DOD-STD-1686 Electrostatic Discharge Control Program
- NAVSEA SE 003-11-TRN-010 Electrostatic Discharge Training Manual
- JEDEC Standard Publication 108

facilities for static-free workstation

The minimum acceptable static-free workstation consists of a work surface covered with static dissipative material attached to ground through a $1\text{ M}\Omega \pm 10\%$ resistor, an attached grounding wrist strap with integral $1\text{ M}\Omega \pm 10\%$ resistor for each operator, and air ionizer(s) of sufficient capacity for each operator. The wrist strap must be connected to the static dissipative material. Ground must utilize the standard building earth ground; refer to Figure 1. Conductive floor tile/carpet along with conductive shoes can be used in lieu of the conductive wrist straps for non-seated personnel. The Site Safety Engineer must review and approve all electrical connections at the static-free workstation prior to its implementation.

Air ionizers must be positioned so that the devices at the static-free workstations are within a 4-foot arc measured by a vertical line from the face of the ionizer and 45 degrees on each side of this line.

General grounding requirements are to be in accordance with Table 1.



All electrical equipment sitting on the conductive table top must be hard grounded but must be isolated from the static dissipative work surface.

NOTE A: Earth ground is not computer ground or RF ground or any other limited-type ground.

Figure 1. Static-Free Workstation

facilities for static-free workstation (continued)

Table 1. General Grounding Requirements

	TREATED WITH ANTI-STATIC SOLUTION OR MADE OF CONDUCTIVE MATERIAL	GROUNDED TO COMMON POINT	STATIC DISSIPATIVE MATERIAL
Handling equipment/handtools	X		X
Metal parts of fixtures and tools/storage racks		X	
Handling trays/tubes	X		X
Soldering irons/baths		X	
Table tops/floor mats	X	X	X
Personnel		X [†]	

[†] Using a wrist strap with 1 M Ω $\pm$ 10% resistor

usage of antistatic solution in areas to control the generation of static charges

The use of antistatic chemicals (antistats) may be a supplemental part of an overall organized ESD program. Any antistatic chemical application must be considered as a means to reduce or eliminate static charge generation on nonconductive materials in the manufacturing or storage areas.

The application of any antistatic chemical in a clean room of class 10,000 or less cannot be permitted. Accordingly, any user of antistatic solutions must consider the following precautions:

- Antistatic spray or solutions in any form cannot be applied to energized electrical parts, assemblies, panels, or equipment.
- Antistatic chemical applications cannot be performed in any area when bare chips, raw parts, packages, and/or personnel are exposed to spray mists and evaporation vapors.

The need for initial application and frequency of reapplication can be established only through routing electrostatic voltage measurements using an electrostatic voltmeter. The following durability schedule is a reasonable expectation.

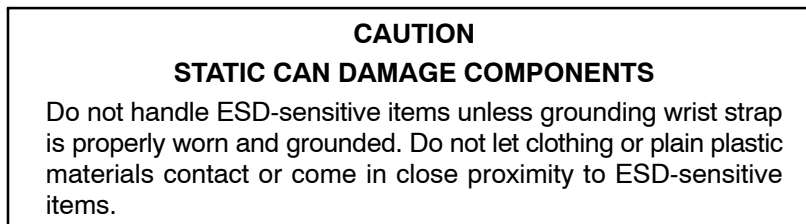
- Soft surfaces (carpet, fabric seats, foam padding, etc.): each six months or after cleaning, by spraying.
- Hard abused surfaces (floor, table tops, tools, etc.): each week (or day for heavy use) and after cleaning, by wiping or mopping.
- Hard unabused surfaces (cabinets, walls, fixtures, etc.): each six months or annually and after cleaning, by wiping or spraying.
- Company-furnished and maintained clothing and smocks: after each cleaning, by spraying or adding antistatic concentrate to final rinse water when cleaned.

The use of antistatic chemicals, their application, and compliance with all appropriate specifications, precautions, and requirements must be the responsibility of the area supervisor where antistatic chemicals are used.

Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies

ESD labels and signs in work areas

ESD caution signs at workstations and labels on static-sensitive parts and containers must be consistent in color, symbols class, voltage-sensitivity identification, and appropriate instructions. Signs must be posted at all workstations performing operations with static-sensitive items. These signs must contain the following information or its equivalent.



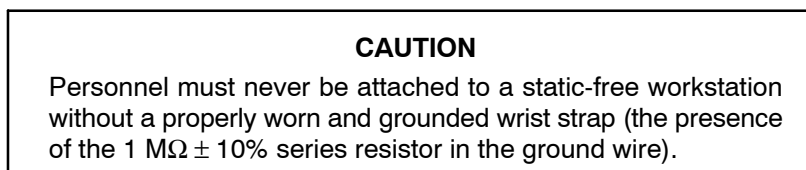
Labels must be affixed to all containers containing static-sensitive items at a place readily visible and proper for the intended purpose. Additionally, labels must be consistently placed on containers and packages at a standard location to eliminate mishandling. Use only QC-accepted and approved signs and labels to identify static-sensitive products and work areas. The use of ESD signs and labels and their information content must be the responsibility of the area supervisor to ensure consistency and compatibility throughout the static-sensitive routing.

relative humidity control

Since relative humidity has a significant impact on the generation of static electricity, when possible, the work area must be maintained within the 40%–60% relative humidity range.

preparation for working at static-free workstation

A workstation with a static dissipative work surface connected to ground through a $1\text{ M}\Omega \pm 10\%$ resistor, a grounding wrist strap with the ground wire connected to the conductive work surface, and an ionizer constitute a static-free workstation (Figure 1). An operator is grounded properly when the wrist strap is in snug (no slack) contact with the bare skin, usually positioned on the left wrist for a right-handed operator. The wrist strap must be worn the entire time an operator is at a static-free workstation. The operator must touch the grounded bench top first before handling static-sensitive items. This precaution must be observed in addition to wearing the grounding wrist strap. If possible, the operator must avoid touching leads or contacts even though he or she is grounded.



An operator's clothing must never make contact or come in close proximity with static-sensitive items. Operators must be especially careful to prevent any static-sensitive items (being handled) from touching their clothing. Long sleeves must be rolled up or covered with antistatic sleeve protector banded to the bare wrist, which must "cage" the sleeve at least as far up as the elbow. Only antistatic finger cots can be used when handling static-sensitive items.

preparation for working at static-free workstation (continued)

Any improperly prepared person, while at or near the work station, must not touch or come in close proximity with any static-sensitive item. It is the responsibility of the operator and the area supervisor to ensure that the static-free work area is clear of unnecessary static hazards, including such personal items as plastic-coated cups or wrappers, plastic cosmetic bottles or boxes, combs, tissue boxes, cigarette packages, and vinyl or plastic purses. All work-related items, including information sheets, fluid containers, tools, and part carriers must be approved for use at the static-free workstation.

general handling procedures and requirements (for ESDS devices and assemblies)

- All static-sensitive items must be received in an antistatic/conductive container and must not be removed from the container except at the static-free workstation. All protective folders or envelopes holding documentation (lot travelers, etc.) must be made of nonstatic-generating material.
- Each packing (outermost) container and package (internal or intermediate) must have a bright yellow warning label attached, stating the following information or equivalent:



The warning label must be legible and easily readable to normal vision at a distance of three feet.

- Static-sensitive items are to remain in their protective containers except when actually in use at the static-free station.
- Before removing an item from its protective container, the operator must place the container on the conductive grounded bench top, make sure the wrist strap fits snugly around the wrist and is properly plugged into the ground receptacle, and then touch their hands to the conductive bench top.
- All operations on the items must be performed with the items in contact with the grounded bench top as much as possible. Conductive magazine are not allowed to touch the hard-grounded test gear on bench top.
- Ordinary plastic solder-suckers and other plastic assembly aids must not be used.
- In cases where it is impossible or impractical to ground the operator with a wrist strap, a conductive shoe strap can be used along with conductive tile/mats.
- When the operator moves from any other place to the static-free workstation, the start-up procedure must be the same as in Preparation for Working at Static-Free Workstation.
- The ionizer must be in operation prior to presenting any static-sensitive items to the static-free workstation, and must be in operation during the entire time period when the items are at the workstation.
- "Plastic snow" polystyrene foam, "peanuts," or other high-dielectric materials must never come in contact with, or be used around, electrostatic-sensitive items, unless they have been treated with an antistat (as evidenced by pink color and generation of less than ± 100 volts).
- Static-sensitive items must not be transported or stored in trays, tote boxes, vials, or similar containers made of untreated plastic material unless items are protectively packaged in conductive material.

Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies

packaging requirements

Packaging of static-sensitive items is to be in accordance with its category (see Device Sensitivity). The use of tape and plain plastic bags is prohibited. All outer and inner containers are to be marked as outlined in General Handling Procedures and Requirements. Conductive magazines/boxes can be used in lieu of conductive bags.

specific handling procedures for static-sensitive items

stockroom operations

- Containers of static-sensitive items are not to be accepted into stock unless adequately identified as containing static-sensitive items.
- Items may be removed from the protective container (magazine/bag, etc.) for the purpose of subdividing for order issue only by a properly grounded operator at an approved static-free workstation as defined in the Facilities for and Preparation for Working at Static-Free Workstation.
- All subdivided lots must be repackaged carefully in protective containers (magazine/bag, etc.) prior to removal from the static-free workstation and labeled to indicate that the package(s) contain static-sensitive items. If it is suspected that a static-sensitive item is not protected adequately, the item must not be transferred to another container; it must be returned to the originator for disposition unless the originator is a customer. In that case, the QC engineer must contact the customer and negotiate an appropriate disposition.
- It is the responsibility of the stockroom supervisor to ensure that all personnel assigned to this operation are familiar with the handling procedures as outlined in this specification. A copy of this specification is to be posted in the vicinity of the static-free workstation(s) so that it is accessible to the operators. Stock handlers and all others who might have occasion to move stock are to be instructed to avoid direct contact with unprotected static-sensitive items.

module and subassembly operations

- Static-sensitive items are not to be received from a stockroom, kitting, or machine insertion area unless received in approved static-protective packaging and properly labeled to indicate that the contents are static-sensitive.
- All single station, progressive-line manual-assembly operators, and visual inspectors prior to wave soldering operations are to be grounded properly with a grounding wrist strap when handling static-sensitive items.
- Progressive lines used as single stations where operators work on a mix of boards, both static-sensitive and nonstatic-sensitive, require that all operators working on the line be properly grounded. This is necessary to accommodate the sliding of static-sensitive boards along the assembly bench or across positions not engaged in the assembly of this type board.
- It is the responsibility of the area supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection must be made using an electrostatic voltmeter to ensure that the static-free workstations are in the proper working order and to ensure that operators are wearing grounding wrist straps properly (snugly and in contact with bare skin).



specific handling procedures for static-sensitive items (continued)

soldering and lead-forming operations

- All soldering machines, conveyors, cleaning machines, and equipment must be grounded electrically to ensure that they are at the same ground potential as the grounded operators working on their stations. No machine surfaces exposed to static-sensitive items are to be above ground potential.
- All processing equipment must be grounded, including all loading and unloading stations, that is, the stations before and after each piece of processing equipment.
- All nonmetallic, static-generating components in the handling systems must be treated to ensure protection from static.
- All workstations must be identified by posting signs as outlined in ESD Labels and Signs in Work Areas.
- Operators are to be properly grounded with a grounding wrist strap during handling, loading, unloading, inspection, rework, or proximity to static-sensitive items.
- Unloading-operators working at a grounded station must place static-sensitive items into approved static-protective bags or containers.
- All manual soldering, repair, and touch-up workstations on the solder line are to be static protected. Operators are to wear grounding wrist straps when working on static-sensitive items. Only grounded-tip soldering/desoldering irons are allowed when working on static-sensitive items.
- It is the responsibility of the area supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection must be made using an electrostatic voltmeter to ensure that the static-free workstations are in proper working order and to ensure that the operators are wearing grounding wrist straps properly (snugly and in contact with bare skin).

electrical testing operations

- All electrical test stations must be static-protected. Operators must be grounded properly when working on these items.
- Reused antistatic magazines must be monitored for maintenance of antistatic characteristics.
- Devices must be in an antistatic/conductive environment except at the moment when actually under test.
- Devices must not be inserted into or removed from circuits or tester with the power on or with signals applied to inputs to prevent transient voltages from causing permanent damage.
- All unused input leads must be biased if possible.
- Device or module repairs must be performed at static-free workstations with the operator attached to a grounding wrist strap. Grounded-tip soldering irons must be used when working on static-sensitive items.
- Static-sensitive items must be handled through all electrical inspections in static protective containers. Removal of the items from the protective containers must be done at a static-free workstation as discussed in Preparation for Working at a Static-Free Workstation. The units must be returned to the containers before leaving the station.

Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies

specific handling procedures for static-sensitive items (continued)

- All such items must be shipped with an ESD warning label affixed as shown under the General Handling Procedures and Requirements (for ESD sensitive devices and assemblies).
- It is the responsibility of the area supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection must be made using an electrostatic voltmeter to ensure that the static-free workstations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly and in contact with bare skin).

packing operations

- Static-sensitive items are not to be accepted into the packing area unless they are contained in a static-protected bag or conductive container.
- A static-sensitive item delivered to the packer within an approved container or bag and found to be in order regarding identification must be packed in the standard shipping carton or other regular packaging material. Containers are to be labeled in accordance with General Handling Procedures and Requirements.
- Any void-fillers must be made of an approved antistatic material.

burn-in operations

- Burn-in board loading and unloading of static-sensitive items must be done at a static-free workstation.
- Shorting clips/shorted connectors must be installed on the board plug-in tab prior to loading any units into the board sockets. The clip/connectors must be taken off just prior to plugging the board into the oven connector. The clip/connector must be installed immediately upon removal of the board from the oven connector. Installation and removal of the clip/connector must be done by a properly grounded operator.
- All automatic or semi-automatic loading and unloading equipment must be properly electrically grounded.
- It is the responsibility of the area supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection must be made using an electrostatic voltmeter to ensure that the static-free workstations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly and in contact with bare skin).

customer-returned-item handling procedure

Receipt of ESD sensitive-labeled items is to be done at a static-free workstation and handled in accordance with applicable sections within this guideline.

quality control provision

sampling

Each manufacturing, stockroom, and testing operation handling ESD sensitive devices is audited a minimum of once each quarter for compliance with all terms of this specification by the responsible process control or QRA organization. Ground continuity and the presence of uncontrolled static voltages are considered critical and must be checked more frequently as specified below.

ground continuity (minimum of once a week)

Ground connections (grounding wrist strap, ground wires on cords, etc.) must be checked for electrical continuity. The presence of a $1\text{ M}\Omega \pm 10\%$ resistor in the ground connections between both the operator wrist straps to the work surface and the work surface to ground connector must be verified.



Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies

grounded conditions (minimum of once a week)

A visual inspection must be made to determine full compliance with this specification at static-free workstations during handling of static-sensitive items, including operator being grounded as required, static-sensitive items not being handled in unprotected or unauthorized areas, and no static-generating materials at the grounded workstation.

sleeve protectors (minimum of once a week)

A visual check must be made to determine that each operator wearing loose-fitting or long-sleeved clothing either has sleeves properly rolled or covered with sleeve protectors and is properly grounded with a wrist strap to the bare skin.

static voltage levels (minimum of once a week)

In addition to the visual inspections, a sample inspection using an electrostatic voltmeter to check for uncontrolled electrostatic voltages at or near electrostatic-controlled workstations.

conductive floor tiles (minimum of once a month)

Conductive floors must have a resistance of not less than 100 k Ω from any point on the tile to earth ground. Also, resistance from any point-to-point on the tile floor three (3) feet apart must be not less than 100 k Ω . The test methods to be used are ASTM-F-150-72 and NFPA 99.

records

Written records must be kept of all ESD QC audits.

training

Training is applicable for all areas where individuals come in contact with ESD-sensitive devices. It is the responsibility of each area supervisor to make sure that his/her people receive ESD training initially and every 12 months thereafter to maintain proficiency. Training may include static fundamentals, a review of applicable parts of this specification guideline, and actual applications in the work area.



**Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS)
Devices and Assemblies**
