Introduction

The Kintex UltraScale FPGA KCU105 is a development board created by Xilinx. It is aimed to prototype medium-to-high volume applications. The KCU105 uses Ethernet and dual USB-to-UART capabilities to interface with a host computer and set up the FPGA. Texas instruments have created a platform where the KCU105 can interface with TI's latest and most popular high speed data converters Evaluation Modules (EVM) as if it were connected to a TI development board. The platform also allows users to operate the High Speed Data Converter Pro Graphic User Interface (HSDC Pro GUI) software to capture data from an Analog-to-Digital converter (ADC) as well as generate data for a Digital-to-Analog convert (DAC).

Functionality

The KCU105 has a standard FMC connector that proves an interface between FMC-based development boards and all TI JESD204B ADC and DAC EVMs. **To acquire data, receive data, and do register read and writes using a host PC, the FPGA transmits and receives data across three Serial Peripheral Interface (SPI) busses using dedicated pins on the FMC.** For communicating, the KCU105 uses Ethernet for connecting to a host PC through a local network and dual USB-to UART bridge interface. The KCU105 also has an industry-standard JTAG connection for configuring the FPGA over USB.

Hardware Configuration

Refer to Xilinx KCU105 for configuration. Refer to specific TI's ADC/DAC EVM for configuration.

Software Start Up

- Instructions for HSDC Pro v4.42 or greater. (Same as TSW14J10EVM)

Download the latest version of HSDC Pro GUI to a local directory on a host PC. This can be found on the TI website by entering "HIGH SPEED DATA CONVERTER PRO GUI INSTALLER" in the search parameter window at www.ti.com.....

- USB interface and Drivers

Connecting Ethernet, UART, and JTAG connector. Ensure Silicon Labs drivers are installed. Configuring a terminal applications (Tera Term, Hyperterm, Putty) to communicate with the COM port assigned to Silicon Labs interface.

- Download instructions for Xilinx Vivado design tool.

https://www.xilinx.com/products/design-tools/vivado.html

Downloading Firmware example

Instruction on downloading firmware to KCU105, give KCU105 GPIO LED status…..
The user GPIO LEDs on the evaluation boards are used to provide additional visual status indications. The LEDs are assigned as follows:

0 – Rx SYNC, ON = SYNCB deasserted by Rx core
1 – Tx SYNC, ON = SYNCB deasserted by Tx core
2 – RX Reset done, ON = RX reset complete
3 – DRP CLK, Flashing = CLK Active
4 – DXI CLK, Flashing = CLK Active
5 – TX/RX CORECLK, Flashing = CLK Active
6 – GT REFCLK, Flashing = CLK Active
7 – TX EMPTY, ON = There is no data available for the TX core from AXI DMA

DAC and ADC GUI configuration File changes when using a Xilinx development platform

The configuration files that come with the TI ADC and DAC EVM GUIs are setup to operate with the Altera-based TI TSW14J56EVM. There are configuration files created for other Xilinx developments boards like the Virtex VC707 or Zync ZC706. With the latest firmware, some GUI can be configured as if it was connected to the TSW14J56EVM. Depending on the case, the ADC/DAC may be configured with the GUI, Xilinx configuration files, or a couple of changes to the settings of the LMK04828 registers. See example sections.

The firmware for the Xilinx Development Platforms use a separate clock input for REFCLK and Core clock to give maximum flexibility and support all line rates and subclasses with a single programmable design. The Xilinx IP used in the firmware can be driven by a single clock in many circumstances (see the clocking section of the Xilinx IP product guide for more details).

THE REFCLK and Core clk are determined by the following line rate conditions:

	MaxLr(Gbps)	1.2	1.6	1.9	2	2.4	3.2	3.9	4	4.9	6.5	7.9	8.1	8.2	9.8	12.5
	MinLr(Gbps)	1	1.201	1.601	1.901	2.001	2.401	3.201	3.901	4.001	4.901	6.501	7.901	8.101	8.201	9.801
xMult																
2		Y	Y													
10		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		
20					Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
40									Y	Y	Y	Y	Y	Y	Y	Y

Figure 2 Valid xMult line rate ranges.

Line rate switching is supported across the entire speed range supported by transceivers. The ratio of REFCLK to line rate multipliers is also programmable. The line rate is determined by…. The multiplier is programmed in HSDC PRO by the ini files.

Note: REFCLK = line rate/ xMult

Example:

A line rate of 5.0G is in the range between 4.901Gbps and 6.5Gbps and is supported by the xMults values of 10,20, and 40. Therefore, the possible values for REFCLK are:

5.0G/10 = 500MHz, 5.0G/20 = 250MHz, 5.0G/40 = 125MHz

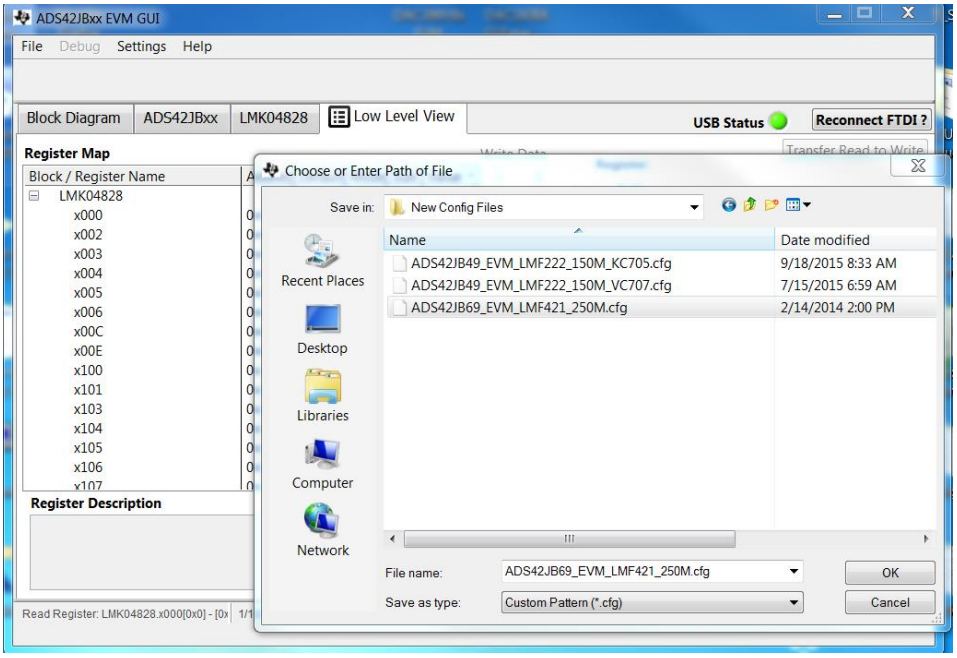
ADS42JB69/49 EVM startup with Xilinx KCU105

1. Connect the ADC to FMC HPC connector J22 on the KCU105.
2. Connect the power cables to the KCU105.
3. Connect two USB micro B cables between the KCU105 and a host computer with Vivado loaded: one between the USB to JTAG interface J1, and the other between the dual USB-UART port J4.
4. Connect a micro USB cable between ADC and computer.
5. Open a serial port connection with any sort of serial terminal software, e.g. TeraTerm, Hercules, etc.
6. Initialize a serial port communication to Silicon Labs Dual CP210x USB to UART Bridge: **Enhanced** COM Port. Set the baud rate of this serial connection to **115200**, and leave all other defaults as set.
7. Open another serial port connection and connect to Silicon Labs Dual CP210x USB to UART Bridge: **Standard** COM Port. Ensure the baud rate of this serial connection is **9600**, leaving all other defaults as set.
   (If you do not see these COM ports, open the Device Manager and install the proper drivers)
8. Connect an Ethernet cord from the KCU105 to a local network (same as the host computer)
9. Power up the KCU105 board. There should be information scrolling on the Enhanced COM port.

Next:

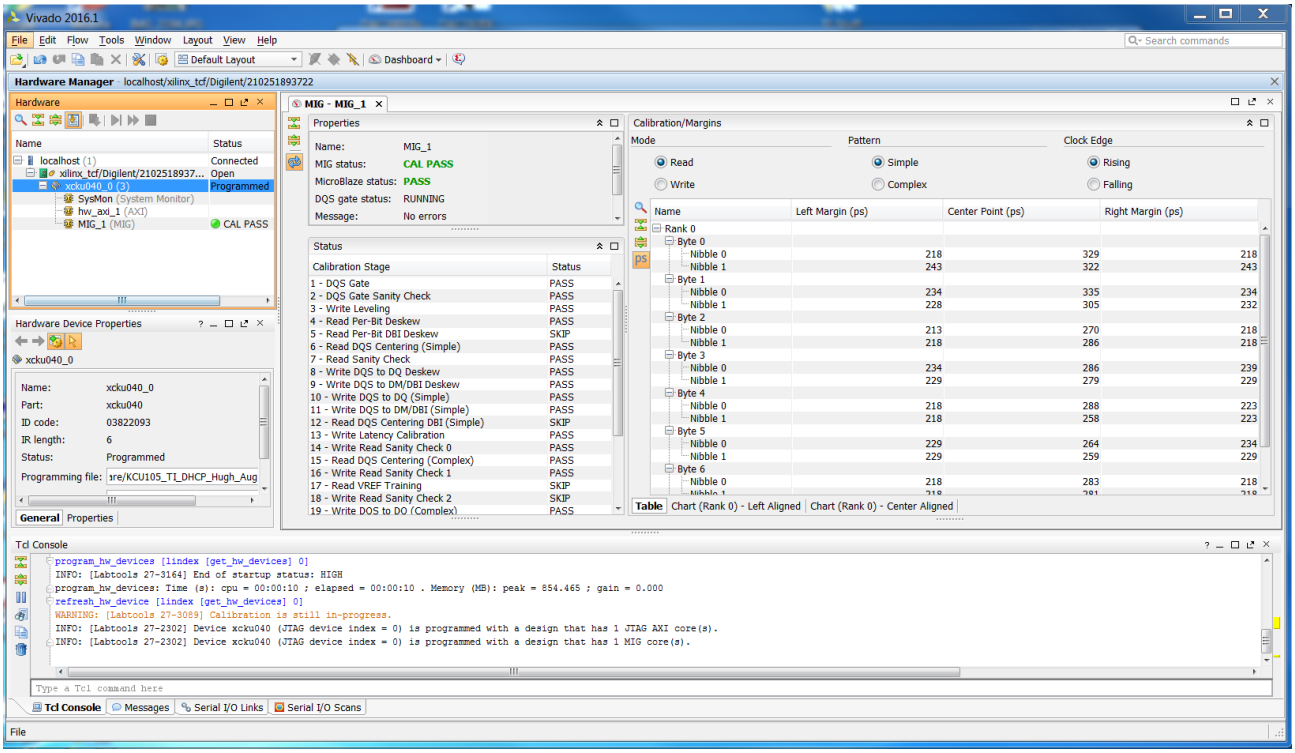
1. Connect the power cable to the ADS42JB49 EVM and open the ADS42JBXX GUI.
   (This guide uses the updated GUI for the ADS42JBXX)
2. Go to the ADS42JBXX tab and click on “Device Reset” in the top left corner.
3. Go to the LMK0428 tab and click on “RESET” in the top left corner.
4. Go to the “Low Level View” tab and click on “Load Config”. Select the proper configuration file. In this case we are using an ADS42JB69 in a 421 mode at a sampling rate of 250MHz:
   ADS42JB69_EVM_LMF421_250M.cfg

Note: The configuration file can be used for both the ADS42JB69 and ADS42JB49

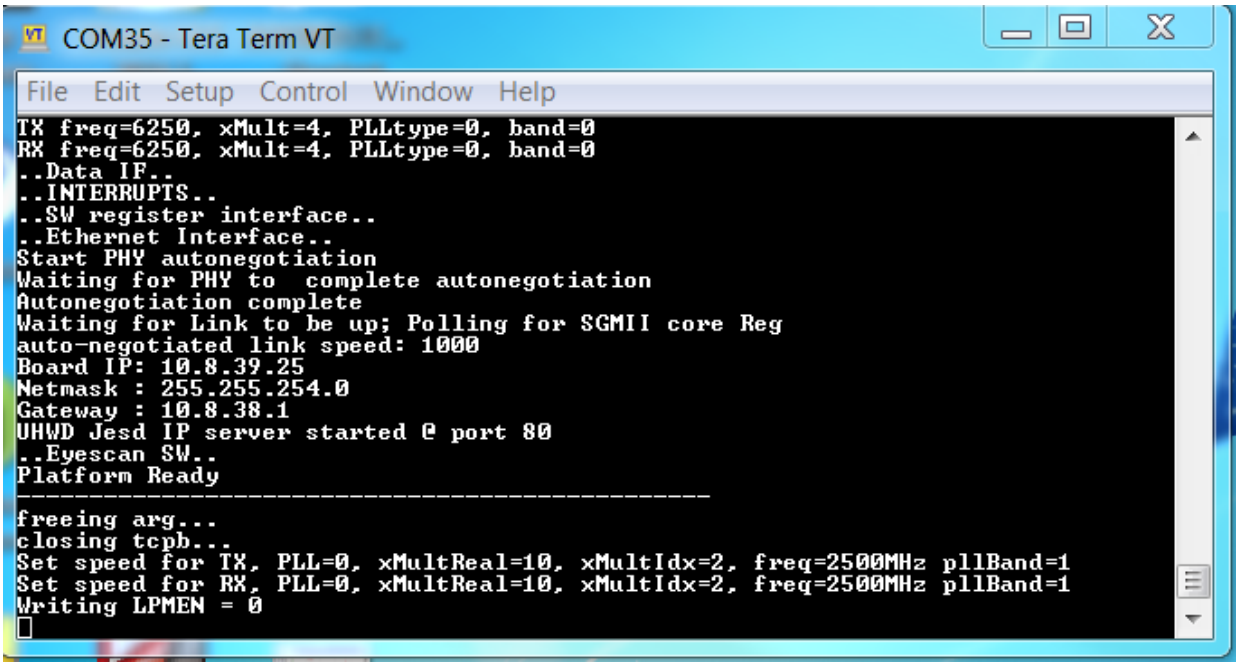


To program the FPGA, do the following steps:

1. Open Xilinx Vivado 2016.1 design tool
2. Double click on "Open Hardware Manager".
3. Click on "Open Target" (located on the green bar), and select "Open New Target"
   (You can also go to Tools -> Open New Target)
4. Click on "Next" twice. Select the Hardware Target, and click "Next" again.
5. Click on "Finish".
6. Click on "Program device" (located on the green bar). Select xcku040_0.
   (You can also go to Tools -> Program device)
7. Select the proper bit stream file. In this case, the firmware for the KCU105 is:
   "KCU105_TI_DHCP.bit."
8. Click on "Program."
9. A new window will open showing the status of the programming. Once this reaches 100%, the FPGA is programmed.
   (Make sure the calibration passes and that there are no errors)



The board IP address will be available on the Standard COM port.



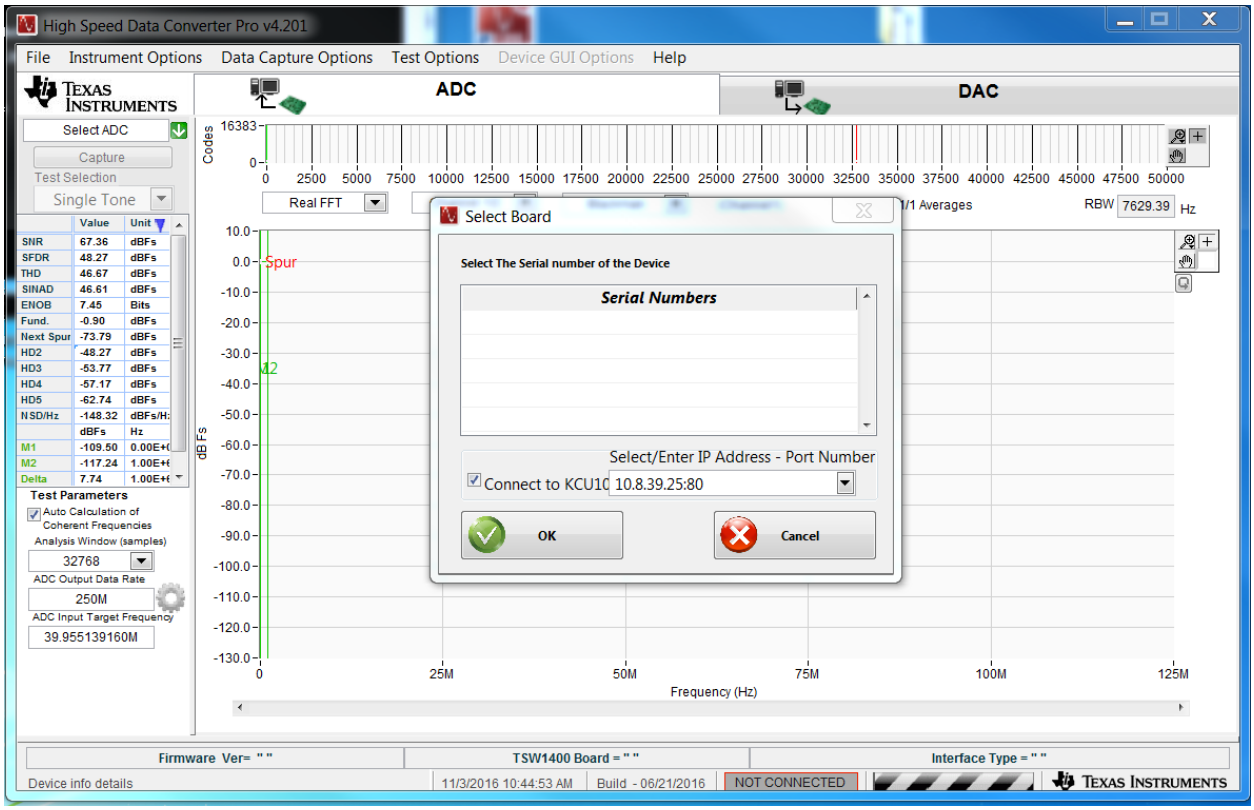
Next, the VADJ8 voltage must be set to 1.8V. This is set in the Enhanced COM port terminal.

1. Navigate to the Enhanced COM port window. Return to the main menu by entering "0" in the terminal.
2. Select "Adjust FPGA Mezzanine Card (FMC) settings" by entering "4"
3. "Set FMC VADJ to 1.8V" by entering "4"
4. Return to the main menu by entering "0"
5. To check this voltage, select "Get the Power Systems Voltages" by entering "2"
6. Enter "7" to "Get VADJ1D8 voltage." The voltage should appear above the menu.
7. Return to main menu by entering "0"

It is recommended that the FPGA is reprogrammed and the VADJ1D8 voltage reset every time after programming the ADC.

Open the latest version of HSDC Pro GUI v4.201 (under Texas Instruments, High Speed Data Converter Pro_KC105) by right clicking on the icon and **running as administrator**.

In the Select Board popup, check "Connect to KCU105." The IP address: Port can either be selected from the drop down menu or entered manually separated by a colon, i.e. IP Address: Port. Both the IP Address and Port number can be found in the Standard COM port terminal.



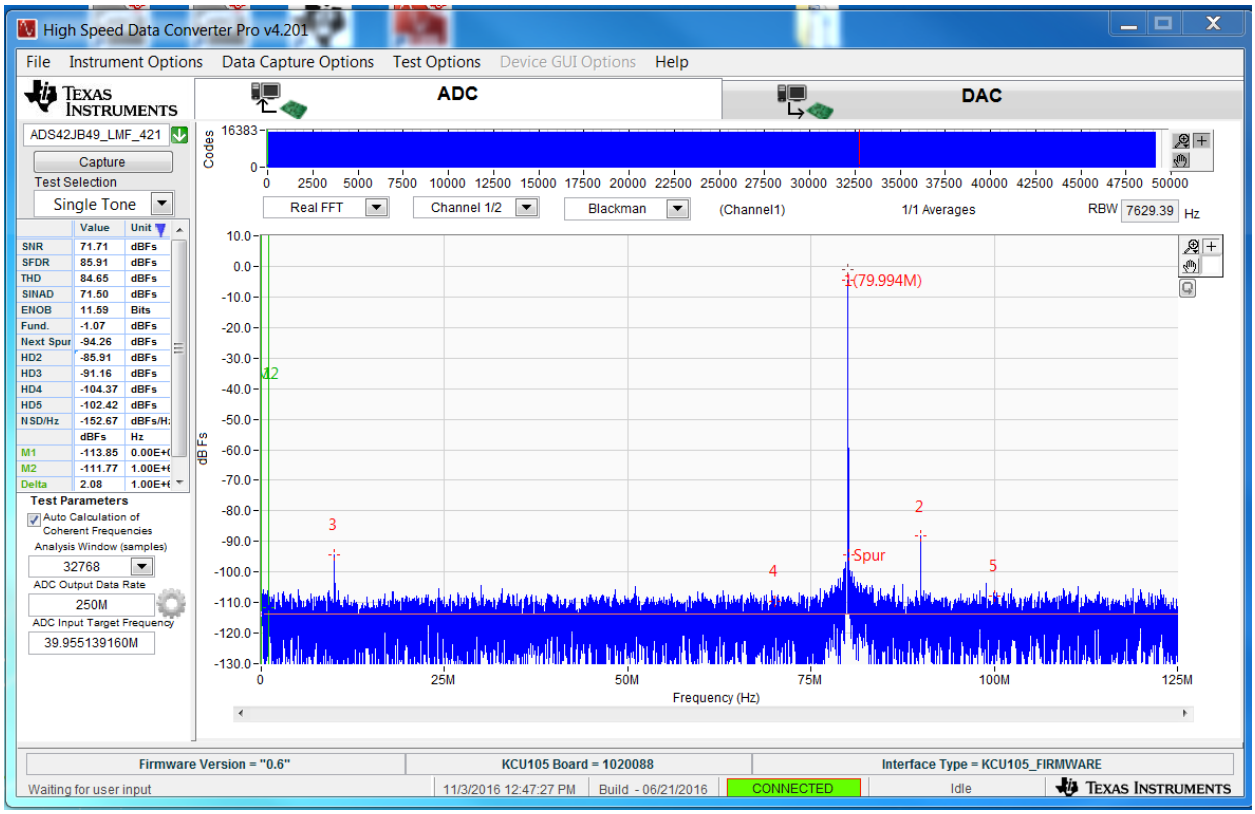
Select the ADC tab, and then select **"ADS42JB69_LMF_421"** using the device drop-down arrow. Make sure the Analysis Window (samples) is no greater than 32,768 (due to the limit of the internal FPGA memory used for this capture). Next enter **250M** in the ADC Output Data Rate window.

The GUI will display the new lane rate (2.5G) and JESD reference clock required by the capture platform FPGA (250M). Click on "OK".

Connect an analog input signal to the SMA connect (J1)

Click on "Capture"

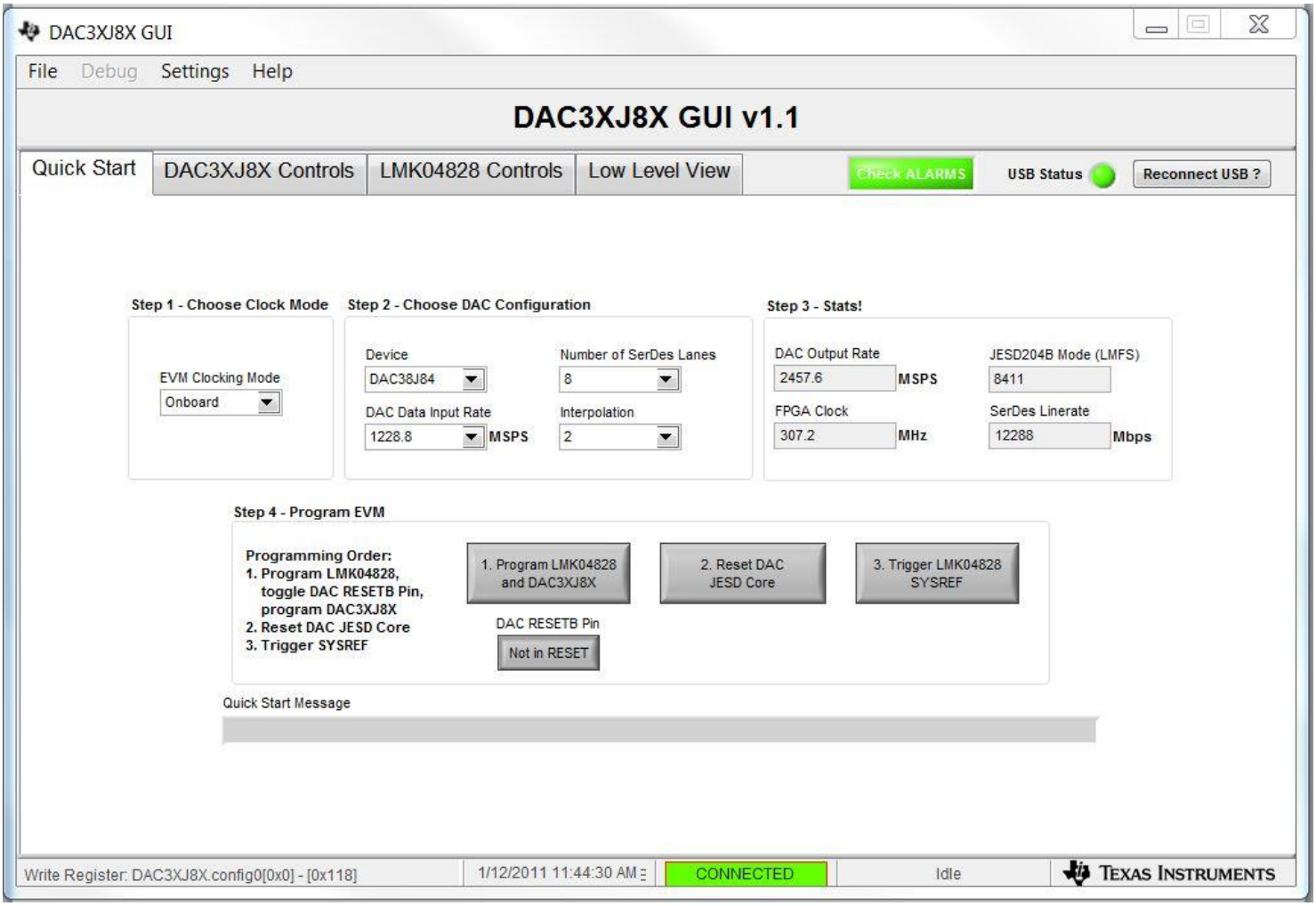
Capture of HSDC Pro using a bandpass filter and a tone of 170MHz @+15.5 dB



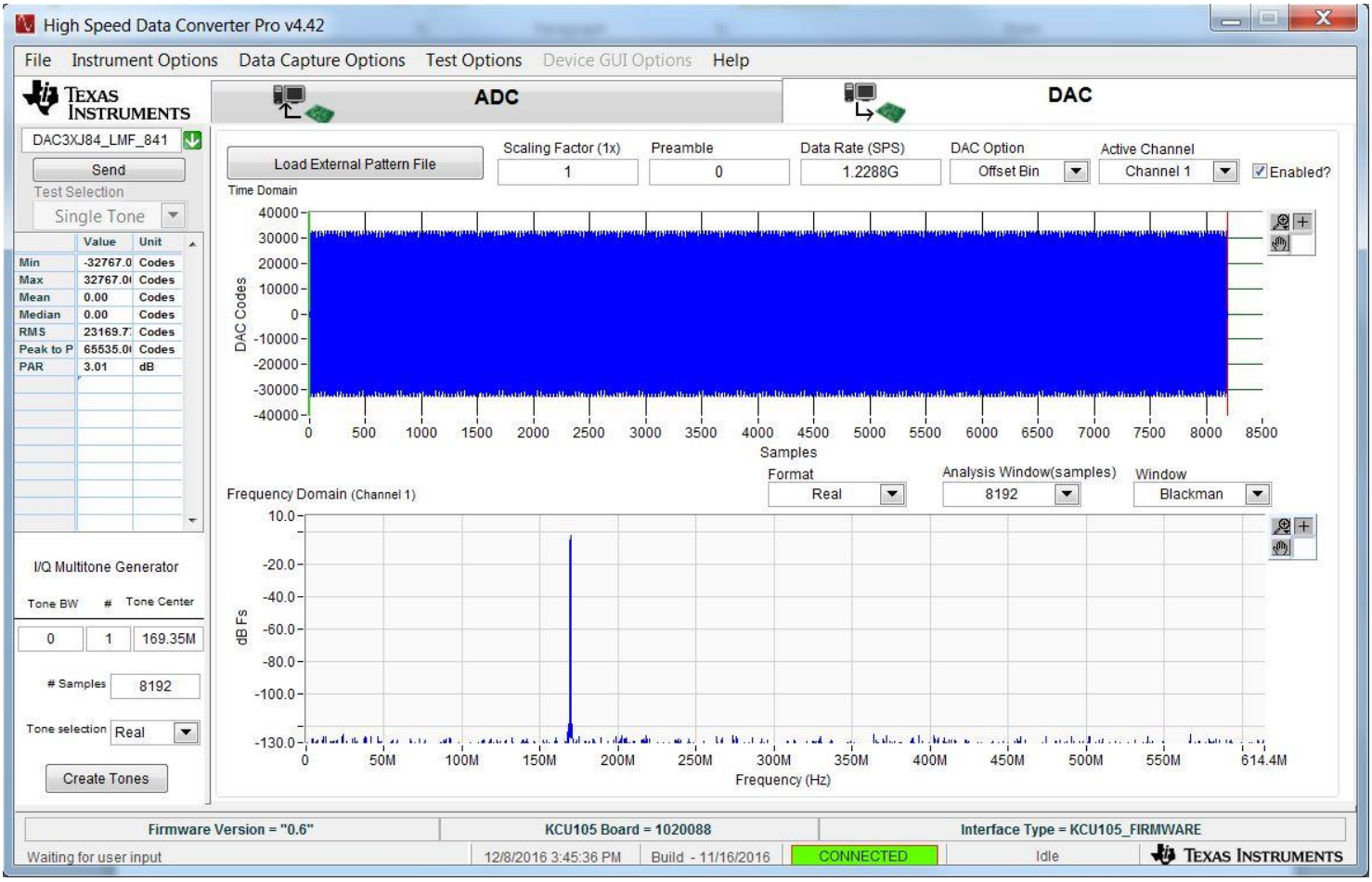
DAC38J84 EVM with Xilinx KCU105 Development Board Set up Example

This section provides an example of using a DAC38J84 using a KCU105. The KCU105 Configuration will be the same as the ADS42J69 for the DAC38J84. With the updated firmware, users can use the DAC38J84 GUI as if it was connected to a TI's TSW14J56. This example will a mode of the DAC38J84 and what needs to be modified.

The setup will be a 841 mode configured as shown:

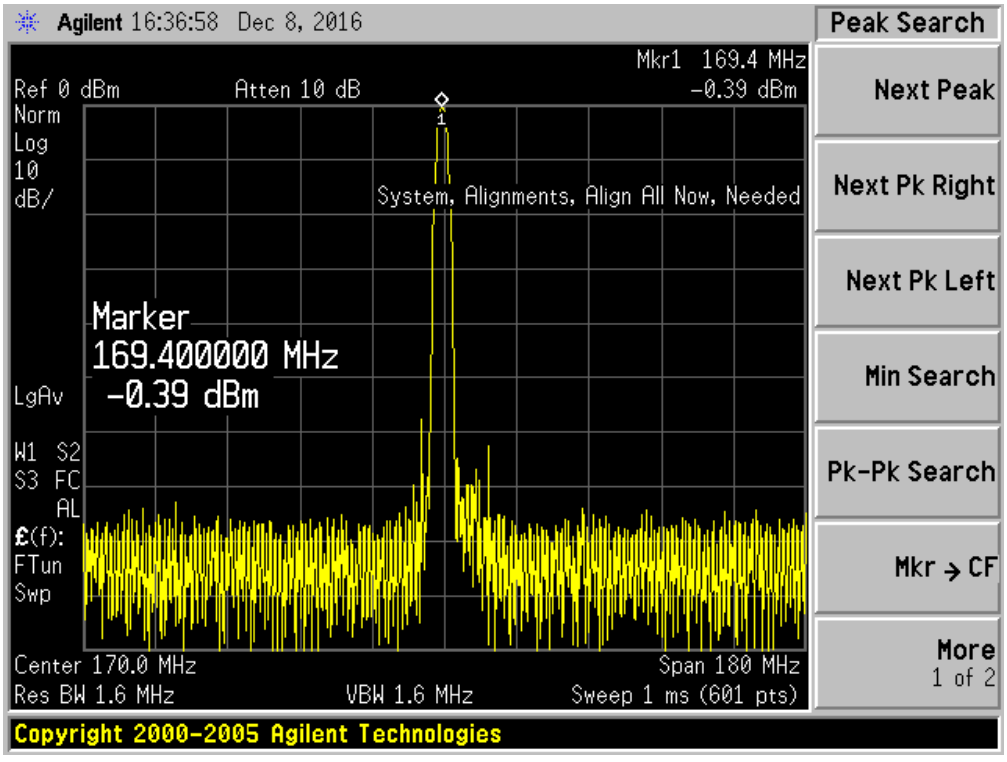


1. Press button **1. Program LMK04828 and DAC3XJ8X**
2. After completion, open HSDC Pro and connect as in the previous example
3. Press on the DAC tab, and select from the dropdown **DAX3XJ84_LMF_841**
4. Add the Data Rate and change the DAC option to **2's Complement**.
5. Set the number of samples to at least **8192**
6. Create a tone. The GUI should be configured as followed:



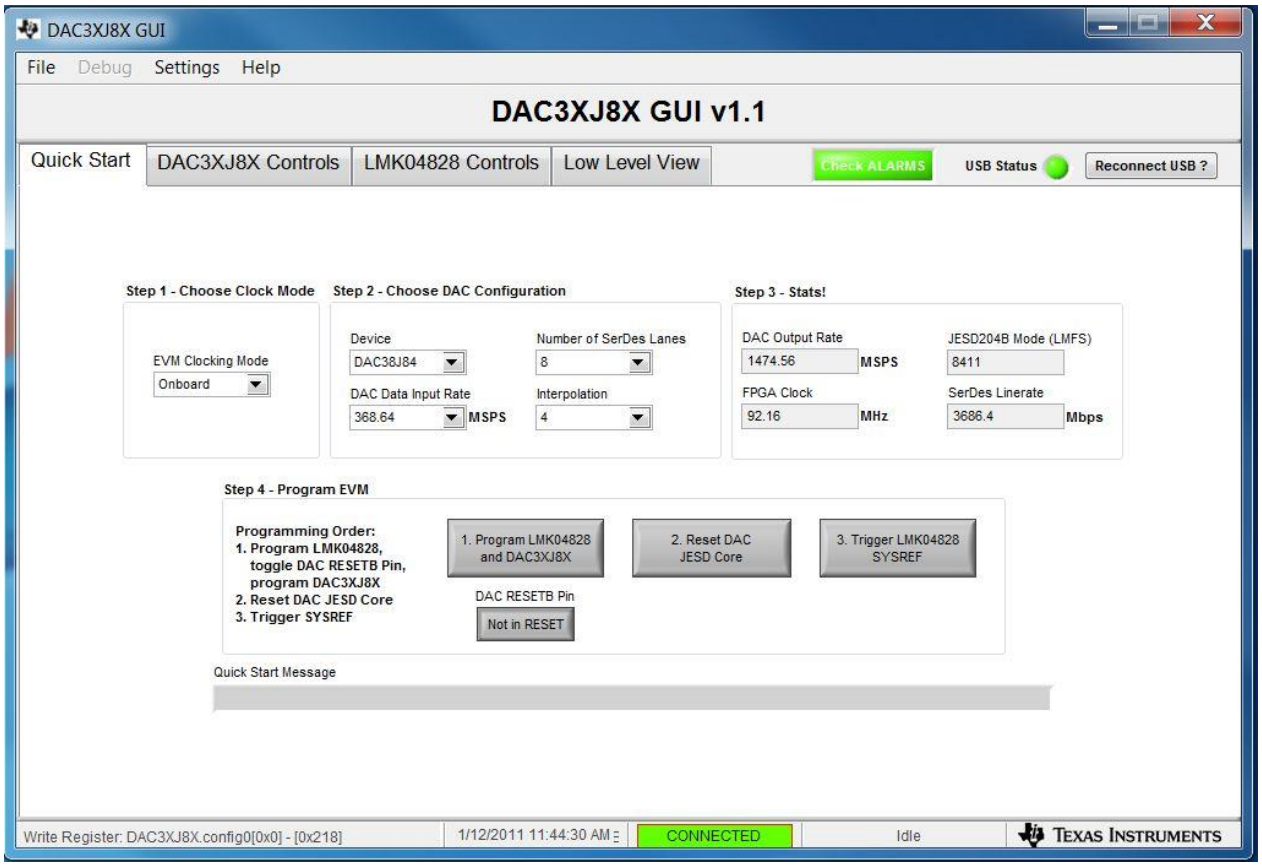
HSDC Pro GUI with Single tone of 169.35MHz

7. Press Send and the current lane rate (12.288GHz) and FPGA Clock (307.2MHz) should match the numbers on the DAC38J84 GUI
8. Go back to the DAC38J84 GUI and press **2. Reset DAC JESD Core and 3. Trigger Button.**
9. Connect an SMA cable to a Spectrum Analyzer and verify the DAC output

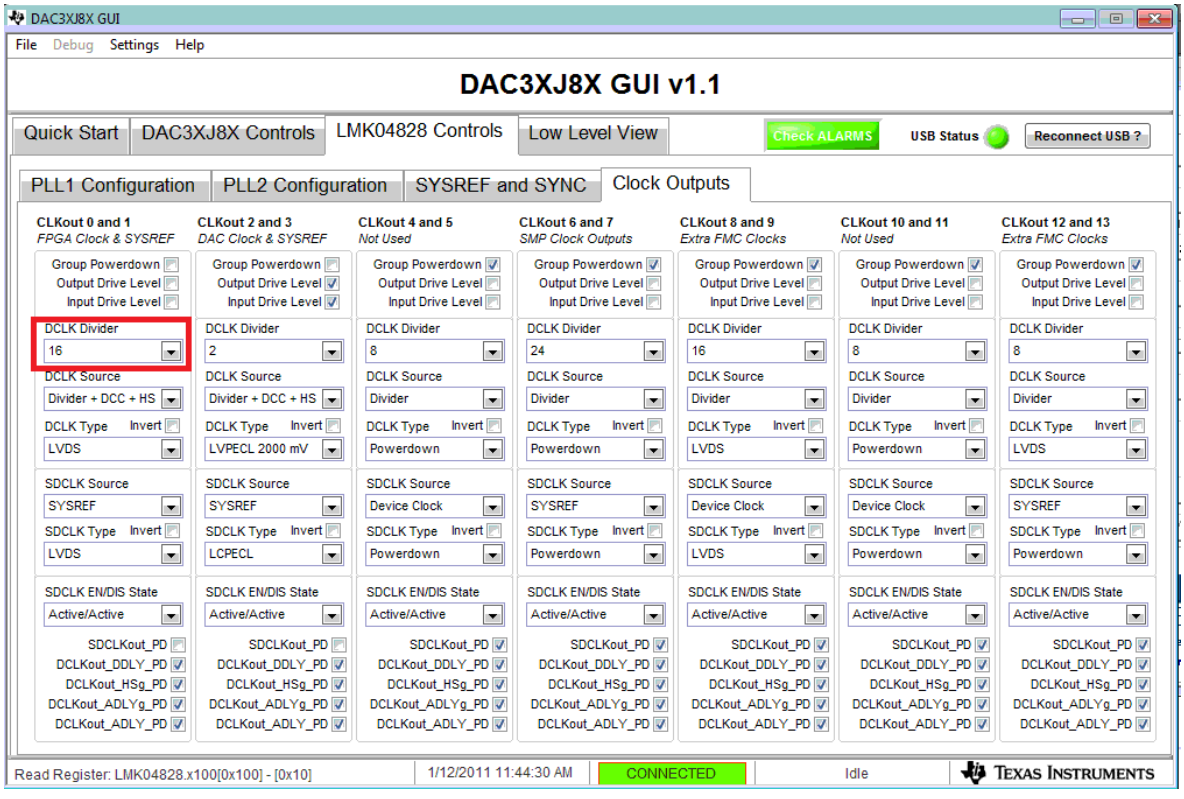


In this example, we will use the same mode, but a different configuration that shows the limitation of the KCU105

1. Configure the DAC as shown:



2. The DAC GUI by default will be configured to generate a FPGA reference clock as line rate/40. Since the linerate is shown to be 3.6G the valid xMult line rate is only supported by x10 and x20 (refer to Figure 1).
3. In order to support this mode, the settings of the LMK04828 registers needs to be changed. Update the DCLK Divider to 16 in the DAC GUI as shown:

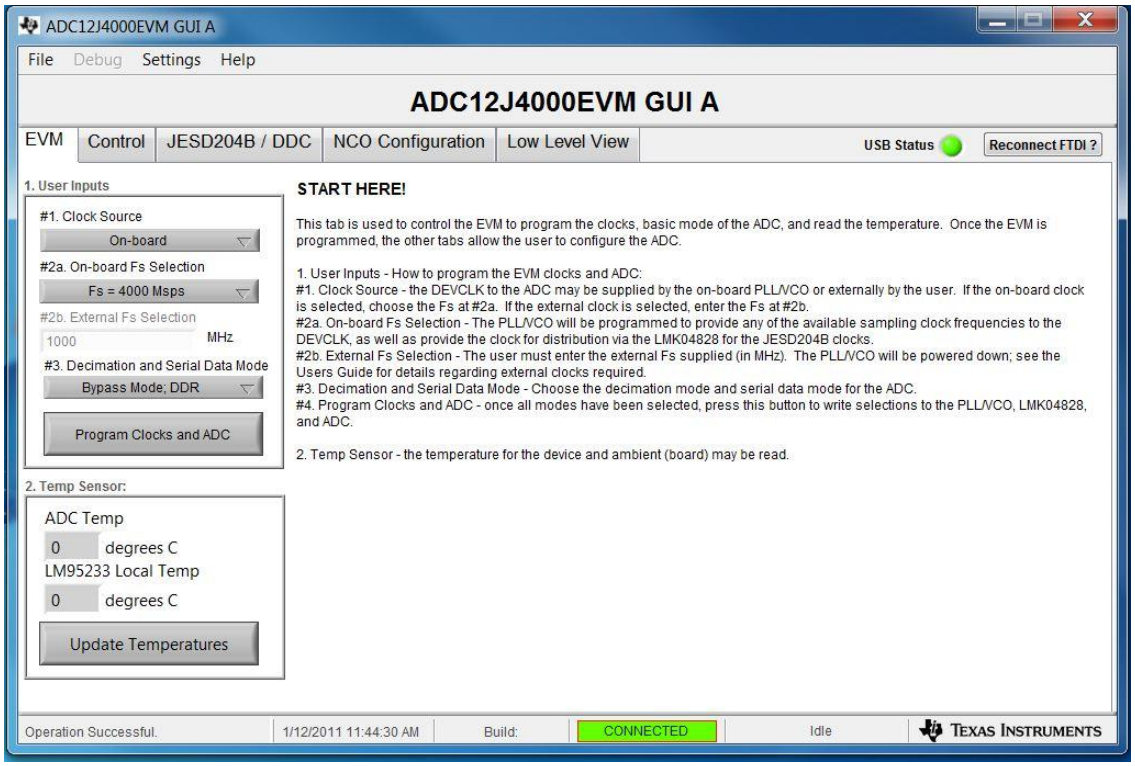


4. Follow the previous procedure to configure HSDC Pro and produce a tone.
   NOTE: The FPGA clock will not match on the HSDC PRO GUI and the DAC38J84 GUI.

ADC12J4000EVM with Xilinx KCU105 Development Board Set up Example

The following is an example of using the Xilinx Ultrascale KCU105 development platform to collect data from an ADC12J400 in bypass mode, as shown in Figure 1 below.

1. Follow the procedure for connecting and establishing communication the KCU105.
2. Connect the ADC12J400 to the FMC HPC connector to J22 on the KCU105.
3. Power up the ADC12J400 and open the ADC12J4000 GUI. Choose On-board as clock, set Fs = 4000MSPS, and set decimation and serial data mode to bypass mode; DDR. Then click Program Clocks and ADC as shown:



4. Continue follow the steps for loading firmware in the Vivado design tool and open HSDC Pro
5. Select “ADC12J4000_BYPASS” using the device drop down arrow. Make sure the Analysis Window is no greater than 32,768.
6. Enter 4G in the ADC Output Data Rate window. Click on “Capture” and the new line rate (8G) and JESD reference clock (200M) should show.
7. The captured result as shown: