

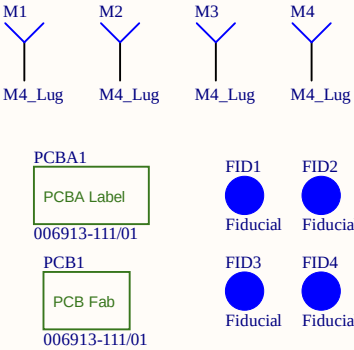
Change Log

Rev 1 [Sebastian Forenza, Aug 2025]
Original release. For integration into Arc Sport Block 4

I2C address mapping (7-bit)

Component	Address
High Powered Amp	0x60
Low Powered Amp	0x6B
Transciever	0x68

Mounting Hardware



PCB FAB	006913-111/01_A	PCBA	006913-111/01_A	VARIANT	[No Variations]
TITLE WAVE					
PROJECT WAVE					
DATE	8/21/2025	ENG	Sebastian Forenza	SHEET	1 OF 1

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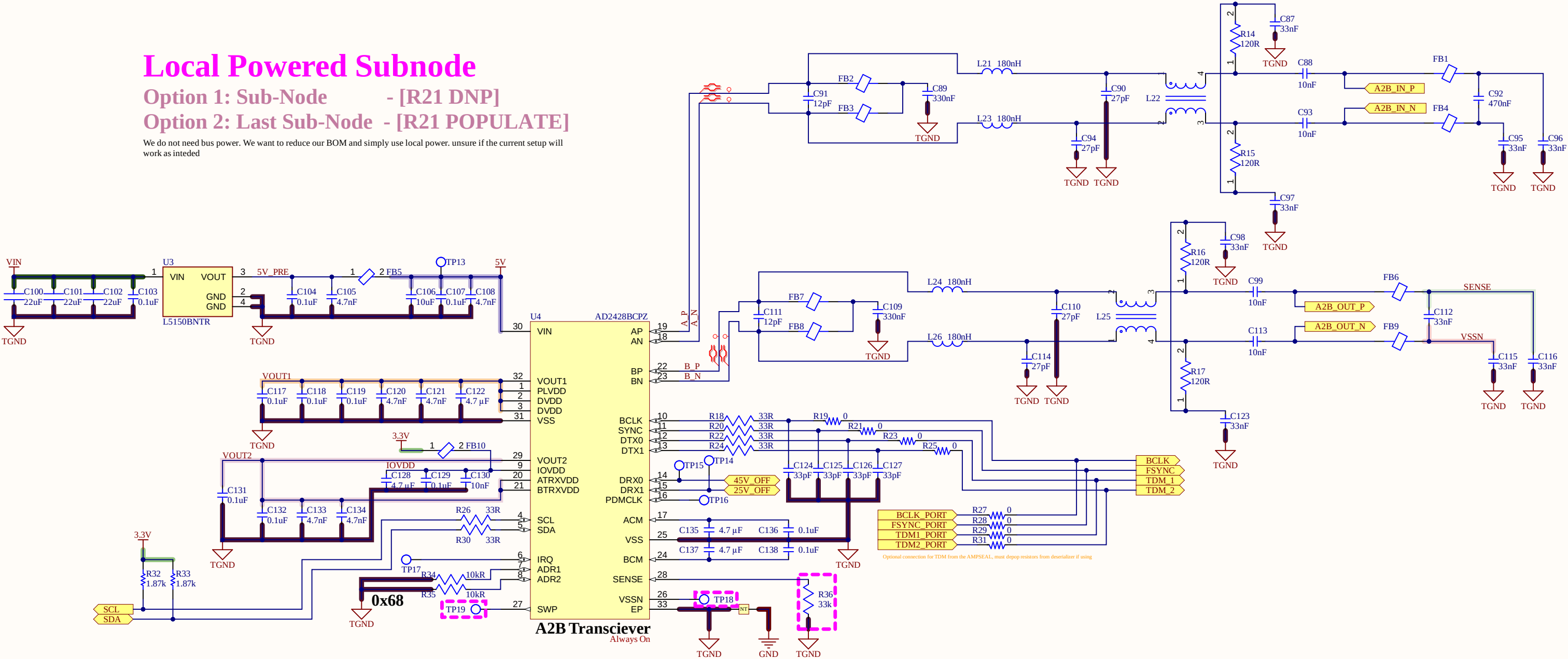


Arc Boat Company
2100 W 195th Street
Torrance, CA 90501
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Local Powered Subnode

- Option 1: Sub-Node - [R21 DNP]
- Option 2: Last Sub-Node - [R21 POPULATE]

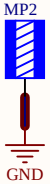
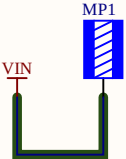
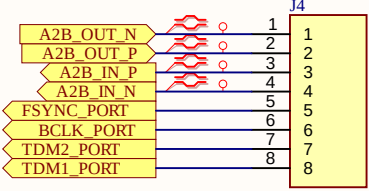
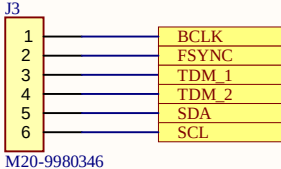
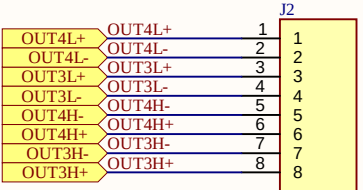
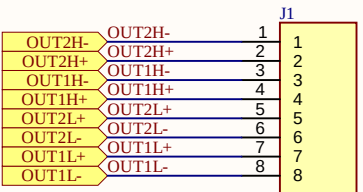
We do not need bus power. We want to reduce our BOM and simply use local power. unsure if the current setup will work as inteded

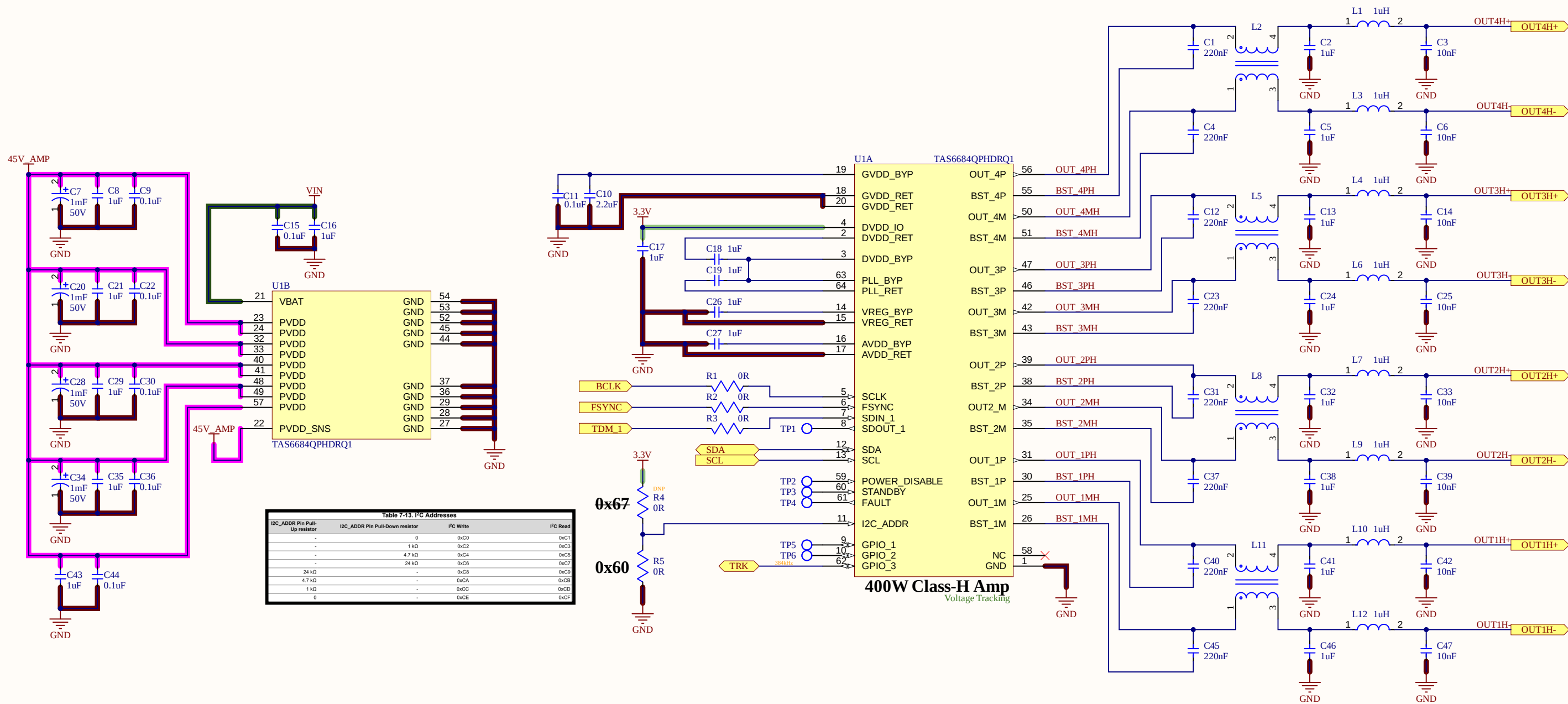


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PCB FAB 006913-111/01_A	PCBA 006913-111/01_A	VARIANT [No Variations]
TITLE A2B Transciever		
PROJECT WAVE		
DATE 8/21/2025	ENG Sebastian Forenza	SHEET * OF *





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PCB FAB 006913-111/01_A	PCBA 006913-111/01_A	VARIANT [No Variations]
TITLE High Power Amp		
PROJECT WAVE		
DATE 8/21/2025	ENG Sebastian Forenza	SHEET * OF *

CONFIGURATION (CFG0, CFG1, CFG2)				
R _{ROA_1}	Level 1 resistance		0.496	0.51
R _{ROA_2}	Level 2 resistance		0.496	0.51
R _{ROA_3}	Level 3 resistance		1.11	1.19
R _{ROA_4}	Level 4 resistance		1.81	1.93
R _{ROA_5}	Level 5 resistance		2.65	2.77
R _{ROA_6}	Level 6 resistance		3.71	3.8
R _{ROA_7}	Level 7 resistance		4.85	5.1
R _{ROA_8}	Level 8 resistance		6.29	6.5
R _{ROA_9}	Level 9 resistance		8.00	8.3
R _{ROA_10}	Level 10 resistance		10.18	10.5
R _{ROA_11}	Level 11 resistance		12.90	13.3
R _{ROA_12}	Level 12 resistance		15.71	16.2
R _{ROA_13}	Level 13 resistance		19.88	20.5
R _{ROA_14}	Level 14 resistance		24.15	24.9
R _{ROA_15}	Level 15 resistance		29.29	30.1
R _{ROA_16}	Level 16 resistance		35.40	36.5

Table 6-2. Overvoltage Protection Level Selection		
OVP Level	OVP Bit 1	OVP Bit 0
60V	0	0
50V	0	1
35V	1	0
28.5V	1	1

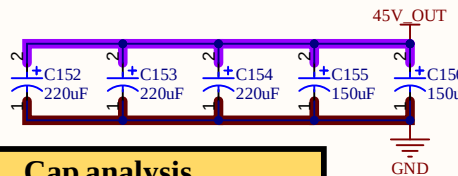
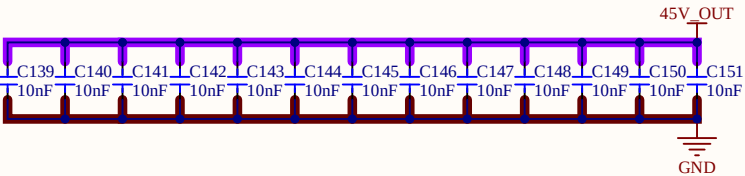
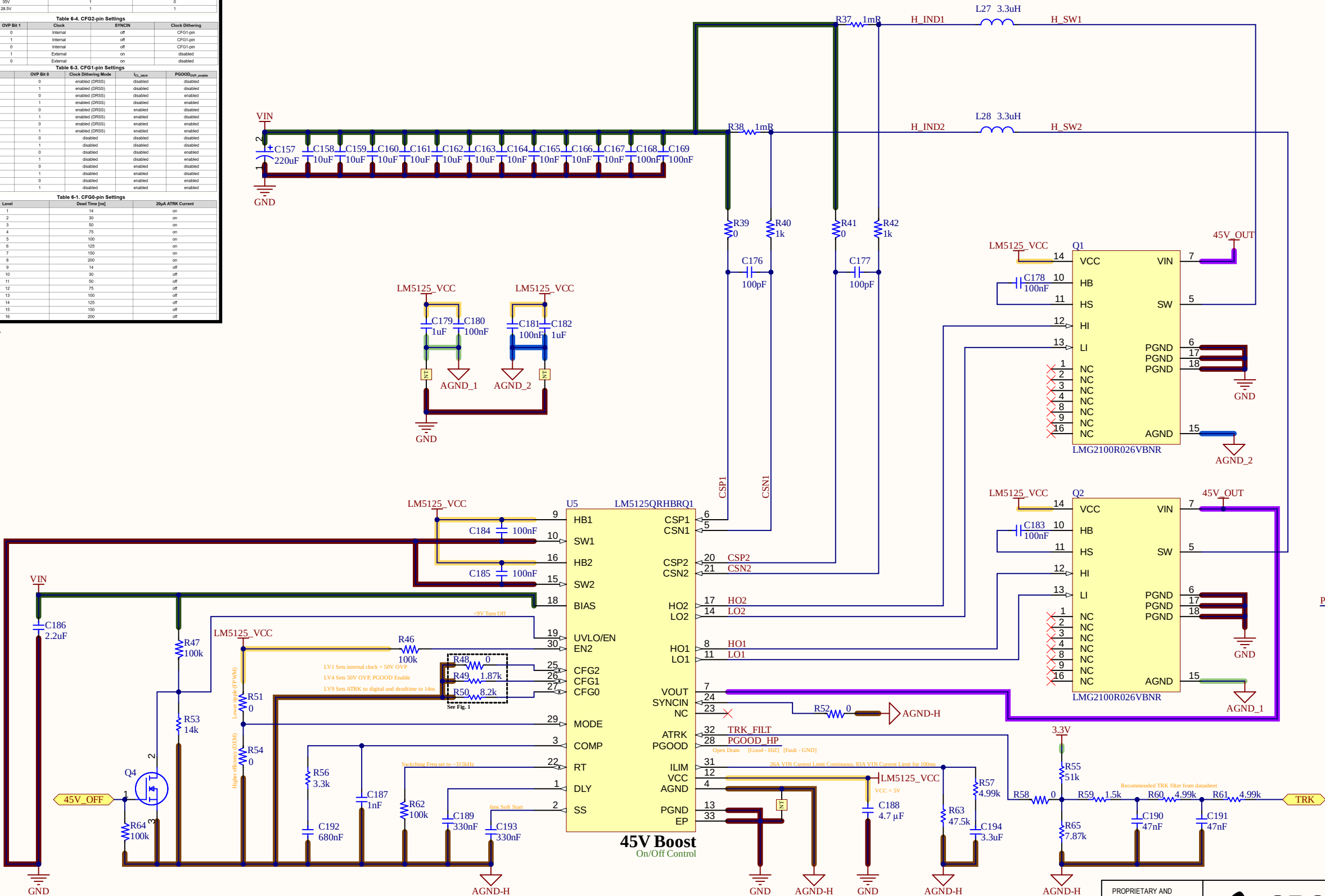
Table 6-4. CFG2-pin Settings			
Level	OVP Bit 1	Clock	Clock Dithering
1	0	Internal	off
2	1	Internal	off
3	0	Internal	off
4	1	Internal	off
5	0	External	on
6	1	External	on

Table 6-3. CFG1-pin Settings			
Level	OVP Bit 0	Clock Dithering Mode	PGOOD _{HP} Sense
1	0	enabled (DRSS)	disabled
2	1	enabled (DRSS)	disabled
3	0	enabled (DRSS)	disabled
4	1	enabled (DRSS)	disabled
5	0	enabled (DRSS)	enabled
6	1	enabled (DRSS)	enabled
7	0	enabled (DRSS)	enabled
8	1	enabled (DRSS)	enabled
9	0	disabled	disabled
10	1	disabled	disabled
11	0	disabled	disabled
12	1	disabled	disabled
13	0	disabled	disabled
14	1	disabled	disabled
15	0	disabled	disabled
16	1	disabled	disabled

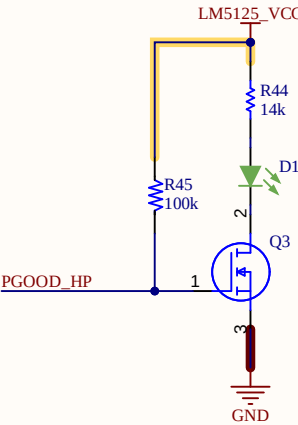
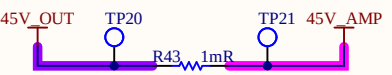
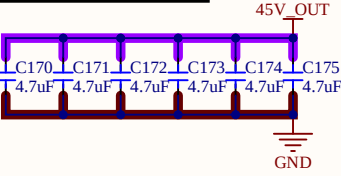
Table 6-1. CFG0-pin Settings		
Level	Dead Time [µs]	20µA ATRK Current
1	14	on
2	30	on
3	50	on
4	75	on
5	100	on
6	125	on
7	150	on
8	200	on
9	14	off
10	30	off
11	50	off
12	75	off
13	100	off
14	125	off
15	150	off
16	200	off

Figure 1

Eval Board Copied : PMP31306



Cap analysis



PCB FAB 006913-111/01_A PCBA 006913-111/01_A VARIANT [No Variations]

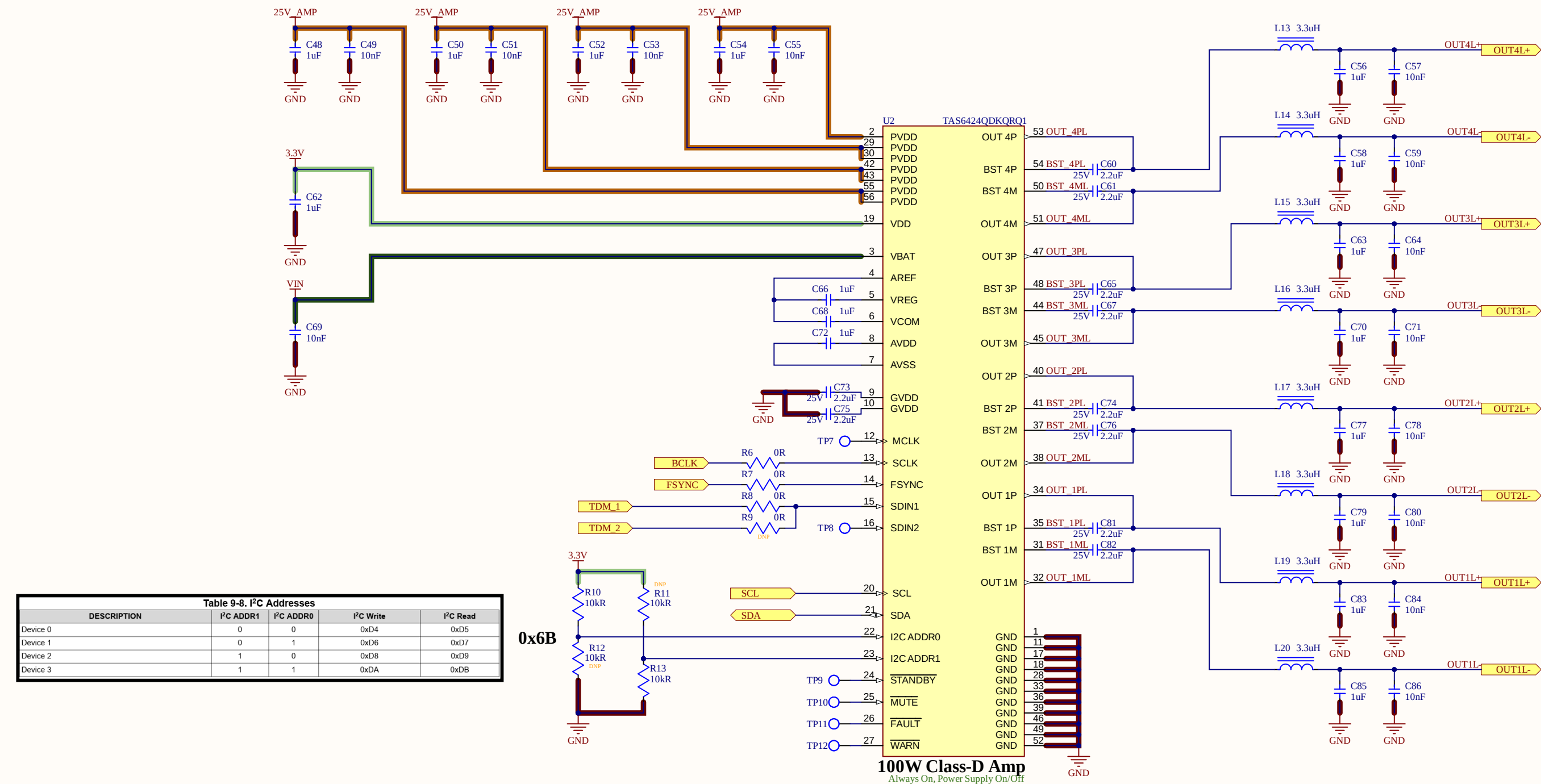
TITLE High Power

PROJECT WAVE

DATE 8/21/2025 ENG Sebastian Forenza SHEET * OF *

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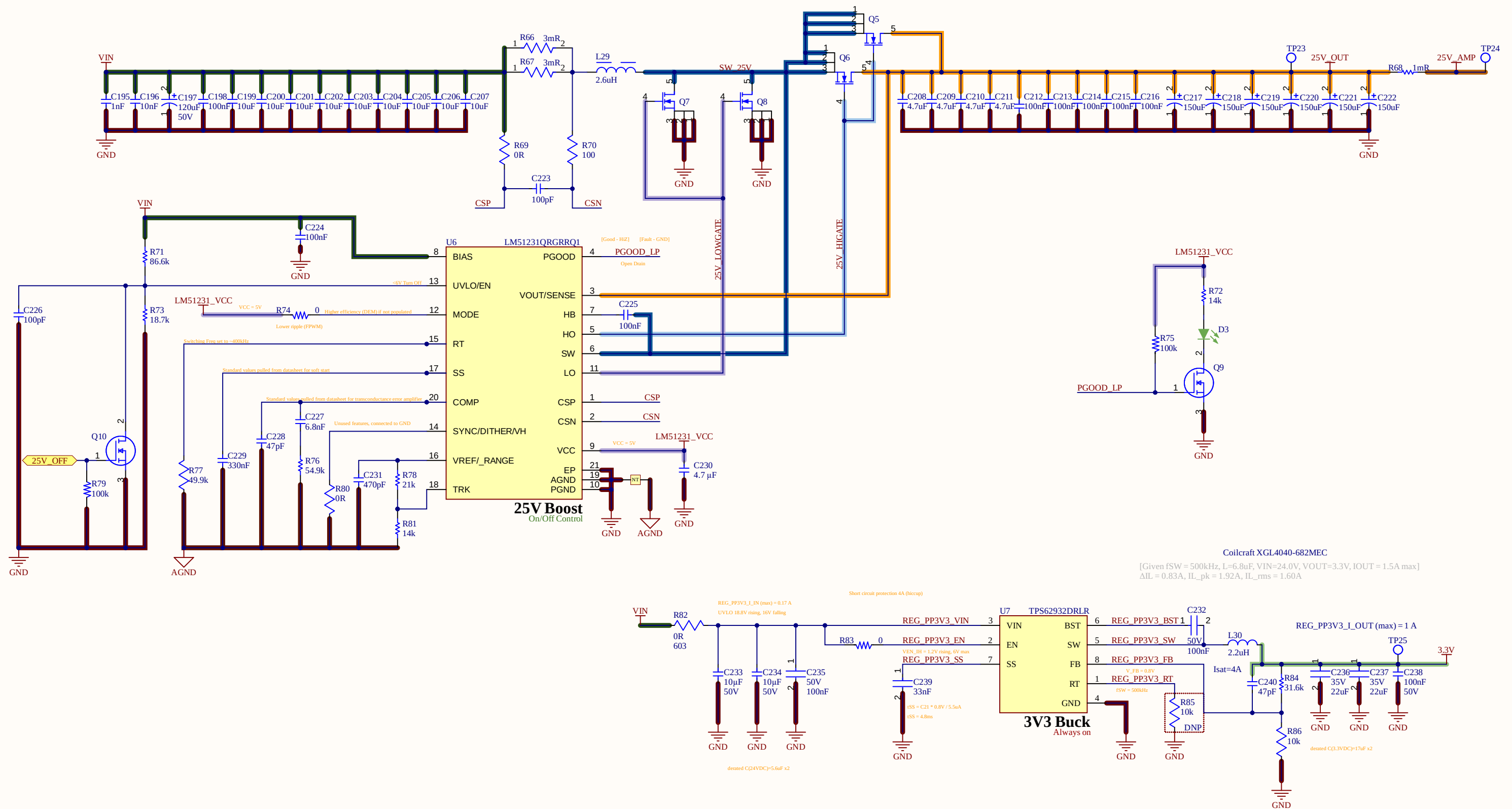


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TITLE Low Power Amp		
PROJECT WAVE		
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TITLE					
Low Power					
PROJECT					
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