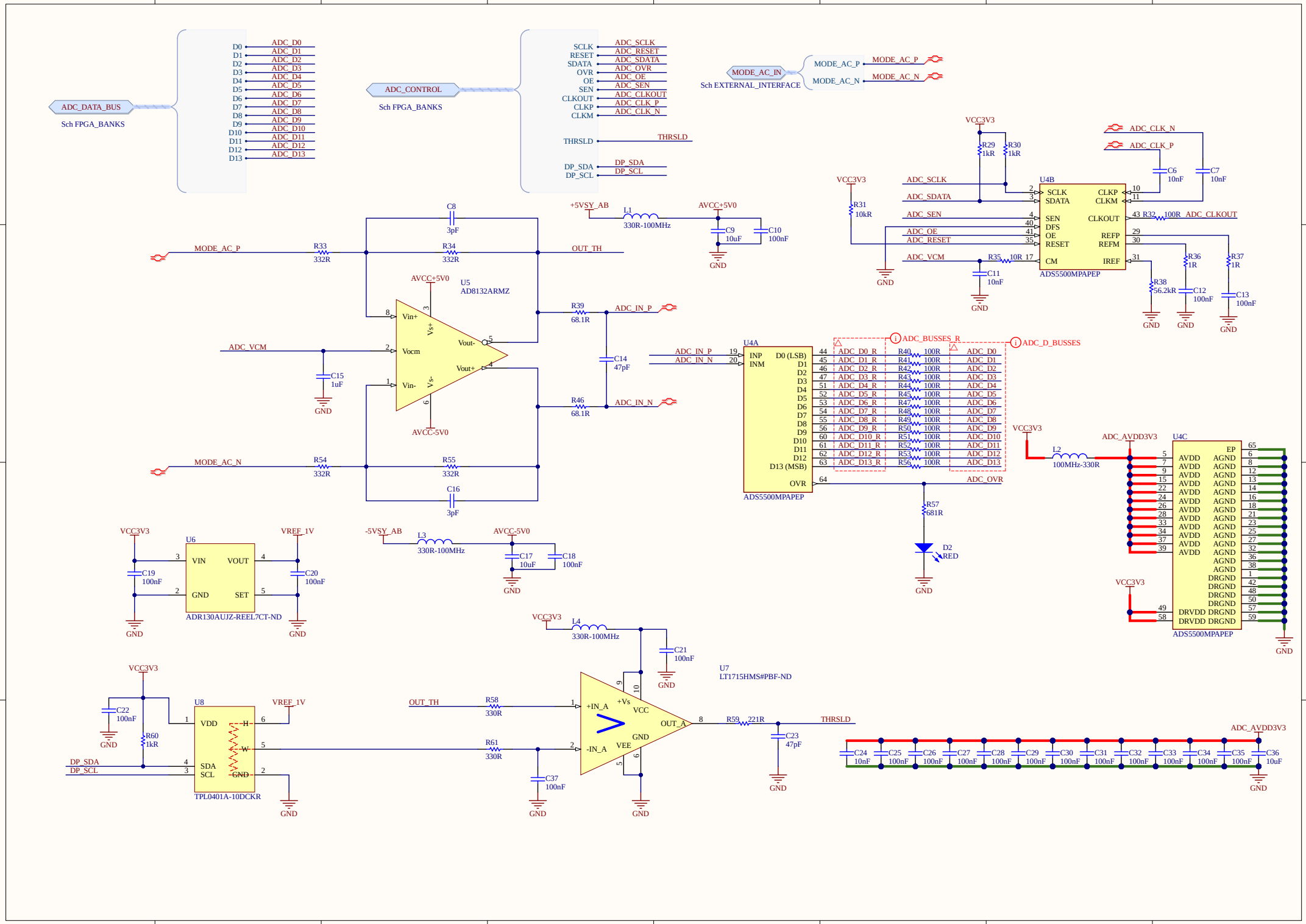
ADC_DATA_BUS
Sch FPGA_BANKS
D0 ADC_D0
D1 ADC_D1
D2 ADC_D2
D3 ADC_D3
D4 ADC_D4
D5 ADC_D5
D6 ADC_D6
D7 ADC_D7
D8 ADC_D8
D9 ADC_D9
D10 ADC_D10
D11 ADC_D11
D12 ADC_D12
D13 ADC_D13
ADC_CONTROL
Sch FPGA_BANKS
SCLK ADC_SCLK
RESET ADC_RESET
SDATA ADC_SDATA
OVR ADC_OVR
OE ADC_OE
SEN ADC_SEN
CLKOUT ADC_CLKOUT
CLKP ADC_CLK_P
CLKM ADC_CLK_N
THRSLD THRSLD
DP_SDA DP_SDA
DP_SCL DP_SCL
MODE_AC_IN
Sch EXTERNAL_INTERFACE
MODE_AC_P MODE_AC_P
MODE_AC_N MODE_AC_N
VCC3V3
R29 1kR
R30 1kR
R31 10kR
U4B
ADS5500MPAPEP
ADC_CLK_N
ADC_CLK_P
C6 10nF
C7 10nF
R32 100R ADC_CLKOUT
R35 10R
C11 10nF
R36 1R
R37 1R
R38 56.2kR
C12 100nF
C13 100nF
GND
+5VSY_AB
L1 330R-100MHz
AVCC+5V0
C9 10uF
C10 100nF
C8 3pF
MODE_AC_P
R33 332R
R34 332R
OUT_TH
U5
AD8132ARMZ
Vin+
Vocm
Vin-
Vout-
Vout+
Vs+
Vs-
ADC_VCM
C15 1uF
AVCC-5V0
R39 68.1R
ADC_IN_P
C14 47pF
R46 68.1R
ADC_IN_N
MODE_AC_N
R54 332R
R55 332R
C16 3pF
U4A
INP
INM
D0 (LSB)
D13 (MSB)
OVR
ADS5500MPAPEP
ADC_BUSSES_R
ADC_D_BUSSES
R40 100R
R57 681R
D2 RED
L2 100MHz-330R
ADC_AVDD3V3
U4C
EP
AVDD
AGND
DRGND
DRVDD
ADS5500MPAPEP
U6
ADR130AUJZ-REEL7CT-ND
VIN
VOUT
GND
SET
VREF_1V
C19 100nF
C20 100nF
-5VSY_AB
L3 330R-100MHz
AVCC-5V0
C17 10uF
C18 100nF
L4 330R-100MHz
C21 100nF
U7
LT1715HMS#PBF-ND
+IN_A
-IN_A
+Vs
VCC
GND
VEE
OUT_A
R58 330R
R61 330R
C37 100nF
R59 221R
THRSLD
C23 47pF
C22 100nF
R60 1kR
U8
TPL0401A-10DCKR
VDD
SDA
SCL
H
W
DP_SDA
DP_SCL
C24 10nF
C25 100nF
C26 100nF
C27 100nF
C28 100nF
C29 100nF
C30 100nF
C31 100nF
C32 100nF
C33 100nF
C34 100nF
C35 100nF
C36 10uF