

DAC3xJ8x Device Initialization and SYSREF Configuration

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ABSTRACT

In JESD204B subclass 1 system, system reference signal (SYSREF) plays an important role to ensure all the devices in the system are synchronized and initialized correctly. For the DAC3xJ8x family of DAC devices, the SYSREF not only serves as a signal to initialize the JESD204B link, but it also provides a timing signal to some of the internal digital blocks such as the NCO and complex mixer to ensure multiple DAC3xJ8x devices have the same processing latency across the digital blocks. This application note describes the basic mechanics and configuration of the SYSREF signal for the DAC3xJ8x family of DAC devices.

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1 Acronyms

DAC –	Digital-to-analog converter
CW –	Constant wave (or sine wave)
Multi-frame (K) –	The number of frames in the multi-frame in JESD204B specification.
Frame (F) –	The number of octets in a frame in JESD204B specification.
QMC –	Quadrature modulator correction signal processing block.
JESD204B TX –	JESD204B transmitter. In a JESD204B system of FPGA/ASIC and the DAC3xJ8x device, this is referred to as FPGA/ASIC.
JESD204B RX -	JESD204B receiver. In a JESD204B system of FPGA/ASIC and the DAC3xJ8x device, this is referred to as DAC3xJ8x.
LMFC –	Local multi-frame clock. This is a JESD204B sub-clock indicating the boundary of multi-frame.
S2P –	Serial-to-parallel conversion. This refers to the data packing on the JESD204B RX.
P2S –	Parallel-to-serial conversion. This refers to the data packing on the JESD204B TX.
SYSREF –	System reference clock. This refers to the reference needed in the JESD204B subclass 1 system where the reference clock is used to align LMFC.
DAC3xJ8x –	A family of JESD204B subclass 1 DAC devices.

2 Introduction

The DAC38J84 family of devices (DAC3xJ8x) are complex, mixed-signal, high-performance digital-to-analog converter (DAC) devices with the JESD204B receiver block (JESD204B RX) for high-speed serial-to-parallel (S2P) data transfer. Also included are various digital signal processing blocks such as interpolation filters, mixers, and quadrature modulator correction filters. Due to the operating nature of these digital blocks, the DAC3xJ8x has various divided down clocks running internally, including the local multi-frame clock (LMFC) for JESD204B data transfer.

The DAC3xJ8x is part of the JESD204B system, and the JESD204B system implements high-speed parallel-to-serial (P2S) on the JESD204B TX device and S2P transfer on the JESD204B RX device. The packing of the data depends on the frame and multiple frames of octets, depending on the S2P or P2S transfer. If one cycle of these high-speed data transfers after the P2S stage is misaligned and delayed in time, a relatively larger amount of data may be shifted in time after the S2P process, therefore resulting in a much larger latency variation.

To achieve the overall system synchronization, the DAC3xJ8x LMFC alignment with the overall system multi-frame clock is critical. Without alignment, the relative latency of the data transfer from JESD204B TX device to the DAC3xJ8x JESD204B RX side varies. The DAC3xJ8x is a JESD204B, subclass 1 device using an external system reference clock (SYSREF) signal as a common reference for multiple devices. The ultimate goal of using a global distributed SYSREF for LMFC is to ensure all the JESD204B devices (include TX and RX) are aligned upon initialization. The overall latency of the JESD204B data transfer can be deterministic, which may also be important for system designers who wish to implement multiple device synchronization in the system.

With JESD204B subclass 1, SYSREF is source synchronous to the device clock and should come from the same clock source. It can be a one-shot pulse, gapped periodic, or periodic signal. In the case of a gapped or periodic signal, the SYSREF must be an integer multiple of the LMFC to prevent SYSREF from occurring in the middle of a multi-frame.

System designers can implement deterministic latency between a JESD204B TX and JESD204B RX device when the internal LMFC clocks are aligned to the edge of the device clock when the SYSREF is sampled high. This should also align or reset all the internal clocks of the TX and RX devices. Furthermore, you can achieve multiple device synchronization by ensuring that the deterministic latency is the same for each TX-to-RX link in your group of devices.

The clock chip generates the SYSREF signal that meets the setup and hold times of the device clock and must be distributed to each group of TX and RX devices with matched trace lengths to ensure proper alignment of the signals. System designers should use a clock chip, such as the LMK04828, capable of generating both the SYSREF and the device clocks to minimize the skew between the signals. The timing signals required for subclass 1 are shown in Figure 1.

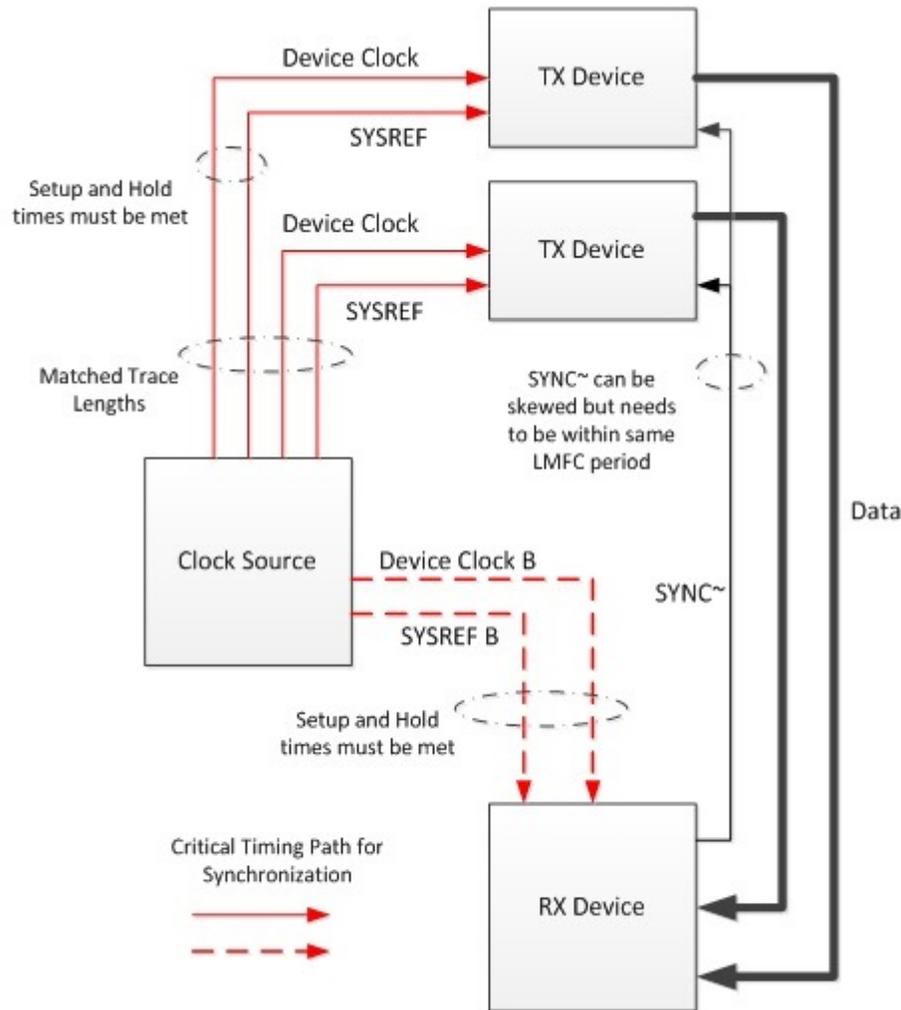


Figure 1. Subclass 1 Timing Signals With Trace Length Matched SYSREF and Device Clock Groups

It is not mandatory for the clock chip to generate the exact same SYSREF for all TX and RX devices, but the clock chip should generate different SYSREFs in such a way that there is a deterministic relationship between when SYSREF is sampled high in all of the devices. In this case, as shown in Figure 2, the latency is deterministic but not minimized.

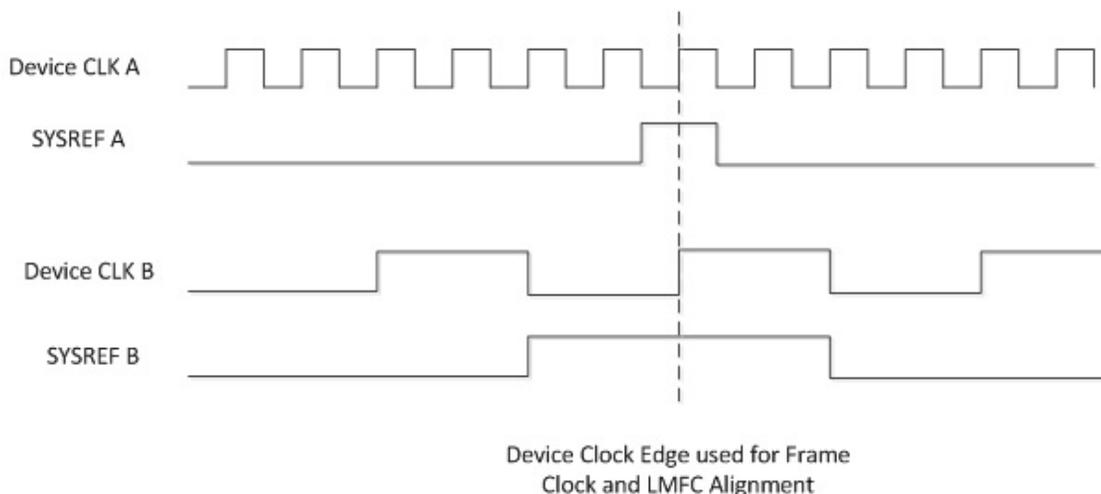


Figure 2. Multiple Devices Using Different SYSREF and Device Clocks With a Deterministic Relationship

Once the system completes LMFC alignment, future SYSREF pulses can be a reference to check the alignment of the local frame and multiframe clocks. Be sure to turn SYSREF off during normal operation, as a periodic SYSREF signal runs at a sub-harmonic of the sampling clock and may create unwanted spurs. If the SYSREF signal is coupled onto the DAC3xJ8x output, the frequency spectrum of the DAC3xJ8x output typically shows two CW spurs that are on both sides of the main signal output. The distance of the spurs to the main signal is at the SYSREF frequency, due to the modulation from the noise coupling.

The DAC3xJ8x is a subclass 1 device and only uses the \sim SYNC signal in the code group synchronization (CGS) process. The \sim SYNC is not a critical timing signal for a subclass 1 JESD204B system. The DAC3xJ8x has one pair of LVDS signals (SYNCBp/n) and two pairs of CMOS signals (SYNCA and SYNCB) that can represent the \sim SYNC of up to two JESD204B links (Link0, Link1, or both). Upon the triggering of SYSREF to the internal digital blocks, the respective \sim SYNC signals are in logic LOW to start the link initialization process.

3 LMFC and SYSREF Period

To calculate the LMFC of various JESD204B link configurations, refer to Equation 1.

$$\text{LMFC (Hz)} = \frac{\text{SERDES Line Rate (bps)}}{10 F K}$$

where

- F = number of octets per frame
- K = number of frames per multi-frame

(1)

If periodic SYSREF signal is used through the system, the SYSREF frequency must be an integer factor of the LMFC.

$$\text{SYSREF (Hz)} = \frac{\text{SERDES Line Rate (bps)}}{10 n F K}$$

where

- n = positive integers of 1, 2, 3, ...

(2)

4 DAC3xJ8x Clock Divider and JESD204B Logic

4.1 Clock Divider and JESD204B Logic Core Descriptions

The DAC3xJ8x has a clock divider block and a JESD204B logic block. The clock divider is to provide divided-down clocks for all the digital logics such as JESD204B logic, FIR filter logics for the interpolation filters, and complex mixers. Figure 3 shows the simplified clock divider structure. The source of the clock divider comes from the DACCLK, and the clock divider can be reset by the SYSREF signal.

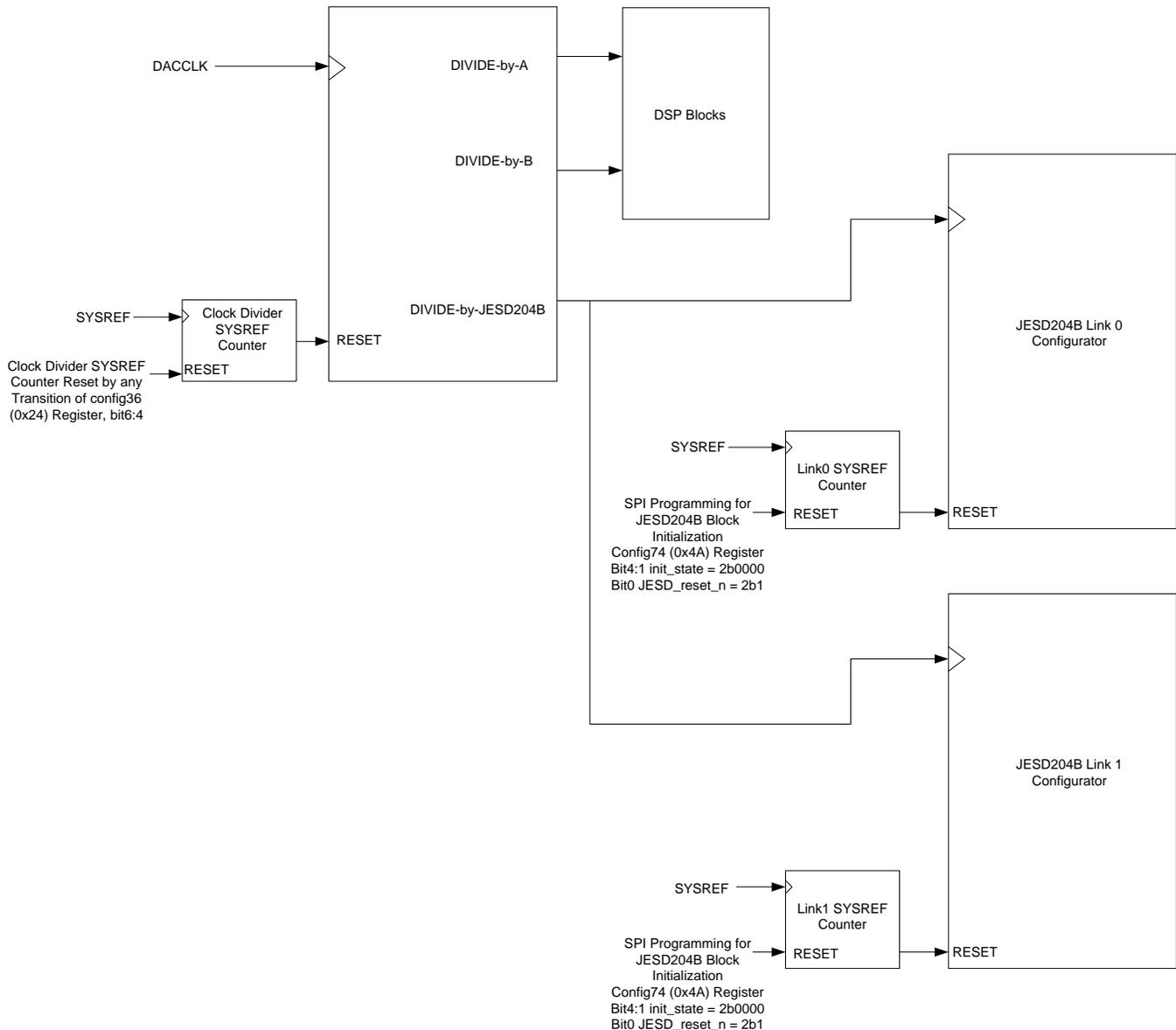


Figure 3. Clock Divider and JESD204B Simplified Circuit Diagrams

The JESD204B logic block operates on one of the divided-down clocks from the clock divider. The DAC3xJ8x JESD204B only supports up to two independent links (that is, Link1 and Link0). If only one link is used, the default link should be Link0. Therefore, configure only `sysref_mode_link1` and `sysref_mode_link0`. Set both `sysref_mode_link3` and `sysref_mode_link2` to 4b'000.

Both the clock divider and JESD204B block are the essential blocks for the JESD204B link initialization. After both blocks are initialized through the triggering of SYSREF pulse, the JESD204B link initialization starts. Basically, the DAC3xJ8x issues a sync request to the JESD204B TX (default configuration behavior is to pull the LVDS SYNCB pair from logic HIGH to logic LOW). The JESD204B TX starts the CGS stage, which is the beginning of the JESD204B link start-up.

4.2 Clock Divider and JESD204B Logic Core Initializer

The clock divider and JESD204B block initializers require the SYSREF signal to provide correct initialization for the DAC3xJ8x device operation. They can be armed to register all SYSREF pulses or to register only the first, the second, or the third pulse. The exact configuration for the clock divider depends on config36, bit6:4 *cdvrserv_sysref_mode* (see Table 1), while the configuration for the JESD204B block depends on config92, bit6:4 *sysref_mode_link1* (see Table 2), and config92, bit2:0 *sysref_mode_link0* (see Table 2).

For the clock divider, the start of the clock divider reset pulse count is based on any SPI register transition of config36 (0x24) Register, bit6:4. Basically, upon programming of the *cdvrserv_mode_sysref* register, the clock divider reset counter for SYSREF starts and determines which SYSREF pulse to use. TI recommends initializing the clock divider logic before the JESD204B Link0 and Link1 logic since the Link0 and Link1 logic blocks derive their clock from the main clock divider.

For the Link0 and Link1 logic block, the start of the SYSREF pulse count for the initializer is based on the time instance when the JESD204B block is initialized through config74, *init_state* = 4b'0000 and config74, *jesd_reset_n* = 1b'1 (see Table 3). These register writes allows the JESD204B block initializers to start and begin counting the SYSREF edges. Note that the JESD204B blocks can be initialized at a later time by deterministic SYSREF pulses. The SYSREF pulse to the clock divider and to the JESD204B logic block do not have to be the same. They must have the same relationship even after a certain period of time. Basically, the SYSREF pulses have to occur at the expected time without any time delay or phase shift as shown in Figure 4.

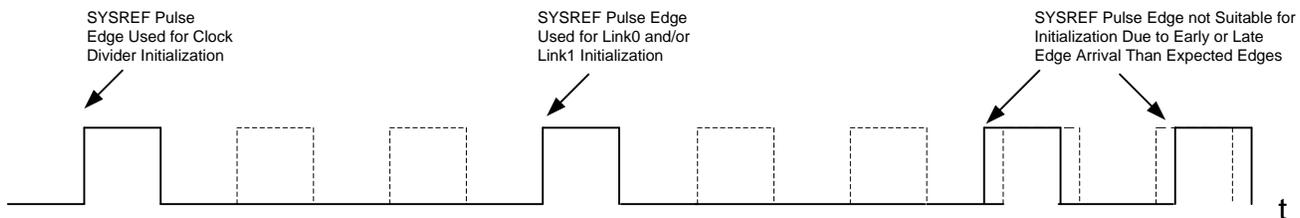


Figure 4. SYSREF Pulses Used for Clock Divider and Link0 or Link1 Initialization With Deterministic Relationship

Table 1. Register Name: config36 – Address: 0x24, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config36	0x24	15:13	reserved	Reserved	000
		12:7	reserved	Reserved	000000
		6:4	<i>cdvrserv_sysref_mode</i>	Determines how SYSREF is used to sync the clock dividers in the device. 000 = Do not use SYSREF pulse 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses.	000
		3:2	reserved	Reserved	00
		1:0	reserved	Reserved	00

Clock Divider SYSREF Counter reset by any transition of config36 (0x24) Register, bit6:4

Table 2. Register Name: config92 – Address: 0x5C, Default: 0x1111

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config92	0x5C	15	err_cnt_clr_link3 ⁽¹⁾	A transition from 0≥1 causes the error_cnt for link3 to be cleared.	0
		14:12	sysref_mode_link3 ⁽²⁾	Determines how SYSREF is used in the JESD synchronizing block. 000 = Don't use SYSREF pulse 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses. 101 = Skip two SYSREF pulses then use only the next one 110 = Skip two SYSREF pulses then use all pulses.	001
		11	err_cnt_clr_link2 ⁽¹⁾	A transition from 0≥1 causes the error_cnt for Link2 to be cleared.	0
		10:8	sysref_mode_link2 ⁽²⁾	Determines how SYSREF is used in the JESD synchronizing block. 000 = Don't use SYSREF pulse 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses. 101 = Skip two SYSREF pulses then use only the next one 110 = Skip two SYSREF pulses then use all pulses.	001
		7	err_cnt_clr_link1	A transition from 0≥1 causes the error_cnt for Link1 to be cleared.	0
		6:4	sysref_mode_link1	Determines how SYSREF is used in the JESD synchronizing block. 000 = Don't use SYSREF pulse 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses. 101 = Skip two SYSREF pulses then use only the next one 110 = Skip two SYSREF pulses then use all pulses.	001
		3	err_cnt_clr_link0	A transition from 0≥1 causes the error_cnt for Link0 to be cleared.	0
		2:0	sysref_mode_link0	Determines how SYSREF is used in the JESD synchronizing block. 000 = Don't use SYSREF pulse 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses. 101 = Skip two SYSREF pulses then use only the next one 110 = Skip two SYSREF pulses then use all pulses.	001

⁽¹⁾ err_cnt_clr_link3 and err_cnt_clr_link2 are not used in the DAC3xJ8x family.

⁽²⁾ Set sysref_mode_link3 and sysref_mode_link2 to 3b'000 at all times since DAC3xJ8x does not utilize link3 and link2.

Table 3. Register Name: config74 – Address: 0x4A, Default: 0x001E

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config74	0x4A	15:8	lane_ena	Turn on each SerDes lane as needed. Signal is active high. bit15 : SerDes lane7 enable bit14 : SerDes lane6 enable bit13 : SerDes lane5 enable bit12 : SerDes lane4 enable bit11 : SerDes lane3 enable bit10 : SerDes lane2 enable bit9 : SerDes lane1 enable bit8 : SerDes lane0 enable	0x00
		7:6	jesd_test_seq	Set to select and verify link layer test sequences. The error for these sequences comes out the lane alarms bit0. 1= fail and 0 = pass. 00 : test sequence disabled 01 : verify repeating D.21.5 high frequency pattern for random jitter 10 : verify repeating K.28.5 mixed frequency pattern for deterministic jitter 11 : verify repeating ILA sequence	00
		5	dual	Turn on "DUAL DAC" mode. This disables the clocks to the C and D data paths, reducing the power of the DIG block.	0
		4:1	init_state	Put the JESD block into "INIT_STATE" mode when high. During this mode the JESD can be programmed and its outputs will stay at zero. NOTE: See the JESD description of the correct startup sequence.	1111
		0	jesd_reset_n	Reset the JESD block when low. NOTE: See the JESD description of the correct startup sequence.	0

For Link0 and Link1 configuration, the pulse count starts after the following JESD204B initialization register:

```
init_state = 4b'1111 and jesd_reset_n = 1b'0
init_state = 4b'1111 and jesd_reset_n = 1b'1
init_state = 4b'0000 and jesd_reset_n = 1b'1
```

4.3 SYSREF Gating

Once the overall system establishes the DAC3xJ8x JESD204B RX link to the system JESD204B TX link, the SYSREF signal to the DAC3xJ8x may be turned off to save power consumption and also reduce noise coupled into the DAC3xJ8x output. If `cdvrser_sysref_mode`, `sysref_mode_link1`, and `sysref_mode_link0` are set to register only the single rising edge of SYSREF, the SYSREF signal may be turned off at any time after the link is established. TI recommends setting the clock divider and the JESD204B block initializer to register single SYSREF pulses, if possible, to prevent false re-initialization due to potential SYSREF glitches or noise coupling. Also, since the clock divider provides the JESD204B clock, TI recommends system designers initialize the clock divider using either the first or second pulse, and then initialize the JESD204B block using either the second or the third pulse. Basically, the initialization of the JESD204B block is staggered behind the initialization of the clock divider.

Some system designers may prefer a continuous SYSREF signal present at all times to ensure stable system synchronization. Typically in this situation, the clock divider and JESD204B block are set to register all SYSREF pulses. If at any time the SYSREF signal needs to be disabled, the system designer must plan for additional transient behaviors, depending on the network between the SYSREF driver and SYSREF receiver. The easiest approach is first to set `cdvrser_sysref_mode`, `sysref_mode_link1`, and `sysref_mode_link0` to all zeros to prevent clock divider and JESD204B logic from re-initializing due to the transients of disabling SYSREF. After programming these initializers to all zeros, disabling SYSREF will not affect these digital core blocks. The approach to prevent transient behaviors from falsely triggering the SYSREF receiver are described in [AC Coupled Approach](#) and [DC Coupled Approach](#).

5 SYSREF Initialization for DSP Blocks

Various DSP blocks on the DAC3xJ8x such as NCO, mixer, and QMC may be initialized by SYSREF as an option. This is one of the best options to achieve deterministic initialization to multiple device DSP blocks.

5.1 Initializing the Digital Signal Processing Blocks

The initialization of the DSP blocks in the DAC3xJ8x family is similar to the DAC348x family. The first option is using the JESD204B_syncout feature to initialize some of the blocks, and the JESD204B_syncout triggers upon the completion of the JESD204B link establishment. The SYSREF can also be used, but the designer must take care of potential interruption of JESD204B block and clock divider block once these blocks are initialized. If the SYSREF is used to initialize various DSP blocks, the designer must program the JESD204B block and clock divider block to not look at the SYSREF signal to prevent false initialization. The same AUTO-SYNC and SIF_SYNC feature available on the DAC348x family also carried forward to the DAC3xJ8x family. For more details, refer to *DAC348x Device Configuration and Synchronization* ([SLAA584](#)).

The most suitable initialization SYSREF signal for these DSP blocks is a single pulse SYSREF. [Figure 5](#) shows the initialization signal selection block for the complex mixer blocks and NCO block. Using these DSP block requires the JESD204B link to be established, therefore the initialization of these DSP blocks comes after the clock divider and JESD204B block initialization. TI recommends setting the clock divider and JESD204B block to register only single pulse-based SYSREF or to disable registering SYSREF after link establishment. This prevents the JESD204B link from false re-initialization when the DSP blocks are being initialized with SYSREF pulses.

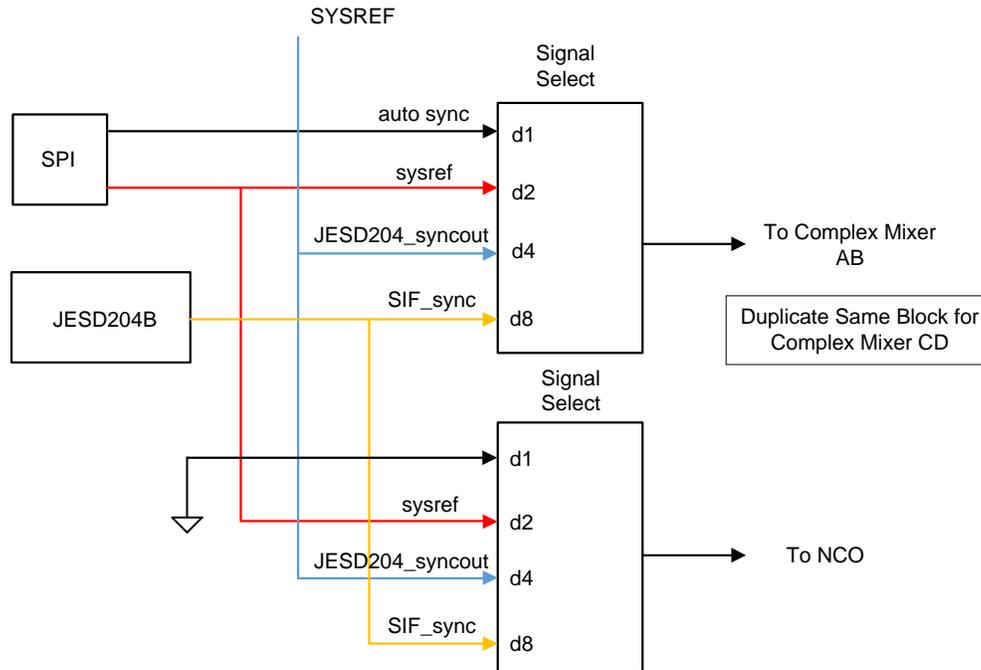
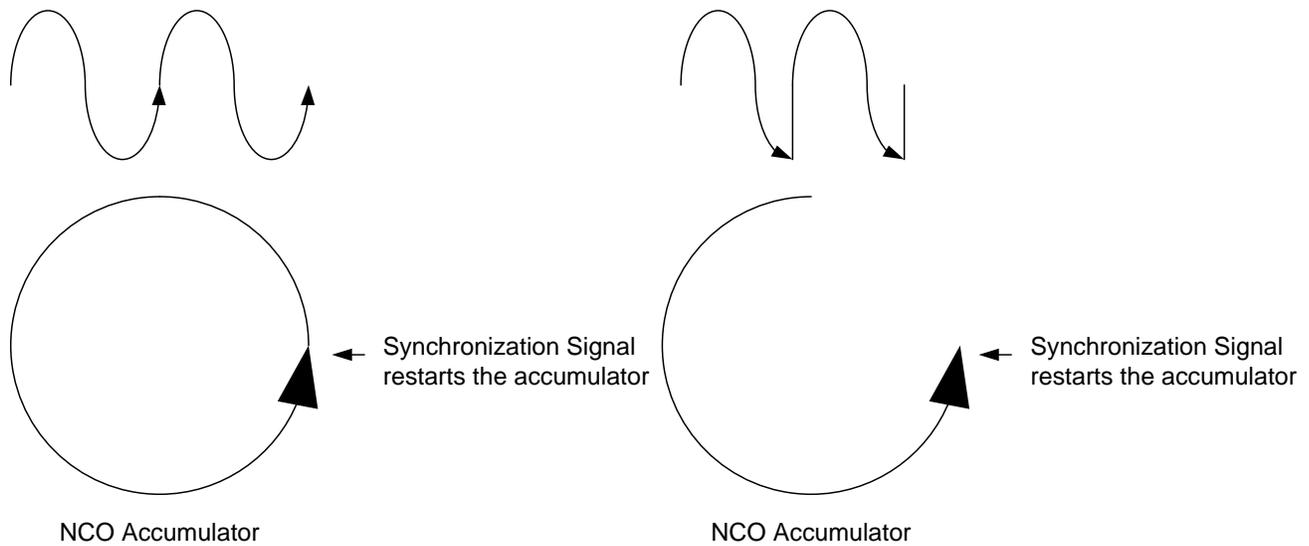


Figure 5. DSP Initialization Signal Options

Using periodic SYSREF pulses to initialize these DSP blocks may cause periodic interruption to the DSP operation. For instance, if the NCO accumulator is initialized by the SYSREF with periodic pulses, then the NCO frequency must be an integer multiple of the SYSREF period. Otherwise, the NCO accumulator cannot cycle through the counter completely before the next SYSREF reset. As shown in [Figure 6](#), use the SYSREF initialization feature with caution.



The NCO frequency is an integer multiple of the synchronization signal. The NCO can cycle through completely before the next reset.

The NCO frequency is not integer multiple of synchronization signal. The NCO cannot cycle through completely before the next reset. Output waveforms are distorted.

Figure 6. NCO Accumulator Operation with Repetitive Synchronization Signals

6 DAC3xJ8x DACCLK and SYSREF Receivers

The DAC3xJ8x DACCLK and SYSREF receivers (shown in Figure 7) have delay-matched receiver design given the external clock and SYSREF inputs have identical driver behavior and are AC coupled. The internal resistor divider networks set the common mode voltage of the DACCLK and SYSREF receivers at 0.5 V nominal.

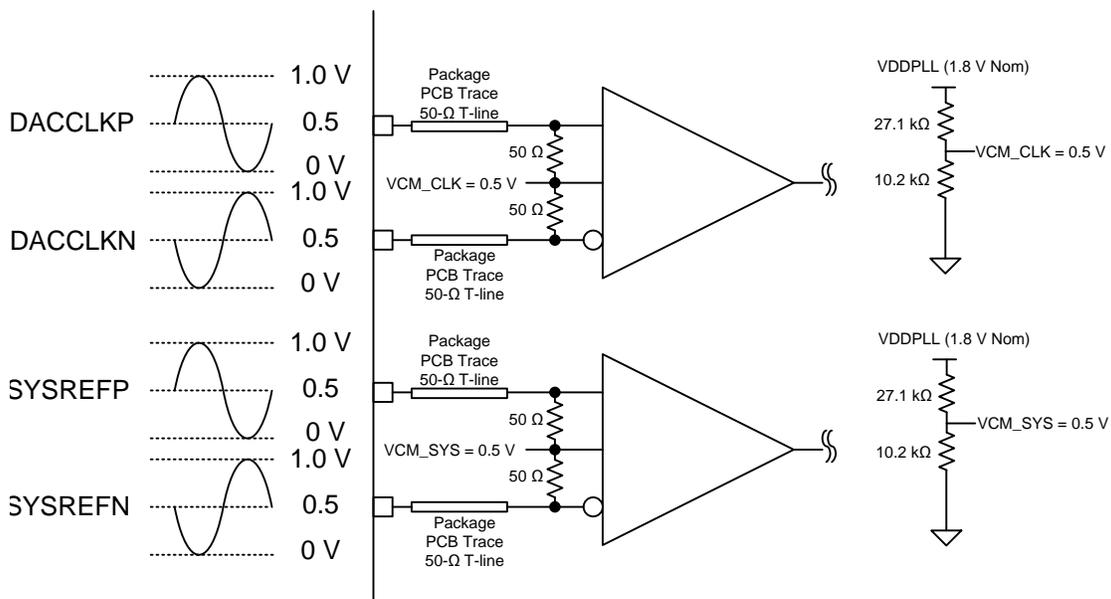


Figure 7. DACCLKp/n and SYSREFp/n Receiver Circuits

Each input leg of the receiver has on-chip 50-Ω termination that is tied to the respective VCM node. Based on the DAC3xJ8x datasheet, the minimum swing for each leg is 400 mVpp of |Vid|. Since the input presented at each pin cannot swing below ground, the maximum swing for each leg can theoretically be 1Vpp of |Vid|.

To achieve high clock-signal performance, both the DACCLK and SYSREF receivers have no hysteresis mechanism build-in. Therefore, if any of the digital core initializers are actively looking for SYSREF while the SYSREF receiver inputs are both set at VCM, these digital circuits may register false SYSREF triggering, mainly from noise disturbance near the receiver threshold. If any digital block initializers are actively registering a SYSREF signal, a differential voltage of 100 mVpp must be present at the SYSREF receiver to avoid false triggering due to noise disturbance.

The timing relationship between the DACCLK and SYSREF signal is stringent in a JESD204B system. Therefore, the signal path network of the DACCLK and SYSREF signals must be as similar as possible to ensure that the signal relationship is maintained from the launch of the signal, through their respective channels to the DACCLK and SYSREF input receivers. The SYSREF timing requirements depend on whether deterministic latency of the JESD204B link is required. If deterministic latency is required, then the SYSREF signal must meet setup and hold requirements relative to the DACCLK signal. If deterministic latency is not required, then the SYSREF signal may be supplied as an asynchronous signal resulting in latency variation in the orders of multiple clock periods.

TI recommends AC coupling for the SYSREF interface as described in [AC Coupled Approach](#). For certain instances, DC coupled SYSREF interface may also be implemented with discretion. Please see [DC Coupled Approach](#) for details.

7 AC Coupled Approach

The AC coupled network ensures both the DACCLK and SYSREF signal timing are well matched and controlled, given the DACCLK and SYSREF drivers are identical in behavior. Due to this, TI recommends this network for applications requiring deterministic latency across the DAC3xJ8x device or multiple DAC3xJ8x device synchronization. [Figure 8](#) shows an example interface from the LMK04828 LVPECL driver.

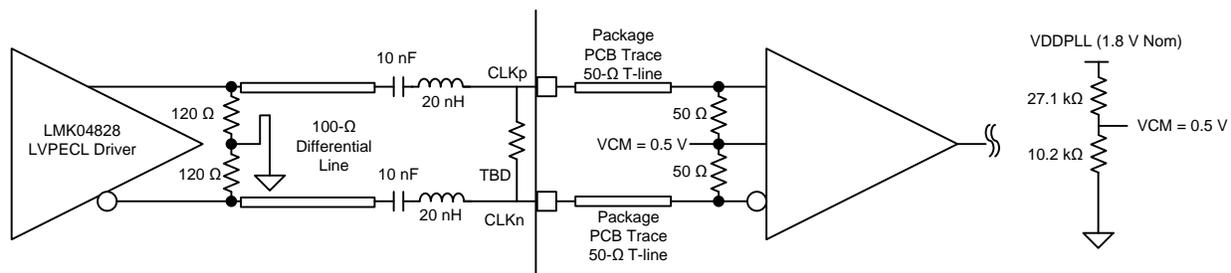


Figure 8. LMK04828 LVPECL Interface

The AC coupled network requires series capacitors to allow the common mode voltage on both the SYSREF driver and SYSREF receiver to establish independently. Therefore, the series capacitors, along with the DAC3xJ8x SYSREF receiver on-chip 50-Ω termination, forms a high-pass response to isolate the common mode voltage of the driver and receiver. The high-pass corner is the typical first order response with cut-off frequency and time constant as follows:

$$F_c = \frac{1}{2\pi RC} \quad \tau = RC \quad (3)$$

7.1 Compatible SYSREF Signals for AC Coupled Networks

The AC coupled network allows the implementation of the typical three types of SYSREF signals: periodic, gapped periodic, or one shot pulse. Periodic SYSREF signal is the most ideal situation for overall system synchronization because this maintains constant, steady bias for both the driver and receiver and also allows consistent SYSREF pulses for device synchronization. When implementing gapped periodic or one shot pulse, however, system designers must pay special attention to the SYSREF driver and the overall AC coupled network. The ideal SYSREF driver for gapped periodic or one shot pulse is that the driver must maintain common mode bias between idle period and active period. This behavior maintains the charge of the series capacitor and does not impact the SYSREF waveform at the receiver side. The trade-off is mainly based on the concern for double sideband spurs and additional power consumption due to the active SYSREF driver. Refer to [Table 4](#) for detail.

Table 4. Comparison Among Period, Gapped Period, and One Shot SYSREF

	Periodic	Gapped Periodic or One Shot
Benefits	Constant, steady bias for both driver and receiver. Consistent, timely SYSREF pulses for device synchronization. Active SYSREF signaling prevents potential false SYSREF triggering at the receiver due to noise disturbance.	No risk for double sideband spurs due to active SYSREF driver. Saves system power consumption by disabling SYSREF driver. Useful for initializing various DSP blocks such as QMC and Mixer in multiple DAC3xJ8x device synchronization scenario. Clock Divider and JESD204B blocks must be programmed to not register SYSREF after JESD204B link establishment to avoid false re-initialization of the link.
Drawbacks	Potential double sideband spurs modulated onto the DAC output spectrum. Additional power consumption from active SYSREF driver. Difficult to implement DSP block initialization due to the cyclic nature of SYSREF. For instance, the NCO frequency may not be correct due to continuous reset of SYSREF pulses.	SYSREF driver must be pre-biased at its own VCM to avoid transients during active state. SYSREF receiver may register false SYSREF triggering during SYSREF driver idle state. If any digital block initializers are actively registering SYSREF signal, a differential voltage of 100 mVpp must be present at the SYSREF receiver to avoid noise disturbance.

7.2 SYSREF Driver Constraints for Gapped Periodic or One Shot SYSREF

As long as the SYSREF driver can maintain its own VCM, and ensure the VCM does not change between idle and active state, system designers may implement gapped periodic or one-shot SYSREF for the AC coupled network. The TI TINA SPICE simulation in Figure 9 shows a typical LVPECL driver interfacing with the DAC3xJ8x SYSREF receiver in AC coupled fashion. The driver has a typical V_{OH} of 2.21 V and V_{OL} of 1.25 V, and the VCM of the driver at steady state is 1.73 V. The AC coupling capacitor is the typical 100-nF value with on-chip 50- Ω resistor at the SYSREF receiver. The time constant is in the range of 5 μ s. The driver has been pre-biased at 1.73 V for 100 μ s of simulation time and started to toggle immediately after 100 μ s. As the results in Figure 10 show, at the receiver side after the AC coupling capacitor, the toggling remains smooth and no transients are observed due to the driver pre-bias at VCM.

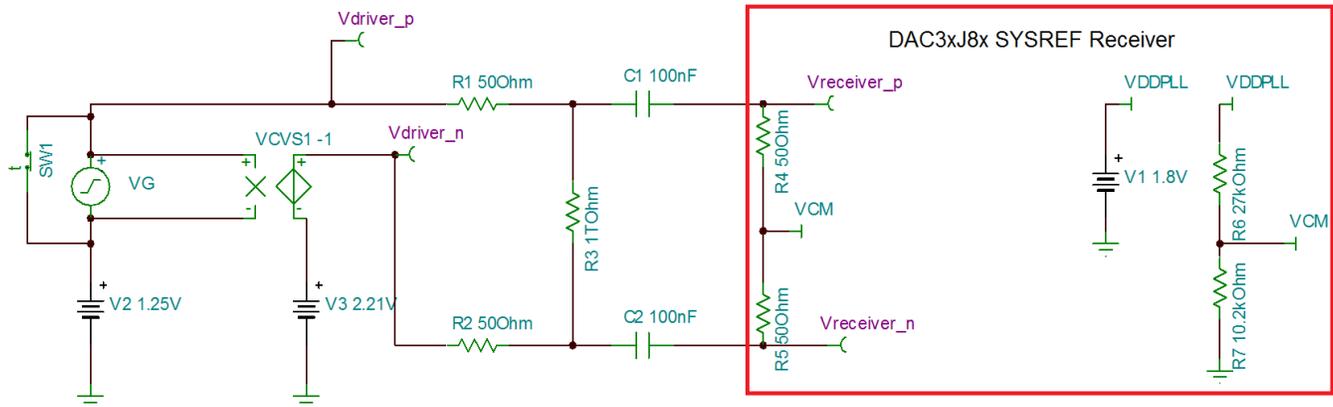


Figure 9. TI TINA SPICE Simulation Model

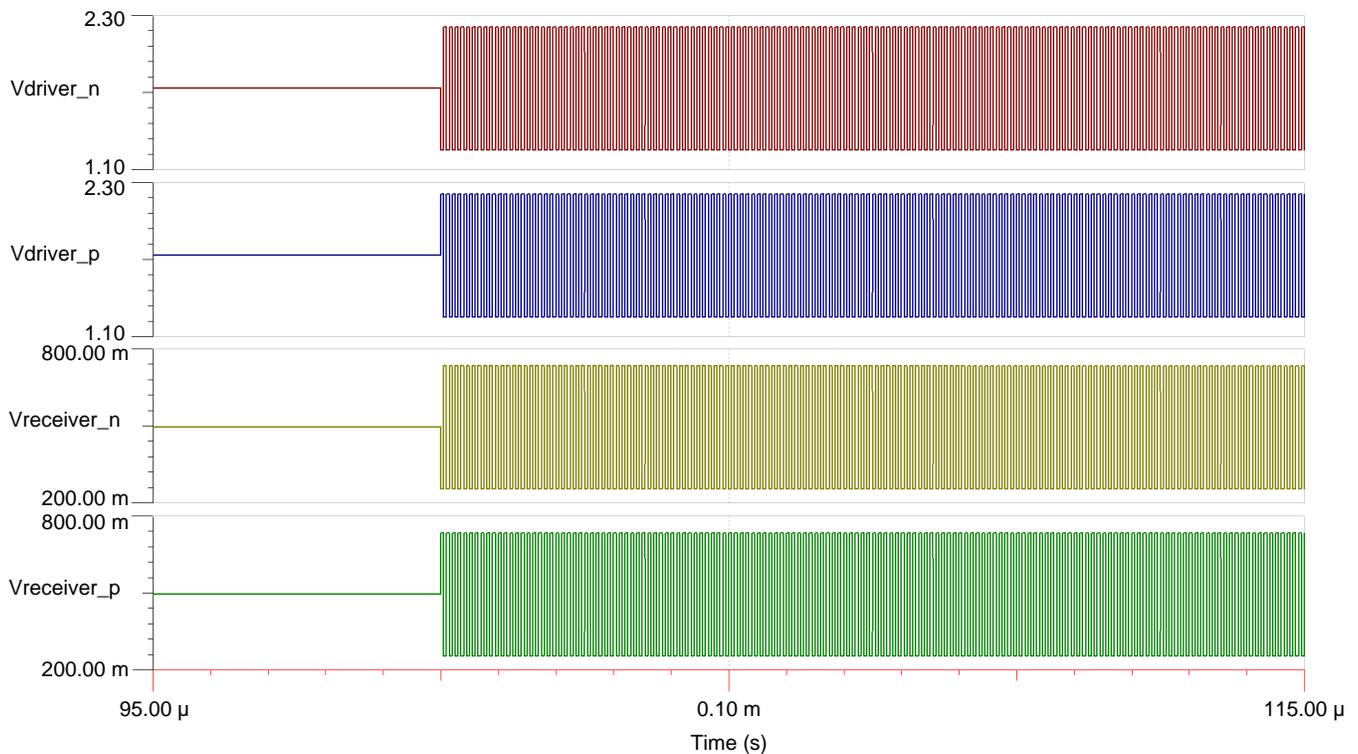


Figure 10. TI TINA Simulation Result (Pre-Biased)

If the SYSREF driver cannot maintain common mode voltage between the idle period and active period, then the charge of the series capacitor is disturbed in between the period. Since the voltage delta across a capacitor cannot change instantaneously, the SYSREF waveform at the receiver side may rise above or fall below (depending on the initial voltage delta across the cap) such that the initial waveforms may impact the receiver behavior due to the variation of the VCM on both legs of the receiver input.

For instance, consider the SYSREF driver that transitions to one leg at V_{OH} and another at V_{OL} during idle time and transition to VCM during active time. Upon triggering of the active state for the SYSREF, it may take a couple of time constants for the VCM to settle as shown in Figure 11. During the initial stage, the SYSREF may not register the SYSREF signal correctly.

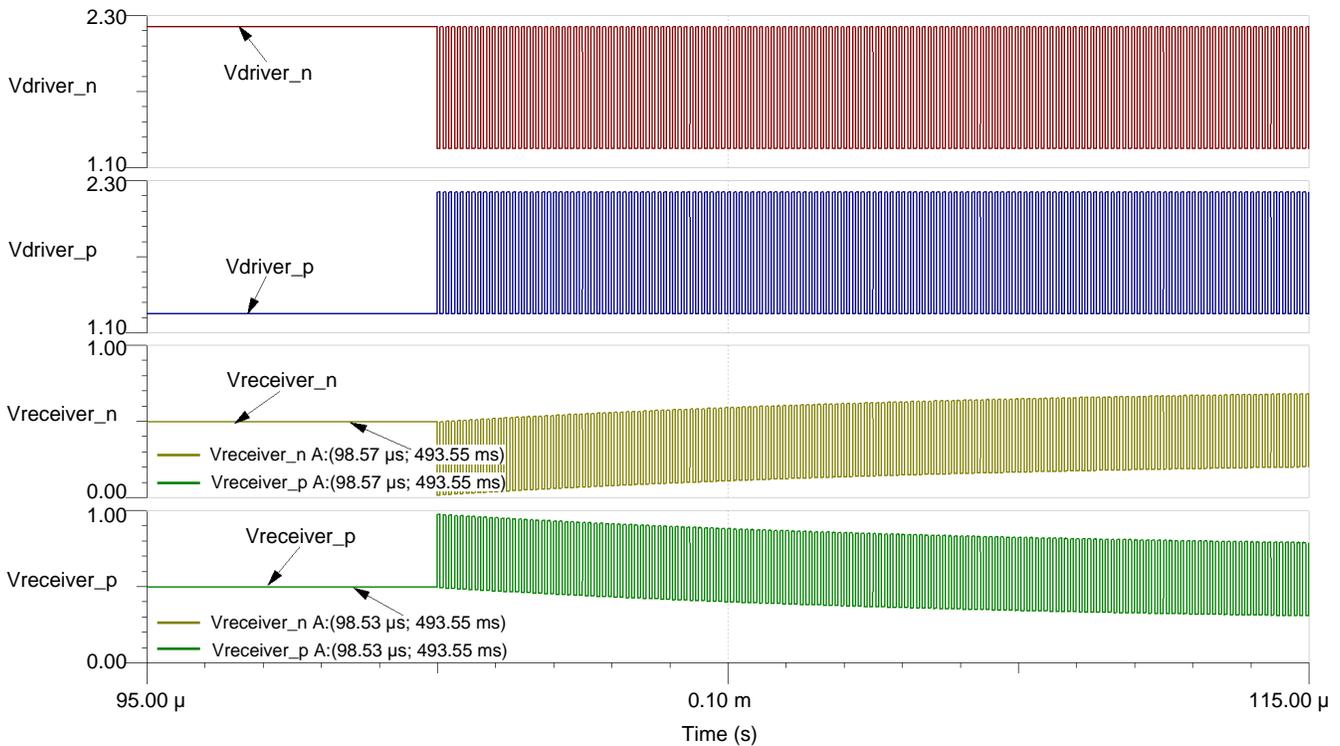


Figure 11. TI TINA Simulation Result (Not Pre-Biased)

For situations similar to the one previously described, where the SYSREF driver has a pre-bias of either differential logic HIGH or differential logic LOW, system designers may consider adding a set of parallel L+R networks to balance out the differential driver at VCM as shown in Figure 12. The inductor basically provides a DC short to balance out the VCM, and the resistor is used to tune out the voltage delta between the two legs if the sink and source current are different. With this implementation, the designers need to consult with the SYSREF driver manufacturer for such recommendation and evaluate the impact of such a network to the operating lifetime of the SYSREF driver. The SYSREF driver can be tuned to be pre-biased with symmetrical VCM for smooth transition before and after the driver active stage. Also, the AC coupling capacitor value may also be increased to maintain VCM stability longer, due to a larger amount of charge in the capacitor.

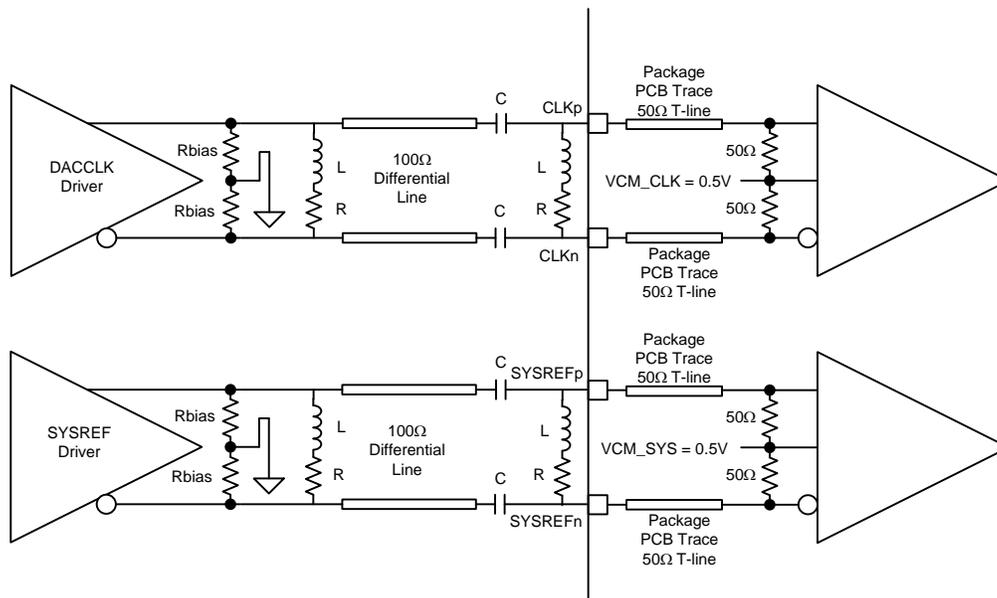


Figure 12. Matched DACCLK and SYSREF Network with Shunt L+R Network

Moreover, both the DACCLK and SYSREF receiver path may have such implementation to form a part of a matched bandpass network. The printed-circuit-board (PCB) layout of both paths may be matched, but the exact bandpass frequency and components may not match since the DACCLK is usually a much higher frequency than SYSREF. This may be an option if the DACCLK port is being used as a slow reference clock for the DAC3xJ8x on-chip PLL path.

7.3 Digital Block Initializer Configuration for AC Coupled Network

Regardless of the SYSREF signal type, both the clock divider and JESD204B block initializer should register only a single pulse of SYSREF. As mentioned in the clock divider and JESD204B block section, since the clock divider provides the JESD204B clock, TI recommends that system designers initialize the clock divider using either the first or second pulse, and then initialize the JESD204B block using either the second or the third pulse. Basically, the initialization of the JESD204B block is staggered behind the initialization of the clock divider. If there are concerns regarding the common mode voltage stability during the initial SYSREF driver idle to active transition, initialize the clock divider using the second pulse and then initialize the JESD204B using the third pulse. The overall JESD204B link initialization requires least three gapped SYSREF pulses in this case.

Table 5. Clock Divider and JESD204B Block Initializer Settings

	First Pulse Only	Second Pulse Only	Third Pulse Only
Clock Divider (Config36 0x24 Register)	0x20	0x30	N/A
JESD204B Block (Config92 0x5c Register)	Single Link: 0x0002 Dual Link: 0x0022	Single Link: 0x0003 Dual Link: 0x0033	Single Link: 0x0005 Dual Link: 0x0055

Indicate Recommended Setting

For Link0 and Link1 configuration, the pulse count starts after the following JESD204B initialization register:

```
init_state = 4b'1111 and jesd_reset_n = 1b'0
init_state = 4b'1111 and jesd_reset_n = 1b'1
init_state = 4b'0000 and jesd_reset_n = 1b'1
```

Various DSP blocks such as NCO and QMC may be initialized by SYSREF if needed. As previously mentioned, the most suitable initialization SYSREF signal for these DSP blocks is a single pulse SYSREF. Since the clock divider and JESD204B blocks already registered single pulse during link initialization and ignore all other pulses, re-issuing of SYSREF to these DSP blocks does not trigger false link re-initialization.

7.4 Fixed V_{OL} Input Bias Setup for AC Coupled Network

If these DSP blocks are programmed to initialize with SYSREF, then the respective initializer constantly registers any SYSREF pulses. Depending on system requirements, if these DSP block initializers are not turned off, they must be programmed to initialize with SYSREF at all times. This may be the case for systems requiring multi-DAC3xJ8x device synchronization. The main concern in this particular setup is that both SYSREF receiver input legs are self-biased at VCM. Any noise disturbance on the receiver input falsely triggers the initializers.

To avoid false triggering of SYSREF due to noise disturbance to the SYSREF receiver input, designers may add a pull-up and pull-down network to create fixed V_{OL} input as shown in Figure 13. The following network introduces 100-mVpp differential to the SYSREF receiver. The equivalent AC load is slightly less than 100- Ω differential since the pull-up and pull-down network are fairly large values when compared to on-chip 100- Ω termination. Since SYSREF is a low-speed signal, the impact to SYSREF terminal signal integrity is minimum.

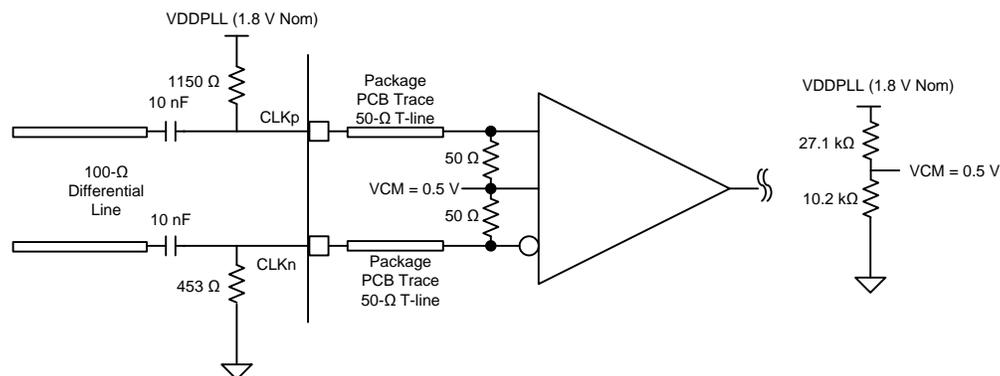


Figure 13. Pull-up and Pull-down Fixed V_{OL} Network

7.5 Typical Start-up Procedure for AC Coupled SYSREF Network

Use the following steps to start-up a typical AC coupled SYSREF network:

1. Power up the FPGA/ASIC and start the JESD204B transmitter system.
2. Power DAC3xJ84 and provide DACCLK. For periodic SYSREF, the SYSREF may be provided at any time as long as the SYSREF driver can maintain stable VCM and minimum transients during JESD204B link establishment.
3. Reset DAC3xJ8x by toggling the RESETB pin from logic HIGH to logic LOW and then back to logic HIGH.
4. Program the DAC3xJ8x as needed for the application:
 - a. Clocking configurations registers: on-chip PLL: config49 (0x31) to config51 (0x33)
 - b. SERDES parameter: config59 (0x3B) to config63 (0x3F)
 - c. JESD204B parameters: config70 (0x46) to config98 (0x62)
 - d. Various DSP blocks: enable the blocks through config0 (0x00) to config2 (0x02) and program respective filter coefficients from config 8 (0x08) to config25 (0x19). DSP block initializers are set from config30 (0x1E) to config32 (0x20).
5. Check alarm_from_pll, alarm_rw0_pll, and alarm_rw1_pll (if applicable), in config108, 0x6C to see if the on-chip PLL and SERDES PLLs are locked. If not, please check the DAC programming and DACCLK.
6. Program config74 (0x4A) to initialize JESD204B block of the DAC (that is, init_state = 4b'1111 and jesd_reset_n = 1b'0). The SYNCB should be in logic HIGH at this point.
7. alarm_sysref_err in config0x6c are active at this point.
8. Program config36 (0x24) = 0x30 => clock divider use sysref skip one pulse and then use next .
9. Program config92 (0x5c) = 0x0005 => use skip two pulses and then use next. Ignore Link1, Link2, and Link3 since they are not used.
10. Clear sysref alarm at this point. Repeat step 7 to 10 again if error persists.
11. Program config74 (0x4A) to initialize the JESD204B block of the DAC (0x4A = 0x0F1F, init_state = 4b'1111, and jesd_reset_n = 1b'1).
12. Program config74 (0x4A) to initialize the JESD204B block of the DAC (0x4A = 0x0F01, init_state = 4b'0000, and jesd_reset_n = 1b'1).
13. Clear alarm_sysref_err in config108, bit13 for Link1 (if needed), and bit12 for Link0 at this point. Repeat steps 7 to 13 again, if error persists.
14. If periodic SYSREF is present or if gapped periodic SYSREF is triggered, the LVDS SYNCB should be in logic Low.
15. SYSREF may be disabled as long as VCM remains stable. This can be done at a much later time to prevent possible transient pulses affecting the link initialization.
16. Check for alarms in registers config100 (0x64) to config109 (0x6D) and also ALARM CMOS pin. If error is observed, repeat steps 6 to step 16 again to ensure correct SYSREF is provided for LMFC alignment.
Check for standard JESD204B errors, FIFO errors, and LOS errors. If these errors are observed, TI recommends repeating steps 6 to 15 to ensure optimal initialization.
 - a. For the JESD204B errors, the JESD204B standard requires at least resync upon code synchronization error, 8b/10b not in table error, and 8b/10b disparity error.
 - b. The end user must decide how to respond to other JESD204B errors.
17. If the DAC3xJ8x is error free, enable TXENABLE and start DAC output transmission.

8 DC Coupled Approach

System design may implement a DC coupled network for the SYSREF receiver with discretions. The primary reason for implementing a DC coupled network is to utilize pulsed SYSREF without concerns from SYSREF driver pre-bias and RC time constants. Due to various scenarios and driver interface types, this section highlights an example based on the DAC3xJ8x EVM design. The concern for DC coupled networks is mainly driven by the fact that the DACCLK and SYSREF may have different coupling network and different driver behavior, and difference in behavior may cause slight mismatch in the overall propagation delay between the DACCLK path and SYSREF path.

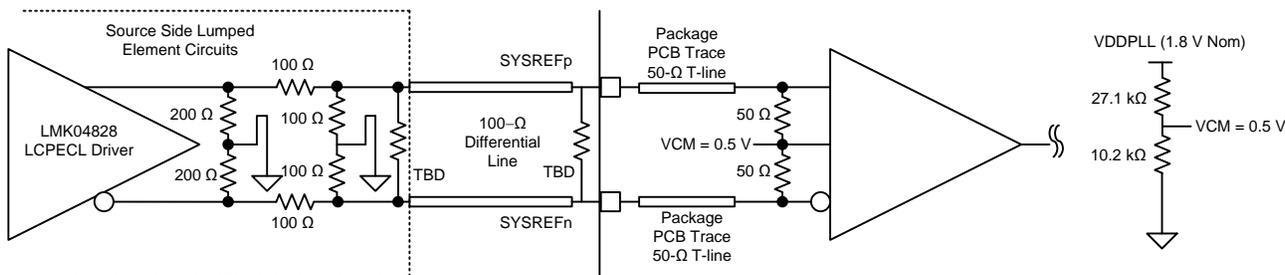


Figure 14. LCPECL DC Coupled Network

The ideal scenario for the DC coupled approach is to provide the DC coupled network for both the DACCLK and SYSREF paths. However, other limitations arise such as the clock driver amplitude and phase noise performance. For instance, the DAC3xJ8x EVM has the DACCLK AC coupled while the SYSREF is DC coupled. The main reason to keep the DACCLK AC coupled is that the LVPECL driver on the LMK04828 side can achieve the best phase noise performance in this condition. DC coupling requires an LCPECL driver, which does not have as high a phase noise performance as AC coupling with an LVPECL driver. TI typically recommends high clock swing drivers such as LVPECL to allow the DAC to achieve the best noise performance.

If the DACCLK path has the LVPECL, AC coupled network while the SYSREF path has the LCPECL, DC coupled network, the system designer must ensure that under these conditions, the delay of the DACCLK path and the delay of the SYSREF are matched. This would involve the IBIS modeling of the clock driver delay propagation and associated PCB trace delay simulation. Physical measurements may be needed to ensure matched delay. In the EVM scenario, both the digital and analog delay feature of the LMK04828 can compensate the potential propagation delay difference.

Regarding the SYSREF input bias on default EVM setup, LMK04828 drives the SYSREF in DC coupled fashion with LCPECL driver. The common mode is divided down to 0.5 V through resistor divider. The LMK04828 driver can be programmed such that during idle state, the SYSREF driver will output V_{OH} and V_{OL} on the positive and negative leg of the driver, respectively. The idle state can be in continuous SYSREF mode with driver power down or in pulsed SYSREF mode with the pulses finished. This creates 0.55 V and 0.45 V on the positive and negative input of the SYSREF receiver. The 100-mV difference is sufficient to prevent unintended assertions.

The major benefit of the DC coupled approach is elimination of potential delay due to the RC time constant. Since DC coupling does not have capacitors to charge, the SYSREF pulses can trigger the initialization blocks immediately. System design may implement pulsed SYSREF signal freely once the concern of propagation delay is compensated. Start-up procedures for DC coupled network remains the same as start-up procedures for AC coupled network except that periodic SYSREF is removed from this scenario.

8.1 Typical Start-up Procedure for DC Coupled SYSREF Network

Use the following steps to start-up a typical DC coupled SYSREF network:

1. Power up the FPGA/ASIC and start the JESD204B transmitter system.
2. Power DAC3xJ84 and provide DACCLK.
3. Reset DAC3xJ8x by toggling the RESETB pin from logic HIGH to logic LOW and then back to Logic HIGH.
4. Program the DAC3xJ8x as needed for the application:
 - a. Clocking configurations registers: on-chip PLL: config49 (0x31) to config51 (0x33)
 - b. SERDES parameter: config59 (0x3B) to config63 (0x3F)
 - c. JESD204B parameters: config70 (0x46) to config98 (0x62)
 - d. Various DSP blocks: config0 (0x00) to config2 (0x02) and respective coefficients from config 8 (0x08) to config25 (0x19). DSP block initializers are set from config30 (0x1E) to config32 (0x20).
5. Check alarm_from_pll, alarm_rw0_pll, and alarm_rw1_pll (if applicable) in config108, 0x6C to see if the on-chip PLL and SERDES PLLs are locked. If not, please check the DAC programming and DACCLK.
6. Program config74 (0x4A) to initialize JESD204B block of the DAC (that is, init_state = 4b'1111 and jesd_reset_n = 2b'0). The SYNCB should be in logic HIGH at this point.
7. alarm_sysref_err in config0x6c are active at this point.
8. Program config36, 0x24 = 0x30 => clock divider use sysref skip one pulse and then use next.
9. Program config92, 0x5c = 0x0005 => use skip two pulses and then use next. Ignore Link1, Link2, and Link3 since they are not used.
10. Clear sysref alarm at this point. Repeat step 7 to 10 again if error persists.
11. Program config74 (0x4A) to initialize JESD204B block of the DAC (0x4A = 0x0F1F, init_state = 4b'1111, and jesd_reset_n = 1b'1).
12. Program config74 (0x4A) to initialize JESD204B block of the DAC (0x4A = 0x0F01, init_state = 4b'0000, and jesd_reset_n = 1b'1).
13. Clear alarm_sysref_err in config108, bit13 for Link1 (if needed), and bit12 for Link0 at this point. Repeat step 7 to 13 again if error persists.
14. If periodic SYSREF is present or if gapped periodic SYSREF is triggered, the LVDS SYNCB should be in logic Low. Disable SYSREF with known logic level present at SYSREF port.
15. Check for alarms in registers config100 (0x64) to config109 (0x6D) and also ALARM CMOS pin. If error is observed, repeat steps 6 to 16 again to ensure correct SYSREF is provided for LMFC alignment.
 Check for standard JESD204B errors, FIFO errors, and LOS errors. If these errors are observed, TI recommends repeating steps 6 to 15 to ensure optimal initialization.
 1. For the JESD204B errors, JESD204B standard requires at least resync upon code synchronization error, 8b/10b not in table error, and 8b/10b disparity error.
 2. The end user must decide how to response to other JESD204B errors.
16. If DAC3xJ8x is error free, enable TXENABLE and start DAC output transmission.

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