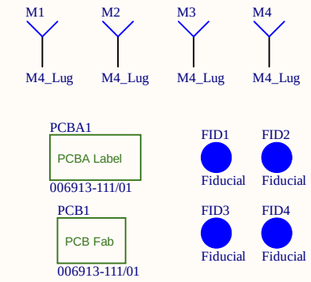
Change Log

Rev 1 [Sebastian Forenza, Aug 2025]
Original release. For integration into Arc Sport Block 4

I2C address mapping (7-bit)

Component	Address
High Powered Amp	0x60
Low Powered Amp	0x6B
Transciever	0x68

Mounting Hardware



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PCB FAB 006913-111/01_A	PCBA 006913-111/01_A	VARIANT [No Variations]

TITLE: WAVE

PROJECT: WAVE

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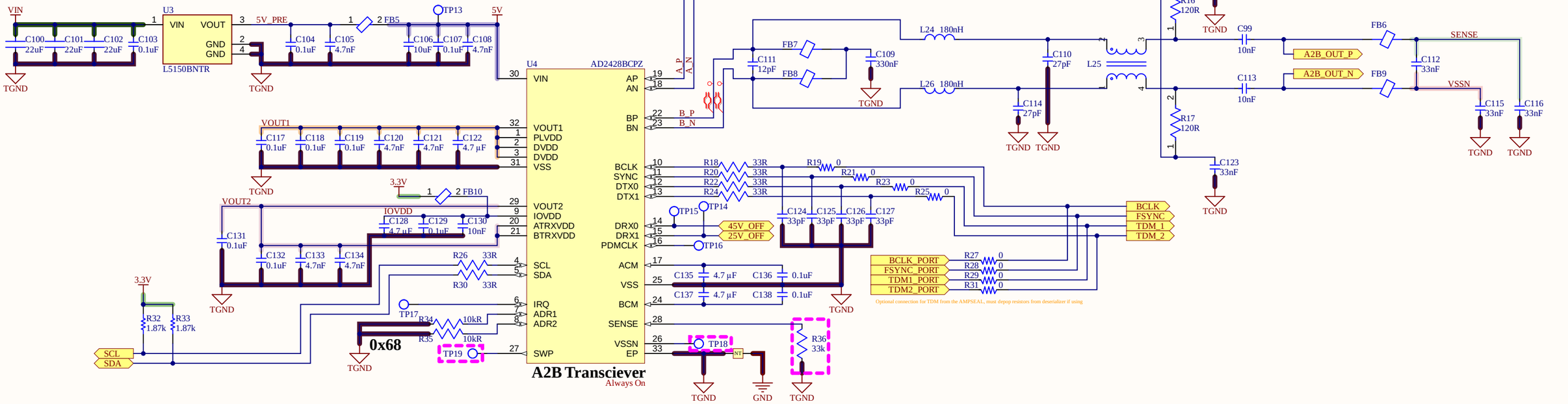
Local Powered Subnode

Option 1: Sub-Node - [R21 DNP]

Option 2: Last Sub-Node - [R21 POPULATE]

We do not need bus power. We want to reduce our BOM and simply use local power. unsure if the current setup will work as inteded



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TITLE: A2B Transciever

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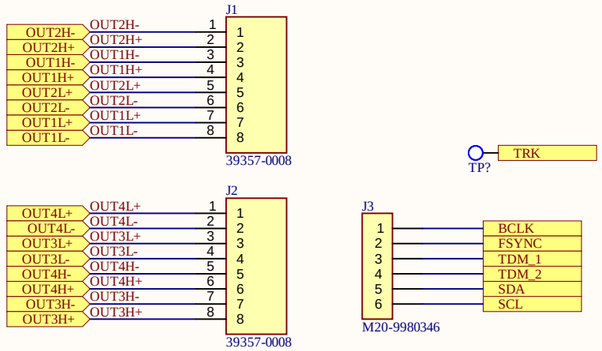

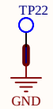

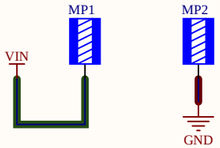

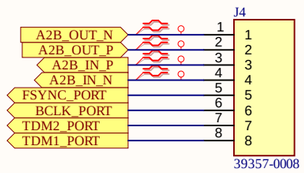

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TITLE: Connectors

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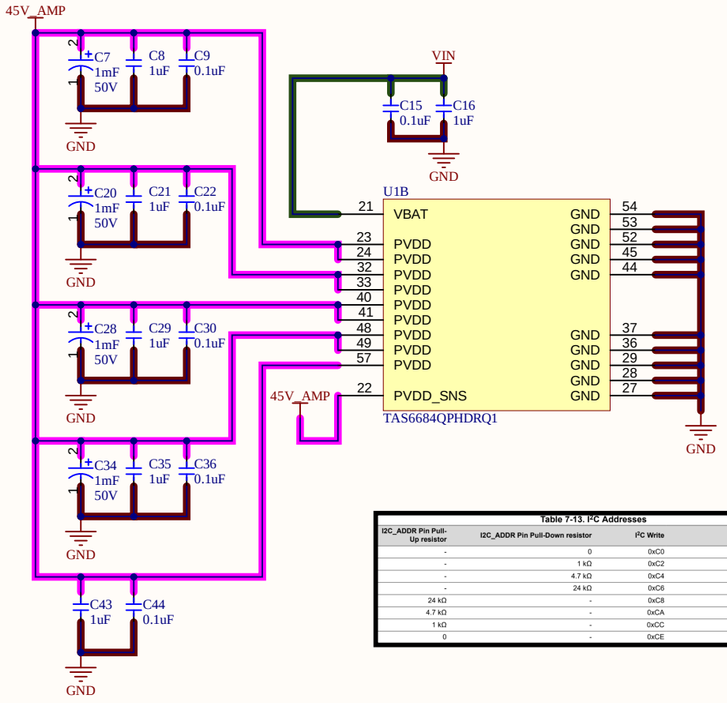
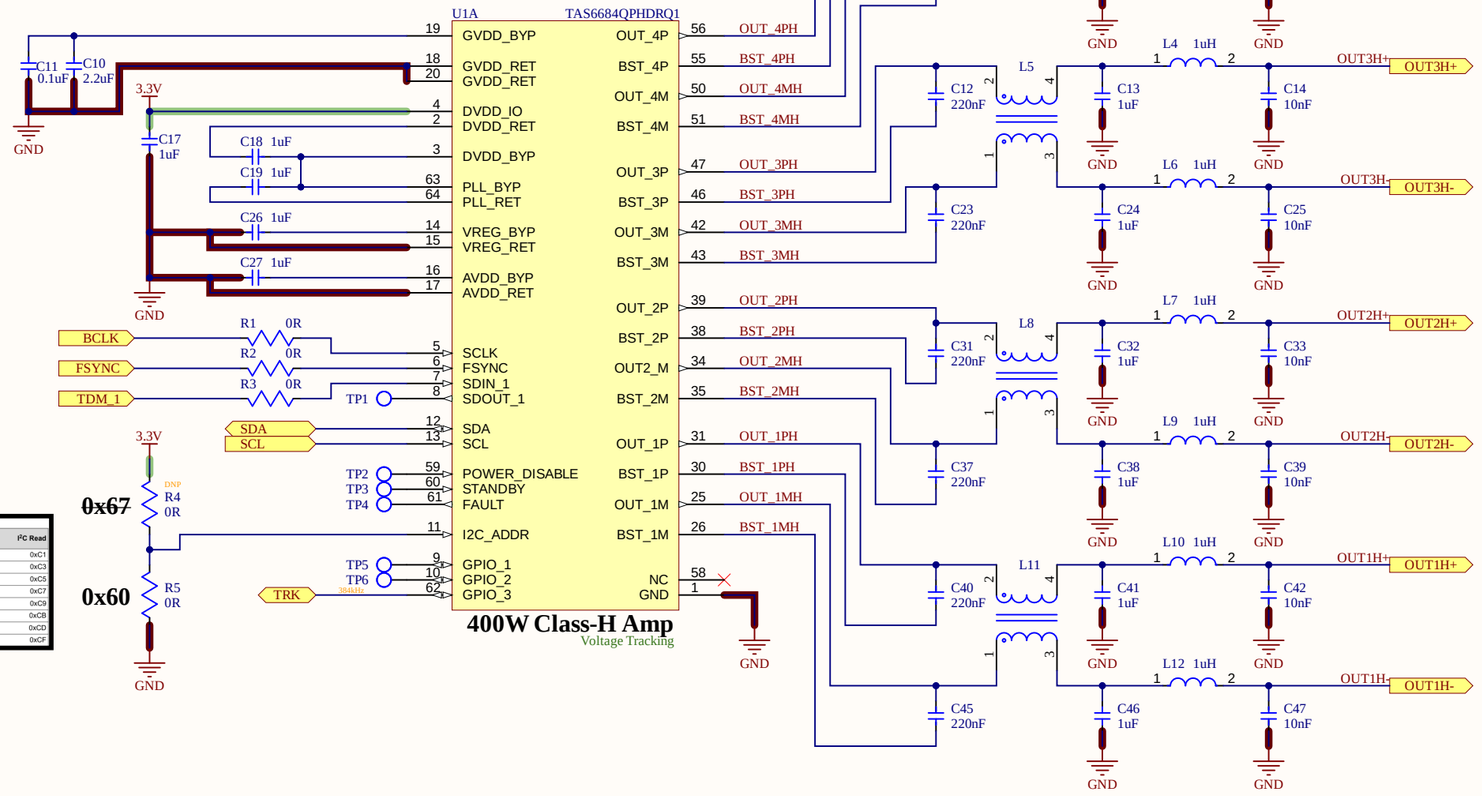


Table 7-13. I²C Addresses			
I2C_ADDR Pin Pull-Up resistor	I2C_ADDR Pin Pull-Down resistor	I²C Write	I²C Read
-	0	0xC0	0xC1
-	1 kΩ	0xC2	0xC3
-	4.7 kΩ	0xC4	0xC5
-	24 kΩ	0xC6	0xC7
24 kΩ	-	0xC8	0xC9
4.7 kΩ	-	0xCA	0xCB
1 kΩ	-	0xCC	0xCD
0	-	0xCE	0xCF



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PCB FAB 006913-111/01_A	PCBA 006913-111/01_A	VARIANT [No Variations]
TITLE: High Power Amp		
PROJECT: WAVE		
DATE 8/21/2025	ENG Sebastian Forenza	SHEET * OF *

CONFIGURATION (CFG0, CFG1, CFG2)					
R_{CFGx_1}	Level 1 resistance		0	0.1	kΩ
R_{CFGx_2}	Level 2 resistance	0.496	0.51	0.526	kΩ
R_{CFGx_3}	Level 3 resistance	1.11	1.15	1.19	kΩ
R_{CFGx_4}	Level 4 resistance	1.81	1.9	1.93	kΩ
R_{CFGx_5}	Level 5 resistance	2.65	2.7	2.82	kΩ
R_{CFGx_6}	Level 6 resistance	3.71	3.8	3.94	kΩ
R_{CFGx_7}	Level 7 resistance	4.95	5.1	5.26	kΩ
R_{CFGx_8}	Level 8 resistance	6.29	6.5	6.68	kΩ
R_{CFGx_9}	Level 9 resistance	8.00	8.3	8.50	kΩ
R_{CFGx_10}	Level 10 resistance	10.18	10.5	10.81	kΩ
R_{CFGx_11}	Level 11 resistance	12.90	13.3	13.70	kΩ
R_{CFGx_12}	Level 12 resistance	15.71	16.2	16.69	kΩ
R_{CFGx_13}	Level 13 resistance	19.88	20.5	21.11	kΩ
R_{CFGx_14}	Level 14 resistance	24.15	24.9	25.65	kΩ
R_{CFGx_15}	Level 15 resistance	29.20	30.1	31.00	kΩ
R_{CFGx_16}	Level 16 resistance	35.40	36.5	38.60	kΩ

Table 6-2. Overvoltage Protection Level Selection

OVP Level	OVP Bit 1	OVP Bit 0
64V	0	0
50V	0	1
35V	1	0
28.5V	1	1

Table 6-4. CFG2-pin Settings

Level	OVP Bit 1	Clock	SYNCIN	Clock Dithering
1	0	Internal	off	CFG1-pin
2	1	Internal	off	CFG1-pin
3	0	Internal	off	CFG1-pin
4	1	External	on	disabled
≥5	0	External	on	disabled

Table 6-3. CFG1-pin Settings

Level	OVP Bit 0	Clock Dithering Mode	t_{CL_latch}	$PGOOD_{OVP\_enable}$
1	0	enabled (DRSS)	disabled	disabled
2	1	enabled (DRSS)	disabled	disabled
3	0	enabled (DRSS)	disabled	enabled
4	1	enabled (DRSS)	disabled	enabled
5	0	enabled (DRSS)	enabled	disabled
6	1	enabled (DRSS)	enabled	disabled
7	0	enabled (DRSS)	enabled	enabled
8	1	enabled (DRSS)	enabled	enabled
9	0	disabled	disabled	disabled
10	1	disabled	disabled	disabled
11	0	disabled	disabled	enabled
12	1	disabled	disabled	enabled
13	0	disabled	enabled	disabled
14	1	disabled	enabled	disabled
15	0	disabled	enabled	enabled
16	1	disabled	enabled	enabled

Table 6-1. CFG0-pin Settings

Level	Dead Time [ns]	20µA ATRK Current
1	14	on
2	30	on
3	50	on
4	75	on
5	100	on
6	125	on
7	150	on
8	200	on
9	14	off
10	30	off
11	50	off
12	75	off
13	100	off
14	125	off
15	150	off
16	200	off

Figure 1

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Cap analysis

45V_OUT
C139 10nF C140 10nF C141 10nF C142 10nF C143 10nF C144 10nF C145 10nF C146 10nF C147 10nF C148 10nF C149 10nF C150 10nF C151 10nF
GND

45V_OUT
C152 220uF C153 220uF C154 220uF C155 150uF C156 150uF
GND

45V_OUT
C170 4.7uF C171 4.7uF C172 4.7uF C173 4.7uF C174 4.7uF C175 4.7uF
GND

45V_OUT TP20 TP21 45V_AMP
R43 1mR

VIN
C157 220uF C158 10uF C159 10uF C160 10uF C161 10uF C162 10uF C163 10uF C164 10nF C165 10nF C166 10nF C167 10nF C168 100nF C169 100nF
GND

R37 1mR H_IND1 L27 3.3uH H_SW1
R38 1mR H_IND2 L28 3.3uH H_SW2

R39 0 R40 1k R41 0 R42 1k
C176 100pF C177 100pF

LM5125_VCC C179 1uF C180 100nF AGND_1
LM5125_VCC C181 100nF C182 1uF AGND_2
GND

LM5125_VCC Q1 LMG2100R026VBNR
14 VCC, 10 HB, 11 HS, 12 HI, 13 LI, 1 NC, 2 NC, 3 NC, 4 NC, 8 NC, 9 NC, 16 NC
VIN 7, SW 5, PGND 6, PGND 17, PGND 18, AGND 15
C178 100nF
45V_OUT
GND
AGND_2

LM5125_VCC Q2 LMG2100R026VBNR
14 VCC, 10 HB, 11 HS, 12 HI, 13 LI, 1 NC, 2 NC, 3 NC, 4 NC, 8 NC, 9 NC, 16 NC
VIN 7, SW 5, PGND 6, PGND 17, PGND 18, AGND 15
C183 100nF
45V_OUT
GND
AGND_1

LM5125_VCC
R44 14k
R45 100k
D1
Q3
PGOOD_HP
GND

U5 LM5125QRHBRQ1

HB1	9	CSP1	6
SW1	10	CSN1	5
HB2	16	CSP2	20
SW2	15	CSN2	21
BIAS	18	HO2	17
UVLO/EN	19	LO2	14
EN2	30	HO1	8
CFG2	25	LO1	11
CFG1	26	VOUT	7
CFG0	27	SYNCIN	24
MODE	29	NC	23
COMP	3	ATRK	32
RT	22	PGOOD	28
DLY	1	ILIM	31
SS	2	VCC	12
		AGND	4
		PGND	13
		EP	33

LM5125_VCC
C184 100nF
C185 100nF
CSP1 CSN1 CSP2 CSN2 HO2 LO2 HO1 LO1
<9V Turn Off
LV1 Sets internal clock = 50V OVP
LV4 Sets 50V OVP, PGOOD Enable
LV9 Sets ATRK to digital and deadtime to 30ns
R46 100k
R48 0
R49 1.87k
R50 8.2k
See Fig. 1
R52 0 AGND-H
PGOOD_HP
Open Drain [Good - HIZ] [Fault - GND]
TRK_FILT
Switching Freq set to ~215kHz
6ms Soft Start
26A VIN Current Limit Continuous /83A VIN Current Limit for 100ms
LM5125_VCC
VCC = 5V
C188 4.7 µF
R57 4.99k
R63 47.5k
C194 3.3uF
NT
GND AGND-H GND AGND-H

VIN
C186 2.2uF
R47 100k
R53 14k
R51 0
R54 0
Lower ripple (FPWM)
Higher efficiency (DEM)
Q4
45V_OFF
R64 100k
R56 3.3k
C192 680nF
C187 1nF
R62 100k
C189 330nF
C193 330nF
AGND-H

3.3V
R55 51k
R58 0
R59 1.5k
R60 4.99k
R61 4.99k
TRK
Recommended TRK filter from datasheet
C190 47nF
C191 47nF
R65 7.87k
AGND-H

45V Boost
On/Off Control

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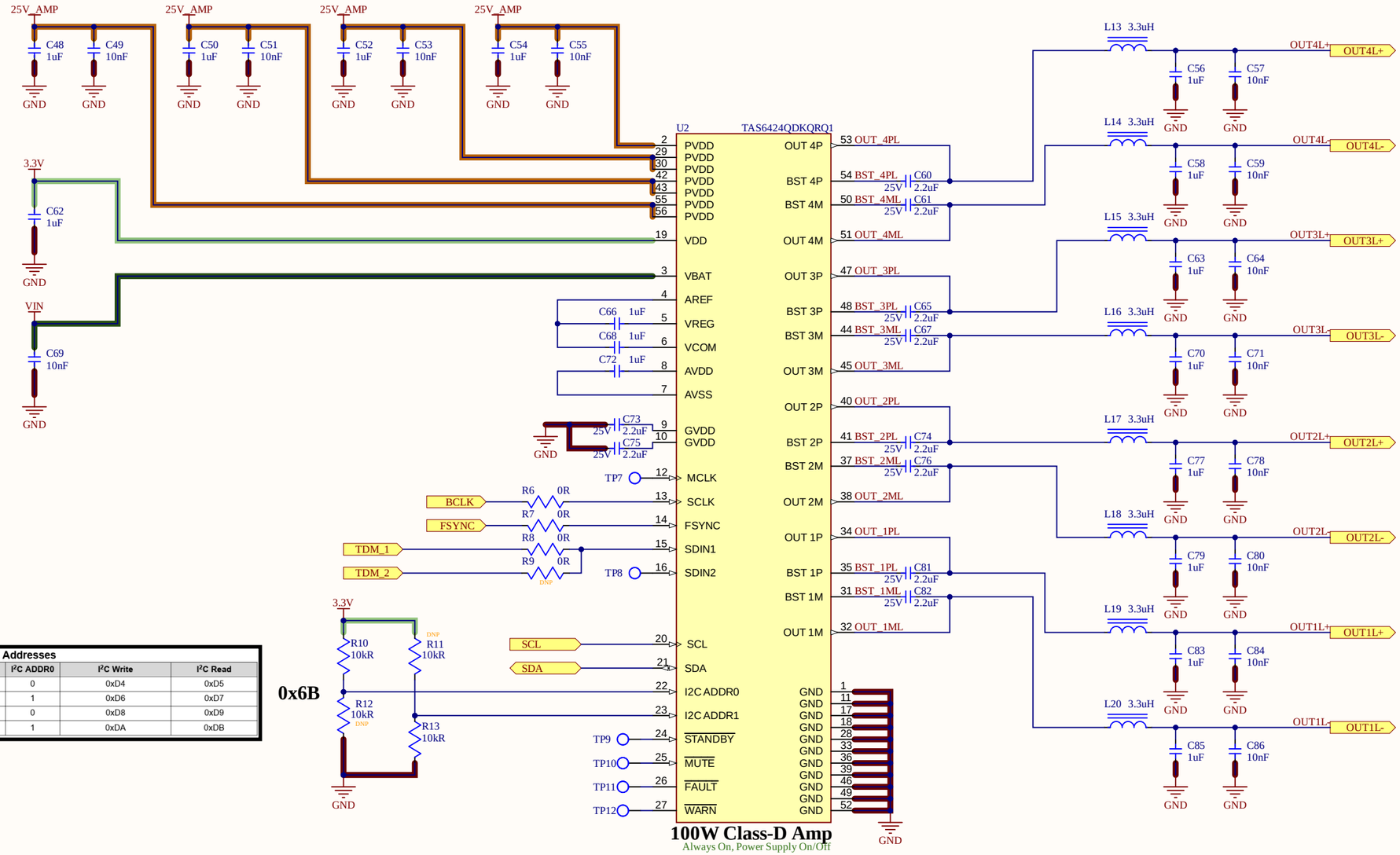

0x6B

Table 9-8. I²C Addresses

DESCRIPTION	I²C ADDR1	I²C ADDR0	I²C Write	I²C Read
Device 0	0	0	0xD4	0xD5
Device 1	0	1	0xD6	0xD7
Device 2	1	0	0xD8	0xD9
Device 3	1	1	0xDA	0xDB

100W Class-D Amp

Always On, Power Supply On/Off

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PROJECT: WAVE

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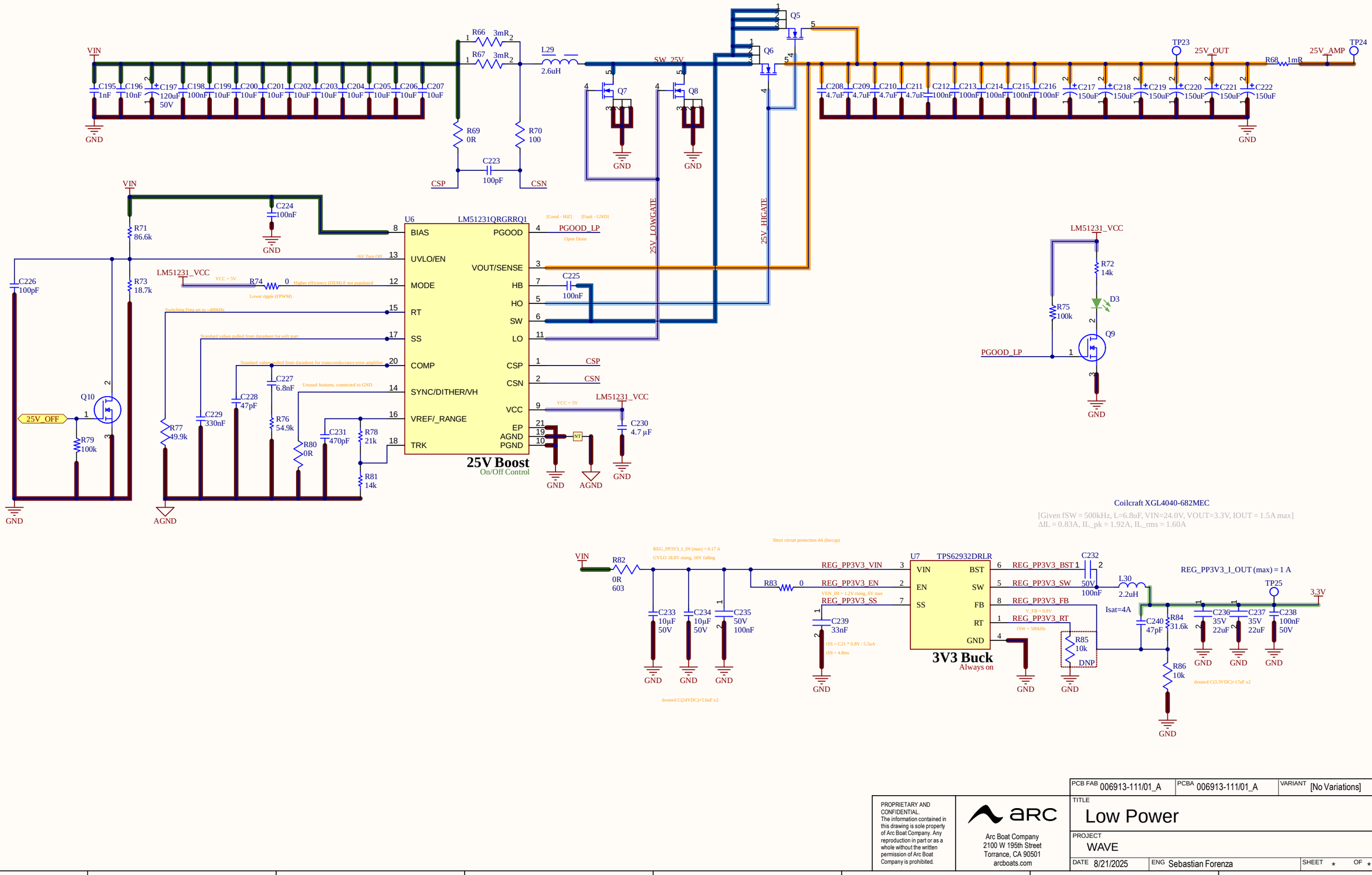

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