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16-Bit 1-Gsps Digitizer Reference Design With AC and DC Coupled Fixed Gain Amplifier

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Design Resources

TIDA-00823	Tool Folder Containing Design Files
TSW54J60EVM	Product Folder
ADS54J60EVM	Product Folder
LMH3401EVM	Product Folder
TSW54J60 Design Package	EVM Design Package
LMH3401 Design Package	EVM Design Package

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Design Features

- Flexible Transformer Coupled Analog Input on the LMH3401 Path to Allow for a Variety of Source and Frequencies
- Options for AC or DC Coupling, Single-Ended or Differential Inputs
- Easy to Use Software GUI to Configure the ADS54J60 and LMK04828 for a Variety of Configurations Through a USB Interface
- Quickly Evaluate ADC Performance Through High-Speed Data Converter Pro Software
- Simple Connections to TSW14J56EVM Capture Card

Featured Applications

- Radar Antenna Arrays
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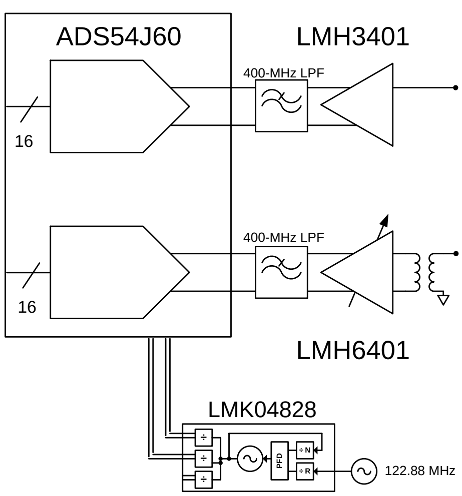
- Digitizers



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2 Circuit Description

This reference design discusses the use and performance of the Ultra-Wideband Fixed-gain high-speed amplifier, the LMH3401 to drive the high-speed analog-to-digital converter (ADC), the ADS54J60 device. Different options for common-mode voltages, power supplies, and interfaces are discussed and measured, including AC-coupling and DC-coupling, to meet the requirements for a variety of applications.

This type of circuit may be used in Software Defined Radio, Military Communications, Test Equipment, Cable head-end receiver, Radar receiver and Digitizer applications.

3 Introduction

This reference design, the TSW54J60EVM, serves as a comprehensive summary of the performance and trade-offs when driving an ADC with high-speed amplifiers. A printed-circuit board was developed in order to test different setups in AC and DC coupled applications. This board consists of an ADS54J60 device, which is a dual-channel, 16-Bit, 1-GSPS ADC, and two high-speed fully-differential amplifiers: the LMH3401 (Fixed gain) and the LMH6401 (Digital variable gain). This board uses the LMH6401 amplifier to drive one channel of the ADC and a LMH3401 to drive the other channel. The board includes a jitter-cleaning clock generator (LMK04828), a USB interface to allow operation with TI's High Speed Data Converter Pro GUI, and TI power solution LDO's, and switchers. The JESD204B standard interface allows the EVM to be used with the TITSW14J56EVM capture board or other JESD204B compatible platforms for data analysis.

The LMH3401 is an Ultra-Wideband, Fixed-gain, Fully-Differential Amplifier (FDA) designed for DC to radio frequency (RF), intermediate frequency (IF) or high-speed time-domain applications with signal bandwidths up to 2 GHz. The device is an ideal analog-to-digital converter (ADC) driver for DC or AC-coupled applications. The device supports both single-and split-supply operation for driving an ADC. A common-mode reference input pin is provided to align the amplifier output common-mode with the ADC input requirements.

The LMH3401 includes internal feedback and gain set resistors to provide 16-dB of gain when configured for single-ended inputs driven from a 50-Ω source. When used in fully-differential configuration, 12 dB is obtained when matching the input to a 100-Ω differential source. The on-chip resistors simplify PCB design and ensure the highest performance over the useable bandwidth.

This document includes the general considerations when driving an ADC with an amplifier, such as common-mode voltages, power supplies, AC-coupling and DC-coupling, and filter interfaces. This document also includes a discussion of the measured performance. This TIDesign only focuses on the LMH3401 channel driving the ADS54J60. TIDesign TIDUB15 features the LMH6401 channel driving the ADS54J60. See the *TSW54J60EVM Evaluation Mode* User's Guide, (SLAU649A), for more information regarding operation and testing of this EVM.

4 General Considerations

4.1 AC-Coupled, Single-Ended Source to a Differential Gain Configuration

The LMH3401 may be used to amplify and convert single-ended input signals to differential output signals. The gain from the single-ended input to the differential output is 16 dB. To maintain proper balance in the amplifier and avoid offsets at the output, the unused input pin must be biased to the same voltage as the input DC voltage, and the impedance on the unused pin must match the source impedance of the driven input pin.

If a 50-Ω source is AC-coupled to the input, the alternate input is AC-coupled to ground through a 50-Ω termination.

NOTE: the ac coupling on both inputs provides a similar frequency response to balance the gain over frequency. In single-ended to differential applications, the input impedance is actively set by the amplifier. This active input impedance match allows for lower noise than the case of a purely resistive input impedance.

Detailed solutions for input impedance calculations are shown in the *Input Impedance Calculations* section of the LMH3401 Data sheet.

When considering the input impedance of the LMH3401, the device input pins move in a common-mode sense with the input signal. The common-mode current functions to increase the apparent input impedance at the device input into the gain element over the value of R_G. Input signals may also cause input clipping if this common-mode signal moves beyond the input range. This input active impedance issue applies to both AC- and DC-coupled designs and requires somewhat more complex solutions for the resistors to account for this issue.

The full set of resistor value calculations is included in the *Resistor Design Equations for Single-to-Differential Applications* section of the data sheet.

AC-coupling is the default configuration of the LMH3401 path on the TSW54J60EVM. TI recommends that the AC-coupling configuration be used if the application does not require processing of signals close to DC. The TSW54J60 provides an option to input a 50 Ω single-ended input or a true 100-Ω differential signal for the LMH3401 device.

On the TSW54J60EVM, the LMH3401 operates from a single-supply voltage of 5.0 V. Single supply operation is most appropriate when the signal path is ac coupled and the input and output common-mode voltages are set to mid-supply by the CM pin and are preserved by coupling capacitors on the input and output.

The CM input controls the output common-mode voltage. CM has no internal biasing network and must be driven by an external source or resistor divider network to the positive power supply. The TSW54J60EVM provides option to drive CM from either the ADC or an external source using a test point (TP1).

The output of the amplifier goes through a 370MHz low pass filter before connecting to the ADC. The specifications of the filter and data captured plots are shown in Section 6.

Figure 1 shows the default configuration of the LMH3401 channel of the TSW54J60EVM.

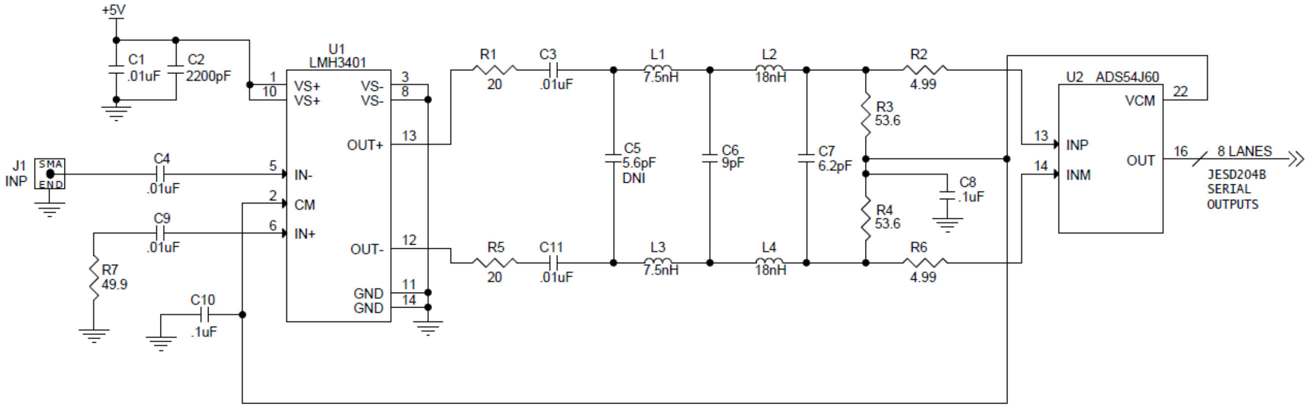

Figure 1. LMH3401 AC-Coupled Configuration

4.2 DC-Coupled Single Ended Source to Differential Gain Configuration

The LMH3401 path driving the ADS54J60 can be either DC- or AC-coupled at the inputs. The LMH3401 device provides excellent performance as a fixed-gain single-ended to differential output amplifier down to DC. Figure 2 shows a typical DC-coupled configuration where an LMH3401 device is used to produce a balanced differential output signal for the ADS54J60 input.

In order to DC-couple the LMH3401 input path, care must be taken to ensure the common-mode voltage is set within the input common-mode range of the LMH3401. Refer to the *Electrical Characteristics* table in the LMH3401 data sheet to set the input common-mode voltage within the device range.

When interfacing an amplifier to an ADC in a DC-coupled application, it is required to match the output CM voltage of the amplifier close to the input CM voltage of the ADC. Best performance is achieved when the ADC input pins are at the same voltage as the ADC CM pin or $(INP_{ADC} + INM_{ADC})/2$ equals VCM_{ADC}. Interfacing the LMH3401 to the ADS54J60 is made easier by an option provided in the amplifier to control the output common-mode voltage using the CM pin of the amplifier.

See the *TSW54J60EVM Evaluation Module User's Guide*, section 5.2.3 in (SLAU649A), for more information regarding testing with this mode of operation.

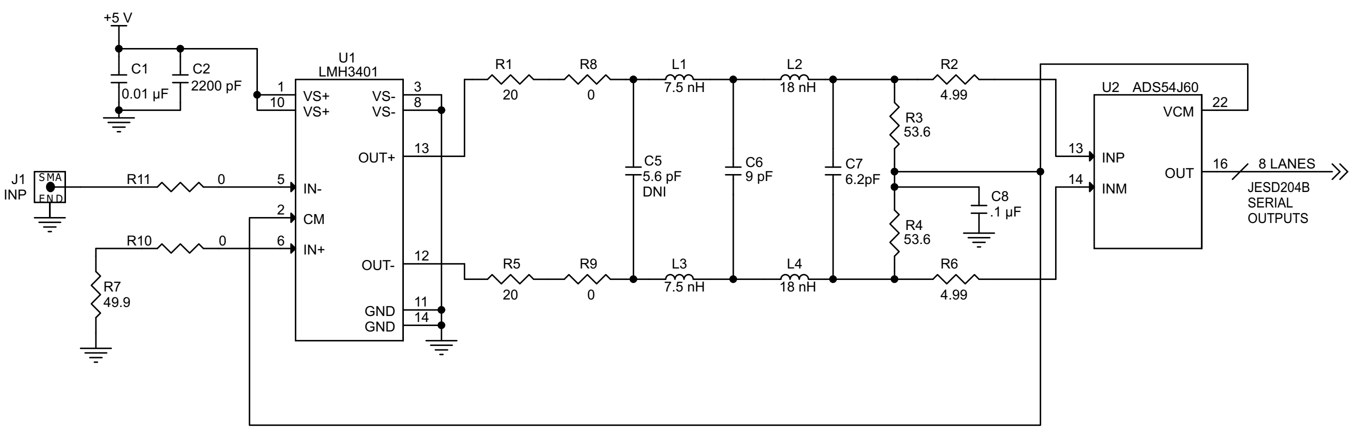

Figure 2. Interfacing the LMH3401 With the ADS54J60 in DC-Coupled Configuration

5 Common Mode Consideration

5.1 DC-Coupled Configuration

To achieve the best performance while DC-coupling an amplifier and ADC interface, be sure to match the output CM voltage of the amplifier to the input CM voltage of the ADC. For DC-coupled applications, the LMH3401 provides an option to control the output common-mode voltage using the Common Mode (CM) input pin. Device performance is optimal when the output common-mode voltage (V_{OCM}) is within ±0.5 V of mid-supply and performance degrades outside the range when the output swing approaches clipping levels.

In single-ended input mode, in order to maintain proper balance in the amplifier and avoid offsets at the output, the unused input pin must be biased to the same voltage as the input dc voltage, and the impedance on the unused pin must match the source impedance of the driven input pin.

Like all FDA devices, the output average voltage (common-mode) is controlled by a separate common-mode loop. The target for this output average is set by the CM input pin. The V_{OCM} range extends from 1.1 V below the mid-supply voltage to 1.1 V above the mid-supply voltage when using a 5-V supply. Note that on a 3.3-V supply the output common-mode range is quite small. For applications using a 3.3-V supply voltage, the output common-mode must remain close to the mid-supply voltage. The input common-mode voltage offers more flexibility than the output common-mode voltage. The input common-mode range extends from the negative rail to approximately 1 V above the mid-supply voltage when powered with a 5-V supply.

In this design, the V_{OCM} of the LMH3401 is set by the VCM from the ADS5460 by default. For the ADS54J60, the input CM voltage needs to be maintained as close to 2.1 V as specified in the *ADS54J60 Dual-Channel, 16-Bit, 1.0-GSPS Analog-to-Digital Converter* data sheet (SBAS706B). The ADC input CM voltage of 2.1 V makes it easier for the LMH3401 to be run on a single +5V supply, and use the CM pin to set the output CM voltage to 2.1 V, which is within ±0.5 V of mid-supply.

The default configuration of the EVM does not provide a perfectly balanced input due to the single-ended input configuration. To demonstrate the harmonic distortion performance of the LMH3401, the output common mode must be within several mV's to meet the input DC offset of the ADC inputs. To accomplish this, a Bias-T is used to adjust the DC level of the input signal of the LMH340. An external Vcm source is used then to maintain an output common voltage that is within specification for the ADC input common mode range. After the offset of the LMH3401 was set to within a few millivolts, the external Vcm was adjusted to provide the optimal performance. In this test case, the input common mode DC level of LMH3401 was set to around 0.414 V by providing 0.204 V to the Bias-T DC input. This is within the input common-mode range of LMH3401 (V_S- – 0.7 to V_S+–1.2). With the external Vcm set to 2.4V from an external source applied to the CM input, this provided a balanced common mode input to the ADC at approximately 2.31 V, which is within the ADC specification.

Since the LMH3401 is configured as a single-ended input, a bandpass filter is used to improve the SFDR from the signal source and a 6-dB attenuation pad for better impedance matching. The setup is as shown in Figure 3.

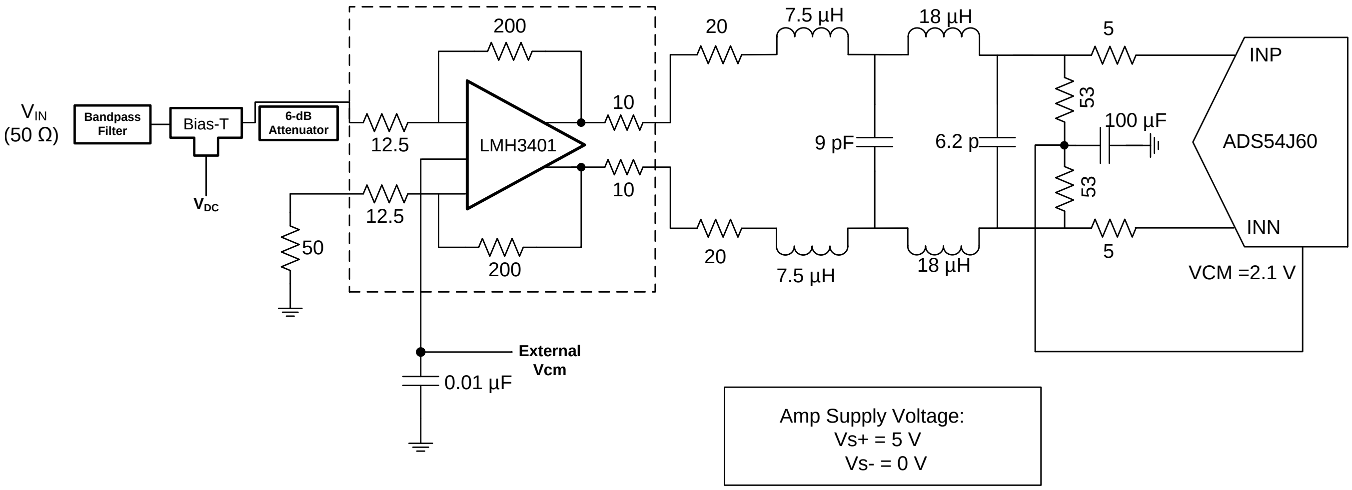

Figure 3. Balancing the DC Offset of the LMH3401 Using a Bias-T and External DC Source

A 170-MHz tone was used as the test tone, and the ADC was sampling at Fs= 983.04Msps. Figure 4 shows the captured results.

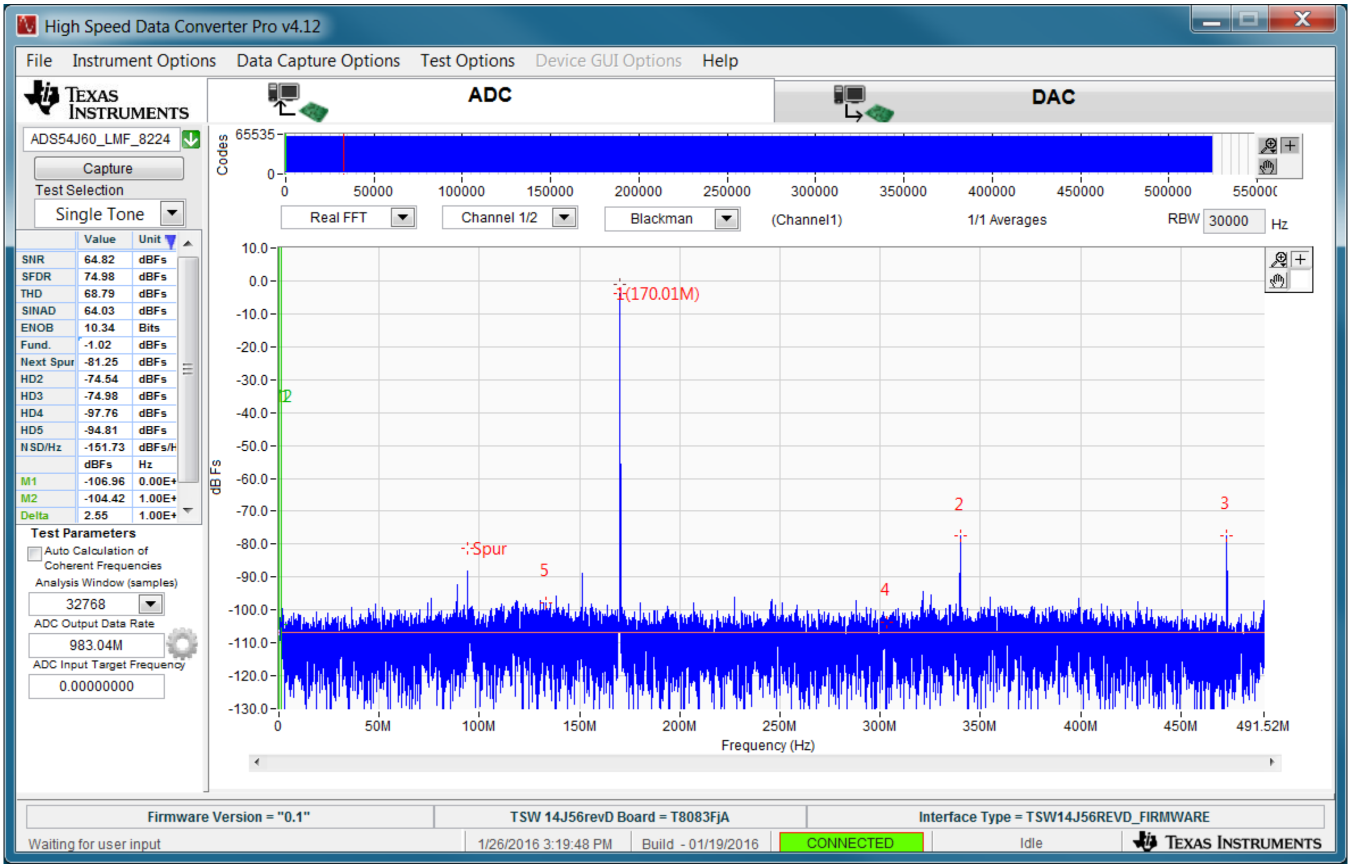

Figure 4. 170-MHz IF, DC-Coupled, With DC Balanced Input

6 Filter Design

The TSW54J60EVM follows the LMH3401 with a 370-MHz 4th order Chebyshev Low-Pass Filter (LPF) filter to remove out-of-band noise and harmonics aliasing into the first Nyquist zone of the ADS54J60. The filter has been designed for less than 2-dB pass-band ripple with cut-off frequency at 370 MHz, and stop-band attenuation of 30 dB at 1 GHz. The circuit is appropriately biased to match the ADC common-mode level by connecting the VCM output to the common mode termination. Figure 5 shows the filter simulated response.

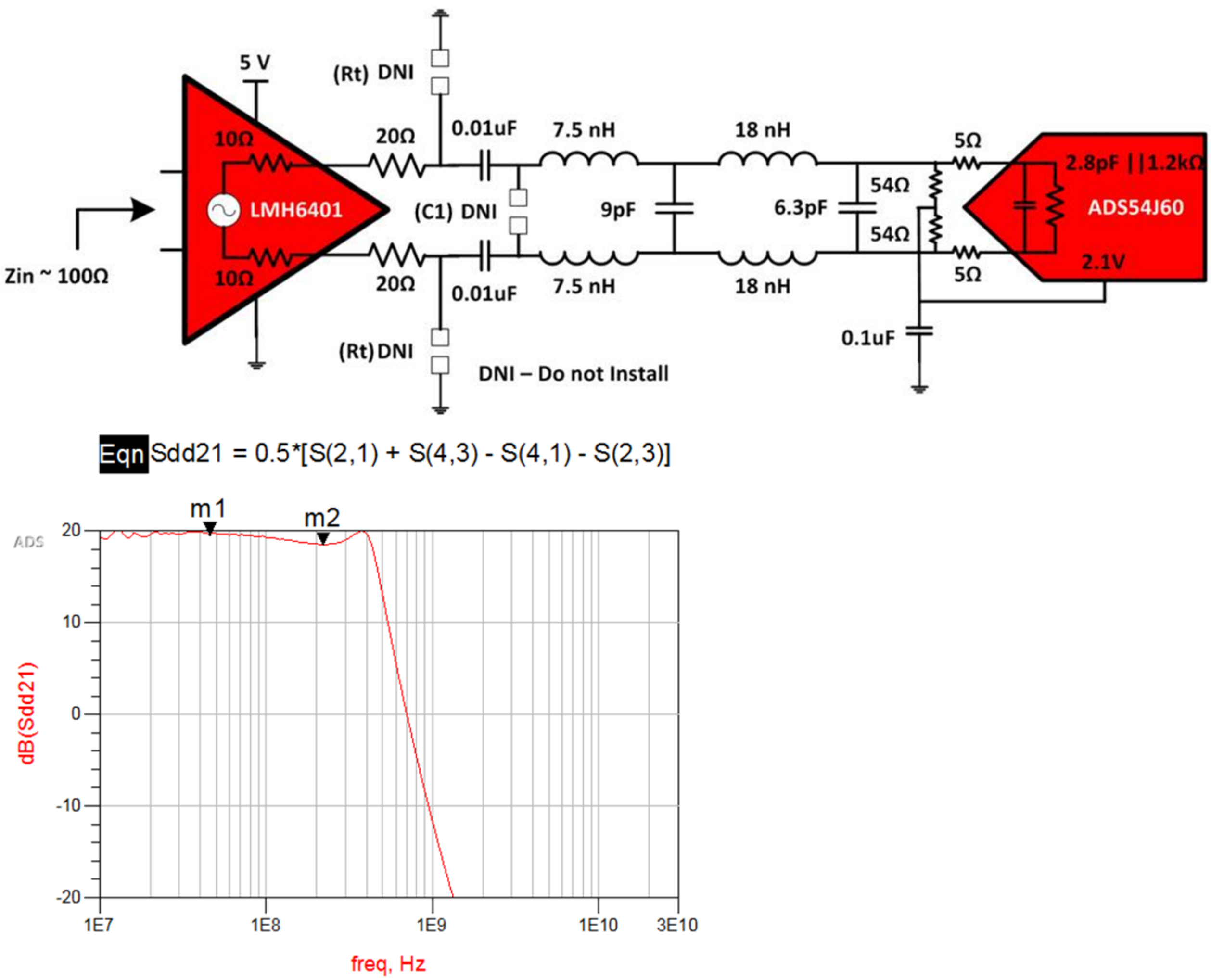

Figure 5. 370-MHz Low-Pass Filter and Simulation Response

Figure 6 shows the measured performance of this filter.

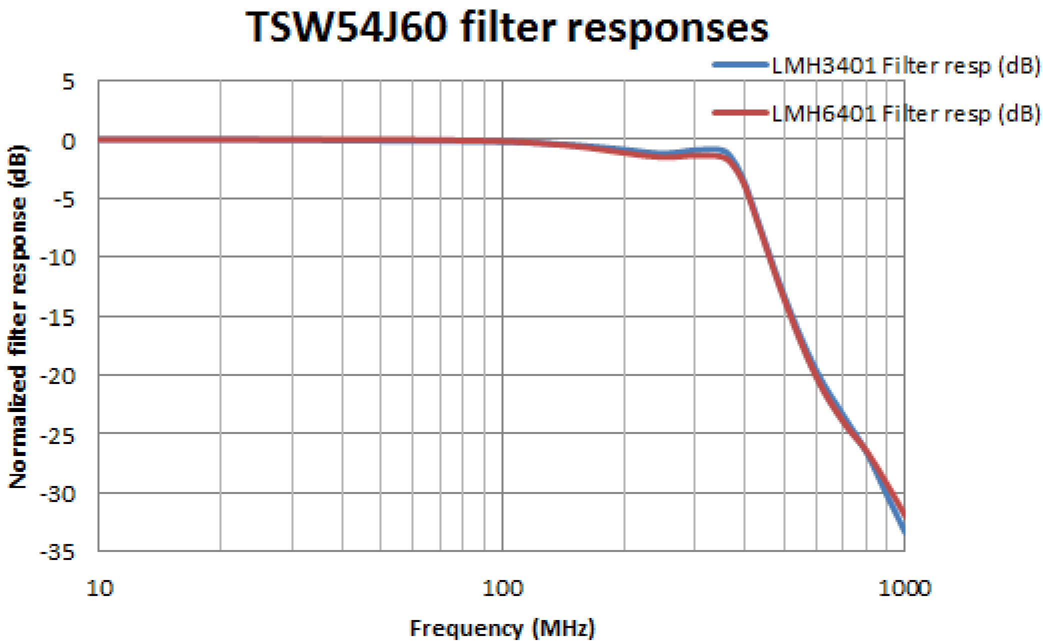

Figure 6. 370-MHz Low-Pass Filter Measured Responses

The LMH3401, as with most RF amplifiers, has two 10-Ω, on-chip resistors on each output leg to provide isolation from board parasitic at the output pins. When designing a filter between the amplifier and the interfacing circuitry (ADC), the filter source impedance must be calculated by taking into account the two 10-Ω, on-chip resistors. Table 1 lists the calculated external source impedance values (R_{O+} and R_{O-}) required for various matched filter loads (R_L). An important note is that the filter design between the LMH3401 and the ADC is not limited to a matched filter, and source impedance values (R_{O+} and R_{O-}) can be reduced to achieve higher swing at the filter outputs. Achieving lower loss in the filter source impedance resistors or higher swing at the filter outputs is often desirable because the amplifier must reduce the output swing to maintain the same full-scale input at the ADC. Thus, better linearity performance occurs.

The 370-MHz, un-matched, low-pass filter between the LMH3401 and ADS54J60 is shown in Figure 4, with (R_{O+} and R_{O-}) set to 20 Ω and RL set to 100 Ω. Since the ADC input impedance (RL) is set to 100 Ω and the termination resistors including the two on-chip 10-Ω resistors on LMH3401 output is 60 Ω, the termination loss (or insertion loss) between the LMH3401 and ADS54J60 is approximately 4-dB (or 2-dB). The termination loss is calculated by the voltage division between the ADC input and the termination resistors at the amplifier output.

$$VIN_{ADC}(diff) = Loss \times VOUT_{AMP}(diff) \tag{1}$$

For the LMH3401 and the ADS54J60 interface, use:

$$Loss(dB) = 20 \times \log10\left(\frac{R_L}{R_L + R_{0+} + R_{0-} + 20}\right) \tag{2}$$

Table 1 lists the load component values.

Table 1. Load Component Values [(1)]

LOAD (R_L)	R_{O+} and R_{O-} FOR A MATCHED TERMINATION	TOTAL LOAD RESISTANCE AT AMPLIFIER OUTPUT	TERMINATION LOSS
50 Ω	15 Ω	100 Ω	6 dB
100 Ω	40 Ω	200 Ω	6 dB
200 Ω	90 Ω	400 Ω	6 dB
400 Ω	190 Ω	800 Ω	6 dB
1 kΩ	490 Ω	2000 Ω	6 dB

(1) The total load includes termination resistors.

7 Power Supply Considerations

The LMH3401 device may operate with either a single or dual supply, and with either DC-coupling or AC-coupling. The advantage of AC-coupling over DC-coupling is that it offers more freedom of choice in regard to power supply. The main concern with DC-coupling is ensuring that the input common-mode voltage does not violate the device operating conditions. By AC-coupling the input of the driver, the input self-biases at the level set by the output CM (VCM) pin which ensures optimal operation.

If a single supply is used, AC-coupling the amplifier when driving an ADC is easier in relation to common-mode settings. The TSW54J60EVM uses a 5-V single supply configuration for both the LMH3401 and LMH6401 amplifiers.

If DC-coupling must be used with a single supply, the common-mode output of the driver must operate at VS+ / 2 (in this case, 2.5 V) and DC level shifting must be used to match the common mode of the ADC. The appropriate common mode is set by using a voltage divider as described in the Common Mode Considerations section. The drawback is this method results in a loss of signal power because the amplifier must drive a larger voltage to overcome the attenuation of the voltage divider, which results in degraded performance.

The input common-mode voltage (V_{ICM}) of the DC-coupled driver input must also be considered. While the output common-mode voltage (V_{OCM}) is set at V_{CM}, V_{ICM} may have a small delta compared to V_{OCM} based on the internal feedback resistors. This delta may generate a flow-back current that wastes power in the feedback resistors. Also, based on the signal source, the delta may cause issues in some applications that may require a buffer amplifier before the fully-differential amplifier.

If the application uses a split supply, an advantageous approach is to use a non-symmetric supply operation. For example, non-symmetric supply operation with a DC-coupled application driving an ADC that requires an input common mode of 2.0 V. Using +4.5V and –0.5V supplies will allow to set the amplifier output CM to 2.0 V.

The following summarizes the AC-coupling and DC-coupling differences between a single-supply operation and a split-supply operation.

Single Supply Operation (5 V):

- ***AC-Coupling:***
- The CM is biased at 2.5 V at the output of the amplifier.
- Easily adapts to any required ADC input CM.
- Filter design between the amplifier and the ADC interface becomes easier because the DC level shifting is not required.
- ***DC-Coupling:***
- The input CM of the amplifier may differ from the output CM, which leads to current leakages.
- Adapting to the input CM of the ADC requires a voltage divider which leads to losses in signal power and potential distortion issues.

Split-supply Operation:

- **AC-Coupling:**
  - The CM is biased at the output of the amplifier.
  - Easily adapts to any required ADC input CM.
- **DC-Coupling:**
  - Best solution if the supply may be set to match the required input CM of the ADC.
  - Voltage divider is not required which leads to easier interface configuration.
  - Increases the number of supplies which increases board space and cost.

8 Results

Table 2 and Figure 7 were made using results from a TSW54J60 connected to a TSW14J56EVM and the HSDC Pro GUI. Data was collected with the board configured from DC and AC-coupling. Two signal generators, band pass filters, and 3 dB attenuators were used, along with a power combiner for the two tests. Data was collected using frequencies ranging from 70 MHz to 250 MHz. Figure 8 shows captured data using Two Tone format in the test selection option of HSDC Pro GUI. The two two tones were centered around 170 MHz, separated by 2 MHz.

Table 2. Measured Results

FREQUENCY	70	125	150	220	250
DC-coupled	**–78.045**	**–73.835**	**–73.685**	**–72.495**	**–71.54**
IMD3L	82.03	74.92	75.04	72.87	71.69
IMD3U	74.06	72.75	72.33	72.12	71.39
AC-coupled	**–79.04**	**–76.96**	**–77.94**	**–77.865**	**–75.545**
IMD3I	79.86	78.11	78.9	78.43	76.11
IMD3U	78.22	75.81	76.98	77.3	74.98

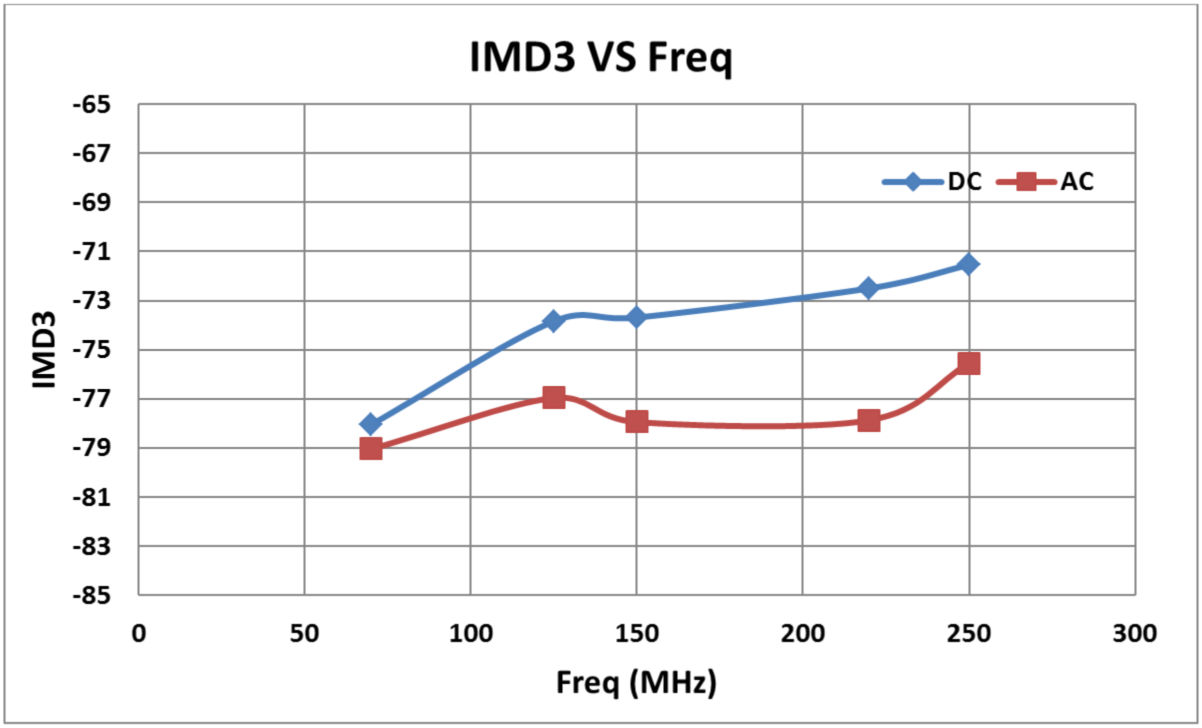

Figure 7. Two-Tone Test Results Across Frequency

Figure 8 is a screen shot from HSDC Pro GUI of a two-tone test using (169 MHz and 171 MHz).

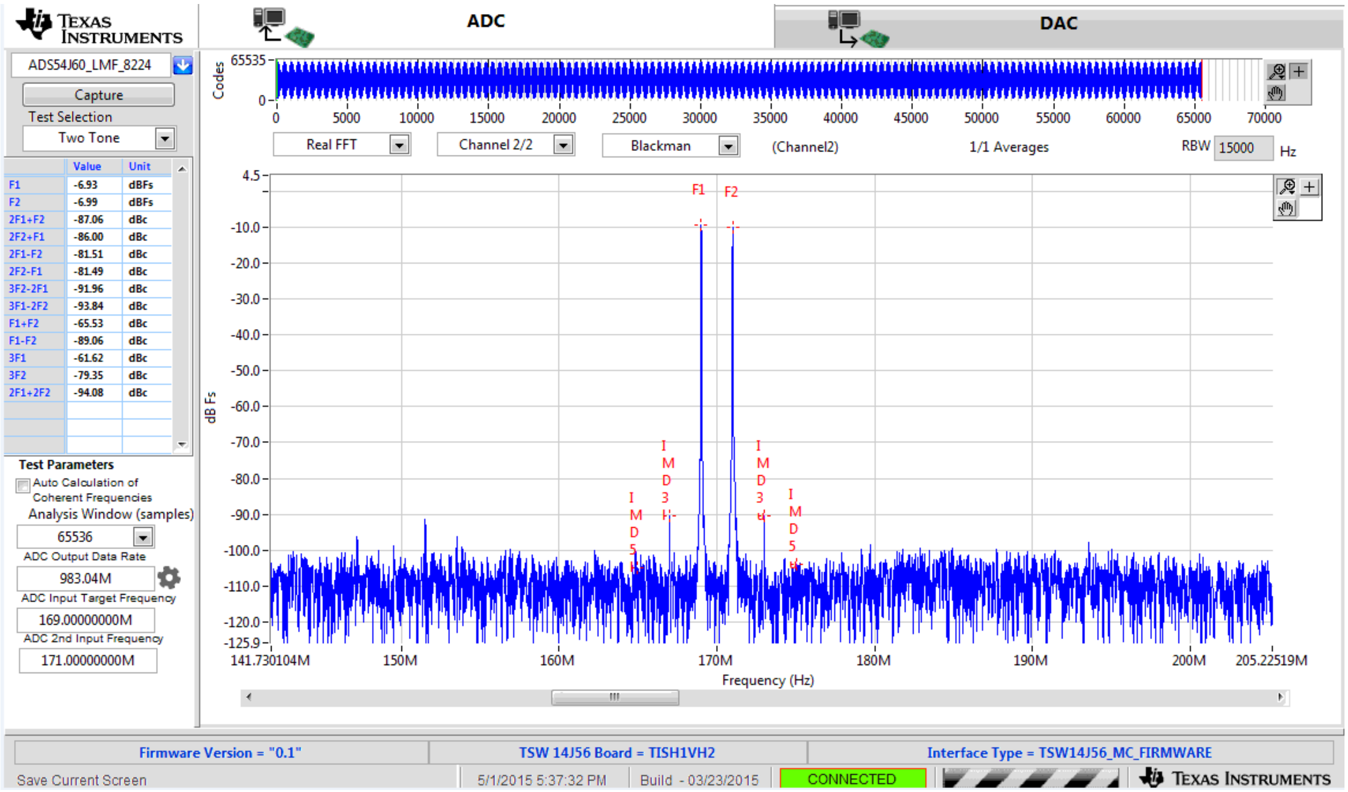

Figure 8. FFT of Two-Tone Test

The measured results show that the LMH3401 device is a good solution to drive a high-speed ADC such as the ADS54J60 device for single-ended differential high speed, wide input voltage range digitizer applications. The LMH3401 device may be set in either DC-coupled or AC-coupled configuration. An important consideration is proper common-mode biasing. One difficulty with the DC-coupling case is the need to provide the optimal common-mode voltage at the amplifier output pins and the ADC input pins. Another challenge with DC-coupling is the requirement to level-shift the DC source to the amplifier's input common mode voltage.

In terms of SNR and SFDR, the performance may be improved if time is spent to optimize the interface circuit and filtering, likely further than what is shown in this document. One way of improving the SFDR performance is by designing the output filter with lower termination resistor values at the amplifier output and keeping the same ADC input impedance. Such an output filter design lowers the amplifier output swing for the same full-scale input at the ADC and results in lower SFDR.

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