With SerDes and Lane Configuration showed in Fig1 and my first FPGA design (24MHz sine wave for both CHA & CHB ) I got the signals in Fig2.

Fig 1:

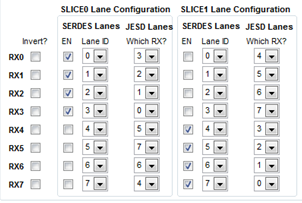


Fig 2:

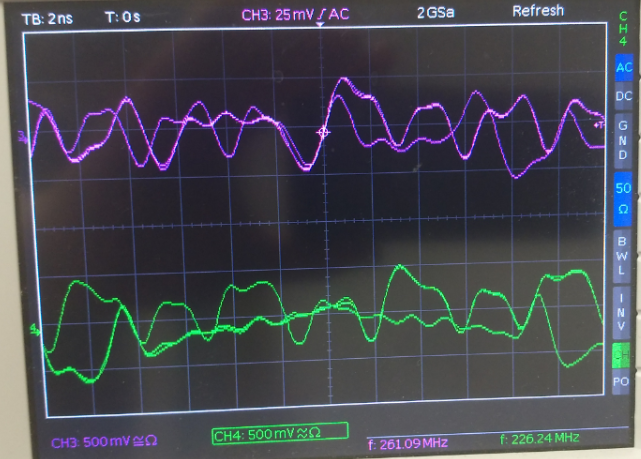


Fig 3 shows the SerDes signal paths in the EVM and ZCU102 schematics. For example, DAC Pin RX0p connects to pin A30 of the FMC connector, then bank 229 TX0p on the FPGA board. Bank 229 TX0p is located at tile X1Y8.

I assigned channel 0 to X1Y8, channel 1 to X1Y11, etc. in the FPGA design. So that Rx0 physically corresponds to TX0, RX1 to TX1, etc.. That’s why I have the configuration in Fig 4.

Fig 3:

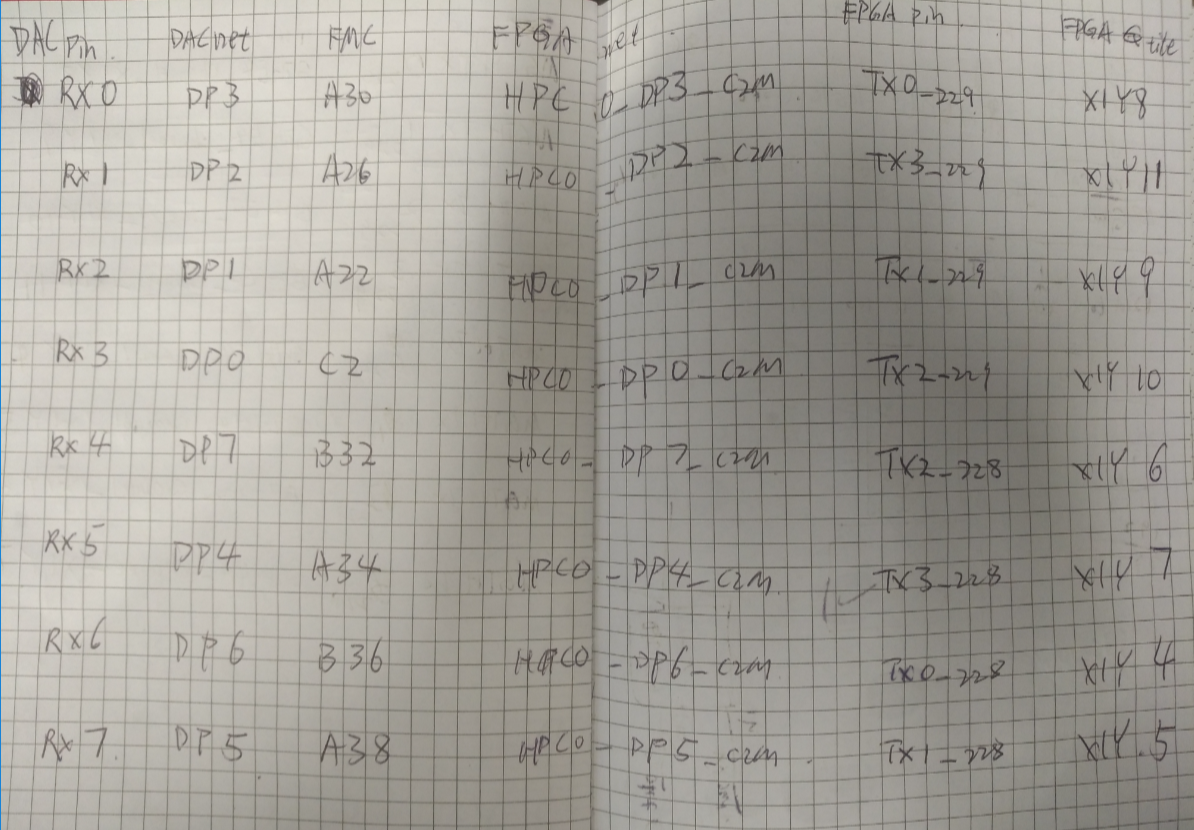


Fig 3:

