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**TSW14J56 DAC INI File Guide**

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| **Rev** | **Date** | **Revision Details** | **Author** |
| 1.0 | 03rd Feb 2014 | Initial Submission | Karthik Abiram |
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Table of Contents

[TSW14J56 DAC INI File for v1.0 DLL 3](#_Toc379220135)

[Sample INI File of v1.0 DLL 3](#_Toc379220136)

[Parameters used by v1.0 DLL 4](#_Toc379220137)

[[DAC] 4](#_Toc379220138)

[[Version 1.0] 5](#_Toc379220139)

# TSW14J56 DAC INI File for v1.0 DLL

## ****Sample INI File of v1****.0 DLL



## Parameters used by v1.0 DLL

DAC INI File for v1.0 contains two sections in the ini file : “[DAC]” and “[Version 1.0]”. Parameters in [DAC] section and all the parameters in [Version 1.0] section are used by the v1.0 DLL.

### [DAC]

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| --- | --- | --- |
| **S/N** | **Parameter** | **Description** |
| 1 | Interface name="TSW14J56\_FIRMWARE" | Firmware file name / Interface ID name in the file TSW14J56\_IID\_Lookup.csv. Interface ID hardcoded in the firmware, and ID in the csv file should match. |
| 2 | Number of channels=2 | Number of DAC channels. Used for data packing in conjunction with channel pattern (Also to decide which columns of an input pattern file will even be interpreted). |
| 3 | Number of Bits=12 | Not really used for generation purposes since data sent out is MSB aligned. But used for some scaling purposes in GUI. |
| 4 | Max sample Rate= 400000000 | Used to give a reference to the user about the sampling rate of the DAC, value to be entered in the “Data Rate” control in DAC. |
| 5 | Bus=16 | Bus Width |
| 6 | config1=16 | Config1 Register Value |
| 7 | config2=1 | Config2 Register Value |
| 8 | Register\_Config="-" | Parameter to write to custom registers of TSW14J56. Eg: Register\_Config="0x400D0:0x04:4,0x400F0:0:4"Format = [Register Address]:[Register Value]:[Number of Bytes to be sent as, which is the register size in bytes]All the 3 values in the above format supports entries in both decimal(just the number) and hexadecimal(prefixed with 0x).Multiple registers can be specified separated by comma. |
| 9 | Format Pattern=-1,-2,1,2 | DAC Channel Pattern.//- for lsb//+ for msb//eg -1,-2,1,2= lsb of 1st channel data,lsb of 2nd channel data, msb of 1st channel data,msb of 2nd channel data. |
| 10 | DLL Version=1.0 | (**Required**)Needs to be specified as 1.0 |
| 11 | Device GUI Folder="DAC3XJ84" | (Optional) Folder name of Plugin GUI, if the device GUI needs to be used as a plugin to HSDCPro |
| 12 | Menu Enable="Trigger Option" | (Optional) This parameter is used to over-ride the menu disable settings of the board, for the current device. The menu names specified here will be enabled for the current device. |
| 13 | Menu Disable="Number of Channels" | (Optional) This parameter is used to over-ride the menu enable settings of the board, for the current device. The menu names specified here will be disabled for the current device. |
| 14 | Read EVM Setup Procedure="EVM Setup Procedure not available" | Any specific procedure that needs to be followed for setting up the EVM |
| 15 | Export Parameters = “Switch between Tabs?,Firmware Download?” | (Optional) Used to specify the parameters names to be exported to the Plugin GUI. Currently supported parameters are i)Firmware Download?ii) Switch between Tabs? Note: There should not be any spaces between two consecutive parameters |

### [Version 1.0]

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| --- | --- | --- |
| **S/N** | **Parameter** | **Description** |
| 1 | JESD IP Core\_CS=1 | Configure Megacore JESD IP CORE. The value provided for these parameters is written to the JESD Ip Core registers. A value of 1 is subtracted from the following parameters, before being written to the registers – K, L, M, N, NTotal, and S. For other parameters, the same value is written to the registers. |
| 2 | JESD IP Core\_F=1 |
| 3 | JESD IP Core\_HD=1 |
| 4 | JESD IP Core\_K=32 |
| 5 | JESD IP Core\_L=8 |
| 6 | JESD IP Core\_M=4 |
| 7 | JESD IP Core\_N=16 |
| 8 | JESD IP Core\_NTotal=16 |
| 9 | JESD IP Core\_S=1 |
| 10 | JESD IP Core\_SCR=1 |
| 11 | JESD IP Core\_Tailbits=0 |
| 12 | JESD IP Core\_LaneSync=1 |
| 13 | JESD IP Core\_Subclass=1 |
| 14 | MIF Config= 0.611G to 1.5G:RX:RX\_PMA\_x5,1.5G to 3.125G:RX:RX\_PMA\_x10,3.125G to 8G:RX:RX\_PMA\_x40 | The MIF file that needs to be streamed based on the lane rate calculated from DAC Output Data Rate. Format :[Lower Range] to [Higher Range]:RX:[MIF File Name] |
| 15 | Fabric PLL Counter = 0.611G to 1.5G:0x080404,1.5G to 3.125G:0x080808,3.125G to 8G:0x080202 | Fabric PLL Register Value that needs to be written based on the lane rate calculated from DAC Output Data Rate. Format :[Lower Range] to [Higher Range]:[Fabric PLL Register Value] |
| 16 | Invert Sync Polarity = 0 | JESD Configuration Register Values. |
| 17 | Invert Serdes Data = 1  | JESD Configuration Register Values. |
| 18 | Transceiver Mode = 0 | 0 – TX/RX Only Mode. 1 – Transceiver Mode |
| 19 | Transceiver Data Length Multiplier = 2 | (Optional)The multiplication factor for data length when in transceiver mode |
| 20 | Lane Mapping=lane0:0,lane1:1,lane2:2,lane3:3,lane4:4,lane5:5,lane6:6,lane7:7 | Lane pattern for the LMF modes. |
| 21 | Number of Channels for Lane Rate = 4 | (Optional)If this parmeter is present in ini file, DLL uses this parameter for lane rate calculation |
| 22 | Binary Channel Mode = 8193 | (Optional) This binary channel mode value will be written to TX Control register(Address : 0x20004) after writing the data to the DDR |