1	PCB PN 50-28316 rev 2
4	PCA PN 50-28318 rev 2

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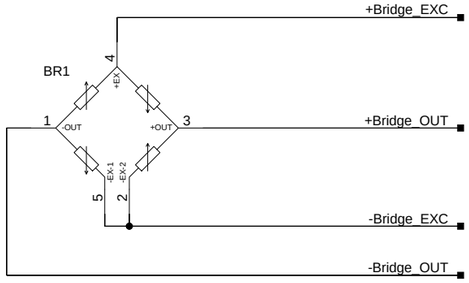
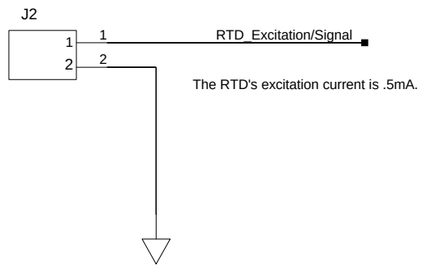
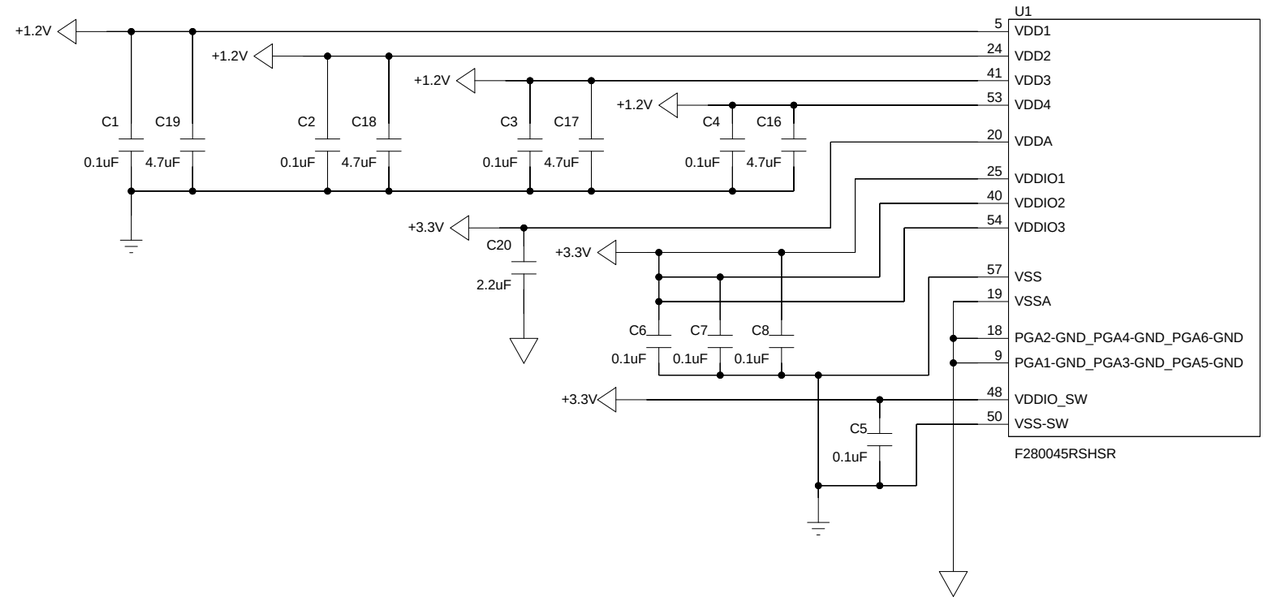
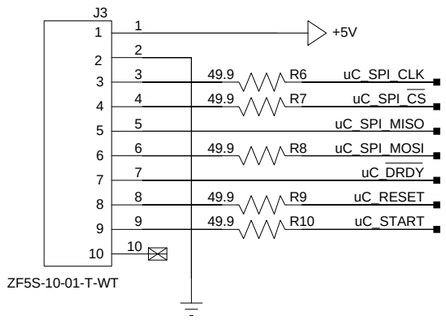
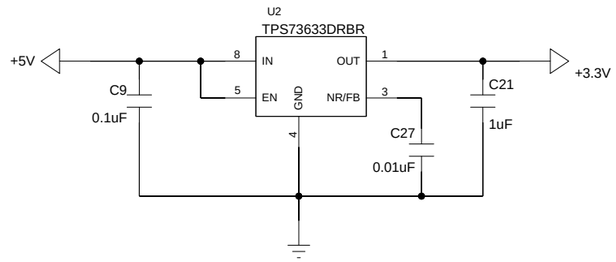




NOTE: The 1.2v voltage is internally generated. Other than the capacitive bypassing, no outside connections should be made to these pins.







NOTE 6/6/2022: rev 2 corrected errors in the power supply circuitry.
VDDIO_SW was not connected to VDDIO. VDDIO_SW is require to be connected to VDDIO.
+3.3V was connected to VDD. +3.3v should never be connected to the VDD pins.
In this configuration, the internal VREG is supplied by VDDIO and generates the 1.2v required to power the VDD pins.
Change the LDO from TPS73133DBVR to TPS73633DRBR. An increase of current output from 150mA to 400mA.

NAME
Sensors, Interconnect and Power
CIRCUIT DIAGRAM

SCALE FREE

REVISED			
DATE	DATE	DATE	DATE
DRAWN	DESIGNED	CHECKED	APPROVED

PCA PN 50-28318 rev 2
PCB PN 50-28316 rev 2
1/3

Horiba STEC

2 / 4	PCB PN 50-28316 rev 2
	PCA PN 50-28318 rev 2

HORIBA GROUP

SCHEMATICS

NOTE 6/6/2022: rev 2 Due to bridge resistance tolerance range, current sensing resistor R29's value has changed to 100 ohm.

The INA190A2 current amplifier is a 50V/V device.
With an excitation current of .6mA, the resulting voltage drop across R29 will be 60mV. The output will be 3.0V.

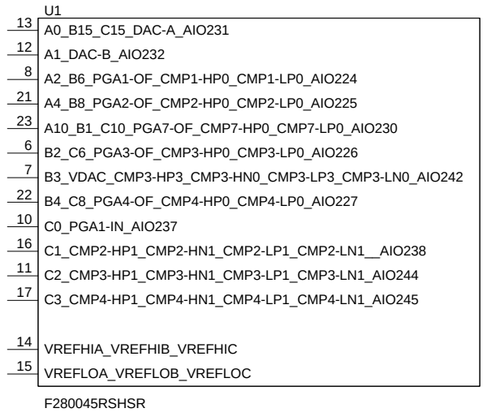
Voltage accorss R24 with .6mA is 90mV.

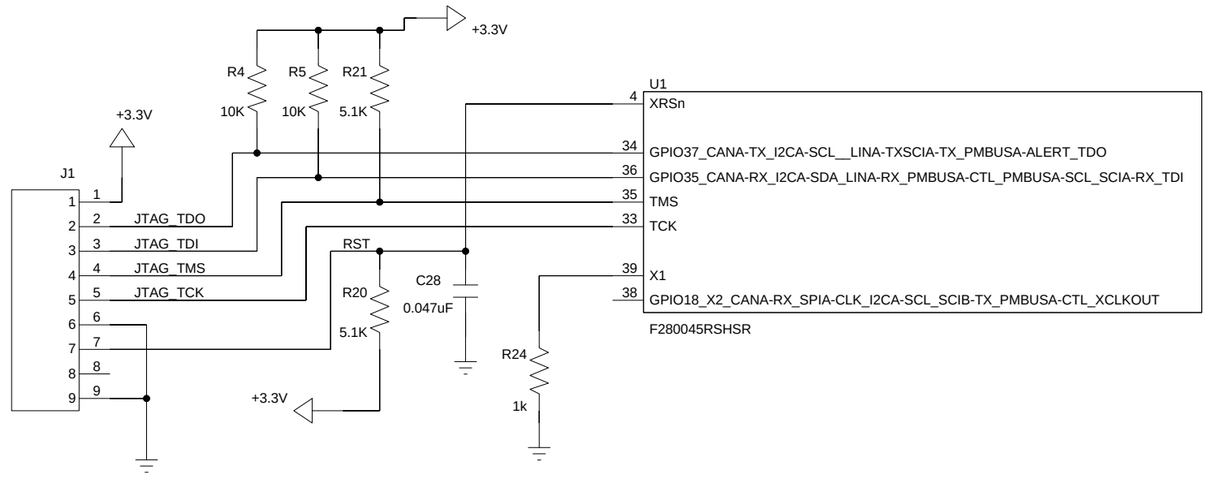
NOTE: Due to the TMUX1111 sweitch, the default output of AIN2 needs to be set lowand AIN3 needs to be set high. See AC Excitation in the ADS1261 data sheet.

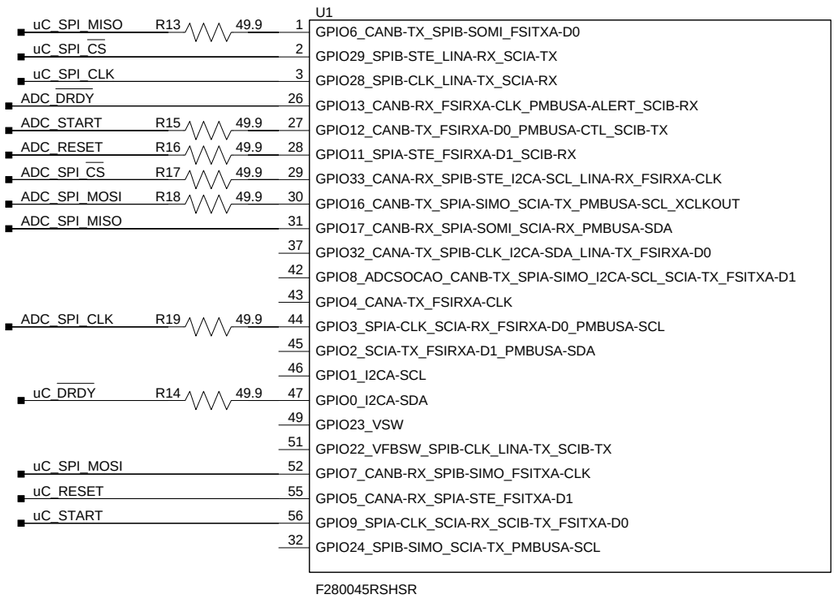
NAME			
ADC CIRCUIT DIAGRAM			
REVISED			SCALE FREE
DATE	DATE	DATE	DATE
DRAWN	DESIGNED	CHECKED	APPROVED

PCA PN 50-28318 rev 2	2 / 3
PCB PN 50-28316 rev 2	

Horiba STEC







NOTE 6/6/2022: rev 2 corrected error in IO.
uC_DRDY was connected to GPIO_VFBSW. This pin should be left open.
Moved uC_DRDY to GPIO0 (pin 47).

NAME
Micro Controller
CIRCUIT DIAGRAM

REVISED			SCALE FREE	
DATE	DATE	DATE	DATE	PCB PN 50-28316 rev 2 3/3
DRAWN	DESIGNED	CHECKED	APPROVED	PCB PN 50-28316 rev 2

Horiba STEC