REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32		
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/landandmaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
JAMES R. ESCHMEYER

DRAWING APPROVAL DATE
20-08-12

REVISION LEVEL

MICROCIRCUIT, DIGITAL-LINEAR, CMOS, 12 BIT, ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-12205**

SHEET 1 OF 32

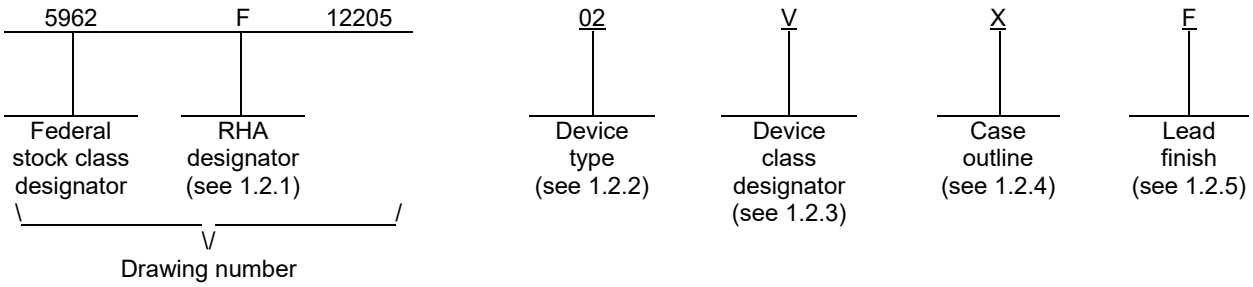
DSCC FORM 2233
APR 97

5962-E325-20

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADC12D1600	CMOS 12 bit analog to digital converter
02	ADC12D1620	CMOS 12 bit analog to digital converter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	376	Ceramic column grid array (CCGA)

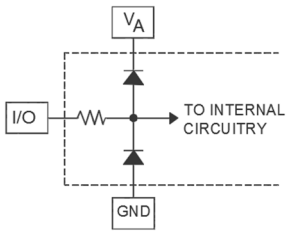
1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage (V_A, V_{TC}, V_{DR}, V_E)	2.2 V
Supply difference maximum ($V_{A/TC/DR/E}$) – minimum ($V_{A/TC/DR/E}$)	0 V to 100 mV
Voltage on any input pin (device 01)	-0.15 V to (V_A + 0.15 V)
Voltage on any input pin (except +VinI, -VinI, +VinQ, -VinQ) (device 02)	-0.15 V to 2.35 V
Voltage on $+V_{IN}$, $-V_{IN}$ (maintaining common mode)	-0.15 V to 2.5 V
Ground difference maximum ($GND_{TC/DR/E}$) – minimum ($GND_{TC/DR/E}$)	0 to 100 mV
Input current at any pin	±50 mA 3/
Power dissipation at $T_C \leq 125°C$:	
Device 01	2.4 W 4/
Device 02	4.4 W 4/
Storage temperature	-65°C to +150°C
Maximum junction temperature (T_J)	+150°C
Electrostatic discharge (ESD):	
Human body model (HBM)	2500 V 5/
Charged device model (CDM)	1500 V

1.4 Recommended operating conditions. 6/

Supply voltage (V_A, V_{TC}, V_E)	+1.8 V to +2.0 V
Driver supply voltage (V_{DR})	+1.8 V to V_A
$+V_{IN}$, $-V_{IN}$ voltage rang	-0.4 V to +2.4 V 7/
$+V_{IN}$, $-V_{IN}$ current range (ac coupled)	±50 mA 7/
$+V_{IN}$, $-V_{IN}$ power:	
Maintaining common mode voltage (ac coupled)	15.3 dBm
Not maintaining common mode voltage (ac coupled)	17.1 dBm
CLK pins voltage range	0 V to V_A
Differential CLK amplitude	0.4 V_{PP} to 2.0 V_{PP}
Case operating temperature range (T_C)	-55°C to +125°C



1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ The analog inputs are protected as shown above. Input voltage magnitudes beyond the absolute maximum ratings may damage this device.
3/ When the input voltage at any pin exceed the power supply limit; (for example, less than GND or greater than VA), the current at that pin should be limited to 50 mA. In addition, over voltage at a pin must adhere to maximum voltage limits. Simultaneously over voltage at multiple pins require adherence to the maximum package power dissipation limits.
4/ Dissipation limit is calculated using JEDEC JESD51-7 thermal model. Higher dissipation may be possible based on specific application thermal situation and specified thermal resistances.
5/ Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor.
6/ Unless otherwise specified, all voltages are measured with respect to GND = GND_{DR} = GND_E = GND_{TC} = 0 V.
7/ Proper common mode voltage must be maintained to ensure proper output code, especially during input overdrive.

1.5 Thermal characteristics.

Thermal metric for case X	Symbol	Device 01	Device 02	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	10.4	13.1	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	---	5.0	°C/W
Thermal resistance, junction-to-board	θ_{JB}	3.2	5.1	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	0.5	2.6	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	---	4.7	°C/W

1.6 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)..... 300 krads(Si) 8/
Single event phenomena (SEP):

No single event latchup (SEL) occurs at effective LET (see 4.4.4.2) ..... ≤ 120 MeV/(mg/cm^2) 9/

No single event functional interrupt (SEFI) occurs at effective LET (see 4.4.4.2) .. ≤ 120 MeV/(mg/cm^2) 9/

8/ Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

9/ Heavy ion testing facility was 88” Cyclotron Facility at Lawrence Berkeley National Laboratory (LBNL) located in Berkeley, California and ion beam energy was 4.5 MeV/nucleon exposed inside a vacuum chamber. No single event latch-up (SEL) or single-event functional interrupt (SEFI) was observed when irradiated with Bismuth(Bi) ions at fluence 1 x 10^7 ions/cm^2 at an angle 35° with bias voltage 1.8 V and 2.0 V corresponding to an effective LET of 120 MeV/(mg/cm^2).
For more information on SEP test results, customers are requested to contact the manufacturer.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC Solid State Technology Association

JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Timing diagrams. The timing diagrams shall be as specified on figure 3.

3.2.4 Functional block diagram. The functional block diagrams shall be as specified on figure 4.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Static converter characteristics							
Integral non-linearity (best fit)	INL	Direct current (dc) coupled, 1 MHz sine wave over ranged	1,2,3	01, 02	-7.5	+7.5	LSB
Differential non-linearity	DNL	DC coupled, 1 MHz sine wave over ranged	1,2,3	01, 02	-1.35	1.35	LSB
Resolution with no missing codes			1,2,3	01, 02		12	Bits
Positive full scale error	PFSE	5/	1,2,3	01, 02	-30	30	mV
Negative full scale error	NFSE	5/	1,2,3	01, 02	-30	30	mV
Out of range output code		$+V_{IN} - -V_{IN} >$ + full scale	1,2,3	01, 02		4095	
		$+V_{IN} - -V_{IN} <$ - full scale			0		
Dynamic converter characteristics.							
1:2 Demux, non-DES mode, non-ECM, non-LSPSM, f_{CLK} = 1.6 GHz, f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS.							
Effective number of bits	ENOB		4,5	01	8.5		Bits
			6		8.1		
			4	02	8.8		
			5		8.7		
			6		8.4		
Signal to noise plus distortion ratio	SINAD		4,5	01	53.0		dBFS
			6		50.6		
			4	02	54.7		
			5		54.1		
			6		52.3		
Signal to noise ratio	SNR		4,5	01	54.6		dBFS
			6		52.5		
			4	02	56		
			5		54.6		
			6		53.5		
Total harmonic distortion	THD		4,5	01		-58.6	dBFS
			6			-55.1	
			4,5	02		-59.2	
			6			-55.5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic converter characteristics – continued.							
1:2 Demux, non-DES mode, non-ECM, non-LSPSM, f_{CLK} = 1.6 GHz, f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS - continued.							
Spurious free dynamic range	SFDR		4,5	01	58.0		dBFS
			6		55.0		
			4	02	58.9		
			5		58.1		
			6		56		
1:2 Demux, non-DES mode, non-ECM, LSPSM, f_{CLK} = 800 MHz, f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS.							
Effective number of bits	ENOB		4,5	01	8.9		Bits
			6		8.5		
			4,5	02	9.1		
			6		8.6		
Signal to noise plus distortion ratio	SINAD		4,5	01	55.4		dBFS
			6		53.0		
			4,5	02	56.5		
			6		53.5		
Signal to noise ratio	SNR		4,5	01	56.4		dBFS
			6		55.8		
			4,5	02	57.6		
			6		56.8		
Total harmonic distortion	THD		4,5	01, 02		-62.3	dBFS
			6			-57.0	
Spurious free dynamic range	SFDR		4,5	01	62.5		dBFS
			6		57.7		
			4,5	02	62.5		
			6		57.5		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Analog input/output and reference characteristics.							
Analog difference input full scale range	V_{IN_FSR}	FSR pin Y3 high	4,5,6	01, 02	750	890	mV_{PP}
Differential input resistance	R_{IN}		1,2,3	01, 02	99	107	Ω
Common mode output voltage	V_{CMO}	$I_{CMO} = \pm 100\ \mu A$	1,2,3	01, 02	1.15	1.35	V
Bandgap reference output voltage	V_{BG}	$I_{BG} = \pm 100\ \mu A$	1,2,3	01, 02	1.15	1.35	V
Digital control and output pin characteristics.							
Digital control pins (DES, LSPSM, CAL, PDI, PDQ, TPM, NDM, FSR, DDRPh, $\overline{ECE}$, SCLK, SDI, $\overline{SCS}$).							
Logic high input voltage	V_{IH}	DES, LSPSM, CAL, PDI, PDQ, TPM, NDM, FSR, DDRPh, $\overline{ECE}$, SCLK, SDI, $\overline{SCS}$	1,2,3	01, 02	0.7 X V_A		V
Logic low input voltage	V_{IL}	DES, LSPSM, CAL, PDI, PDQ, TPM, NDM, FSR, DDRPh, $\overline{ECE}$, SCLK, SDI, $\overline{SCS}$	1,2,3	01, 02		0.3 X V_A	V
Input current high, $V_{IN} = V_A$	I_{IH}	DES, LSPSM, CAL, PDI, PDQ, TPM, NDM, FSR, DDRPh, $\overline{ECE}$, SCLK, SDI, $\overline{SCS}$	1,2,3	01, 02	-1	1	μA
Input current low, V_{IN} = GND	I_{IL}	DES, LSPSM, CAL, TPM, NDM, FSR, DDRPh,	1,2,3	01, 02	-1	1	μA
		SCLK, SDI, $\overline{SCS}$			-30		
		PDI, PDQ, $\overline{ECE}$			-55		
Input leakage current	I_{IH}	$V_{IN} = V_A$	1,2,3	02	-1	1	μA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital outputs pin (data, DCLKI, DCLKQ, ORI, ORQ). See figure 3.							
LVDS differential output voltage	V_{OD}	V_{BG} = floating, OVS = V_A	1,2,3	01	380	840	mV_{PP}
		V_{BG} = floating, OVS = GND			240	650	
		V_{BG} = floating, OVS = High		02	380	840	
		V_{BG} = floating, OVS = Low			240	650	
Change in LVDS output swing between logic levels	$\Delta V_{O\ DIFF}$		1,2,3	01, 02	-20	20	mV
Logic high output level	V_{OH}	CalRun, SDO I_{OH} = -400 µA	1,2,3	01, 02	1.5		V
Logic low output level	V_{OL}	CalRun, SDO I_{OL} = 400 µA	1,2,3	01		0.3	V
				02		0.3	
Power supply characteristics.							
f_{CLK} = 1.6 GHz, 1:2 Demux mode, non-LSPSM.							
Analog supply current	I_A	PDI = PDQ = low	1,2,3	01, 02		1290	mA
Track and hold and clock supply current	I_{TC}	PDI = PDQ = low	1,2,3	01, 02		520	mA
Output driver supply current	I_{DR}	PDI = PDQ = low	1,2,3	01, 02		380	mA
Digital encoder supply current	I_E	PDI = PDQ = low	1,2,3	01, 02		163	mA
Total current	I_T	PDI = PDQ = low	1,2,3	01, 02		2280	mA
		PDI = low, PDQ = high				1300	
		PDI = high, PDQ = low				1300	
Power consumption	PC	PDI = PDQ = low	1,2,3	01, 02		4.4	W

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

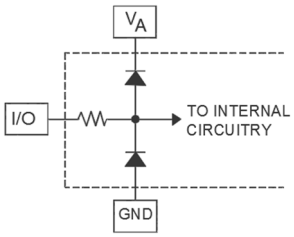
Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
f_{CLK} = 800 MHz, 1:2 Demux mode, LSPSM.							
Analog supply current	I_A	PDI = PDQ = low	1,2,3	01, 02		860	mA
Track and hold and clock supply current	I_{TC}	PDI = PDQ = low	1,2,3	01, 02		380	mA
Output driver supply current	I_{DR}	PDI = PDQ = low	1,2,3	01, 02		350	mA
Digital encoder supply current	I_E	PDI = PDQ = low	1,2,3	01, 02		79	mA
Total current	I_T	PDI = PDQ = low	1,2,3	01, 02		1620	mA
		PDI = low, PDQ = high				940	
		PDI = high, PDQ = low				940	
Power consumption	PC	PDI = PDQ = low	1,2,3	02		3.1	W
Input clock (CLK).							
Maximum input clock frequency	fCLK (max)	Non-LSPSM	4,5,6	01, 02	1.6		GHz
		LSPSM			800		MHz
Minimum input clock frequency	fCLK (min)	Non-DES mode	4,5,6	01		200	MHz
		DES mode				250	
		Non-LSPSM, non-DES mode; LFS = 1B		02		200	
		Non-LSPSM, DES mode				250	
		LSPSM, non-DES mode				200	

1/ Devices supplied to this drawing have been characterized to levels M, D, P, L, R, F of irradiation, but devices supplied are tested at levels R and F. Pre and Post irradiation values are identical unless otherwise specified in Table IA.
When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Unless otherwise specified, the following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V_E$ = +1.9 V; I- and Q- channels ac coupled, FSR pin = high; C_L = 10 pF; differential ac coupled sine wave input clock, f_{CLK} = 1.6 GHZ at 0.5 V_{PP} with 50% duty cycle; V_{BG} = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1 %; analog signal source impedance = 100 Ω differential; 1:2 demultiplex non DES mode; I- and Q- channels; duty cycle stabilizer on. The maximum clock frequency for non-demux mode is 1 GHZ.

TABLE IA. Electrical performance characteristics - Continued.

3/ The analog inputs are protected as shown below. Input voltage magnitudes beyond the absolute maximum ratings may damage this device.



4/ To guarantee accuracy, it is required that V_A, V_{TC}, V_E and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

5/ Calculation of full scale error for this device assumes that the actual reference voltage is exactly its nominal value. Full scale error for this device, therefore, is a combination of full scale error and reference voltage error. See manufacturer's datasheet for information transfer characteristic for relationship between gain error and full scale error, see specification definitions for gain error.

TABLE IB. SEP test limits. 1/ 2/ 3/ 4/

Device type	SEP	Supply voltages	Effective linear energy transfer (LET)
02	No SEL	1.8 V and 2.0 V	LET $\leq$ 120 MeV/(mg/cm^2)
	No SEFI	1.8 V and 2.0 V	LET $\leq$ 120 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by technical review board and qualifying activity.

3/ Tested for single event latch up at worse case temperature, T_C = +125°C $\pm$ 10°C.

4/ Heavy ion testing facility was 88" Cyclotron Facility at Lawrence Berkeley National Laboratory (LBNL) located in Berkeley, California and ion beam energy was 4.5 MeV/nucleon exposed inside a vacuum chamber. No single event latch-up (SEL) or single-event functional interrupt (SEFI) was observed when irradiated with Bismuth (Bi) ions at fluence 1 x 10^7 ions/cm^2 at an angle 35° with bias voltage 1.8 V and 2.0 V corresponding to an effective LET of 120 MeV/(mg/cm^2). For more information on SEP test results, customers are requested to contact the manufacturer.

Case outline X

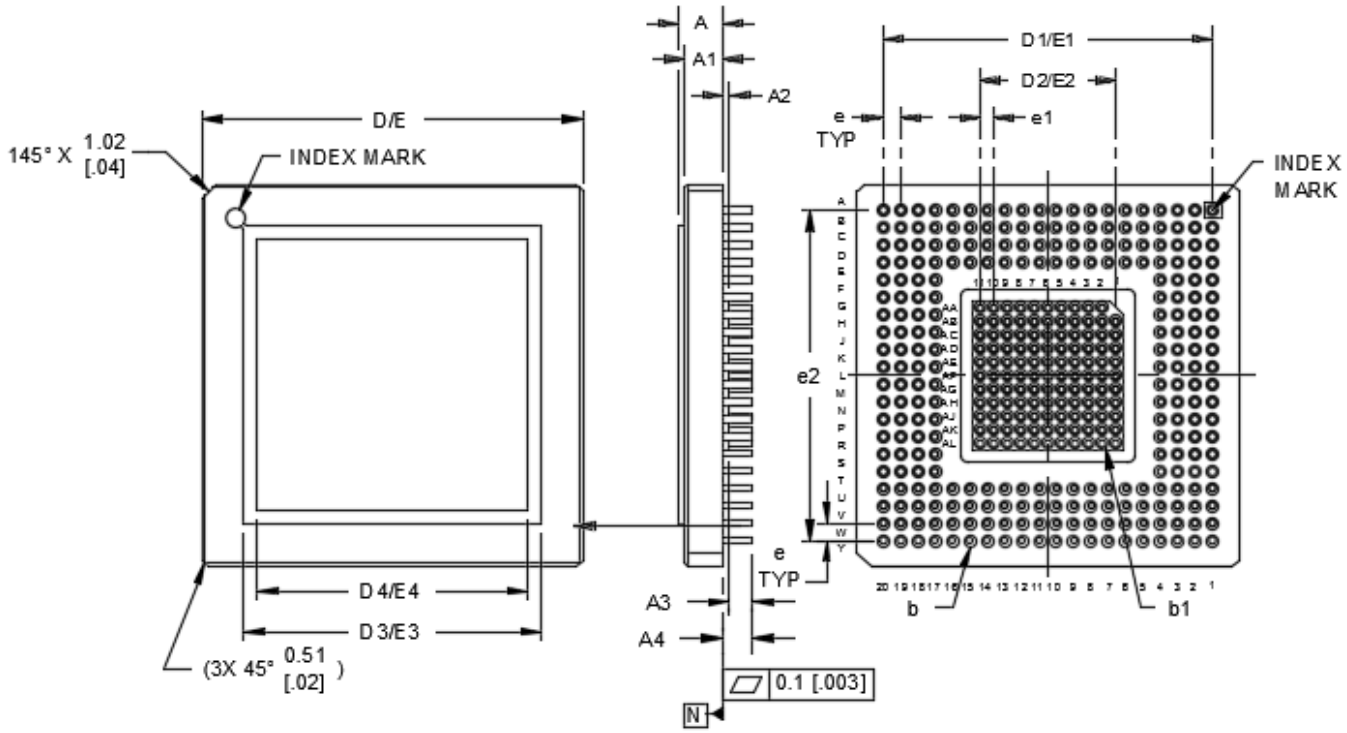


FIGURE 1. Case outline.

Case X

Symbol	Dimensions					
	Inches			Millimeters		
	Min	Nominal	Max	Min	Nominal	Max
A	.116	.127	.138	2.94	3.22	3.5
A1	.101	.110	.119	2.54	2.79	3.04
A2	.015	.020	.025	0.37	0.5	0.63
A3	.062	.0673	.0726	1.575	1.71	1.845
A4	.0817	.0870	.0923	2.075	2.21	2.345
b	.0181	.0201	.0221	0.459	0.51	0.561
b1	.0181	.0201	.0221	0.459	0.51	0.561
D/E	1.0914	1.100	1.1086	27.72	27.94	28.16
D1/E1	.950 BSC			24.13 BSC		
D2/E2	.394 BSC			10.0 BSC		
D3/E3	.8501	.8587	.8673	21.59	21.81	22.03
D4/E4	.777	.7799	.7828	19.734	19.19	19.886
e	.050 BSC			1.27 BSC		
e1	.039 BSC			1.00 BSC		
e2	.950 BSC			24.13 BSC		

NOTE:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.

FIGURE 1. Case outline - continued.

Device types	01, 02						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	GND	B1	Vbg	C1	Rtrim+	D1	V_A
A2	V_A	B2	GND	C2	GND	D2	Rtrim-
A3	SDO	B3	ECEb	C3	Rext+	D3	Rext-
A4	TPM	B4	SDI	C4	SCSb	D4	GND
A5	NDM	B5	CalRun	C5	SCLK	D5	GND
A6	V_A	B6	V_A	C6	GND	D6	CAL
A7	GND	B7	GND	C7	V_A	D7	Vbiasl
A8	V_E	B8	GND_E	C8	V_E	D8	V_A
A9	GND_E	B9	V_E	C9	GND_E	D9	V_A
A10	Dld0+	B10	Dld0-	C10	Dld1+	D10	Dld1-
A11	V_DR	B11	Dld2+	C11	Dld2-	D11	V_DR
A12	Dld3+	B12	Dld3-	C12	Dld4+	D12	Dld4-
A13	GND_DR	B13	Dld5+	C13	Dld5-	D13	GND_DR
A14	Dld6+	B14	Dld6-	C14	Dld7+	D14	Dld7-
A15	V_DR	B15	Dld8+	C15	Dld8-	D15	V_DR
A16	Dld9+	B16	Dld9-	C16	Dld10-	D16	GND_DR
A17	GND_DR	B17	Dld10+	C17	Dl0-	D17	V_DR
A18	Dld11+	B18	Dl0+	C18	V_DR	D18	Dl3+
A19	Dld11-	B19	Dl1+	C19	Dl2+	D19	Dl4+
A20	GND_DR	B20	Dl1-	C20	Dl2-	D20	Dl4-

FIGURE 2. Terminal connections.

Device types	01, 02						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
E1	V_A	H17	DI9+	M1	VinQ-	R1	V_A
E2	Tdiode+	H18	DI9-	M2	GND_TC	R2	GND_TC
E3	VbiasI	H19	DI10+	M3	V_TC	R3	V_TC
E4	GND	H20	DI10-	M4	VbiasQ	R4	V_TC
E17	GND_DR	J1	VinI-	M17	GND_DR	R17	V_DR
E18	DI3-	J2	GND_TC	M18	DQ11+	R18	DQ6+
E19	DI5+	J3	V_TC	M19	DQ11-	R19	DQ6-
E20	DI5-	J4	VbiasI	M20	GND_DR	R20	V_DR
F1	V_A	J17	V_DR	N1	VinQ+	T1	V_A
F2	GND_TC	J18	DI11+	N2	V_TC	T2	GND_C
F3	Tdiode-	J19	DI11-	N3	GND_TC	T3	GND_C
F4	VbiasQ	J20	V_DR	N4	V_A	T4	GND
F17	GND_DR	K1	GND	N17	DQ9+	T17	V_DR
F18	DI6+	K2	VbiasI	N18	DQ9-	T18	DQ3-
F19	DI6-	K3	V_TC	N19	DQ10+	T19	DQ5+
F20	GND_DR	K4	GND_TC	N20	DQ10-	T20	DQ5-
G1	V_TC	K17	ORI+	P1	V_TC	---	---
G2	GND_TC	K18	ORI-	P2	GND_TC	---	---
G3	V_TC	K19	DCLKI+	P3	V_TC	---	---
G4	V_TC	K20	DCLKI-	P4	V_TC	---	---
G17	DI7+	L1	GND	P17	DQ7+	---	---
G18	DI7-	L2	VbiasQ	P18	DQ7-	---	---
G19	DI8+	L3	V_TC	P19	DQ8+	---	---
G20	DI8-	L4	GND_TC	P20	DQ8-	---	---
H1	VinI+	L17	ORQ+	---	---	---	---
H2	V_TC	L18	ORQ-	---	---	---	---
H3	GND_TC	L19	DCLKQ+	---	---	---	---
H4	V_A	L20	DCLKQ-	---	---	---	---

FIGURE 2. Terminal connections - Continued.

Device types	01, 02						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
U1	GND_C	V1	CLK-	W1	DCLK_ RST-	Y1	GND
U2	CLK+	V2	DCLK_ RST+	W2	GND	Y2	V_A
U3	PDI	V3	PDQ	W3	RSV	Y3	FSR
U4	GND	V4	LSPSM	W4	DDRPh	Y4	RCLK+
U5	GND	V5	DES	W5	RCLK-	Y5	RCOut1+
U6	RCOut1-	V6	RCOut2+	W6	V_A	Y6	V_A
U7	VbiasQ	V7	RCOut2-	W7	GND	Y7	GND
U8	V_A	V8	V_E	W8	GND_E	Y8	V_E
U9	V_A	V9	GND_E	W9	V_E	Y9	GND_E
U10	DQd1-	V10	DQd1+	W10	DQd0-	Y10	DQd0+
U11	V_DR	V11	DQd2-	W11	DQd2+	Y11	V_DR
U12	DQd4-	V12	DQd4+	W12	DQd3-	Y12	DQd3+
U13	GND_DR	V13	DQd5-	W13	DQd5+	Y13	GND_DR
U14	DQd7-	V14	DQd7+	W14	DQd6-	Y14	DQd6+
U15	V_DR	V15	DQd8-	W15	DQd8+	Y15	V_DR
U16	V_DR	V16	DQd10-	W16	DQd9-	Y16	DQd9+
U17	GND_DR	V17	DQ0-	W17	DQd10+	Y17	GND_DR
U18	DQ3+	V18	GND_DR	W18	DQ0+	Y18	DQd11+
U19	DQ4+	V19	DQ2+	W19	DQ1+	Y19	DQd11-
U20	DQ4-	V20	DQ2-	W20	DQ1-	Y20	GND_DR

FIGURE 2. Terminal connections - Continued.

Device types	01, 02				
Case outline	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
AA1	---	AC1	GND	AE1	GND
AA2	GND	AC2	GND	AE2	GND
AA3	GND	AC3	GND	AE3	GND
AA4	GND	AC4	GND	AE4	GND
AA5	GND	AC5	GND	AE5	GND
AA6	GND	AC6	GND	AE6	GND
AA7	GND	AC7	GND	AE7	GND
AA8	GND	AC8	GND	AE8	GND
AA9	GND	AC9	GND	AE9	GND
AA10	GND	AC10	GND	AE10	GND
AA11	GND	AC11	GND	AE11	GND
AB1	GND	AD1	GND	AF1	GND
AB2	GND	AD2	GND	AF2	GND
AB3	GND	AD3	GND	AF3	GND
AB4	GND	AD4	GND	AF4	GND
AB5	GND	AD5	GND	AF5	GND
AB6	GND	AD6	GND	AF6	GND
AB7	GND	AD7	GND	AF7	GND
AB8	GND	AD8	GND	AF8	GND
AB9	GND	AD9	GND	AF9	GND
AB10	GND	AD10	GND	AF10	GND
AB11	GND	AD11	GND	AF11	GND

FIGURE 2. Terminal connections - Continued.

Device types	01, 02				
Case outline	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
AG1	GND	AJ1	GND	AL1	GND
AG2	GND	AJ2	GND	AL2	GND
AG3	GND	AJ3	GND	AL3	GND
AG4	GND	AJ4	GND	AL4	GND
AG5	GND	AJ5	GND	AL5	GND
AG6	GND	AJ6	GND	AL6	GND
AG7	GND	AJ7	GND	AL7	GND
AG8	GND	AJ8	GND	AL8	GND
AG9	GND	AJ9	GND	AL9	GND
AG10	GND	AJ10	GND	AL10	GND
AG11	GND	AJ11	GND	AL11	GND
AH1	GND	AK1	GND	---	---
AH2	GND	AK2	GND	---	---
AH3	GND	AK3	GND	---	---
AH4	GND	AK4	GND	---	---
AH5	GND	AK5	GND	---	---
AH6	GND	AK6	GND	---	---
AH7	GND	AK7	GND	---	---
AH8	GND	AK8	GND	---	---
AH9	GND	AK9	GND	---	---
AH10	GND	AK10	GND	---	---
AH11	GND	AK11	GND	---	---

FIGURE 2. Terminal connections - Continued.

Analog front end and clock columns		
Terminal number	Terminal symbol	Description
H1/J1 N1/M1	VinI± VinQ±	Differential signal I- and Q- inputs. In the non-dual edge sampling (non-DES) mode, each I- and Q- input is sampled and converted by its respective channel with each positive transition of the CLK input. In non-ECM (non-extended control mode) and DES mode, both channels sample the I- input. In extended control mode (ECM), the Q- input may optionally be selected for conversion in DES mode by the DEQ bit (Address: 0h, Bit 6). Each I- and Q- channel input has an internal common mode bias that is disabled when DC-coupled Mode is selected. Both inputs must be either AC or DC coupled. The coupling mode is selected by the V_{CMO} pin. In non-ECM, the full scale range of these inputs is determined by the FSR pin; both I- and Q- channels have the same full scale input range. In ECM, the full scale input range of the I- and Q- channel inputs may be independently set via the control register (Address: 3h and Address Bh). Note that the high and low full scale input range setting in non-ECM corresponds to the middle and minimum full scale input range in ECM. The input offset may also be adjusted in ECM.
U2/V1	CLK±	Differential converter sampling clock. In the non-DES mode, the analog inputs are sampled on the positive transitions of this clock signal. In the DES mode, the selected input is sampled on both transitions of this clock. This clock must be ac coupled.
V2/W1	DCLK_RST±	Differential DCLK reset. A positive pulse on this input is used to reset the DCLKI and DCLKQ outputs of two or more devices in order to synchronize then with other devices in the system. DCLKI and DCLKQ are always in phase with each other, unless one channel is powered down, and do not require a pulse from DCLK_RST to become synchronized. The pulse applied here must meet timing relationships with respect to the CLK input. Although supported, this feature has been superseded by autosync.
B1	VBG	Bandgap voltage output or LVDS common mode voltage select. This pin provides a buffered version of the bandgap output voltage and is capable of sourcing/sinking 10 μA and driving a load of up to 80 pF. Alternately, this pin may be used to select the LVDS digital output common mode voltage. If tied to logic-high, the 1.2V LVDS common-mode voltage is selected; 0.8 V is the default.
C3/D3	Rext±	External reference resistor terminals. A 3.3 kΩ ±0.1% resistor should be connected between Rext±. The Rext resistor is used as a reference to trim internal circuits which affect the linearity of the converter; the value and precision of this resistor should not be compromised.
C1/D2	Rtrim±	Input termination trim resistor terminals. A 3.3 kΩ ±0.1% resistor should be connected between Rtrim±. The Rtrim resistor is used to establish the calibrated 100 Ω input impedance of VinI, VinQ, and CLK. These impedances may be fined tuned by varying the value of the resistor by a corresponding percentage; however, the tuning range and performance is not tested for such an alternate value.
E2/F3	Tdiode±	Temperature sensor diode positive (anode) and negative (cathode) terminals. This set of pins is used for die temperature measurements. It has not been fully characterized.

FIGURE 2. Terminal connections - Continued.

Analog front end and clock columns – continued.		
Terminal number	Terminal symbol	Description
Y4/W5	RCLK±	Reference clock input. When the autosync feature is active, and the device is in slave mode, the internal divided clocks are synchronized with respect to this input clock. The delay on this clock may be adjusted when synchronizing multiple ADCs. This feature is available in ECM via control register (Address: Eh)
Y5/U6 V6/V7	RCOut± / RCOut2±	Reference clock output 1 and 2. These signals provide a reference clock at a rate of CLK/4, when enabled, independently of whether the ADC is in master or slave mode. They are used to drive the RCLK of another device, to enable automatic synchronization for multiple ADCs (autosync feature). The impedance of each trace from RCOut1 and RCOut2 to the RCLK of another device should be 100 Ω differential. Having two clock outputs allows the auto synchronization to propagate as a binary tree. Use the DOC bit (Address: Eh, Bit 1) to enable/disable this feature, default is disabled.
Control and status columns		
V5	DES	Dual edge sampling (DES) mode select. In the non-extended control mode (non-ECM), when this input is set to logic high, the DES mode of operation is selected, meaning that the VinI input is sampled by both channels in a time interleaved manner. The VinQ input is ignored. When this input is set to logic low, the device is in non-DES mode, for example, the I- and Q- channels operate independently. In the extended control mode (ECM), this input is ignored and DES mode selection is controlled through the control register by the DES bit (Address: 0h, Bit 7); default is non-DES mode operation.
V4	LSPSM	Low sampling power saving mode (LSPSM) select. In LSPSM, the power consumption is reduced by approximately 20% and some improvement in performance may be seen. The output will be in SDR in 1:2 demux mode and DDR in 1:1 non-Demux mode. The maximum sampling rate in LSPSM in non-DES mode is 800 MSPS. When this input is logic high, the device is in LSPSM and when this input is logic low, the device is in normal or non-LSPSM.
D6	CAL	Calibration cycle initiate. The user can command the device to execute a self calibration cycle by holding this input high a minimum of t_{CAL_H} after having held it low a minimum of t_{CAL_L}. This pin is active in both ECM and non-ECM. In ECM, this pin is logically OR'd with the CAL bit (Address: 0h, bit 15) in the control register. Therefore, both pin and bit must be set low and then either can be set high to execute an on command calibration.
B5	CalRun	Calibration running indication. This output is logic high while the calibration sequence is executing. This output is logic low otherwise.
U3 V3	PDI PDQ	Power down I- and Q- channel. Setting either input to logic high powers down the respective I- and Q- channel. Setting either input to logic low brings the respective I- and Q- channel to a operational state after a finite time delay. This pin is active in both ECM and non-ECM. In ECM, each pin is logically OR'd with its respective bit. Therefore, either this pin or the PDI and PDQ bit in the control register can be used to power down the I- and Q- channel (Address: 0h, bit 11 and bit 10), respectively.

FIGURE 2. Terminal connections - Continued.

Control and status columns - continued		
Terminal number	Terminal symbol	Description
A4	TPM	Test pattern mode select. With this input at logic high, the device continuously outputs a fixed, repetitive test pattern at the digital outputs. In the ECM, this input is ignored and the test pattern mode can only be activated through the control register by the TPM bit (Address: 0h, bit 12).
A5	NDM	Non-demuxed mode select. Settling this input to logic high causes the digital output bus to be in the 1:1 non-demuxed mode. Setting this input to logic low causes the digital output bus to be in the 1:2 demuxed mode. This feature is pin controlled only and remains active during ECM and non-ECM.
Y3	FSR	Full scale input range select. In non-ECM, when this input is set to logic low or logic high, the full scale differential input range for both I- and Q- channel inputs is set to the lower or higher FSR value, respectively. In the ECM, this input is ignored and the full scale range of the I- and Q- channel inputs are independently determined by the settling of Address: m3h and Address Bh, respectively. Note that the high (lower) FSR value in non-ECM corresponds to the middle (minimum) available selection in ECM; the FSR range in ECM is greater.
W4	DDRPh	DDR phase select. In DDR, this input, when logic low, selects the 0° data-to-DCLK phase relationship. When logic-high, it selects the 90° data-to-DCLK phase relationship, for example; the DCLK transition indicates the middle of the valid data outputs. In SDR, when this input is logic low, the output will transition on the rising edge of DCLK. When this input is logic high, the output transition will be on the falling edge of DCLK. This pin only has an effect when the chip is in 1:2 demuxed mode, for example, the NDM pin is set to logic low. In EDM, this input is ignored and the DDFR phase is selected through the control register by the DPS bit (address: 0h, bit 14); the default is 0° mode.
B3	$\overline{\text{ECE}}$	Extended control enable bar. Extended feature control through the SPI interface is enabled when this signal is asserted (logic low). In this case, most of the direct control pins have no effect. When this signal is de-asserted (logic high), the SPI interface is disabled, all SPI registers are reset to their default values, and all available settings are controlled via the control pins.
C4	$\overline{\text{SCS}}$	Serial chip select bar. In ECM, when this signal is asserted (logic low), SCLK is used to clock in serial data which is present on SDI and to source serial data on SDO. When this signal is de-asserted (logic high), SDI is ignored and SDO is in tri-stated.
C5	SCLK	Serial clock. In ECM, serial data is shifted into and out of the device synchronously to this clock signal. This clock may be disabled and held logic low, as long as timing specifications are not violated when the clock is enabled or disabled.
B4	SDI	Serial data in. In ECM, serial data is shifted into the device on this pin while $\overline{\text{SCS}}$ signal is asserted (logic low).
A3	SDO	Serial data out. In ECM, serial data is shifted out of the device on this pin while $\overline{\text{SCS}}$ signal is asserted (logic low). This output is tri-stated when $\overline{\text{SCS}}$ is deasserted.

FIGURE 2. Terminal connections - Continued.

Control and status columns - continued		
Terminal number	Terminal symbol	Description
W3	RSV	Reserved. This pin is used for internal purposes and should be connected to GND through a 100 kΩ resistor.
E3	RSV1	This should be decoupled with a 100 nF capacitor via a low resistance, low inductance path to GND.
F4	RSV2	This pin should be decoupled with a 100 nF capacitor via a low resistance, low inductance path to GND.
Power and ground columns		
A2, A6, B6, C7, D1, D8, D9, E1, F1, H4, N4, R1, T1, U8, U9, W6, Y2, Y6	V_A	Power supply for the analog circuitry. This supply is tied to the ESD ring. Therefore, it must be powered up before or with any other supply.
G1, G3, G4, H2, J3, K3, L3, M3, N2, P1, P3, P4, R3, R4	V_{TC}	Power supply for the track and hold and clock circuitry.
A11, A15, C18, D11, D15, D17, J17, J20, R17, R20, T17, U11, U15, U16, Y11, Y15	V_{DR}	Power supply for the output drivers.
A8, B9, C8, V8, W9, Y8	V_E	Power supply for the digital encoder.
D7, J4, K2	VbiasI	Bias voltage I- channel. This is an externally decoupled bias voltage for the I- channel. Each pin should individually be decoupled with a 100 nF capacitor via a low resistance, low inductance path to GND.
L2, M4, U7	VbiasQ	Bias voltage Q- channel. This is an externally decoupled bias voltage for the Q- channel. Each pin should individually be decoupled with a 100 nF capacitor via a low resistance, low inductance path to GND.
A1, A7, B2, B7, C2, C6, D4, D5, E4, K1, L1, T4, U4, U5, W2, W7, Y1, Y7, AA2:AA11	GND	Ground return for the analog circuitry.
F2, G2, H3, J2, K4, L4, M2, N3, P2, R2, T2, T3, U1	GND_{TC}	Ground return for the track and hold and clock circuitry.
A13, A17, A20, D13, D16, E17, F17, F20, M17, M20, U13, U17, V18, Y13, Y17, Y20	GND_{DR}	Ground return for the output drivers.
A9, B8, C9, V9, W8, Y9	GND_E	Ground return for the digital encoder.

FIGURE 2. Terminal connections - Continued.

High speed digital output columns		
Terminal number	Terminal symbol	Description
K19/K20 L19/L20	DCLKI± DCLKQ±	Data clock output for the I- and Q- channel data bus. These differential clock outputs are used to latch the output data and, if used, should always be terminated with a 100 Ω differential resistor placed as closely as possible to the differential receiver. Delayed and non-delayed data outputs are supplied synchronously to this signal. In 1:2 Demux mode or non-Demux mode, this signal is at ¼ or ½ the sampling clock rate, respectively. DCLKI and DCLKQ are always in phase with each other, unless one channel is powered down, and do not require a pulse from DCLK_RST to become synchronized.
K17/K18 L17/L18	ORI± ORQ±	Out of range output for the I- and Q-channel. This differential output is asserted logic high while the over or under range condition exists, for example, the differential signal at each respective analog input exceeds the full scale value. Each OR result refers to the current data, with which it is clocked out. If used, each of these outputs should always be terminated with a 100 Ω differential resistor placed as closely as possible to the differential receiver.
J18/J19 H19/H20 H17/H18 G19/G20 G17/G18 F18/F19 E19/E20 D19/D20 D18/E18 C19/C20 B19/B20 B18/C17 • M18/M19 N19/N20 N17/N18 P19/P20 P17/P18 R18/R19 T19/T20 U19/U20 U18/T18 V19/V20 W19/W20 W18/V17	DI11± DI10± DI9± DI8± DI7± DI6± DI5± DI4± DI3± DI2± DI1± DI0± • DQ11± DQ10± DQ9± DQ8± DQ7± DQ6± DQ5± DQ4± DQ3± DQ2± DQ1± DQ0±	I- and Q- channel digital data outputs. In non-Demux mode, this LVDS data is transmitted at the sampling clock rate. In Demux mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the delayed data, for example the other ½ of the data which was sampled one clock cycle earlier. Compared with the DId and DQd outputs, these outputs represent the later time samples. If used, each of these outputs should always be terminated with a 100 Ω differential resistor placed as closely as possible to the differential receiver.

FIGURE 2. Terminal connections - Continued.

High speed digital output columns – continued.		
Terminal number	Terminal symbol	Description
A18/A19	DId11±	Delayed I- and Q- channel digital data outputs. In non-Demux mode, these outputs are tri-stated. In Demux mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the non-delayed data, for example, the other ½ of the data which was sampled one clock cycle later. Compared with the DI and DQ outputs, these outputs represent the earlier time samples. If used, each of these outputs should always be terminated with a 100 Ω differential resistor placed as closely as possible to the differential receiver.
B17/C16	DId10±	
A16/B16	DId9±	
B15/C15	DId8±	
C14/D14	DId7±	
A14/B14	DId6±	
B13/C13	DId5±	
C12/D12	DId4±	
A12/B12	DId3±	
B11/C11	DId2±	
C10/D10	DId1±	
A10/B10	DId0±	
•	•	
Y18/Y19	DQd11±	
W17/V16	DQd10±	
Y16/W16	DQd9±	
W15/V15	DQd8±	
V14/U14	DQd7±	
Y14/W14	DQd6±	
W13/V13	DQd5±	
V12/U12	DQd4±	
Y12/W12	DQd3±	
W11/V11	DQd2±	
V10/U10	DQd1±	
Y10/W10	DQd0±	

FIGURE 2. Terminal connections - Continued.

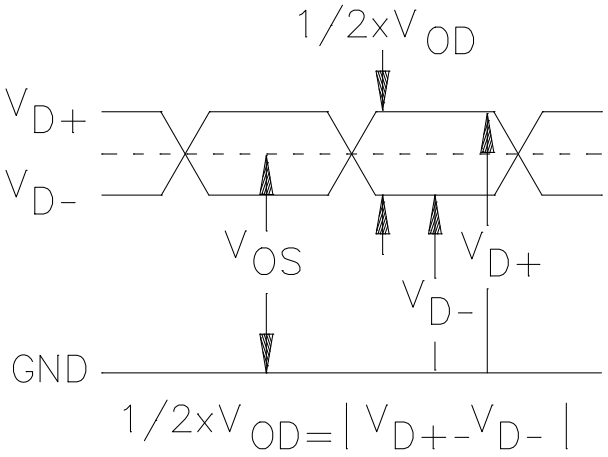


FIGURE 3. LVDS output signal levels.

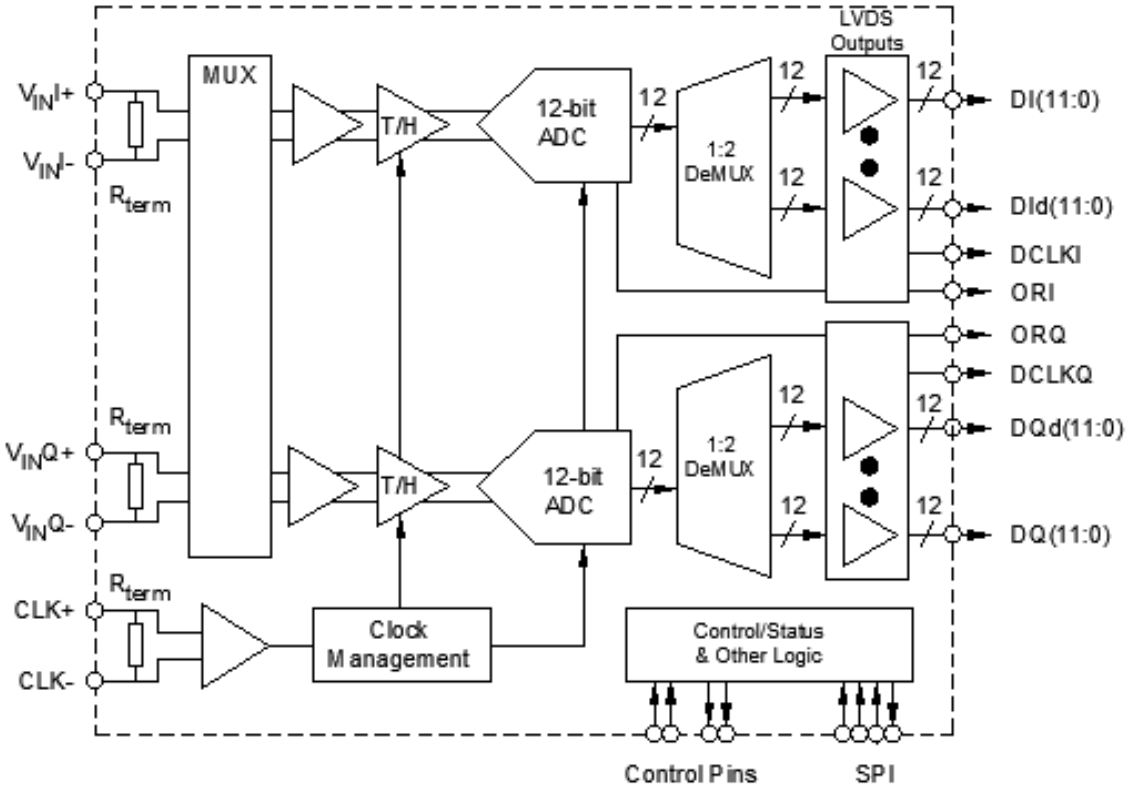


FIGURE 4. Functional block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1,2,3,4,5,6 1/	1,2,3, 1/ 2/ 4,5,6
Group A test requirements (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6 2/
Group D end-point electrical parameters (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6
Group E end-point electrical parameters (see 4.4)	1,4	1,4

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the previous electrical parameters.

TABLE IIB. Burn-in and operating life test delta parameters. 1/ 2/ 3/ T_A = +25°C.

Parameters	Symbol	Conditions	Device type	Delta limits	Limit
Power consumption	P_C	f_{CLK} = 1.6 GHz, 1:2 DEMUX MODE, NON-LSPSM, PDI = PDQ = Low	02	±0.08	W
Power consumption	P_C	f_{CLK} = 800 MHz, 1:2 DEMUX MODE, LSPSM, PDI = PDQ = Low	02	±0.05	W
Signal to noise ratio	SNR	1:2 DEMUX, NON-DES MODE, NON-ECM, NON-LSPSM, f_{CLK} = 1.6 GHz, f_{CLK} = 248 MHz, V_{IN} = -0.5 dBFS	02	±2	dB
Signal to noise ratio	SNR	1:2 DEMUX, NON-DES MODE, NON-ECM, LSPSM, f_{CLK} = 800 MHz, f_{CLK} = 248 MHz, V_{IN} = -0.5 dBFS	02	±2	dB

See footnotes at end of table.

TABLE IIB. Burn-in and operating life test delta parameters - continued. 1/ 2/ 3/ T_A = +25°C.

Parameters	Symbol	Conditions	Device type	Delta limits	Limit
Input leakage current (DES, LSPSM, CAL, TPM, NDM, FSR, DDRPh)	I_{IH}	$V_{IN} = V_A$	02	±0.3	µA
Input leakage current (SCLK, SDI, $\overline{SCS}$)	I_{IH}	$V_{IN} = V_A$	02	±0.5	µA
Input leakage current (PDI, PDQ, $\overline{ECE}$)	I_{IH}	$V_{IN} = V_A$	02	±0.3	µA
Input leakage current (DES, LSPSM, CAL, TPM, NDM, FSR, DDRPh)	I_{IL}	V_{IN} = GND	02	±0.3	µA
Input leakage current (SCLK, SDI, $\overline{SCS}$)	I_{IL}	V_{IN} = GND	02	±0.5	µA
Input leakage current (PDI, PDQ, $\overline{ECE}$)	I_{IL}	V_{IN} = GND	02	±0.5	µA

1/ Delta parameters are measured at T_A = 25°C prior to burn-in and at T_A = –55°C, +25°C, and +125°C after burn-in. The delta in table IIB parameters before and after burn in are covered in the 1000 hour Group C burn in drift analysis.

2/ 240 hour burn in Group A end point electrical parameters are covered per lot basis. 3% PDA is implemented at all post burn in temperature production tests.

3/ Delta parameters are measured on the automated test equipment (ATE) as part of the ATE program at both pre and post burn-in.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C.

4.4.4.2. Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be the maximum rated operating temperature 125°C for the latchup measurements.

f. Bias conditions shall be supply voltage at 2 V for the latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions (SEP).

b. Number of latch ups (SEL).

c. Number of occurrences (SEFI).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-08-12

Approved sources of supply for SMD 5962-12205 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F1220501VXF	3/	ADC12D1600QML
5962F1220502VXF	01295	ADC12D1620QML-SP

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243