**Designing SAR ADC Drive Circuitry**

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Part II: Input Behavior of SAR ADCs

The second of a three-part series, this TechNote examines the load that the input of a modern successive approximation register (SAR) ADC presents to external circuitry. Unlike what may be implied in a product data sheet, this input is a very dynamic load that changes as the sampling and conversion process takes place. Selecting the external charge reservoir circuitry to achieve optimal ac and dc performance, and minimize charge injection effects, is discussed.

The equivalent input of the ADS8361 (Part I http://analogzone.com/acqt0221.pdf and Fig. 1), which is representative of SAR-type ADCs. A review of the operation of these parts is relevant in order to understand their performance limitations.

The analog input signal to be measured is connected differentially to the positive VIN+ and negative VIN- inputs. The sampling and conversion of the input signal was described in detail previously.

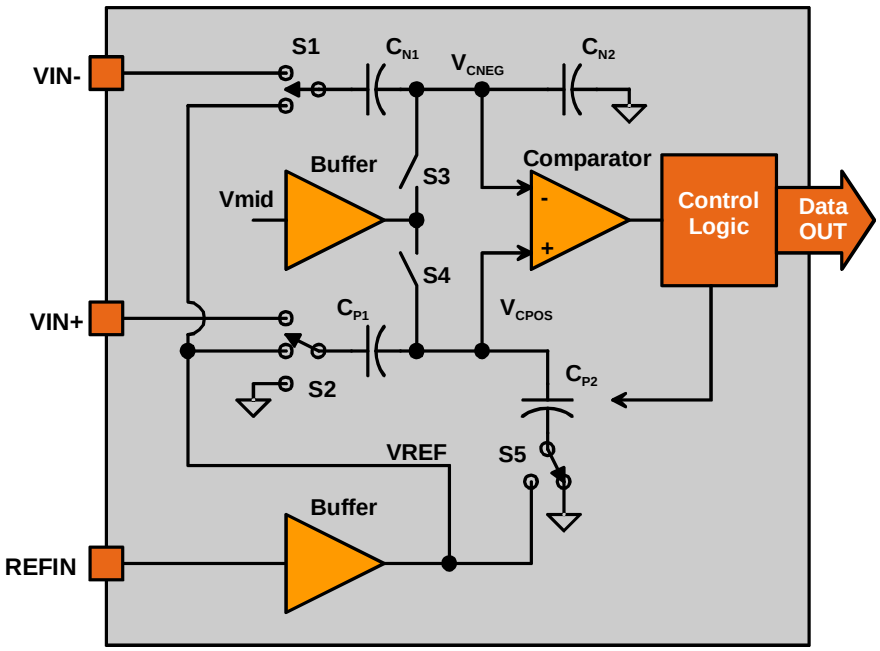



**Fig. 1: Equivalent Input Circuit SAR ADC**

As a starting point for the following analysis, several facts must be considered: at the end of the sampling period the voltages on the capacitors $C_{P1}$ and $C_{N1}$ are stable, the switches S1 and S2 will disconnect the input signal from the sampling capacitors, and the conversion process will start. The result of the conversion will be proportional to the voltage that was captured on the sampling capacitors at the end of sampling period.

## Analysis Of ADC Input During Sampling Time

In a typical application the analog signal to be measured is first conditioned by an operational amplifier, and then filtered with an R-C circuit before being applied to the ADC. In the equivalent input circuit of the ADC (see Fig. 2) sampling capacitor CSH corresponds to the sampling capacitors $C_{P1}$ or $C_{N1}$ (Fig. 1). Before switch SW1 connects CSH to the input signal, it will have an initial charge voltage V0, the result of the previous conversion process. During acquisition SW1 is closed, SW2 is open. The sampling capacitors CSH will be charged through the switch resistor RS1 and resistor R1 from the signal source. In our case the switch resistance RS1 is about 20 Ω.

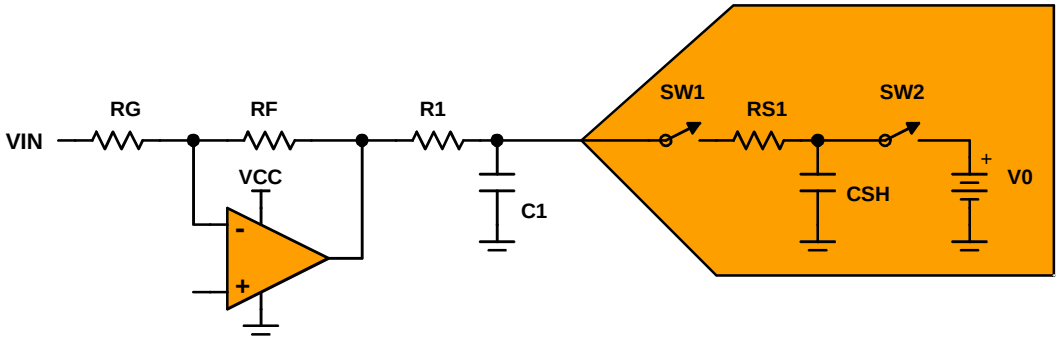



**Fig. 2: Illustrating ADC Behavior During Input Signal Sampling**

## General Analysis Of Sampling Process

While sampling CSH will be charged to the input voltage E through resistor RS1 and switch SW1. The initial charge on the sampling capacitor CSH is V0 (fig. 3).

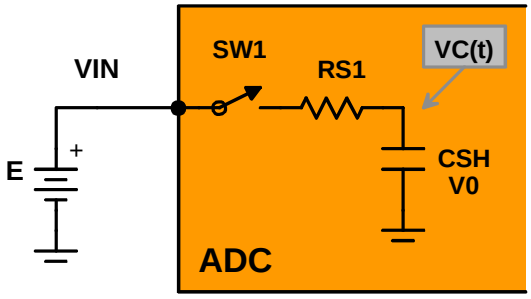



**Fig. 3: General Circuit Showing Sampling Of Input Signal**

After switch SW1 closes the charging process starts. The voltage on the sampling capacitor, denoted VC(t), can be described by Equation 1:

$$V_C(t) = V_0 + (E - V_0) \times (1 - e^{-\frac{t}{\tau}}) \qquad \text{Eq 1}$$

where, $t$ = RS1 * CSH

Our goal is to determine the acquisition time needed to charge the input capacitor to the value that is less than one-half the LSB in error with respect to the input signal. This condition is described by Equation 2:

$$E - V_C(t_{AQ}) \leqslant \frac{1}{2} LSB \qquad \text{Eq 2}$$

A plot of Equation 1 (Fig. 4) shows the voltage change across CSH after SW1 closes.

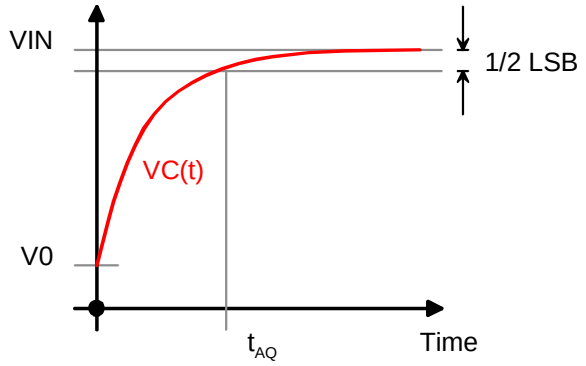



**Fig. 4: Voltage Across Sampling Capacitor During Sampling Period**

The full-scale range (FSR) of the analog input signal of the ADS8361 in single-ended mode is ±Vref around Vref. When the internal 2.5 V reference voltage is used as the reference voltage the analog input signal range is ±2.5 V around 2.5 V. So, the input signal range is from 0 V to 5 V. The difference between the most positive and most negative analog input of the converter operating range is the FSR, in this case 5 V. To analyze the worst-case situation the input signal voltage, E, from the signal source will be equal to the full-scale voltage. The ideal code width of an N-bit converter is 1LSB.

Replacing the value of 1LSB in Equation 2, it is possible to calculate the value to which the input capacitor needs to be charged at the end of the acquisition time:

$$V_C(t_{AQ}) \geqslant E \times (1 - \frac{1}{2^{N+1}}) \qquad \text{Eq 3}$$

Substituting Equation 3 into Equation 1, and assuming that this condition is satisfied at the end of the acquisition time, we get the following result:

$$E \times (1 - \frac{1}{2^{N+1}}) \leqslant V_0 + (E - V_0) \times (1 - e^{-\frac{t_{AQ}}{\tau}}) \qquad \text{Eq 4}$$

Now it is easy to calculate what value is required for *t*:

$$\tau \leqslant \frac{t_{AQ}}{\ln(\frac{E - V_0}{E} \times 2^{N+1})} \qquad \text{Eq 5}$$

Equation 5 can also be written as:

$$t_{AQ} \geqslant k \cdot \tau \qquad \text{Eq 6}$$

Using Equation 5, it is possible to calculate the coefficient k from equation 6. For different ADC resolutions, k will be different. Table 1 lists the theoretical values of k.

**Table 1. Theoretical k Values**

| Resolution of ADC [bits] | k |
|---|---|
| 8 | 5.5 |
| 10 | 6.9 |
| 12 | 8.3 |
| 14 | 9.7 |
| 16 | 11.1 |
| 18 | 12.5 |

In the case of the 16-bit ADS8361 the acquisition time must be at least 11 times greater than the RC time constant. An error margin for component variations and other errors inherent in the ADC the actual recommended factor for k can range from 13 to 18.

## Analysis Of Return Voltage At The Input To ADC

Given the SAR equivalent input circuit (Fig. 3) the values of the equivalent sampling resistor RS1 and capacitor CSH must be known. ADC manufacturers will often provide these values for their converters. What remains unknown is the initial charge V0 on the sampling capacitor at the moment when switch SW1 closes.

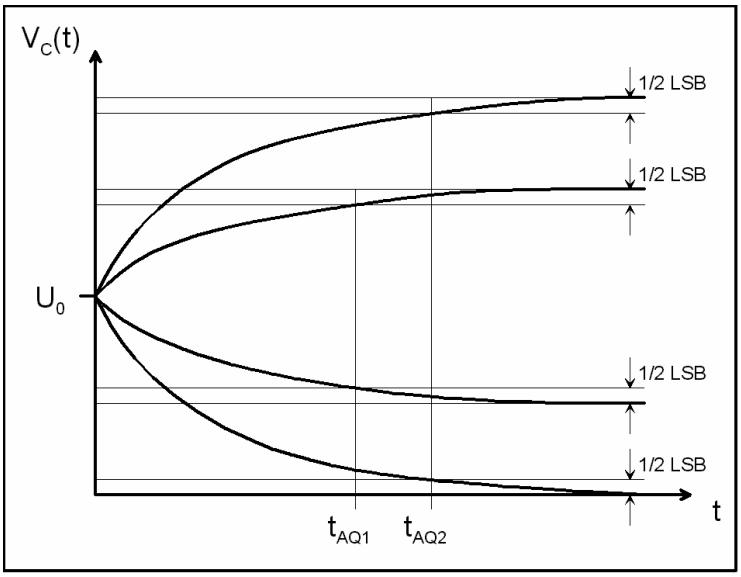



**Fig. 5: Example Of Sampling Capacitor Voltage With Constant V0**

One example of the voltage on CSH (Fig. 5) during sampling shows the initial voltage V0 on the capacitor is always the same, and equal to half the full-scale range of the input signal. It is possible to see that acquisition time $t_{AQ}$ requirements are different for different input voltages. The worst-case scenario occurs when the input signal is close to 0 or full scale. It is obvious that acquisition time $t_{AQ2}$ must be greater than $t_{AQ1}$, and is used as the initial parameter of the input filter and buffer design.

Fig. 6 presents the case where the initial voltage on the sampling capacitor is variable. When the input voltage of the previous conversion was greater than half FSR, the initial charge on the sampling capacitor is constant and equal to half the FSR. Also, when the input voltage from the previous conversion is less than half the FSR the initial charge on the sampling capacitor is variable. Note that converters can present different scenarios regarding the initial charge of the sampling capacitor, not covered in these examples.

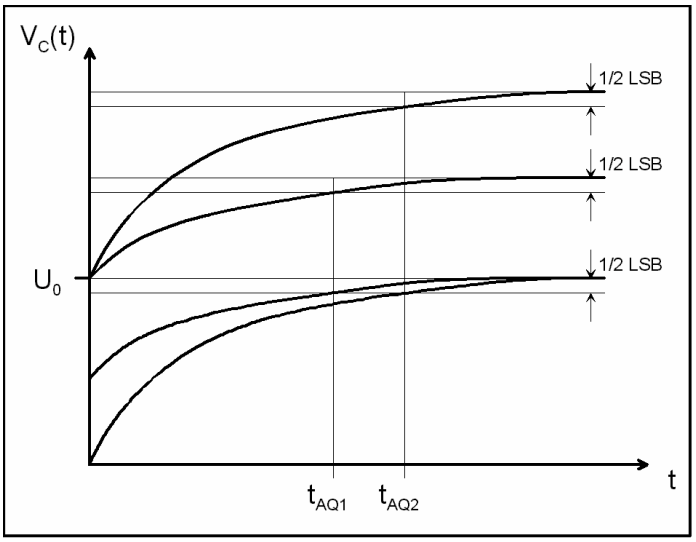



**Fig. 6: Sampling Capacitor Voltage With Variable V0**

**Determining Initial Charge On The Sampling Capacitor**

A simple technique (Fig. 7) can be used to determine the initial charge on the sampling capacitor of the converter, as a function of input voltage, with a relatively high-value resistor on the input magnifying the effect of the sampling capacitor. A signal generator connnected to the resistor applies a sinusoidal signal that covers the converter FSR.

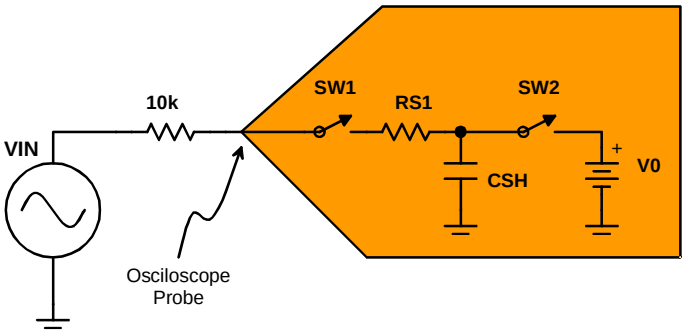



**Fig. 7: Test Circuit To Measure Initial Voltage On Sampling Capacitor**

During this measurement, special care must be taken to use a low capacitance probe. The capacitance of CSH is around 20 pF and can be easily masked by introducing a scope probe capacitor. The following measurements were made using a Tektronix P6202A ActiveFET probe with 500-MHz input bandwidth and less than 2 pF input capacitance.

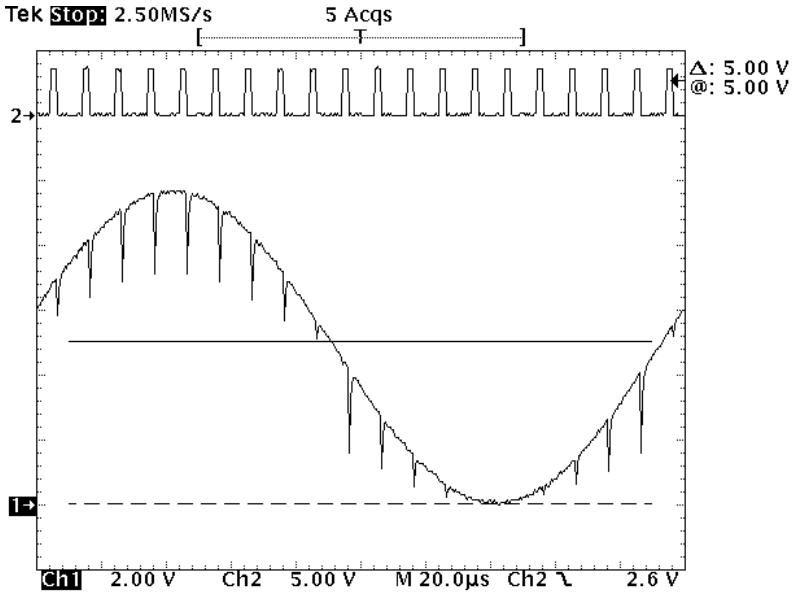



**Fig. 8: Sampling Signal And Positive Analog Input Of Converter**

Fig. 8 shows the sampling signal, or the state of the sampling switch SW1 from Fig. 7, in the top trace. The bottom trace is the capture of the analog input voltage where the initial voltage on the sampling capacitor can be seen, in this case V0 is half the FSR for the input signal that is equal to or greater than that voltage. For the input voltage that is lower, the initial charge on the input capacitor is 0 V. The charging process of the sampling capacitor is shown in more detail in Fig. 9.

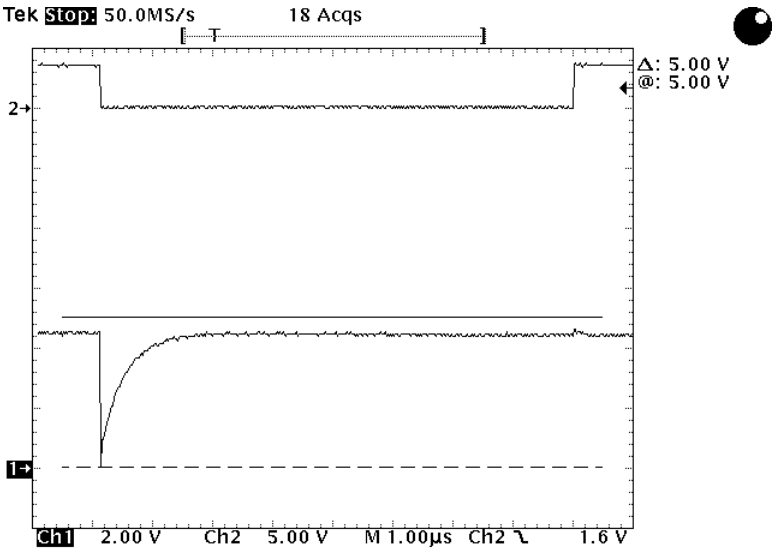



**Fig. 9: Charging Of Sampling Capacitor CSH on the Positive Analog Input**

The same converter has a completely different pattern on the negative analog input. Independent of the input voltage, the initial charge V0 of the sampling capacitor CSH on the negative input is always half the FSR. Fig. 10 shows the results of this measurement.

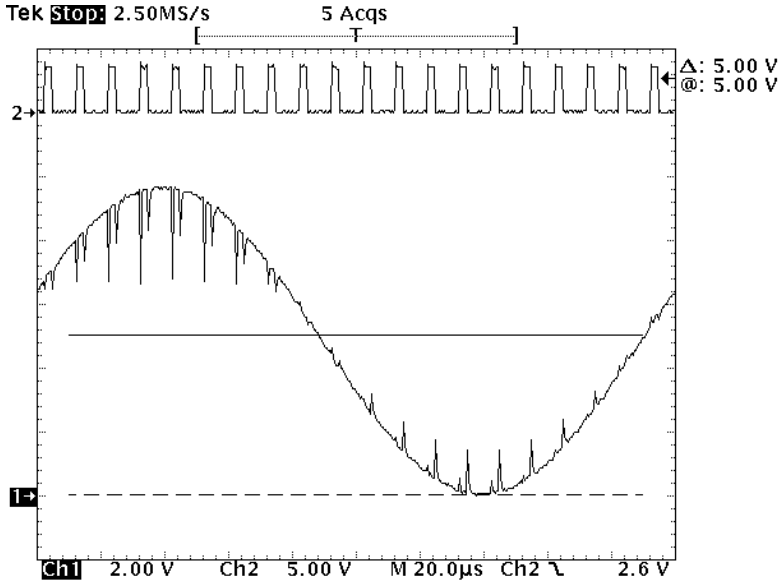



**Fig. 10: Charging Sampling Capacitor CSH On Negative Analog Input**

This charge effect is a charge injection coming out of the converter input pin during each acquisition time when switch SW1 is closed. The effect of this charge is to present a dynamic load to the driving circuitry. As can be seen from the detail (Fig. 9) the example converter causes current to flow in the input pin disturbing it for a period of about 500 ns.

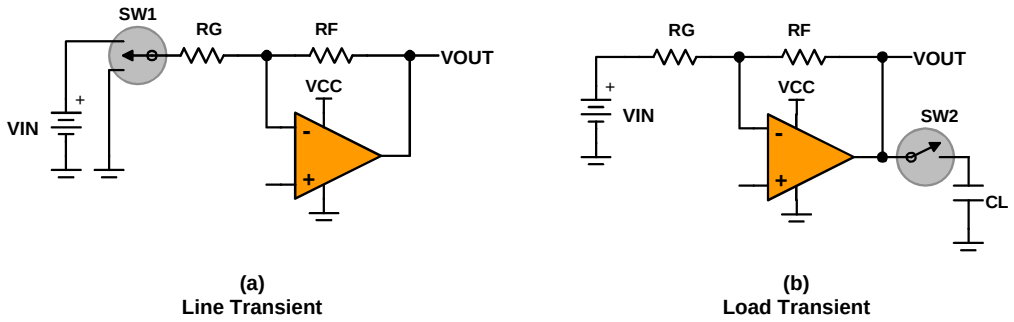



**Fig. 11: Transient Signals Op Amp Sees In Typical Data Acquisition System (a) Line From Switching Of Input Multiplexer (b) Load From Input Of ADC**

Fig. 11 is a simplification of this scenario, showing transient signals that the driving op amp must contend with. If we view the op amp like a voltage regulator, Fig. 11(a) shows the input signal as it might come from an input multiplexer, similar to a line transient to a voltage regulator. Fig. 11(b) shows the dynamic load of the ADC on the op amp, similar to a load transient to a voltage regulator, which regularly specify performance under line and load transient conditions, but op amps do not. The load on the op amp is the often difficult to handle capacitive, potentially causing output drive and stability problems.

## Choosing The External RC Filter Components

Because this dynamic load will disturb the output of the driving op amp some means of isolating the op amp from this load is required. Often this isolation would be by placing a resistor in series from the op amp to the load. But in the case of a SAR ADC the charge injection would still disturb the op amp and a path must be provided for the charge coming out of the ADC. This is done by placing a capacitor across the input of the ADC.

Placing a capacitor across the ADC input creates a simple RC circuit in front of the ADC. Naturally, this RC circuit is a low-pass filter, and can be used to limit the bandwidth of the signal presented. Without this external RC filter the input bandwidth of the ADS8361 is limited only by RS1 and CSH (Fig. 3), so the input bandwidth alone would be $1/(2\pi*20\ \Omega*25\ pF)$ or close to 320 MHz; for a 500-ksample/s converter, this wide bandwidth serves only to add noise into the signal, even after the signal has been appropriately band-limited by the system anti-aliasing filter. Since the RC is already needed to help isolate the op amp from the dynamic load, we can also use it to limit the signal bandwidth, thereby preserving the converter's SNR.

Capacitors have a voltage-dependent characteristic, meaning that capacitance changes with the voltage applied. For the ADC input sampling capacitor CSH this voltage coefficient is apparent (Fig. 12).

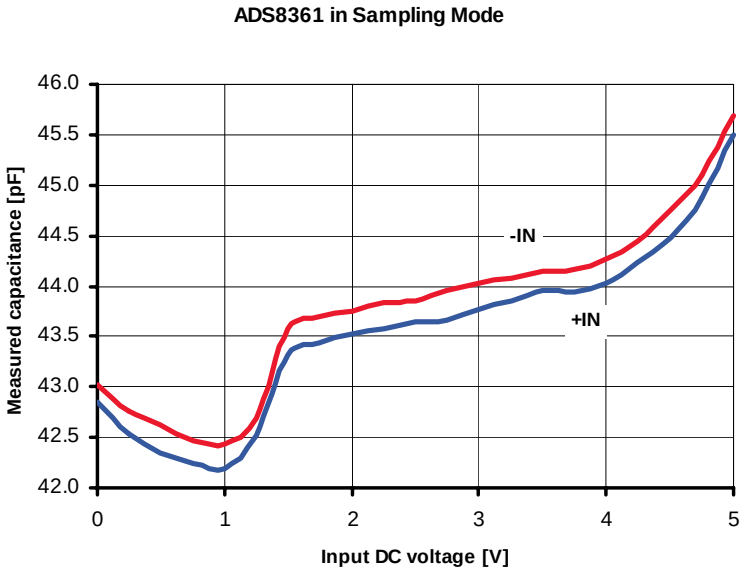
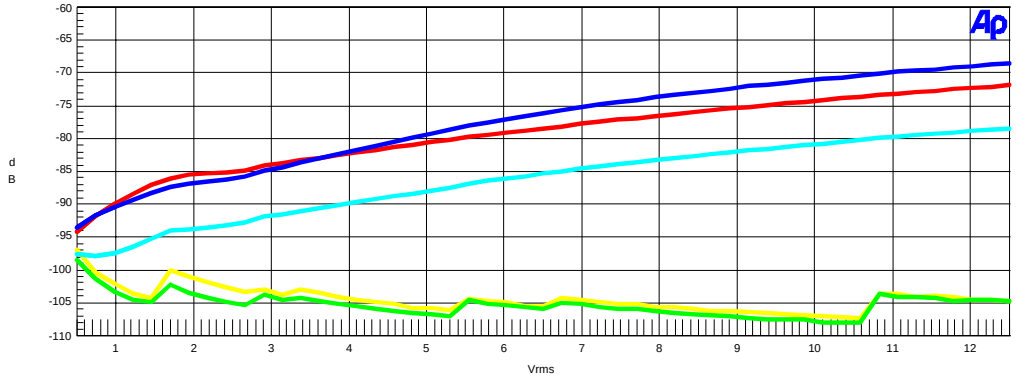



**Fig. 12: Voltage-Dependent Characteristic Of CSH**

An equation that describes this change in one region of the voltage curve is $C = C_0 (1 + KV)$, where $C_0$ is the nominal capacitance, V is the voltage across the capacitance, and K is the voltage coefficient of the capacitor. This voltage-dependent capacitance causes the current necessary to charge the capacitance to vary with voltage (in addition to frequency). This current travels through the ADC driving impedance creating a voltage drop error, which again varies with voltage. Since it is voltage dependent, it creates a

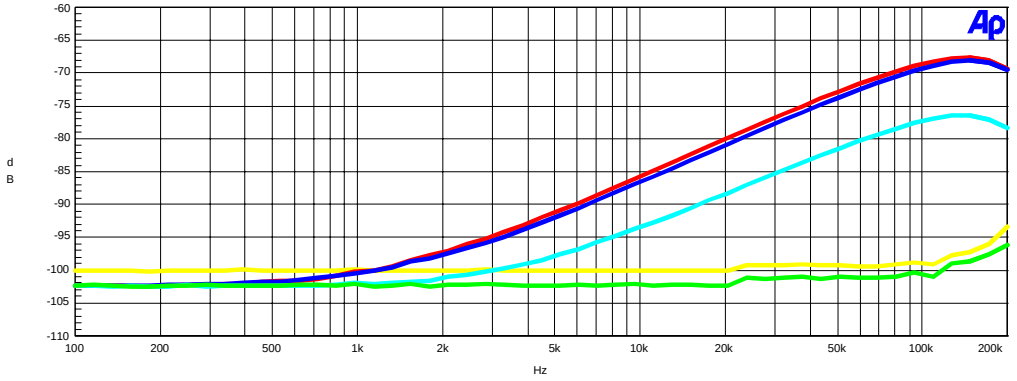
non-linear error. For a sine wave this error contains harmonics since it originates as a current charging a capacitance: non-existent at dc growing larger with frequency.

One other function of the external RC circuit is to use a highly-stable external capacitor to minimize the effects of the internal CSH capacitive voltage coefficient. This function requires that the external capacitor be of a value much larger than CSH and have a low voltage coefficient, a condition requiring the selection of a suitable dielectric. Fig. 13 shows the performance of different dielectrics versus voltage and frequency. For best results silver-mica or C0G capacitors should be used; X7R, Z5U and other types show significant voltage and frequency dependency, and will result in poor dynamic performance with a degradation in the resulting total harmonic distortion (THD).




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Yellow | Solid | 1 | Anlr.THD+N Ratio | Left | C = 0 |
| 2 | 1 | Red | Solid | 1 | Anlr.THD+N Ratio | Left | C1 |
| 3 | 1 | Blue | Solid | 1 | Anlr.THD+N Ratio | Left | C2 |
| 4 | 1 | Cyan | Solid | 1 | Anlr.THD+N Ratio | Left | C3 |
| 5 | 1 | Green | Solid | 1 | Anlr.THD+N Ratio | Left | C4 |

R = 100 ohm, C = 3.3 nF, f = 10 kHz, f(-3dB) = 482 kHz




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
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| 1 | 1 | Yellow | Solid | 1 | Anlr.THD+N Ratio | Left | C = 0 |
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| 3 | 1 | Blue | Solid | 1 | Anlr.THD+N Ratio | Left | C2 |
| 4 | 1 | Cyan | Solid | 1 | Anlr.THD+N Ratio | Left | C3 |
| 5 | 1 | Green | Solid | 1 | Anlr.THD+N Ratio | Left | C4 |

R = 100 ohm, C = 3.3 nF, Vp-p = 5V f(-3dB) = 482 kHz

**Fig. 13: Capacitor Dielectric Effects on THD+N Vs (top) Voltage (lower) Frequency Green Silver Mica And C0G; Yellow Signal Generator Unfiltered; Light Blue X7R; Dark Blue Y5V; Red Z5U**

So, the values of the external RC filter components (R1 and C1 from Fig. 2) can be chosen by following some guidelines. First, the value of C1 should be at minimum greater than 20 times CSH, and either silver mica or C0G dielectric type. This capacitor value will allow the effects of the voltage coefficient of the internal sampling capacitor , CSH, to be minimized. For the ADS8361, with CSH equal to 25 pF, this means that C1 should be larger than 500 pF.

To choose the resistor, R1, the time constant of the RC circuit, $\tau_{fil}$, must be considered. Referring to Equation 6, we see that $\tau_{fil}$ depends on the acquisition time $t_{AQ}$ and the converter resolution as shown in Table 1. For a 16-bit converter $\tau_{fil}$ must be set so that at least 11 time constants are allowed within the converter's operating acquisition time. Assuming that $t_{AQ}$ is 5 µs and C1 is 1 nF, then R1 can be determined from:

$$\tau = R1 * C1 \leq \frac{t_{(AQ)}}{k} = \frac{5\,\mu s}{12} = 416\,ns$$

So R1 must be less than 416 Ω for C1 = 1 nF.

## Conclusion

The analysis has shown the dynamic and nonlinear nature of the load presented by the ADC analog input to the driving op amp. A simple RC circuit will minimize the impact of this dynamic load on the driving op amp. In addition it will limit the noise bandwidth presented to the ADC and further compensates for the nonlinear behavior of the input sampling capacitor. Criteria for the minimum requirements for the RC component values have been established. However, finding the optimum values for a specific application will require creating a test methodology for best results. This methodology will be presented in Part III of this TechNote series.

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