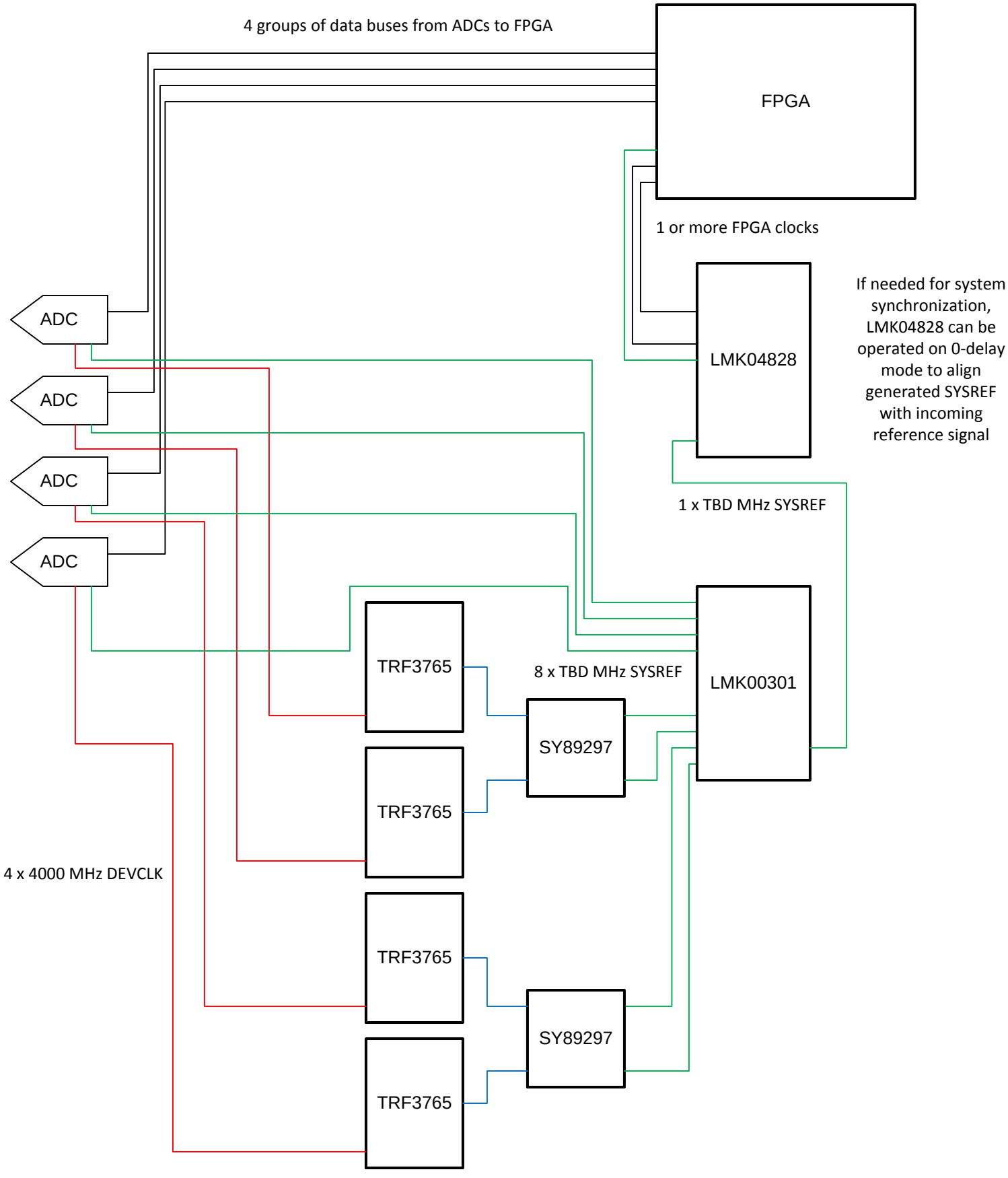
4 groups of data buses from ADCs to FPGA
FPGA
1 or more FPGA clocks
LMK04828
If needed for system synchronization, LMK04828 can be operated on 0-delay mode to align generated SYSREF with incoming reference signal
ADC
ADC
ADC
ADC
1 x TBD MHz SYSREF
LMK00301
8 x TBD MHz SYSREF
TRF3765
TRF3765
TRF3765
TRF3765
SY89297
SY89297
4 x 4000 MHz DEVCLK