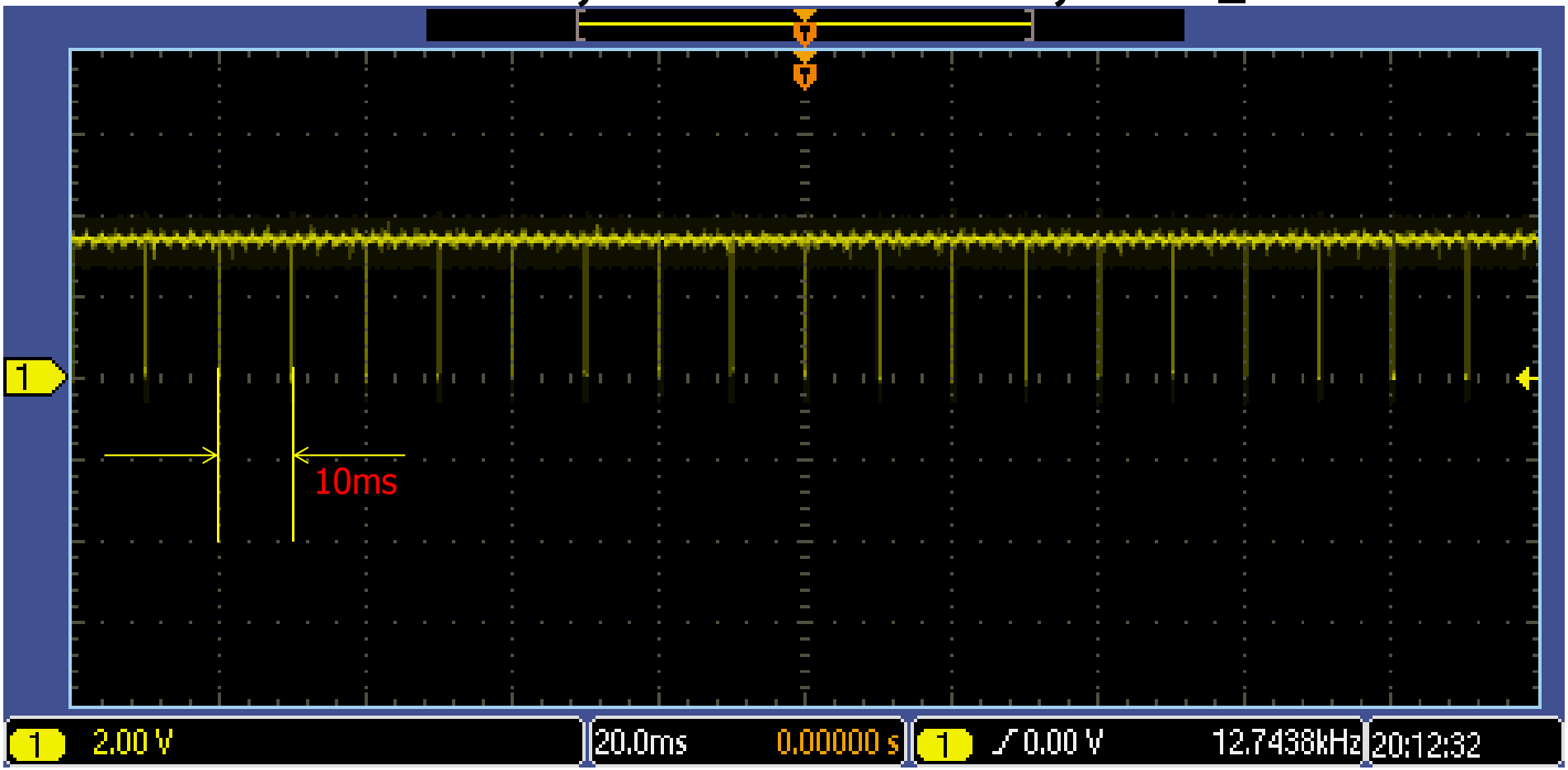
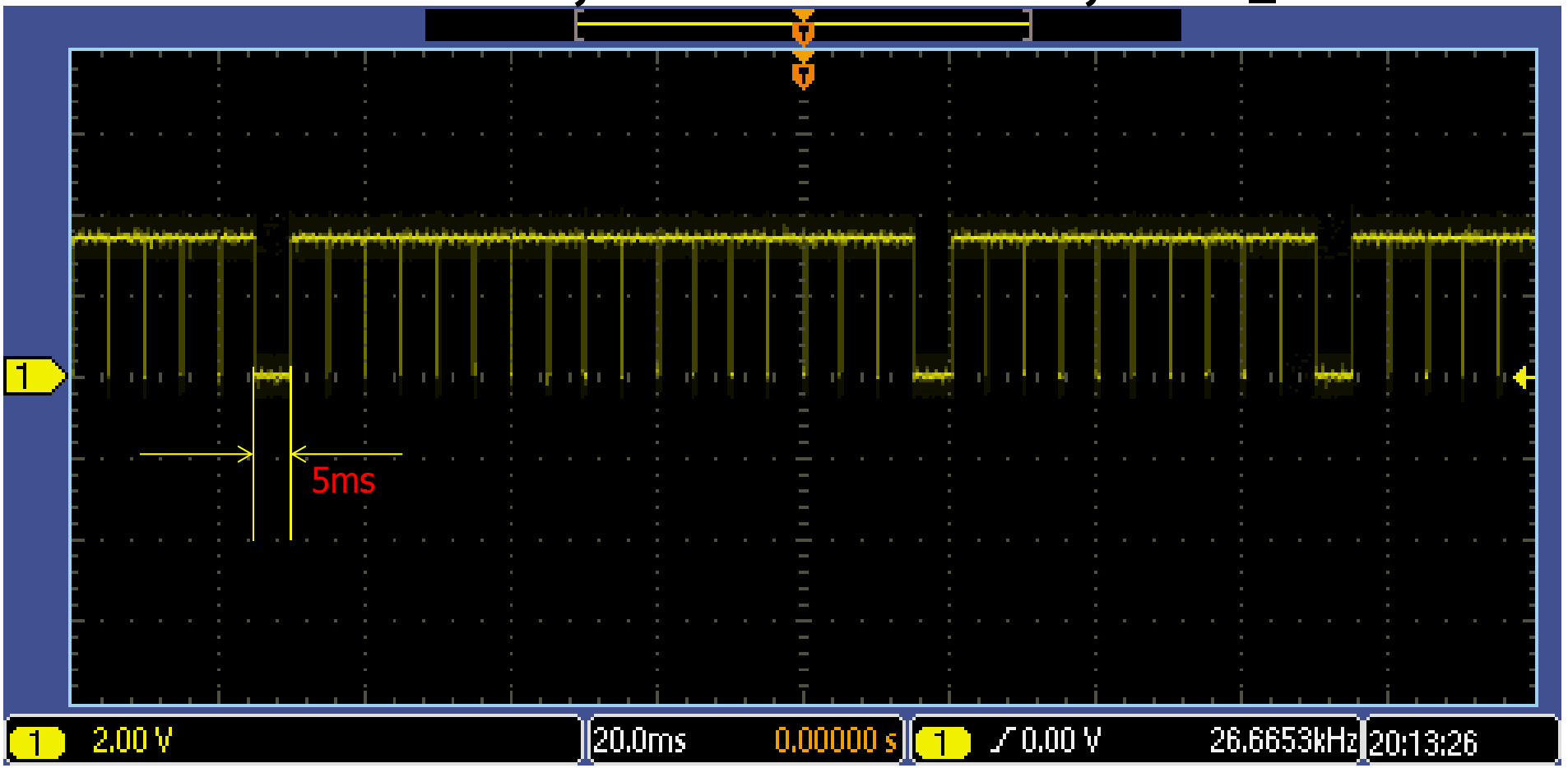
<DRDY – in case of
Data rate 100SPS, fclkin=7.68MHz, Num_Ave=300>



In this case, output data is outputted normally.
And then, DRDY signals operates at even intervals 10ms.

＜DRDY – in case of
Data rate 200SPS, fclkin=3.072MHz, Num_Ave=60＞



In this case, output data is not outputted normally.
And then, DRDY signals keeps Low at odd intervals 5ms.
We think that caluculation formula of data rate is correct, and input clock range is also correct. Could you give some advice?
-Data rate=(fclkin/256)×(1/Num_Ave)=200SPS

Master clock rate	External crystal between XTAL1 and XTAL2	2	7.68	10	MHz
	External oscillator driving CLKIN	0.1	7.68	10	MHz