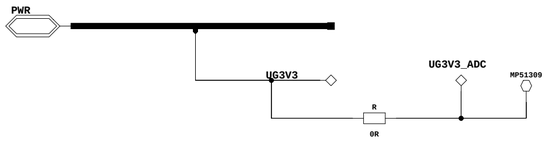
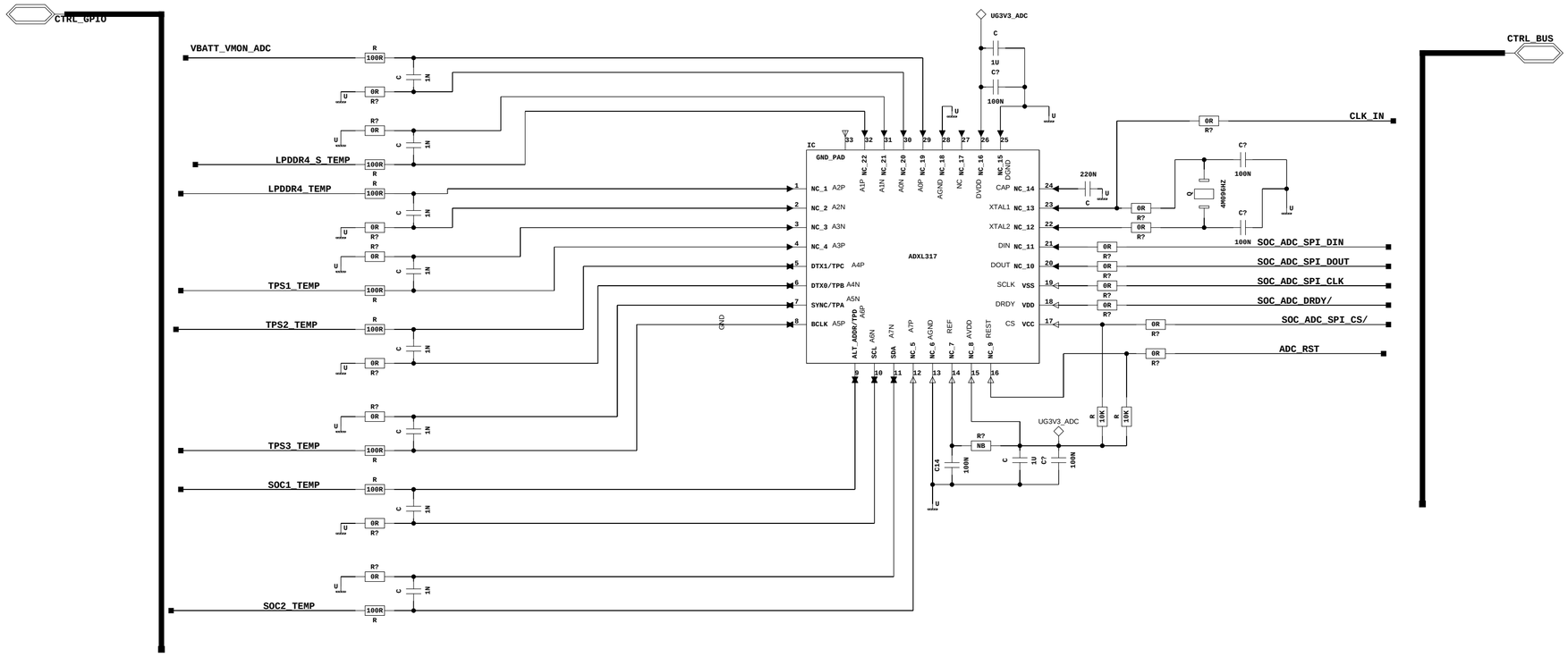


Note: The frequence of SPI_CLK is the same as clk _in .

Note: CLK_IN recommende 4.096MHZ, gain used 1., max is 8.196Mhz

Note: desgin used internal REF 1.2V, so adc input less than 1.2V
Note: Do not place any capacitance on REFIN if the current-detect mode is used.



Rev.	type of change	change-no.	date of change	auth.	checked

	date	name
created		
checked		

schematic	Sheet	Sheets of	Sample
Fub19886	1	1	
substitute for: / substitute by:	Type	Variant	Part Number