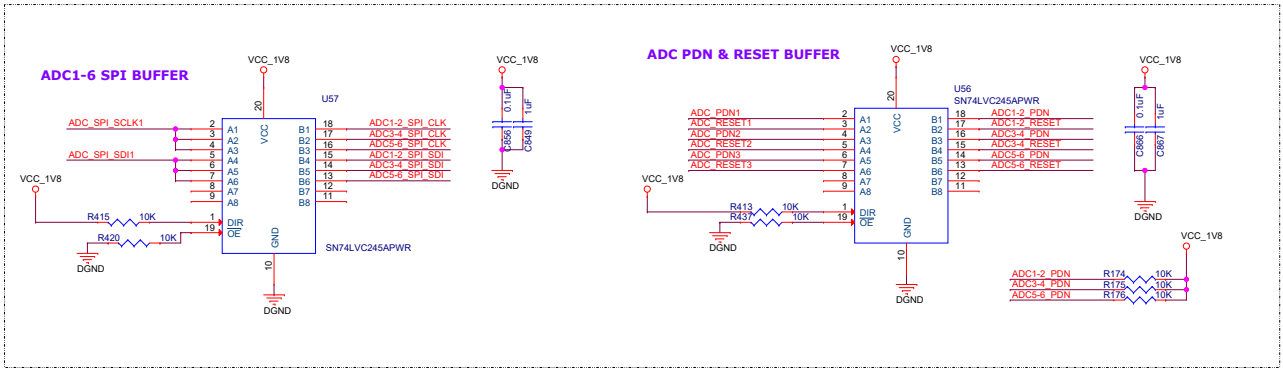


# ADC BUFFERS



## SPI CLK AND SDI TO ADC's

- ADC1-2 SPI CLK >>> ADC1-2\_SPI\_CLK [4,5]
- ADC1-2 SPI SDI >>> ADC1-2\_SPI\_SDI [4,5]
- ADC3-4 SPI CLK >>> ADC3-4\_SPI\_CLK [6,7]
- ADC3-4 SPI SDI >>> ADC3-4\_SPI\_SDI [6,7]
- ADC5-6 SPI CLK >>> ADC5-6\_SPI\_CLK [8,9]
- ADC5-6 SPI SDI >>> ADC5-6\_SPI\_SDI [8]

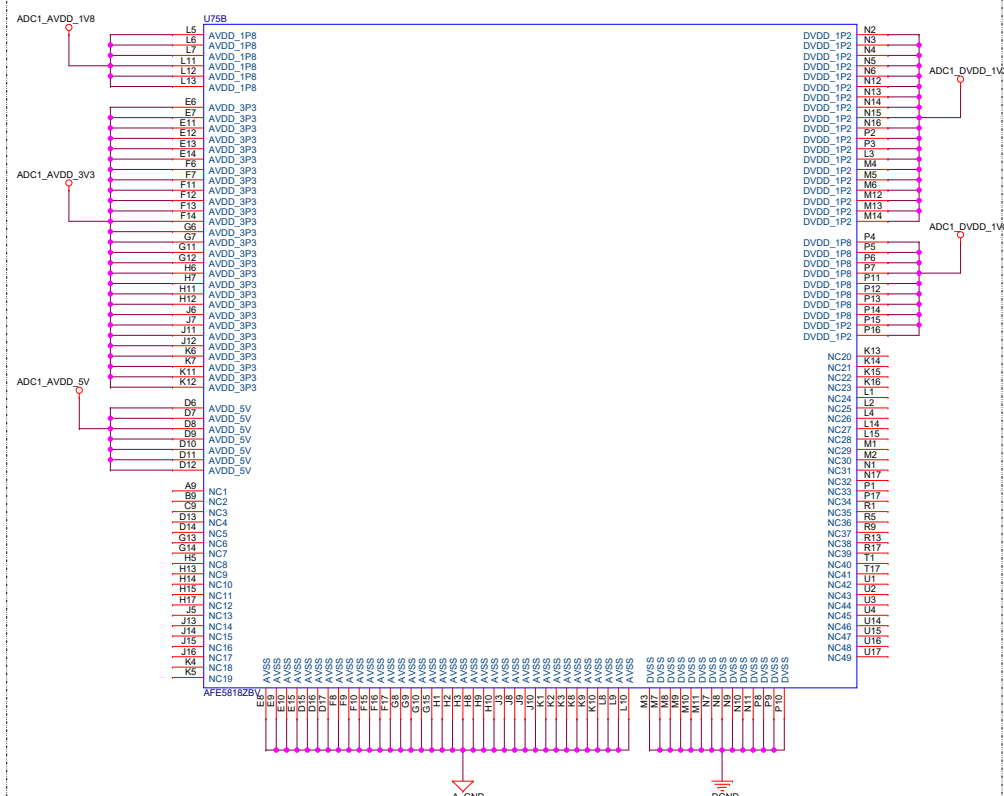
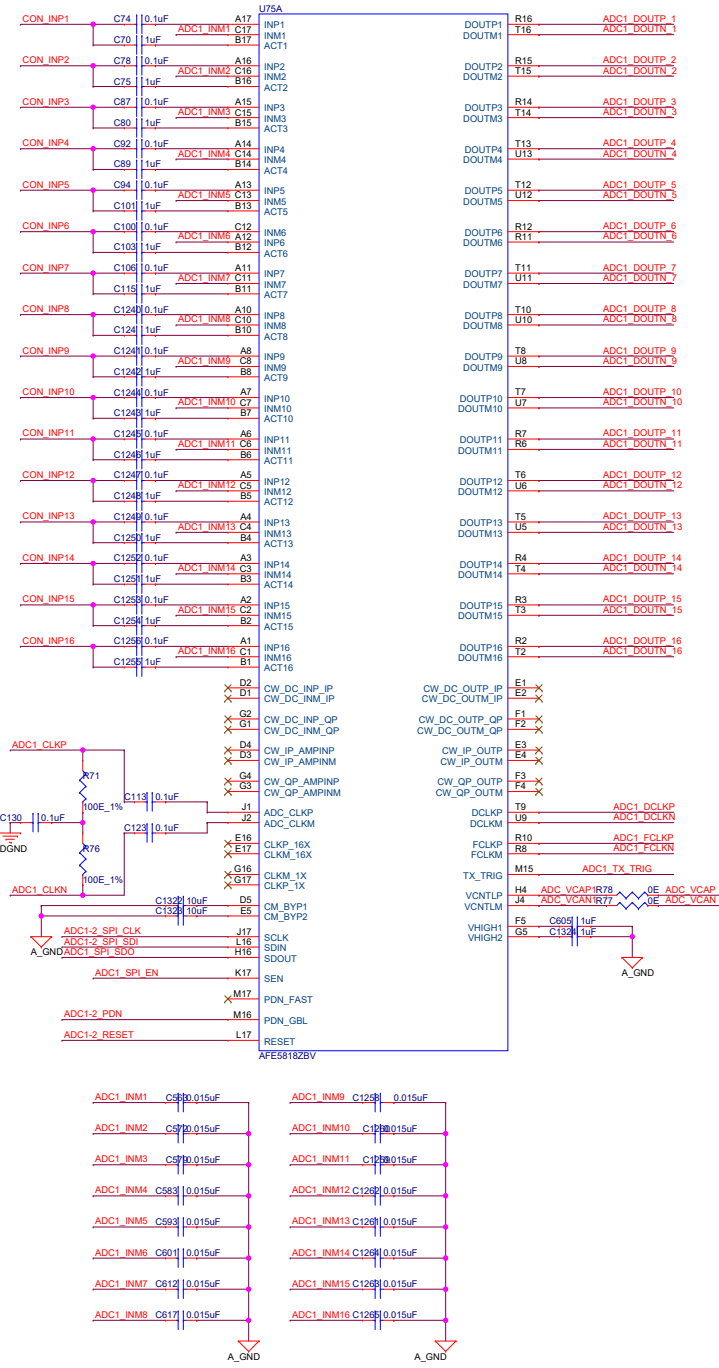
## RESET AND PDN TO ADC's

- ADC1-2 RESET >>> ADC1-2\_RESET [4,5]
- ADC1-2 PDN >>> ADC1-2\_PDN [4,5]
- ADC3-4 RESET >>> ADC3-4\_RESET [6,7]
- ADC3-4 PDN >>> ADC3-4\_PDN [6,7]
- ADC5-6 RESET >>> ADC5-6\_RESET [8,9]
- ADC5-6 PDN >>> ADC5-6\_PDN [8,9]
- ADC\_PDN1 >>> ADC\_PDN1 [13]
- ADC\_RESET1 >>> ADC\_RESET1 [13]
- ADC\_PDN2 >>> ADC\_PDN2 [13]
- ADC\_RESET2 >>> ADC\_RESET2 [13]
- ADC\_PDN3 >>> ADC\_PDN3 [13]
- ADC\_RESET3 >>> ADC\_RESET3 [13]

## ADC SPI LINES

- ADC\_SPI\_SCLK1 >>> ADC\_SPI\_SCLK1 [13]
- ADC\_SPI\_SDI1 >>> ADC\_SPI\_SDI1
- LS1 [14]
- LS2 [14]
- LS3 [14]
- LS4 [14]

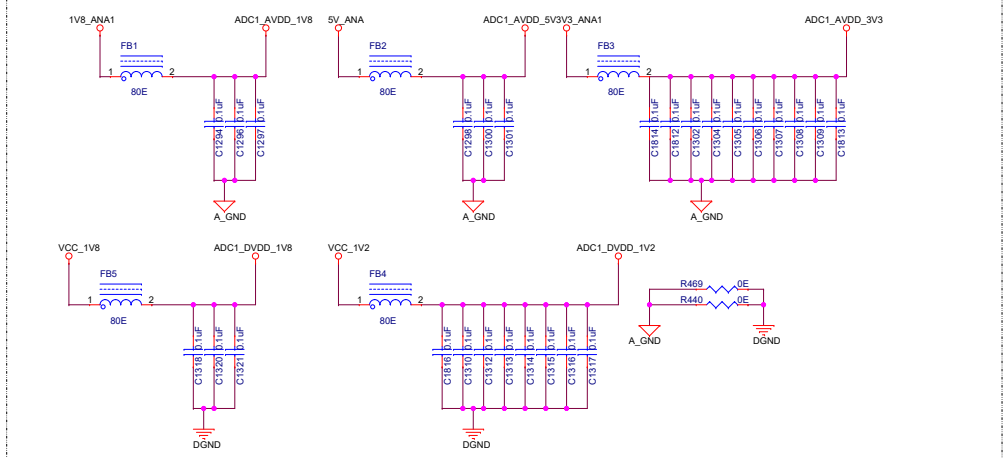
# ADC1



### ADC1 INPUTS

CON_INP1	CON_INP1 (10,26)
CON_INP2	CON_INP2 (10,26)
CON_INP3	CON_INP3 (10,26)
CON_INP4	CON_INP4 (10,26)
CON_INP5	CON_INP5 (10,26)
CON_INP6	CON_INP6 (10,26)
CON_INP7	CON_INP7 (10,26)
CON_INP8	CON_INP8 (10,26)
CON_INP9	CON_INP9 (10,26)
CON_INP10	CON_INP10 (10,26)
CON_INP11	CON_INP11 (10,26)
CON_INP12	CON_INP12 (10,26)
CON_INP13	CON_INP13 (10,26)
CON_INP14	CON_INP14 (10,26)
CON_INP15	CON_INP15 (10,26)
CON_INP16	CON_INP16 (10,26)

## ADC1 DECAPS



### ADC1 OUTPUTS

ADC1_DOUTP_1	ADC1_DOUTP_1 (12)
ADC1_DOUTM_1	ADC1_DOUTM_1 (12)
ADC1_DOUTP_2	ADC1_DOUTP_2 (12)
ADC1_DOUTM_2	ADC1_DOUTM_2 (12)
ADC1_DOUTP_3	ADC1_DOUTP_3 (12)
ADC1_DOUTM_3	ADC1_DOUTM_3 (12)
ADC1_DOUTP_4	ADC1_DOUTP_4 (12)
ADC1_DOUTM_4	ADC1_DOUTM_4 (12)
ADC1_DOUTP_5	ADC1_DOUTP_5 (12)
ADC1_DOUTM_5	ADC1_DOUTM_5 (12)
ADC1_DOUTP_6	ADC1_DOUTP_6 (12)
ADC1_DOUTM_6	ADC1_DOUTM_6 (12)
ADC1_DOUTP_7	ADC1_DOUTP_7 (12)
ADC1_DOUTM_7	ADC1_DOUTM_7 (12)
ADC1_DOUTP_8	ADC1_DOUTP_8 (12)
ADC1_DOUTM_8	ADC1_DOUTM_8 (12)
ADC1_DOUTP_9	ADC1_DOUTP_9 (12)
ADC1_DOUTM_9	ADC1_DOUTM_9 (12)
ADC1_DOUTP_10	ADC1_DOUTP_10 (12)
ADC1_DOUTM_10	ADC1_DOUTM_10 (12)
ADC1_DOUTP_11	ADC1_DOUTP_11 (12)
ADC1_DOUTM_11	ADC1_DOUTM_11 (12)
ADC1_DOUTP_12	ADC1_DOUTP_12 (12)
ADC1_DOUTM_12	ADC1_DOUTM_12 (12)
ADC1_DOUTP_13	ADC1_DOUTP_13 (12)
ADC1_DOUTM_13	ADC1_DOUTM_13 (12)
ADC1_DOUTP_14	ADC1_DOUTP_14 (12)
ADC1_DOUTM_14	ADC1_DOUTM_14 (12)
ADC1_DOUTP_15	ADC1_DOUTP_15 (12)
ADC1_DOUTM_15	ADC1_DOUTM_15 (12)
ADC1_DOUTP_16	ADC1_DOUTP_16 (12)
ADC1_DOUTM_16	ADC1_DOUTM_16 (12)

**Control Signal Connections:**

- ADC1\_DCLKP: J2
- ADC1\_DCLKM: J2
- ADC1\_FCLKP: R10
- ADC1\_FCLKM: R8
- ADC1\_TX\_TRIG: M15
- ADC1-2\_SPI\_CLK: J17
- ADC1-2\_SPI\_SDI: L16
- ADC1-2\_SPI\_SDO: L18
- ADC1-2\_PDN: M17
- ADC1-2\_RESET: L17

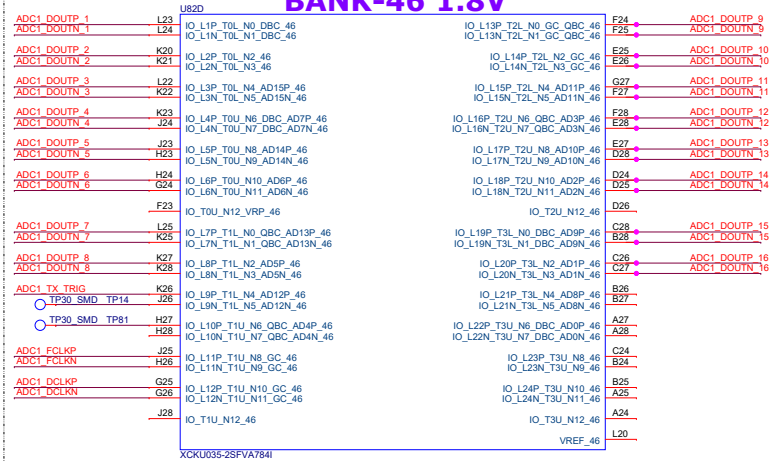
REV NO.	NATURE OF CHANGE	APPROVED BY	DATE	Title	Rev
				<b>ADC1 INTERFACE</b>	

**Mistral Solutions [P] Ltd.**  
 #60 Adarsh regent, 100 Feet Ring Road, Domlur Extension  
 Bangalore 560 071, Ph : +91-80-30912600, Fax : +91-80-2535 6444

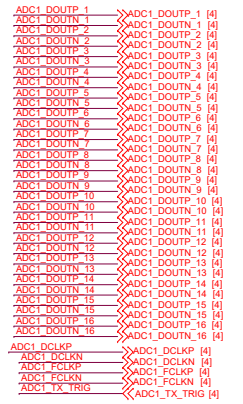
Drawn by: AKSHAY SY	Approved by: SRIDHAR TS	Size	Document Number	A	
Date: Monday, April 15, 2024	Date: Thursday, August 01, 2024	C	MS_PODS_GFS_DAO&PROC_SCH_REVA		
Design file path:		Date: Wednesday, July 31, 2024	Sheet	4	of 26

# FPGA-ADC 1

## BANK-46 1.8V

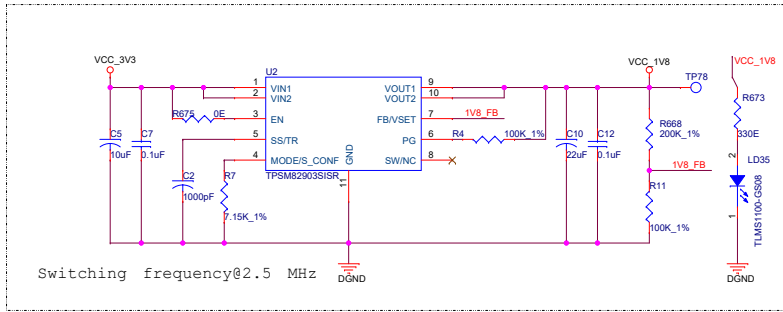


### ADC1 OUTPUTS

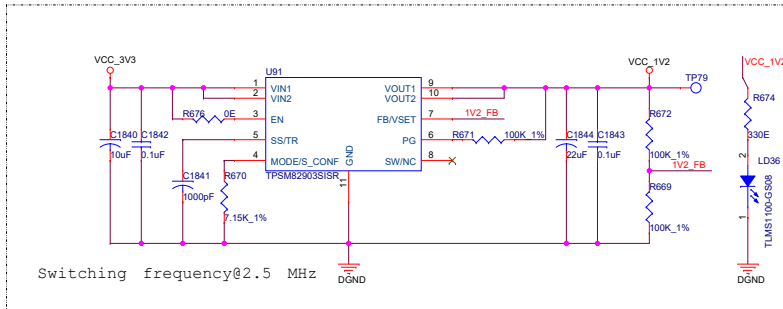



REV NO.	NATURE OF CHANGE	APPROVED BY	DATE	<b>Mistral Solutions [P] Ltd.</b> #60 Adarsh regent, 100 Feet Ring Road, Domlur Extension Bangalore 560 071, Ph : +91-80-30912600, Fax : +91-80-2535 6444	Title	<b>FPGA-ADC1,2,3,4</b>	
					Drawn by: AKSHAY SY Date: Monday, April 15, 2024 Design file path:	Approved by: SRIDHAR TS Date: Thursday, August 01, 2024	Size C
					Date: Wednesday, July 31, 2024	Sheet	12 of 26

### 3.3V to 1.8V@2A GENERATION

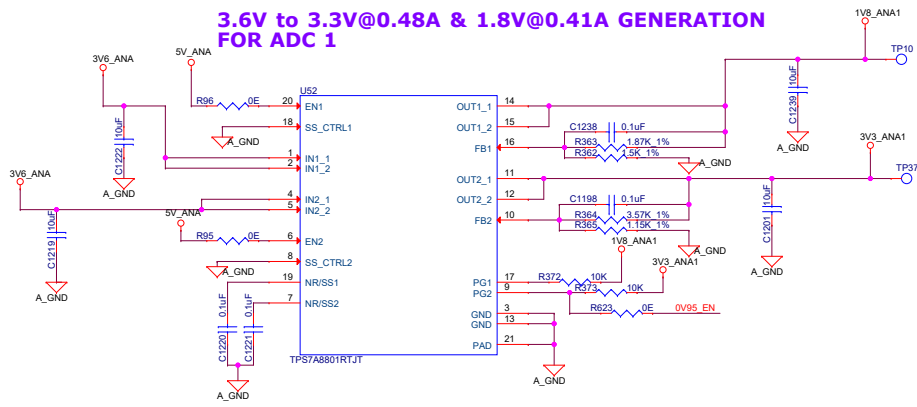



### 3.3V to 1.2V@2A GENERATION



REV NO.	NATURE OF CHANGE	APPROVED BY	DATE	 <b>Mistral Solutions [P] Ltd.</b> #60 Adarsh regent,100 Feet Ring Road, Domlur Extension Bangalore 560 071, Ph : +91-80-30912600, Fax :+91-80-2535 6444		Title	<b>DIGITAL POWER GENERATION</b>	
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						Date: Wednesday, July 31, 2024	Sheet 24 of 26	

### 3.6V to 3.3V@0.48A & 1.8V@0.41A GENERATION FOR ADC 1



REV NO.	NATURE OF CHANGE	APPROVED BY	DATE	 <b>Mistral Solutions [P] Ltd.</b> #60 Adarsh regent, 100 Feet Ring Road, Domlur Extension Bangalore 560 071, Ph : +91-80-30912600, Fax : +91-80-2535 6444	Title	<b>ANALOG POWER GENERATION</b>
				Drawn by: AKSHAY SY Date: Monday, April 15, 2024 Design file path:	Approved by: SRIDHAR TS Date: Thursday, August 01, 2024	Size: Document Number C: MS_PODS_GFS_DAQ&PROC_SCH_REVA Date: Friday, July 26, 2024
						Rev: A Sheet 25 of 26