AFE7070 TEST PROCEDURE

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1 AFE-TEST(Dual Input Clock Mode)

We followed the test procedure for AFE given on page 8 of user_guide_AFE_TSW .

- 1. Connect the AFE7071 EVM to the computer via USB cable.
- 2. Connect 6-V adapter to J9.
- 3. Launch the AFE7071EVM GUI and click Reset USB Port.
- 4. Connect the signal generator to the J4 connector (EXT VCXO) on the AFE7071 EVM. Set the frequency of the signal generator to 130 MHz and amplitude to 0 dBm.



Figure 1: EXT VCXO

5. Connect LO signal from the second signal generator to the J10 connector (LO IN). Set the frequency of the signal generator to 2.1 GHz and amplitude to 5 dBm.



Figure 2: LO Signal

6. Connect J3 (RFOUT) to the spectrum analyzer.

| | OHDE&SC | HWARZ | FSL · SPE | CTRUM ANALYZER · | 9 kHz 3 GHz | | |
|----------|--|---|------------|------------------------------|----------------------|--|--|
| FILE | er1 GHZ Att 30 dB Ref 10.00 dBm | 28W 100 kHz VBW 300 kHz * SWT 205ms | M1[1] | -3.12 dBm 2.000000000 GHz | Select | | |
| SETUP 15 | 0 dBm | | | | Peak | | |
| PRINT | -10 dBm | | | | Next Peak | | |
| HELP | -20 dBm | | | | Next Peak Mode | | |
| | -30 dBm | | | | < abs > | | |
| MODE | -50 dBm | | | | = Mkr Freq | | |
| MENU | -60 dBm | vinasoa wa guny | minister | and the second street | Ref Lvl = Mkr Lvl | | |
| | -80 dBm | ++ | \vdash | | More & | | |
| | CF 2.0 GHz | | | Span 54.3 MHz | | | |
| | | | the second | | | | |

Figure 3: RF_OUT

- 7. Connect the TSW1400 to the computer via USB cable.
- 8. Connect the J1 (CMOS_INTERFACE) connector on the TSW1400 to AFE7071 EVM's J8 connector. Make sure pin 1 of the J1 connector is aligned with pin 1 on the J8 connector before connecting.
- 9. Connect the J7 (CMOS_CLK) on TSW1400 to J5 (CDC OUT) connector on AFE7071 EVM.
- 10. Connect 5-V adapter to J12 on TSW1400.
- 11. Turn the switch (SW7) to the On position.

TSW1400 Quick-Start Operation

After launching HSDC PRO software we done the following settings as per the user manual.

- 1. Select the DAC tab.
- 2. Select CMOS_AFE7070 from the top left drop-down menu.
- 3. Set the Data rate to "65" MHz and DAC Option to Offset Bin.
- 4. Set I/Q Multitone Generator \rightarrow Tone BW to "1M", set (of tones) to "2", and Tone Center to "5M".
- 5. Under Tone selection, select Complex.
- 6. Click the Create Tones button.
- 7. Click Send.



Figure 4: TSW-1400 Settings Screen shot

AFE7070 Settings Contd..

- In the Clock Settings section, we set the clock mode to Dual Input Clock.
- Since we are not using LVDS we disabled it.



Figure 5: AFE7070 Settings Screen Shot

CDCM7005 Settings

- We done the following modifications in the Output Options section of CDCM7005 as per the user manual.
 - $\diamond~Y1~(AFE7070's~CLK_JO)$ must be LVCMOS, with Y1A set to active rather than 3-state.
 - ◊ Y3 (AFE7070's DACCLK) must be LVPECL, with both Y3A and Y3B set to active.
 - $\diamond\,$ Y4 (CDC Out) must be LVCMOS, with Y4A set to active.

| AFE7070 CDCM70 | 05 | | | | Reset | USB Port | | | Exit | 1 AFE70 | 70 Rec | irter Data |
|-------------------|-------------|------------------------------------|--------------------|------------|----------------|--------------------|----------|-----------|---|------------|-----------------|----------------|
| | | | CDCM7005 Operation | Buffer Mod | e | | ⊖ Se | nd All | | x00 | xB0 | 1011 0000 |
| Advanced Options | | Clock & PLL Options | | | Output Options | | | | x02 x03 0000 0011 x03 x10 0001 0000 x04 x0F 0000 1111 | | | |
| Progr. Delay M | 0ps v | Lock Divised | Clock Settings | | | Y0 Outp | ut (Unus | ied) | | x05 x06 | x00 x80 | 1000 0000 |
| | | Digital | M & N Selection | Auto | | 1 | × | 3-state | V YOA | x07 x08 | x13 x00 | 0001 0011 0000 |
| Progr. Delay N | Ups V | Ref. Clk Manual | Ref. Freq (MHz) | 10 | ¥ A | LVCM | | 3+state | YOB YOB | x09 | x7A | 0111 1010 |
| Lock Detect Cycle | 64 🗸 | Ref.Detection on | VCXO Freq (IVIHZ) | 905.04 | ¥. | 1 Outp | ut (AFE/ | 0/U S CLK | 10) | x0A x0B | XEA | 1110 1010 |
| Lock Window | ±8ns 🗸 | | PLL Settings | | | IVCM | | Sustate | V VIB | x0C x0D | x45 x1A | 0100 0101 |
| Fast Lock r | mode off | Status_Ref | M Divider | 125 | | V2 Outer | | | V 110 | XOE | x16 | 0001 0110 |
| | | Status_VCXO Me_Det_voxo | N Divider | 1536 | | 12 Outp | ut (onu: | 3ustate | V2A | ×0F ×10 | xAA xC6 | 1010 1010 |
| Charge Pump | 2.0mA 🗸 | | -B_MOX | 1 | ~ | IVCM | | 2. state | V V2P | ×11 | x24 | 0010 0100 |
| PFD Pulse | +1.5ns 🗸 | CP Direction positive | Phase Shift | /16 | \sim | LVCINI V2.Outro | | 070- 040 | V 120 | x12 | x02 x00 | 0000 0000 |
| | | | PLL Output | | | 13 Outp | | artive | V2A | CDCN | 17005 F | Register Da |
| Hold (On) | ff)/ Powerl | Dwn Frequency Hold-Over Fcn | Output Freq (MHz) | 983.0 | 4 | LVREC | | active | V V3R | Reg | Value 0x005F | : F1F0 |
| Cycle Slip | Preset | CP Frequency | | | | VAOuto | | | 130 | 01 | 0x0202 | A2A1 |
| - Mode | to Vcc/ | 12 Hold-Over Fcn1 | | | | 14 Odip | | active | V44 | 02 | 0xD000 | 0027 |
| Dividers | CP 3-S | itate Hold Fcn always activated | | | | LVCM | | 3-state | V4B | Regist | er Cont | trols |
| | | | | | | | | | | | Send | · |
| | | | | | | | | | | | Read | All |
| | | | | | | | | | | L | oad Re | :gs |

Figure 6: CDCM7005 Settings Screenshot

- Press the Send All button in the Register Controls section.
- Monitor the RF output signal on a spectrum analyzer.
- Monitor the output signal at the RF output connector.



Figure 7: RF-Out

So here instead of SSB output we are getting only LO signal.

2 LED Status



Figure 8: TSW LED STATUS



Figure 9: AFE LED Status

3 AFE-TEST(Single Differential DDR Clock Mode)

For Single Differential DDR Clock Mode All Connections and LO setting are same as above. No Change in HSDC-pro Setup .

In AFE7070 GUI Clock setting in bottom left is changed to Single Differential DDR Clock and in CDCM7005 tab Y1A is set to tri-state(since CLK-IO is not used in this mode) and also the divider of DAC-CLK is made 2(since we are feeding 130 MHz signal to EXT VCXO).By doing the above modification we can ensure that clock of TSW-1400 is still working at 130Mhz and DAC-CLK (which is also used to latch the data in this mode) will work at 65MHz.



Figure 10: CDCM7005 tab Screenshot for Single Differential DDR Clock Mode

Still output on Spectrum Analyzer is same.



Figure 11: RF-OUT for Single Differential DDR Clock Mode