AFE7070 TEST PROCEDURE

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1 AFE-TEST(Dual Input Clock Mode)

We followed the test procedure for AFE given on page 8 of user_guide_AFE_TSW .

1. Connect the AFE7071 EVM to the computer via USB cable.
2. Connect 6-V adapter to J9.
3. Launch the AFE7071EVM GUI and click Reset USB Port.
4. Connect the signal generator to the J4 connector (EXT VCXO) on the AFE7071 EVM. Set the frequency of the signal generator to 130 MHz and amplitude to 0 dBm.

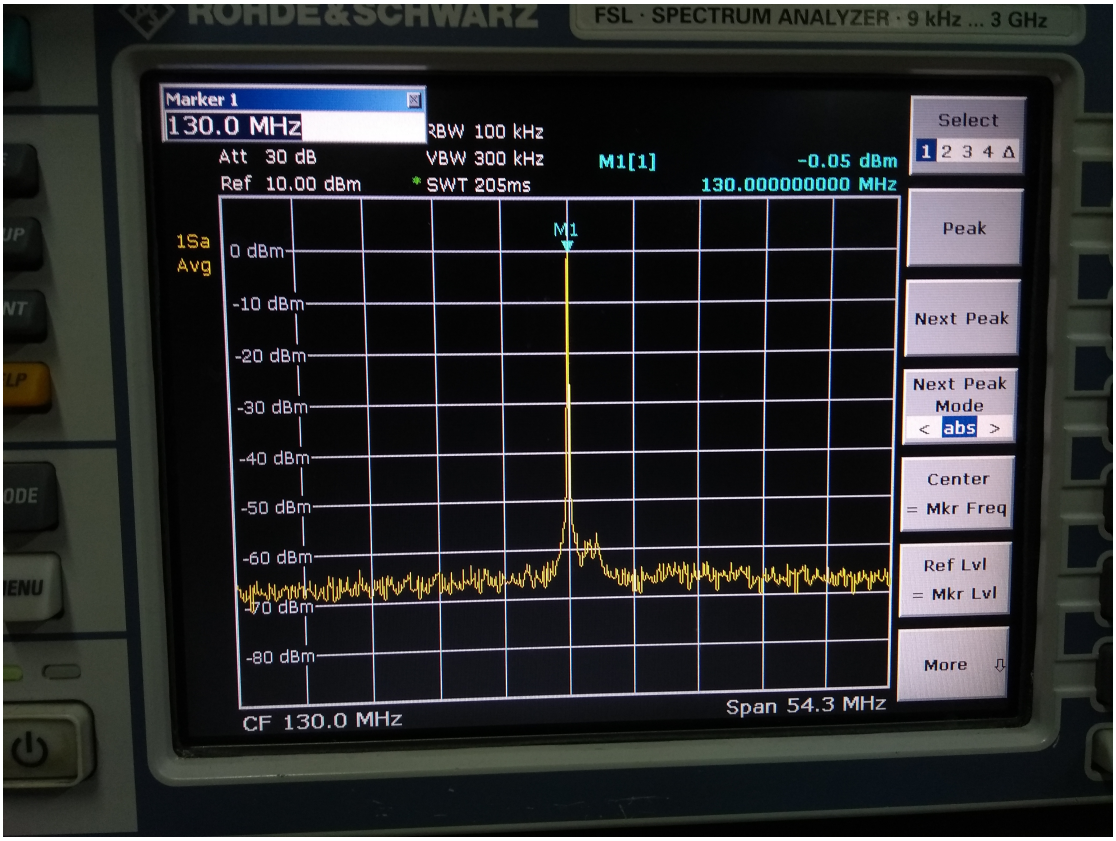

Figure 1: EXT VCXO

5. Connect LO signal from the second signal generator to the J10 connector (LO IN). Set the frequency of the signal generator to 2.1 GHz and amplitude to 5 dBm.

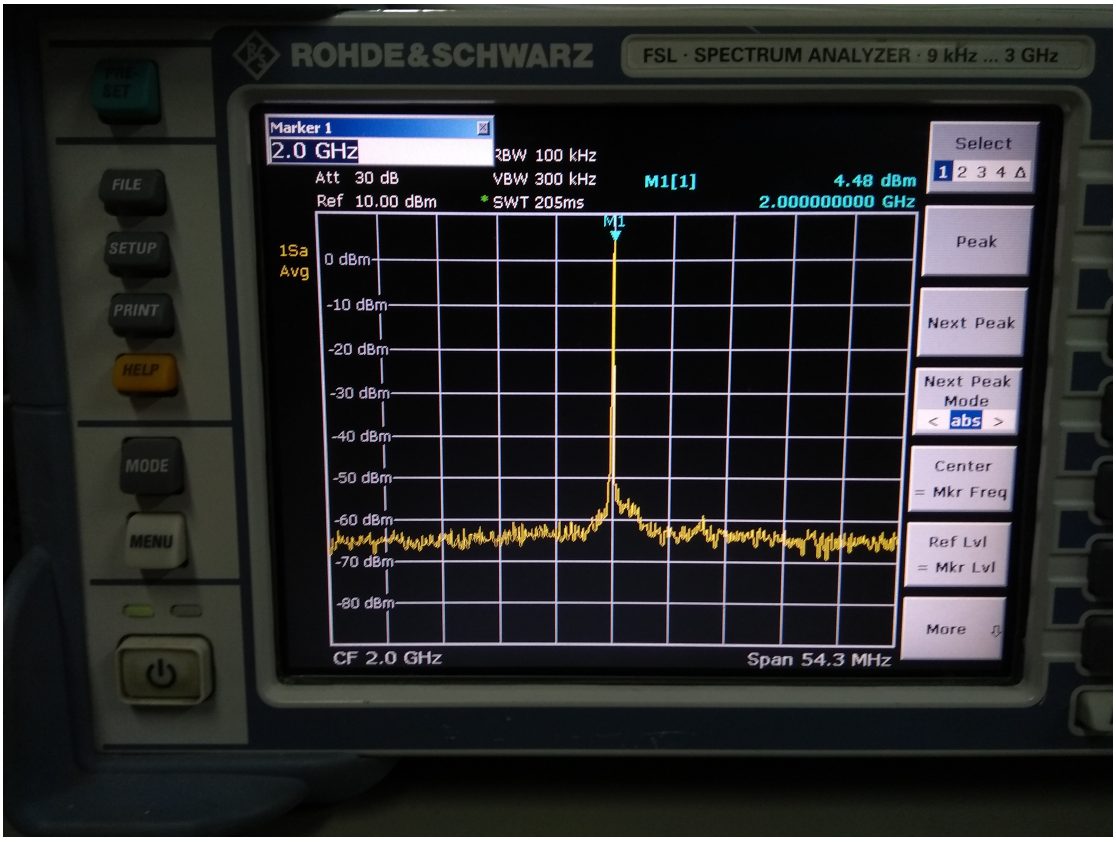

Figure 2: LO Signal

6. Connect J3 (RFOUT) to the spectrum analyzer.

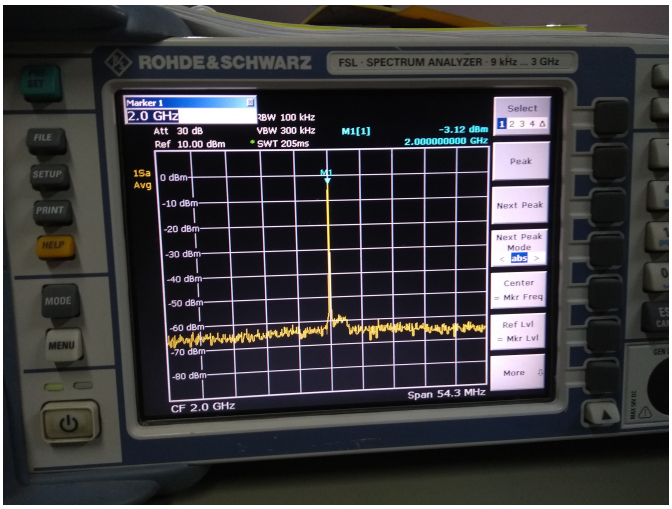

Figure 3: RF_OUT

7. Connect the TSW1400 to the computer via USB cable.
8. Connect the J1 (CMOS_INTERFACE) connector on the TSW1400 to AFE7071 EVM's J8 connector. Make sure pin 1 of the J1 connector is aligned with pin 1 on the J8 connector before connecting.
9. Connect the J7 (CMOS_CLK) on TSW1400 to J5 (CDC OUT) connector on AFE7071 EVM.
10. Connect 5-V adapter to J12 on TSW1400.
11. Turn the switch (SW7) to the On position.

TSW1400 Quick-Start Operation

After launching HSDC PRO software we done the following settings as per the user manual.

1. Select the DAC tab.
2. Select CMOS_AFE7070 from the top left drop-down menu.
3. Set the Data rate to "65" MHz and DAC Option to Offset Bin.
4. Set I/Q Multitone Generator → Tone BW to "1M", set (of tones) to "2", and Tone Center to "5M".
5. Under Tone selection, select Complex.
6. Click the Create Tones button.
7. Click Send.

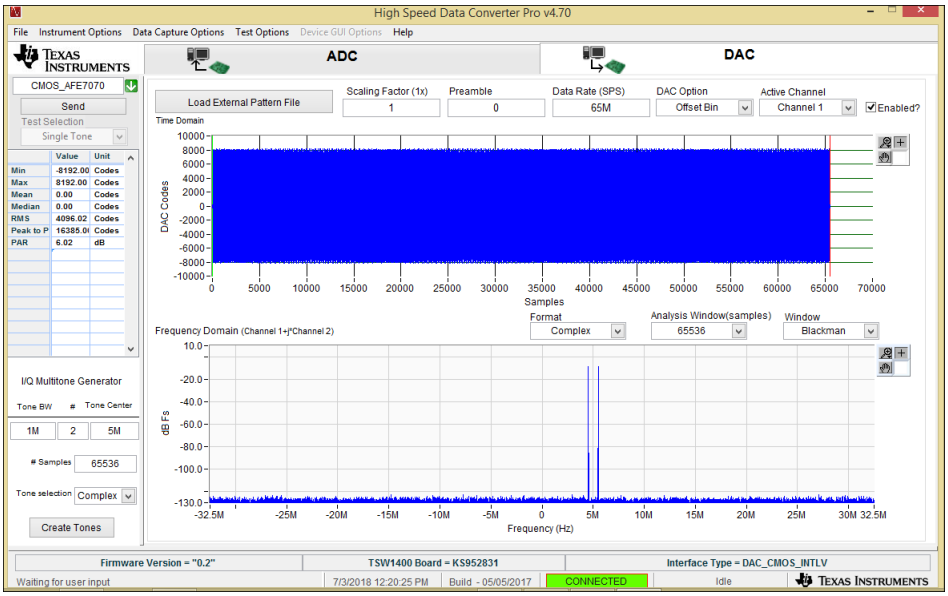

Figure 4: TSW-1400 Settings Screen shot

AFE7070 Settings Contd..

- In the Clock Settings section, we set the clock mode to Dual Input Clock.
- Since we are not using LVDS we disabled it.

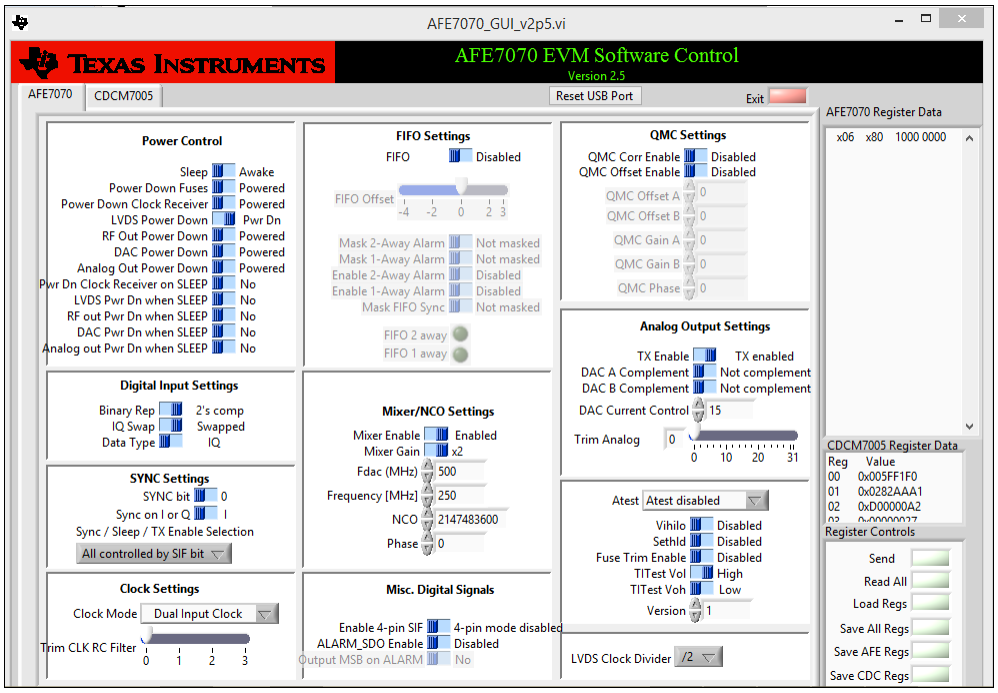

Figure 5: AFE7070 Settings Screen Shot

CDCM7005 Settings

- We done the following modifications in the Output Options section of CDCM7005 as per the user manual.
  - ◇ Y1 (AFE7070's CLK_IO) must be LVCMOS, with Y1A set to active rather than 3-state.
  - ◇ Y3 (AFE7070's DACCLK) must be LVPECL, with both Y3A and Y3B set to active.
  - ◇ Y4 (CDC Out) must be LVCMOS, with Y4A set to active.

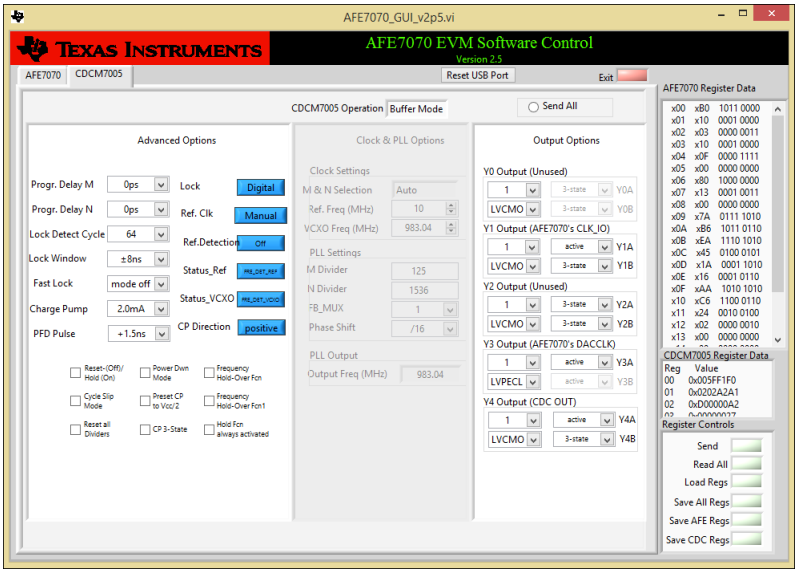

Figure 6: CDCM7005 Settings Screenshot

- Press the Send All button in the Register Controls section.
- Monitor the RF output signal on a spectrum analyzer.
- Monitor the output signal at the RF output connector.

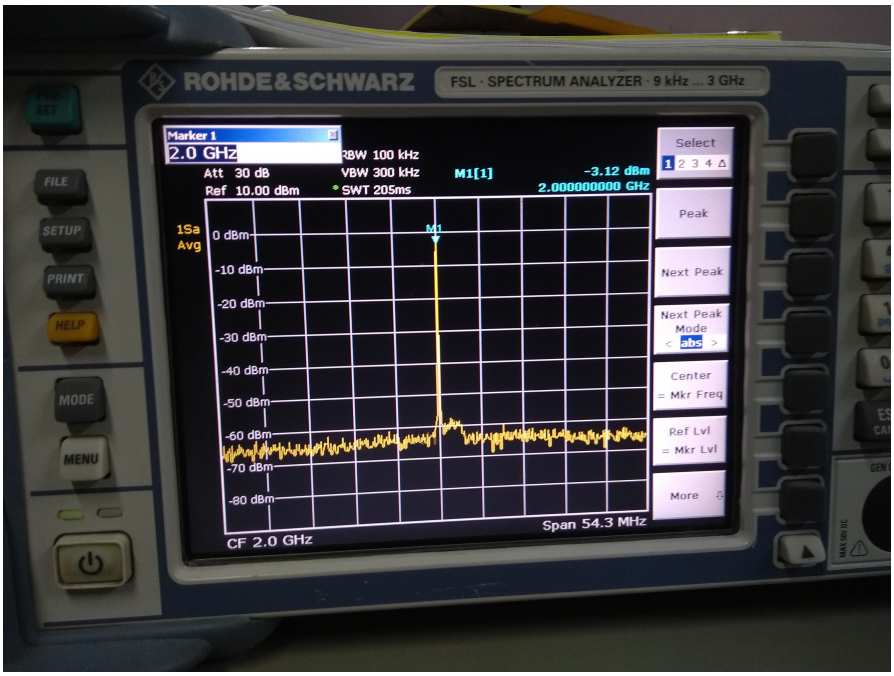

Figure 7: RF-Out

So here instead of SSB output we are getting only LO signal.

2 LED Status

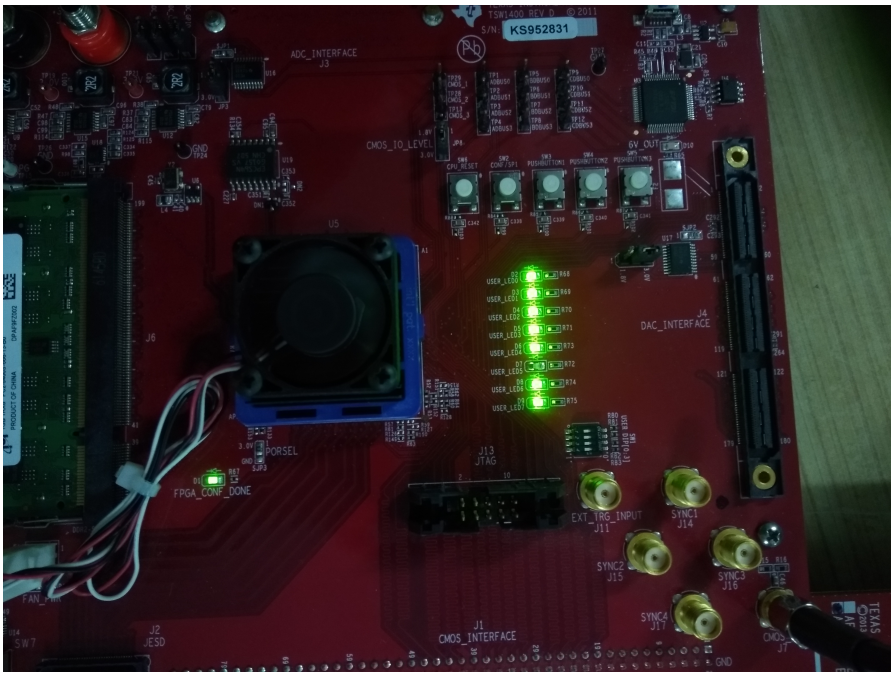

Figure 8: TSW LED STATUS

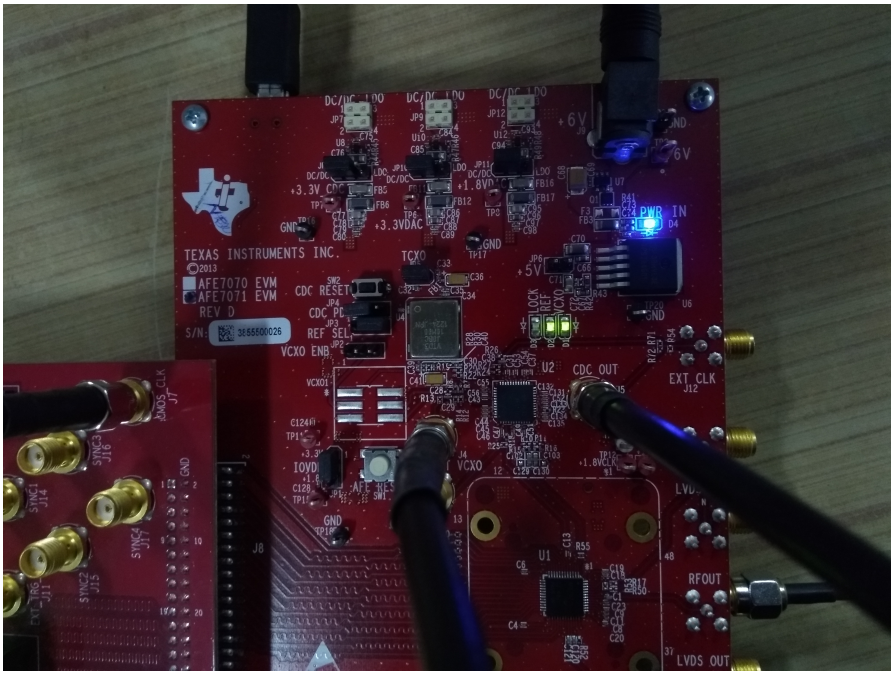

Figure 9: AFE LED Status

3 AFE-TEST(Single Differential DDR Clock Mode)

For Single Differential DDR Clock Mode All Connections and LO setting are same as above.
No Change in HSDC-pro Setup .
In AFE7070 GUI Clock setting in bottom left is changed to Single Differential DDR Clock and in CDCM7005 tab Y1A is set to tri-state(since CLK-IO is not used in this mode) and also the divider of DAC-CLK is made 2(since we are feeding 130 MHz signal to EXT VCXO).By doing the above modification we can ensure that clock of TSW-1400 is still working at 130Mhz and DAC-CLK (which is also used to latch the data in this mode) will work at 65MHz.

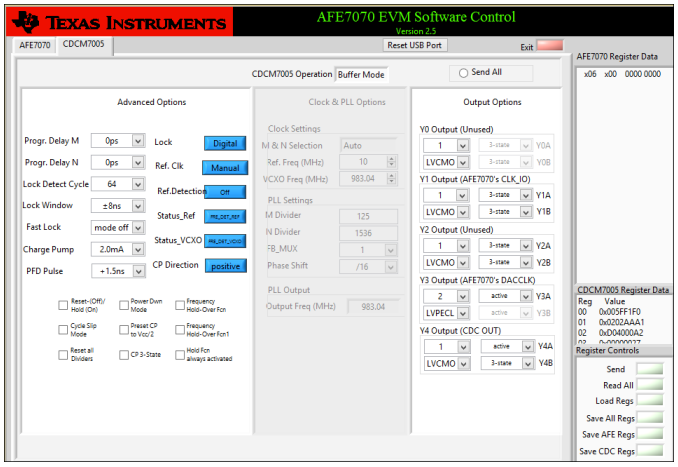

Figure 10: CDCM7005 tab Screenshot for Single Differential DDR Clock Mode

Still output on Spectrum Analyzer is same.

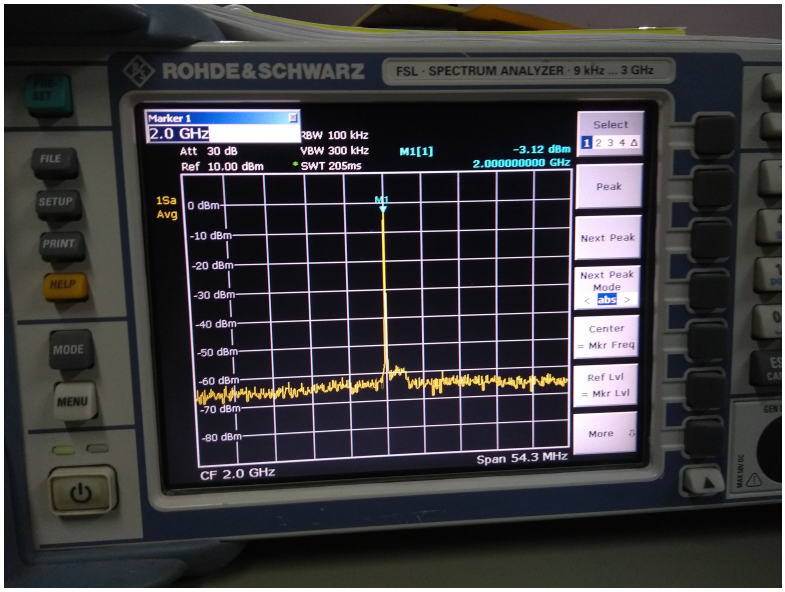

Figure 11: RF-OUT for Single Differential DDR Clock Mode