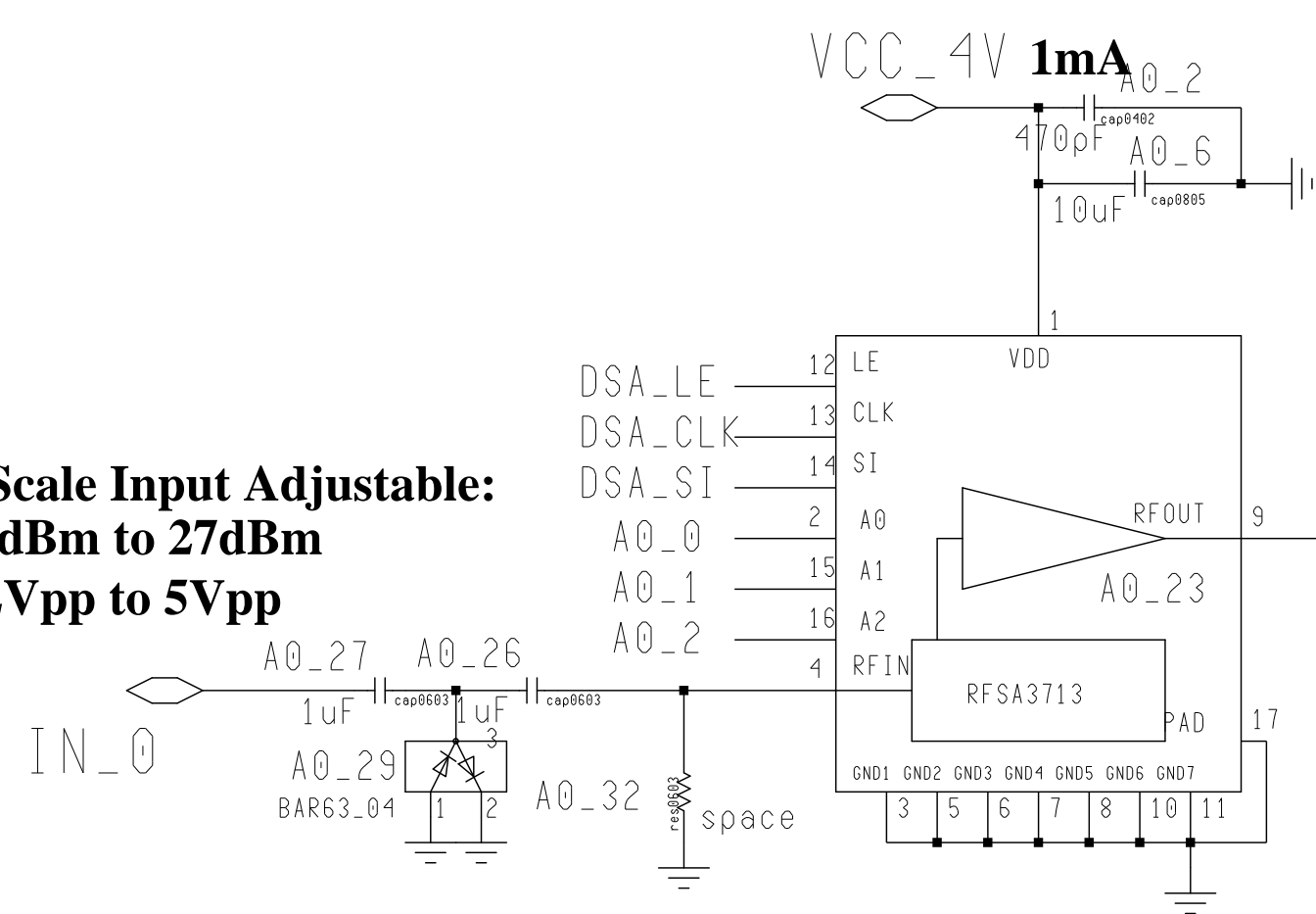


Max 3dB Bandwidth: 2,400MHz

Digital Step Attenuator - 31dB gain control range

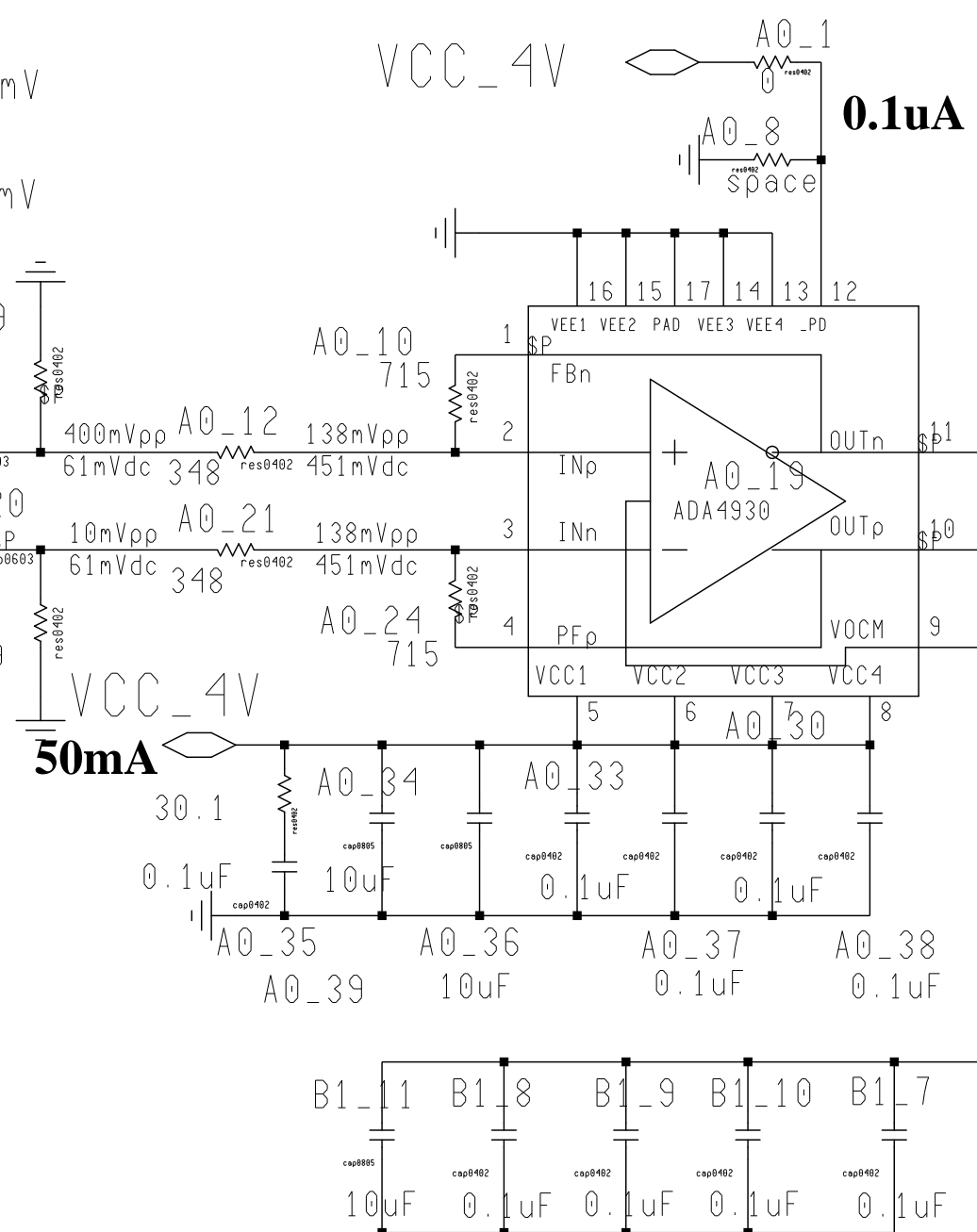
Full Scale Input Adjustable:
-1.6dBm to 27dBm
0.2Vpp to 5Vpp



Actual Gain: 5 - Fixed

Max -3dB Bandwidth: 807MHz

Actual Gain: 1 - Fixed

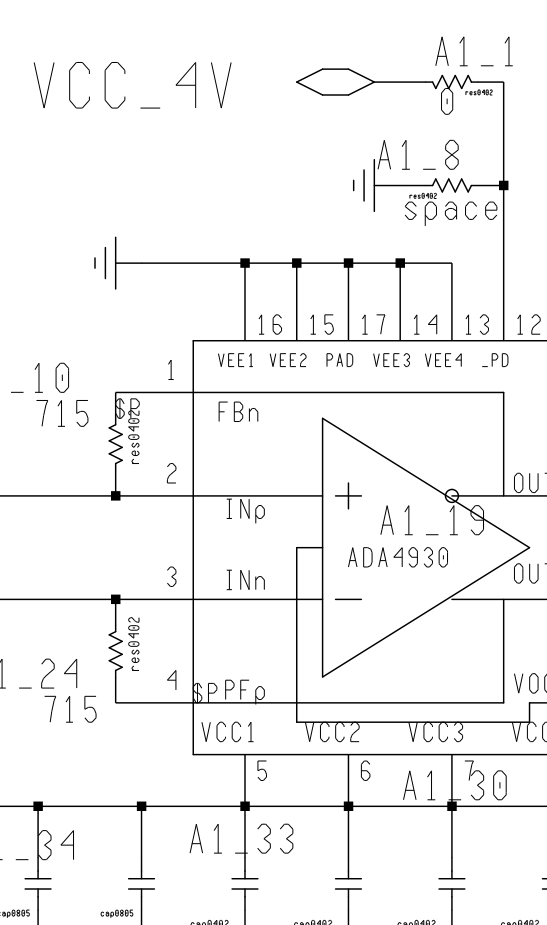
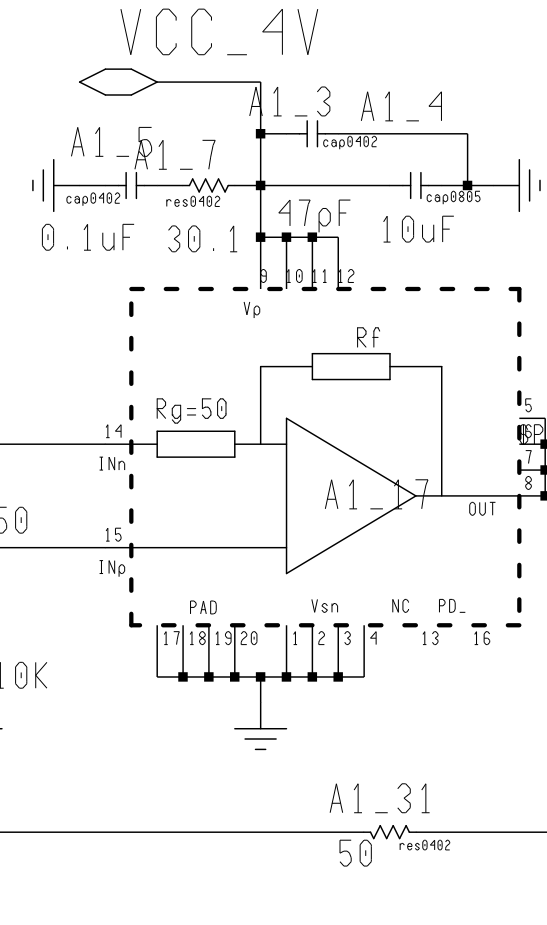
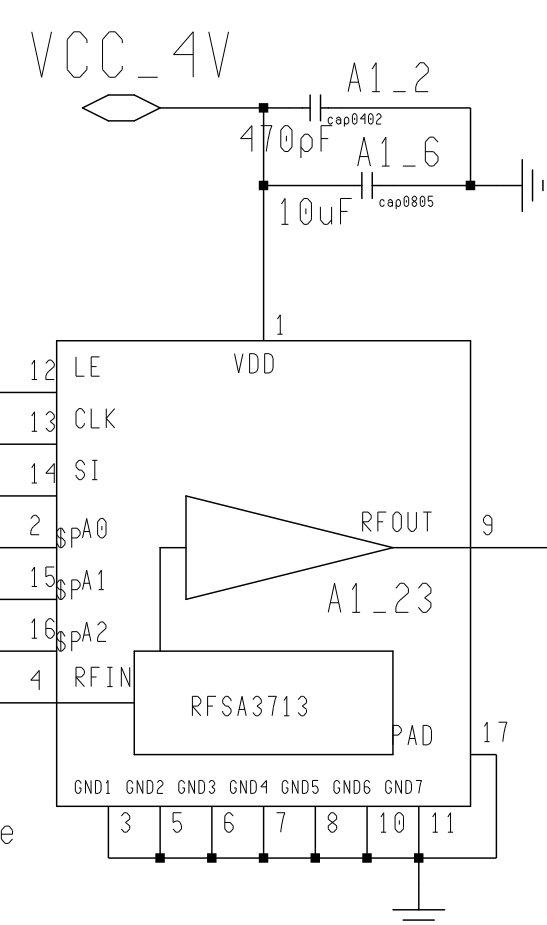
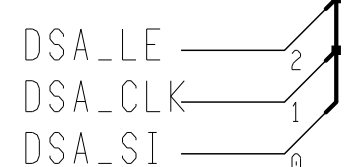


Digital Step Attenuator Control

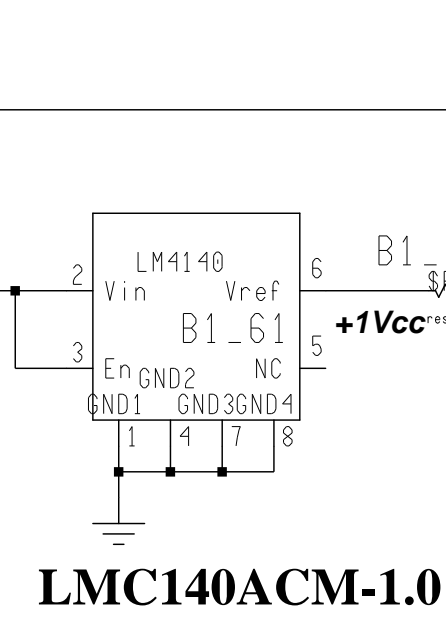
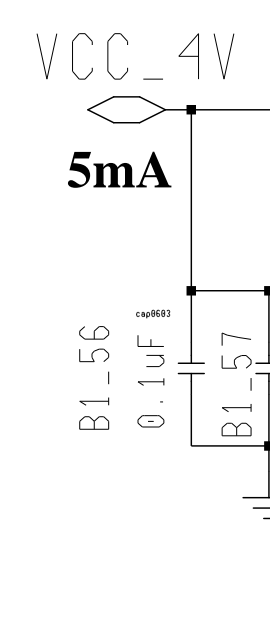
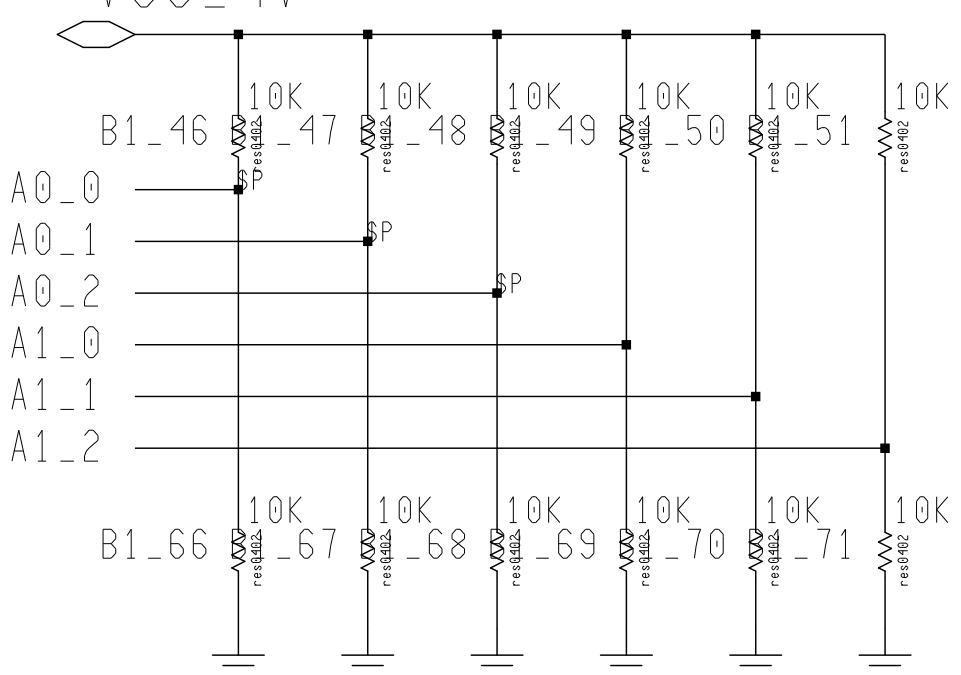
From FPGA - 2.5V I/O Bank

Lines are bussed for all 8 attenuators

DSA_CTRL[2:0]



Address Hardwired



ADC_CTRL[3:0]

From FPGA - 1.8V I/O Bank

ADC_CTRL_COM[3:0]

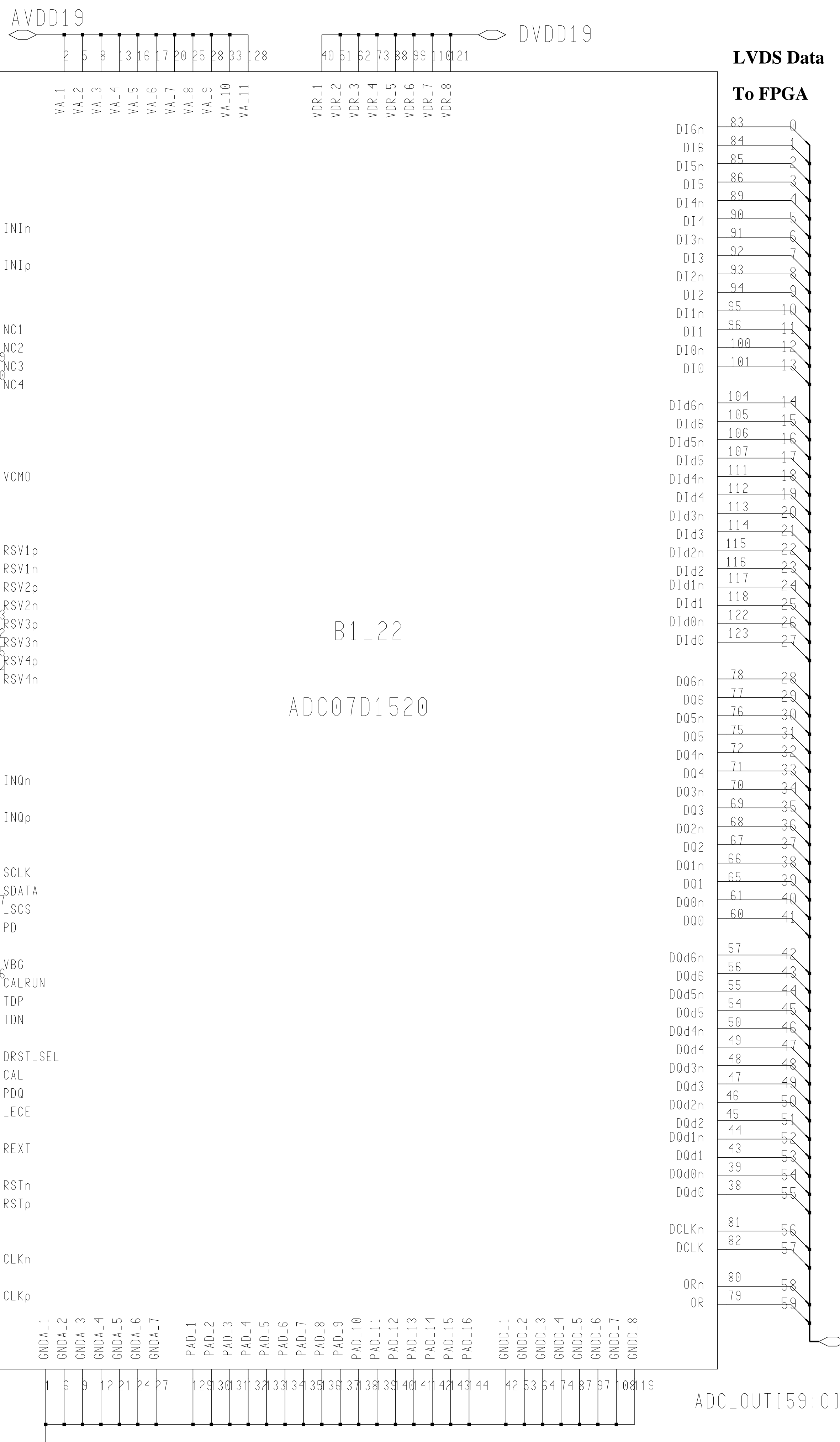
Shared Lines From FPGA - 1.8V I/O Bank

ADC_SYNC[1:0]

From FPGA

ADC_CLK[1:0]

From PLL



LVDS Data

To FPGA

D16n	83	0
D16	84	1
D15n	85	2
D15	86	3
D14n	89	4
D14	90	5
D13n	91	6
D13	92	7
D12n	93	8
D12	94	9
D11n	95	10
D11	96	11
D10n	100	12
D10	101	13
D16n	104	14
D16	105	15
D15n	106	16
D15	107	17
D14n	111	18
D14	112	19
D13n	113	20
D13	114	21
D12n	115	22
D12	116	23
D11n	117	24
D11	118	25
D10n	122	26
D10	123	27
D06n	78	28
D06	77	29
D05n	76	30
D05	75	31
D04n	72	32
D04	71	33
D03n	70	34
D03	69	35
D02n	68	36
D02	67	37
D01n	66	38
D01	65	39
D00n	61	40
D00	60	41
D06n	57	42
D06	56	43
D05n	55	44
D05	54	45
D04n	50	46
D04	49	47
D03n	48	48
D03	47	49
D02n	46	50
D02	45	51
D01n	44	52
D01	43	53
D00n	39	54
D00	38	55
DCLKn	81	56
DCLK	82	57
ORn	80	58
OR	79	59

Notes:
If resistors A0_18, A1_18 are installed, the Fixed Gain Amplifiers A0_17, A1_17 shall not be installed.
In this case, the overall gain is reduced by a factor of 5.

POWER:
4Vcc - 200mA max
1.9V for AVDD19 - 1A max
1.9V for DVDD19 - 0.3A max

Engineer: M. Bogdan	The University of Chicago ADC Channel 0 and 1 1500MHz ADC Module	
Drawn by: M. Bogdan		
DATE: 5/5/2016		
REV. A	DRW. 2868	Sheet 12-1

