Application Report
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DAC38RF8x Test Modes

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ABSTRACT

The DAC38RF8x family of devices comes equipped with multiple test modes to assist users in verifying systems in rapid prototyping situations. This application report covers two of the available tests, the pseudorandom binary-sequence test and JESD204B short pattern test, in detail using the TI DAC38RF8xEVM and TSW14J56EVM capture card.

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Trademarks

1 Introduction to PRBS Test

A pseudorandom binary sequence (PRBS) is a stream of binary information often used in testing high-speed data-transmission signal integrity. Pseudorandom binary sequences are composed of an equal distribution of 0s and 1s and only repeat themselves after 2^{k-1} cycles, where k is the order of the PRBS test. The PRBS test replicates the worst-case data scenarios where the current received bit is unrelated to previous bits. For more information on pseudorandom binary sequences, refer to the Advantest document, *DSP-Based Testing - Fundamentals 50, PRBS (Pseudo Random Binary Sequence)* (Okawara 2013).

The DAC38RF8x supports three different PRBS testing options: PRBS7, PRBS23, and PRBS 31. In this test mode, the PRBS pattern is supplied to the DAC input, typically through an FPGA, and the pattern is compared with the internally generated pattern of the DAC. If the received pattern matches the generated pattern, the test will pass and confirm good signal integrity at the DAC input. Otherwise a flag in one of the DAC registers is set to notify the user of a possible issue.

The following sections outline the required steps to implement the PRBS test using the DAC38RF8x EVM by using the TSW14J56 capture card and corresponding TI GUI software. To run the test without using the TI EVMs and GUIs, configure the DAC to the desired operating state and perform the register writes provided in Section 1.5 to enable the PRBS test mode.

1.1 Required Hardware

This test procedure requires the following lab equipment:

- DAC38RF8xEVM RevE board
- TSW14J56 RevD board
- 5-V DC power supplies
- Signal generator
- Oscilloscope

1.2 Required Software

This test procedure requires the following software:

- HSDC Pro Version 4.8 or higher
- DAC38RF8x EVM GUI

1.3 Hardware Setup

Follow these steps (see Figure 1) to set up the hardware:

Step 1. Connect the TSW14J56 FMC interface connector (J4 of TSW14J56) to DAC38RF8x FMC interface connector (J20 of DAC38RF8x EVM).

Step 2. Connect a USB 2.0 Type A to Mini-B cable from the PC to DAC38RF8x EVM USB Mini-B port (J16).

Step 3. Connect a USB 3.0 Type A to Type B cable from the PC to TSW14J56 RevD USB 3.0 B port (J9).

Step 4. Connect a 5-V power supply to the DAC38RF8x EVM board using J21.

Step 5. Connect a 5-V power supply to the TSW14J56 board using J11.

Step 6. Turn on the TSW14J56 board by moving switch 6 to the ON position.

Step 7. Connect the signal-generator output to LMKCLKIN (J4) of the DAC38RF8x EVM board.

- Configure the signal generator to output a frequency of 368.64 MHz with an amplitude of 10 dBm.
- Ensure that JP10 is removed from the board to enable internal clocking.

Step 8. Attach an oscilloscope probe to the alarm pin of DAC38RF8x EVM board (TP9).

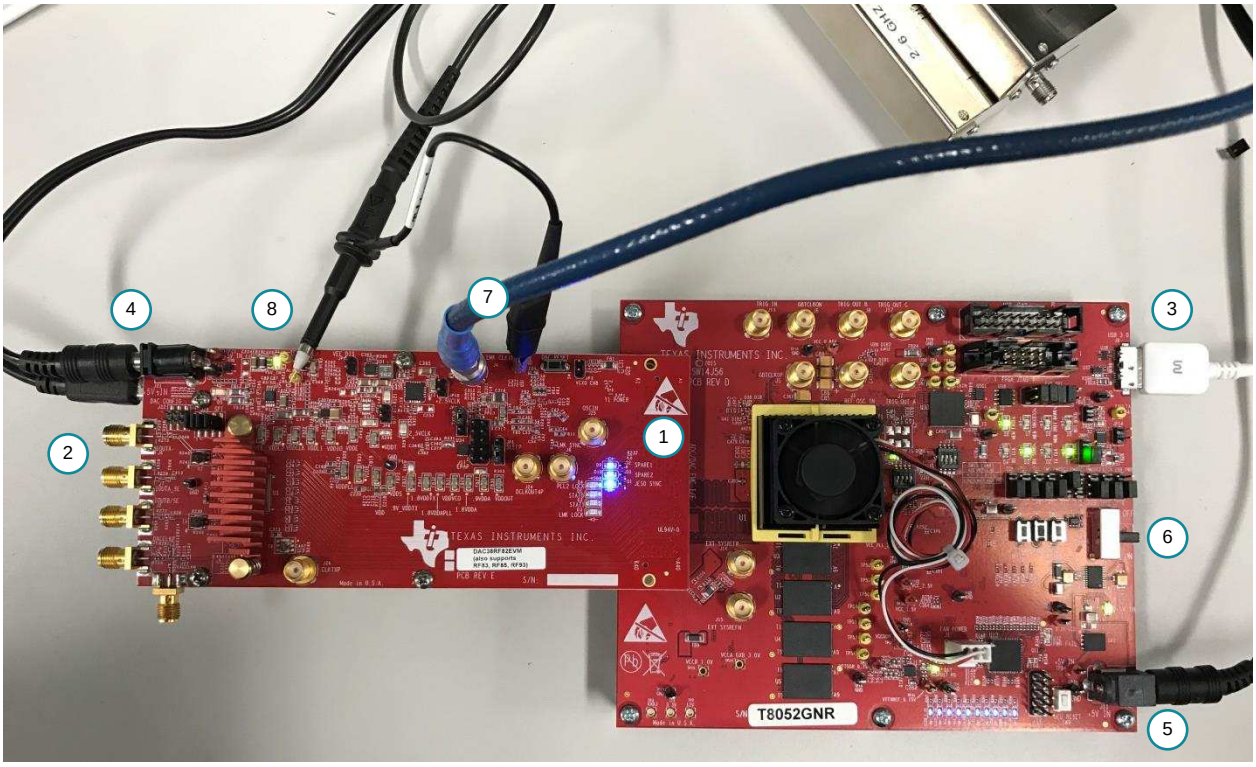


Figure 1. PRBS Hardware Setup

1.4 Configuring the DAC38RF8x

This procedure describes how to configure the DAC into the LMF = 841 mode with internal clocking. If a different configuration is needed, follow a similar procedure and simply vary the values in step 3 and step 4.

Step 1. Launch the DAC38RF8x EVM GUI and select the *Quick Start* tab (see Figure 2).

Step 2. Reset the board by clicking the *Not in RESET* button and then clicking the button again, after the button changes, to bring the board back out of reset. Click the *LOAD DEFAULT* button to load the default values into the registers.

Step 3. Under the *DAC MODE* section, set

- The *# of DACs* field to *Dual DAC*
- The *# of IQ pairs per DAC* to *1 IQ pair*
- The *# of SerDes lanes per DAC* field to *4 lanes*
- The *Desired Interpolation* field to *12x*

Step 4. In the *On-Chip PLL section* check the *PLL Enable* box. Set the *M* field to 6, the *N* field to 1, and the multiplier to *368.64*. The *DAC Clock Frequency* box should automatically change to 8847.36 MHz. Click the *CONFIGURE DAC* button. After this configuration is complete, click the *PLL AUTO TUNE* button. After this configuration is complete, click the *Reset DAC JESD Core & SYSREF TRIGGER* button.

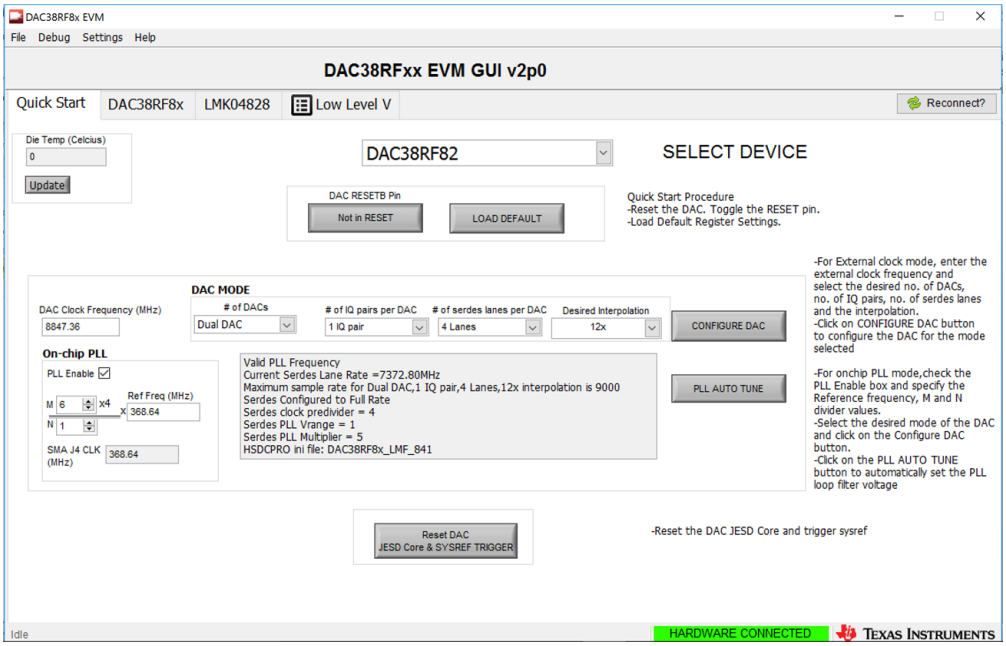


Figure 2. DAC38RF8x EVM GUI Quick Start Tab

Step 5. Select the *DAC38RF8x* tab and navigate to the *Clocking* sub-tab (see Figure 3). The box labeled *PLL LF Voltage* should be populated with a value from 2 to 6. If this value is correct, the configuration and PLL tuning were performed correctly. Otherwise, verify that the contents of the *Quick Start* tab are correct and repeat the previous steps.

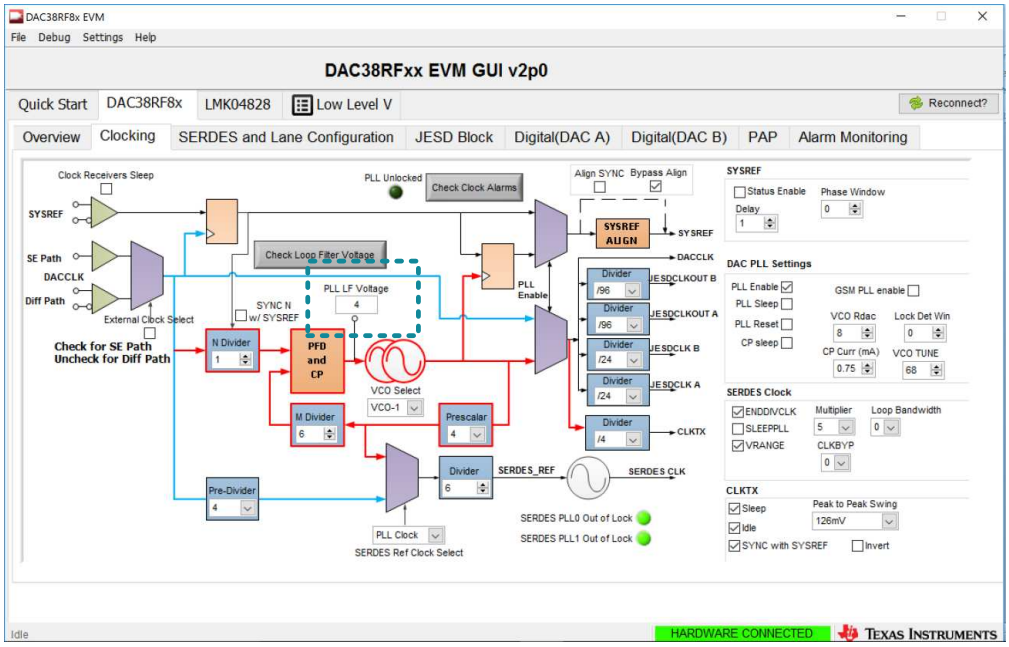


Figure 3. DAC38RF8x EVM GUI Clocking Tab

Step 6. Select the *Alarm Monitoring* sub-tab (see Figure 4). In the *General Alarm and Test* section, select *Alarm Output* in the *ALARM Pin* drop-down menu. Select the *ALARM Pin Polarity* field to be either *Active High* or *Active Low*. Active high causes the alarm pin voltage to be set high if a PRBS error occurs.

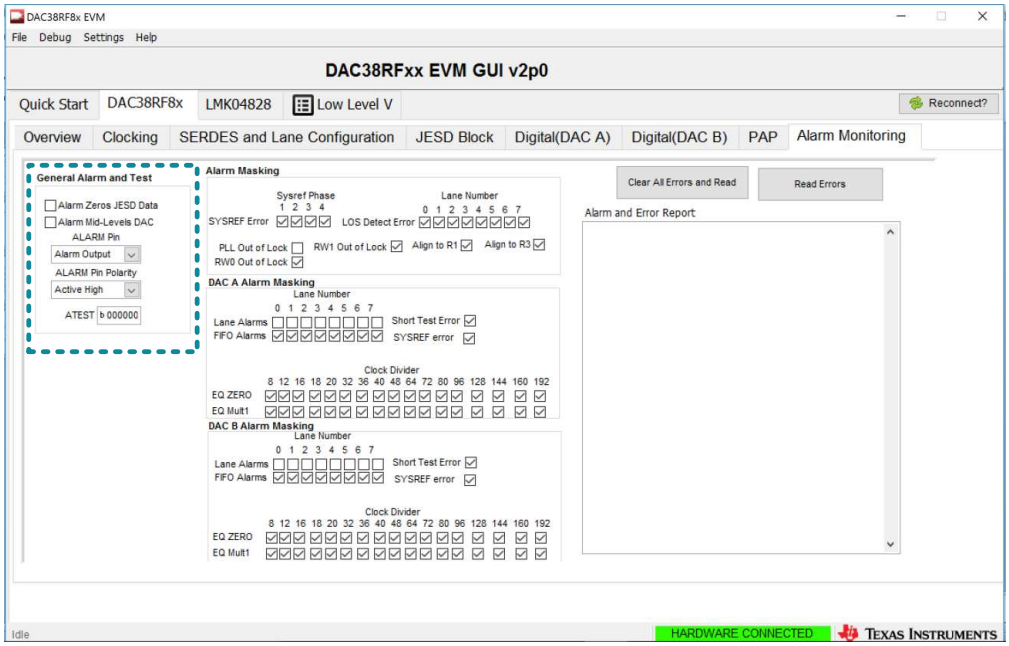


Figure 4. DAC38RF8x EVM GUI Alarm Monitoring Tab

Step 7. Select the *SERDES and Lane Configuration* sub-tab (see Figure 5). In the *Align* drop-down menu select *Disabled*. Next, in the *SERDES Test Pattern* drop-down menu select the desired PRBS test. In the *DTEST* drop-down menu select *TESTFAIL*. In the *DTEST Lane Select* drop-down menu, select the lane to be tested.

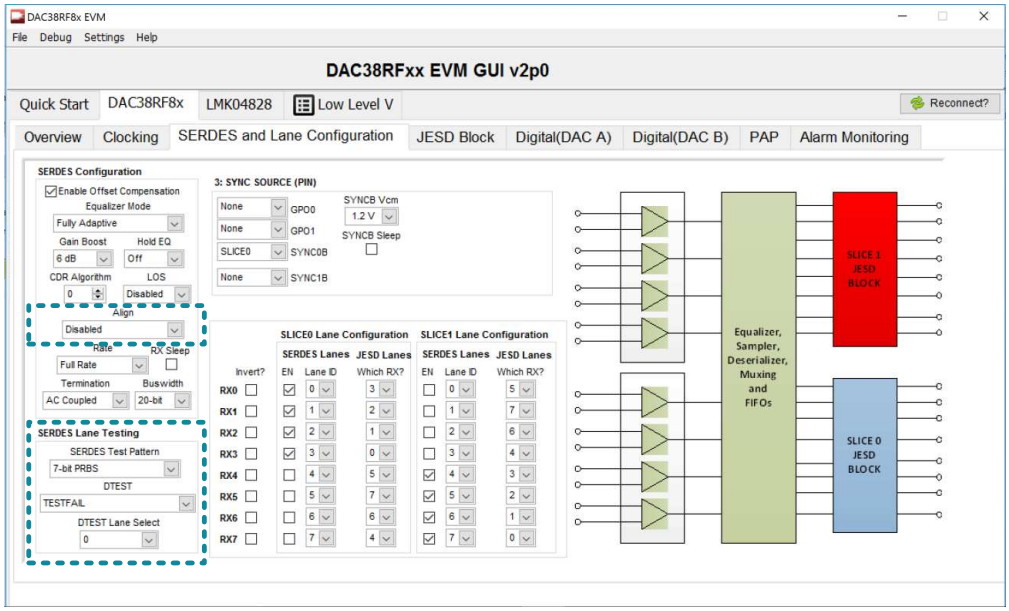


Figure 5. DAC38RF8x EVM GUI SERDES and Lane Configuration Tab

Step 8. Select the *JESD Block* sub-tab (see Figure 6). Ensure that the *Comma Align EN* boxes are not checked.

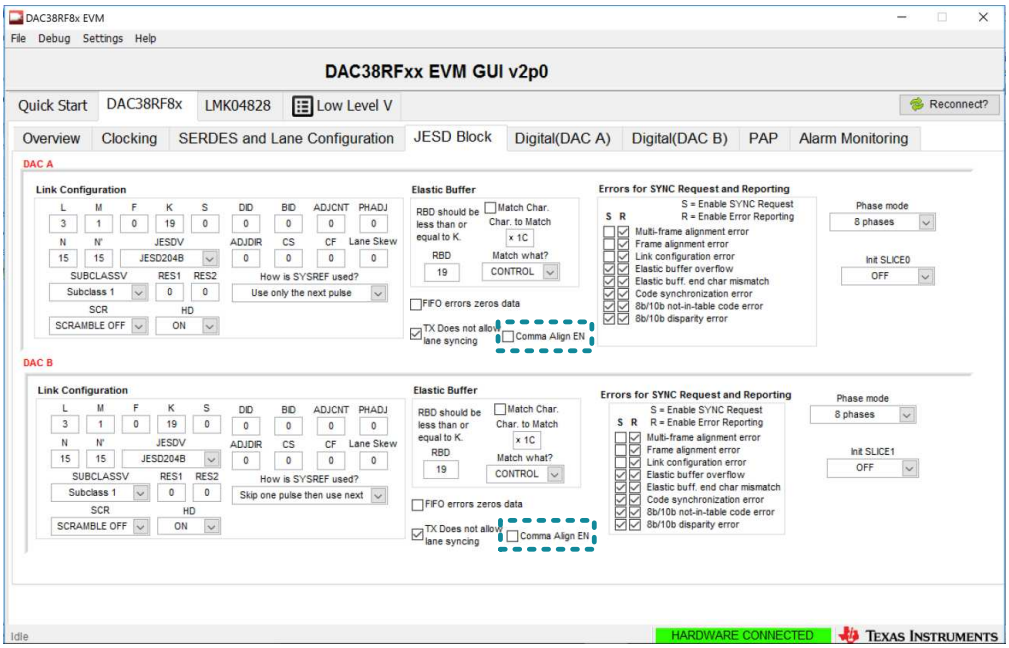


Figure 6. DAC38RF8x EVM GUI JESD Block Tab

1.5 PRBS Register Writes for Custom Setup

If the user is implementing the test without using the TI EVMs or GUI software the following register writes must be made in place of the previous steps to achieve the correct test setup. The registers in the DAC are arranged according to page number and addresses. The page number indicates to which portion of the DAC the registers are associated. The page number is indicated in the low-level view by the first digit in the address field.

Table 1. Register Writes for Custom Setup

	Page	Address	Bit	Value	Function
1.	0	0x00	14, 13	1, 1	Enable alarm output active high
2.	4	0x3E	14	1	Align disable
3.	4	0x1B	11:8	0x3	Set DTEST to TESTFAIL
4.	1	0x4F	0	0	Uncheck Comma Align En
5.	2	0x4F	0	0	Uncheck Comma Align En
6.	4	0x3D	15:12	0x2	To Select PRBS7
7.	4	0x3D	15:12	0x3	To Select PRBS23
8.	4	0x3D	15:12	0x4	To Select PRBS31

NOTE: Users should only perform one of the last three register writes which corresponds to the desired PRBS test. After performing the register writes, send the pattern to the DAC though the FPGA connection.

1.6 TSW14J56 SETUP for PRBS Tests

When the DAC has been configured properly, the PRBS pattern is ready to be sent. Launch the HSDC Pro application and navigate to the *Quick Start* tab. A window pops up asking the user to select a device. Select the TSW14J56 RevD board and click the *OK* button (see Figure 7).

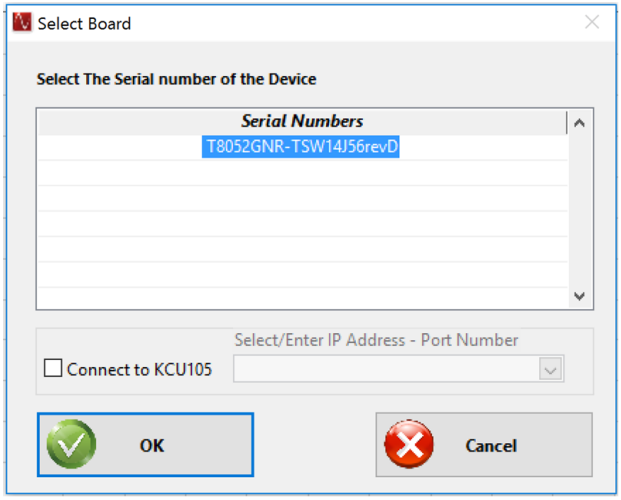


Figure 7. HSDC Pro Select-Board Menu

A box pops up indicating that no firmware is connected. Click the *OK* button and switch to the *DAC* tab in the HSDC Pro application by using the tabs located at the top of the window (see Figure 8).

Figure 8. HSDC Pro DAC Tab

Open the drop-down menu in the top left corner by clicking the green arrow beside the *Select DAC* box. Select *PRBS_DAC38RF8x_LMF_841_RevD*. Click *Yes* in the window that pops up to update the firmware.

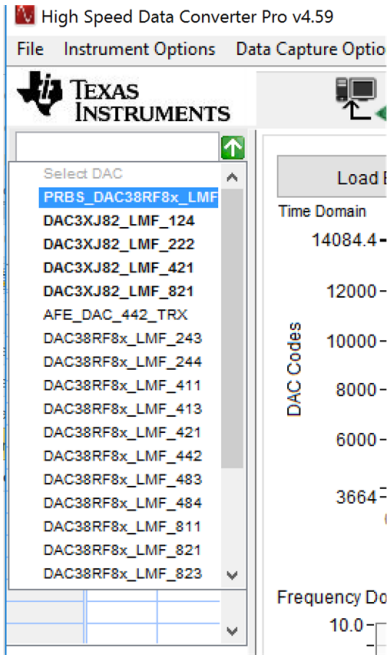


Figure 9. PRBS Testing .ini File Selection

When the firmware is correct, the PRBS pattern is ready to be loaded. Under the *Instrument Options* menu, select *SERDES Test Options*. In the window that pops up, select the transmitter tab at the top. The DAC38RF8x EVM supports PRBS7, PRBS23, and PRBS31. Select the desired PRBS test and click the *Apply* button.

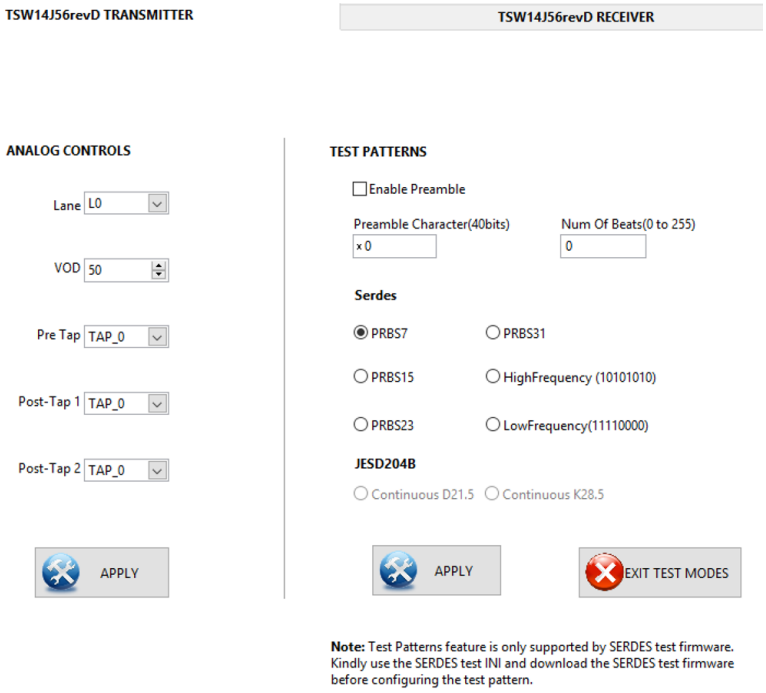


Figure 10. SERDES Test Options Menu

1.7 PRBS Test Results

The PRBS test should now be running. Monitor the alarm pin using the oscilloscope for failures. If no alarms are detected after a few seconds, the PRBS test is passing. Different PRBS tests can be performed by selecting the desired test in the *SERDES and Lane Configuration* tab of the DAC38RF8x EVM GUI and selecting the corresponding test in the HSDC Pro GUI SerDes Test Options. Additionally the other lanes can be tested by selecting the desired lane from the *DTEST Lane Select* drop down in the *SERDES and Lane Configuration* tab.

2 Introduction to JESD204B Short Pattern Test

The DAC38RF8x also comes equipped with software to verify short pattern tests using the JESD204B lanes. The JESD204B short pattern test is a quick and easy way for users to ensure that lane mapping between the FPGA and DAC38RF8X is correct. The following section describes the test setup and procedure for the JESD204B short pattern test using the TI EVMs and GUIs. To perform this test on a different board or without the TI GUI software, configure the DAC into the desired state making sure to include the register writes in Section 2.5.

2.1 Required Hardware

This test procedure requires the following pieces of lab equipment:

- DAC38RFxxEVM REV E board
- TSW14J56 REV D board
- 5-V DC power supplies
- Signal generator

2.2 Required Software

This test procedure requires the following software:

- HSDC Pro Version 4.59 or higher
- DAC38RFx EVM GUI

2.3 Hardware Setup

Follow these steps to set up the hardware:

Step 1. Connect the TSW14J56 FMC interface connector (J4 of TSW14J56) to DAC38RFxx FMC interface connector (J20 of DAC38RFxx EVM).

Step 2. Connect the USB 2.0 Type A to Mini-B cable from the PC to DAC38RFxx EVM USB Mini-B port (J16)

Step 3. Connect the USB 3.0 Type A to Type B cable from the PC to TSW14J56 Rev D USB 3.0 B port (J9)

Step 4. Connect a 5-V power supply to the DAC38RFxx EVM board using J21.

Step 5. Connect a 5-V power supply to the TSW14J56 board using J11.

Step 6. Turn on the TSW14J56 board by moving switch 6 to the ON position.

Step 7. Configure the signal generator to output 5898.24 MHz signal at 16 dBm, and apply signal to the DACCLKP SMA connector (J1).

Step 8. Install Jumper J10 to enable external clocking.

Step 9. Connect the spectrum analyzer input to IOUTA (J6).

2.4 Configuring the DAC38RF8x

The procedure images that follow show how to configure the DAC into the LMF = 4421 mode with external clocking. If a different configuration is needed, follow a similar procedure and vary the values in the DAC MODE box accordingly.

Step 1. Launch the DAC38RF8x GUI and select the *Quick Start* tab. In the *Quick Start* tab, toggle the DAC RESETB pin and click the *LOAD DEFAULT* button.

Step 2. After the default registers have been loaded, configure the DAC to the desired operating mode. The following figures show the setup for the 4421 configuration, but the steps will be the same for all configurations.

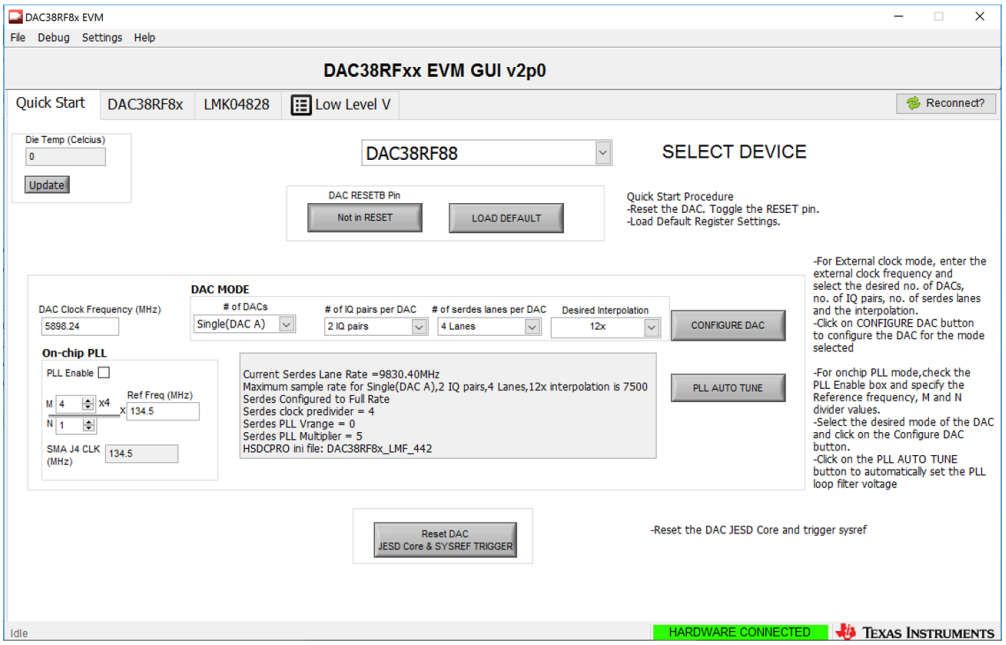


Figure 11. DAC38RF8x GUI (4421 External Clocking Configuration)

Step 3. Select the *DAC38RF8x* tab. In the *Mixer* section, check the *Mixer enable* box for Path AB . In the *NCO* section, check the *NCO enable* box for Path AB and set the NCO frequency to 1000-MHz. Click the *UPDATE NCO* button.

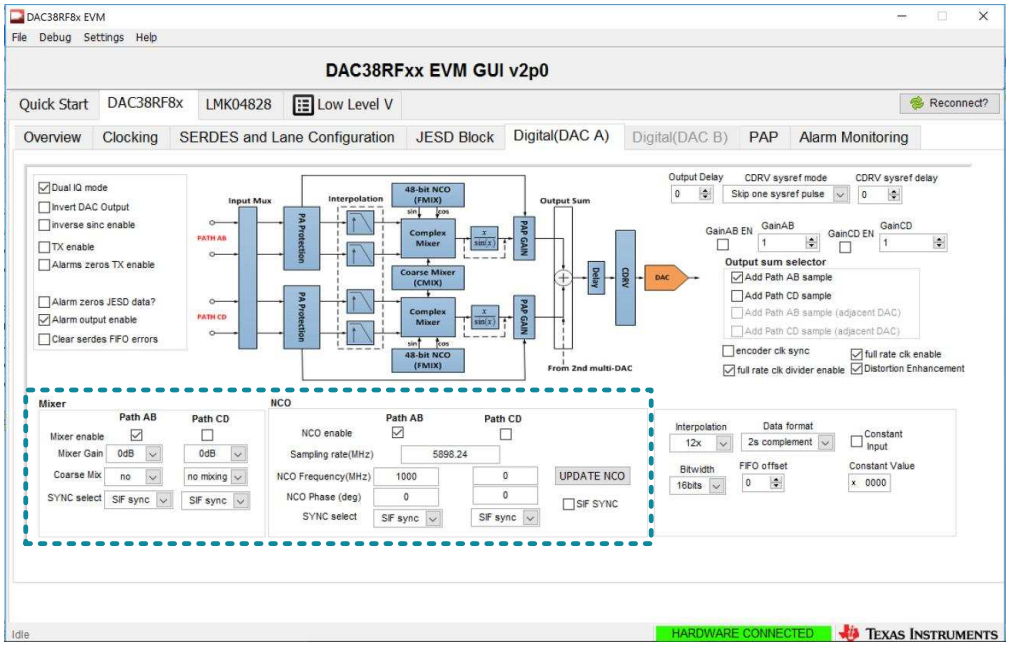


Figure 12. DAC38RF8xEVM GUI Digital (DAC A) Tab

2.5 Register Writes for Custom Setup

To achieve this DAC configuration without the DAC38RF8x EVM GUI, perform the register writes shown in Table 2.

Table 2. DAC38RF8x Register Writes

	Page	Address	Bit	Value	Function
1.	1	0x0C	9, 5	1, 1	Enable mixer and NCO
2.	1	0x1E	15:0	0xC7C1	Update NCO frequency (AB)
3.	1	0x1F	15:0	0x1C71	Update NCO frequency (AB)
4.	1	0x120	15:0	0x2B67	Update NCO frequency (AB)
5.	1	0x121	15:0	0x0000	Update NCO frequency (CD)
6.	1	0x122	15:0	0x0000	Update NCO frequency (CD)
7.	1	0x123	15:0	0x0000	Update NCO frequency (CD)
8.	1	0x1C	15:0	0x0000	Update NCO phase offset (AB)
9.	1	0x1D	15:0	0x0000	Update NCO phase offset (CD)
10.	1	0x28	1	1	SIF Sync
11.	1	0x28	1	0	SIF Sync
12.	2	0x28	1	1	SIF Sync
13.	2	0x28	1	0	SIF Sync

2.6 TSW14J56 SETUP for JESD204B Short Pattern Test

After the DAC38RF8x EVM GUI has been properly configured, the next step is to send the pattern to the DAC. Follow these steps to configure the HSDC pro to send the pattern to the DAC:

Step 1. Launch the HSDC Pro application.

Step 2. A window will pop up asking the user to select a device. Select the TSW14J56 RevD board and click the *OK* button (see Figure 13).

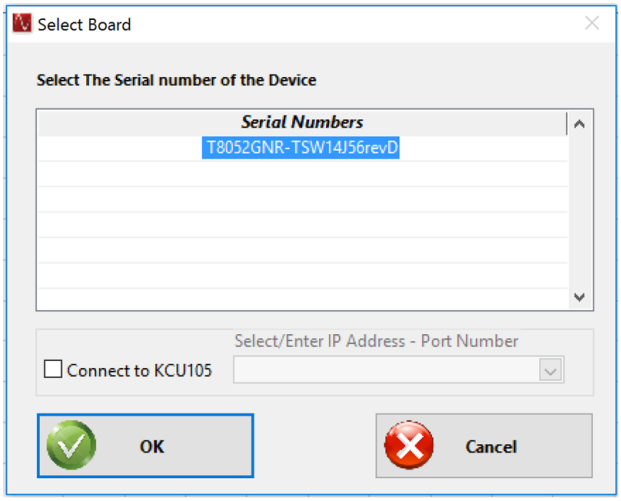


Figure 13. HSDC Pro Select Board Menu

Step 3. A box pops up indicating that no firmware is connected. Click the *OK* button.

Step 4. Switch to the *DAC* tab in the HSDC Pro application by using the tabs located at the top of the window.

Figure 14. HSDC Pro DAC Tab

Step 5. Open the drop-down menu in the top left corner by clicking the green arrow beside the *Select DAC* box. Select the .ini file corresponding to the configuration of the DAC. Click *Yes* in the window that pops up to update the firmware.

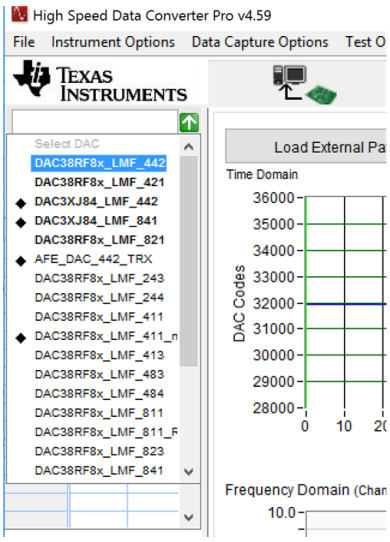


Figure 15. HSDC Pro Select .ini File Menu

Step 6. Change the data rate at the top of the HSDC pro application to the appropriate data rate for the previously selected configuration. The data rate is determined by taking the DAC clock frequency and dividing it by the interpolation rate. In the bottom left corner of the HSDC Pro application, set the tone number to 1 and tone center to 10-MHz (see Figure 16). In the *Tone selection* drop-down menu, select *Complex* and click the *Create Tones* button. Click the *Send*

button.

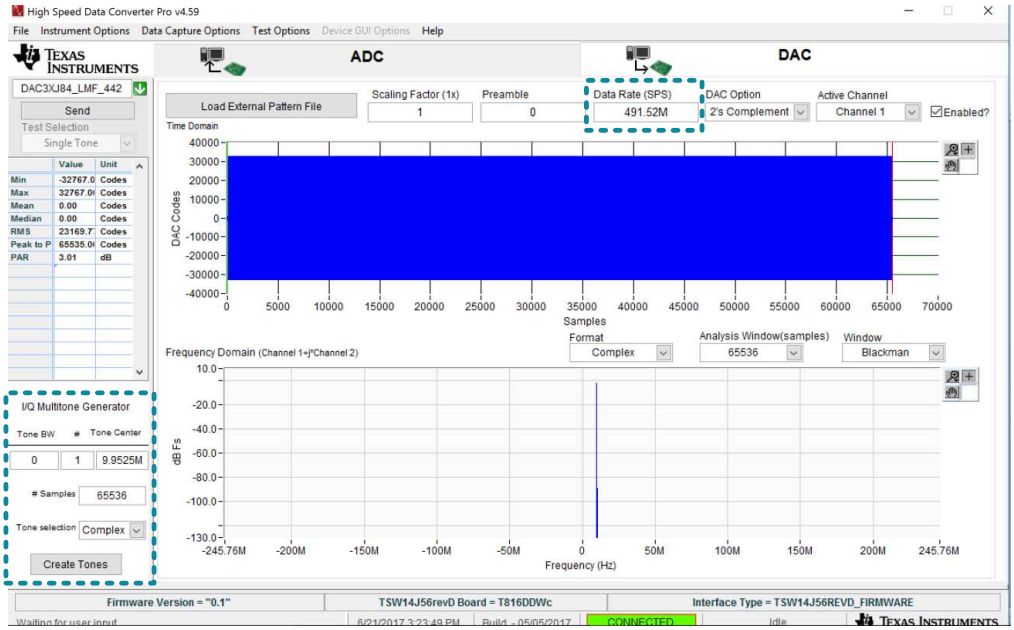


Figure 16. HSDC Pro Tone Creation

Step 7. The spectrum analyzer should now show a tone at 1010-MHz. If the tone is present, the DAC has been configured correctly and is ready to execute the JESD204B short pattern test.

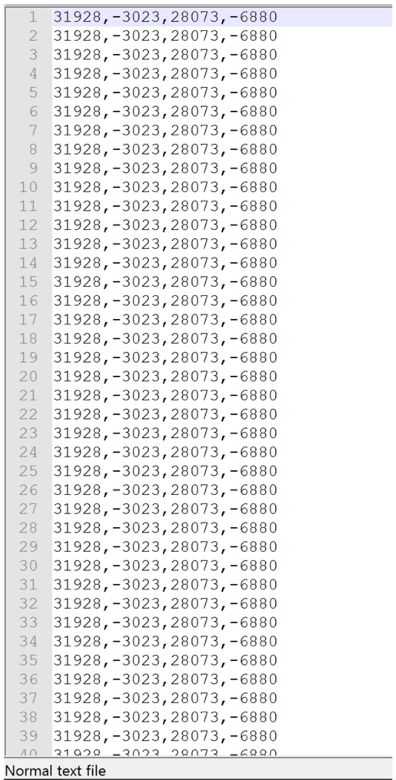
2.7 Short Pattern Test Procedure

To run the short pattern test, the user must first create the pattern file. The pattern file is a CSV file containing the information that is sent to the DAC during the test, and is different for each configuration. Users can look up their corresponding pattern in Table 3. The given patterns are in 2's complement hexadecimal format.

Table 3. JESD204B Short Test Patterns

Pattern	I0	Q0	I1	Q1
82121	7CB8, F431	6DA9, E520	—	—
42111	7CB8	F431	—	—
22210	7CB8	F431	—	—
12410	7CB8	F431	—	—
44210	7CB8	F431	6DA9	E520
24410	7CB8	F431	6DA9	E520
41121	7CB8, F431	—	—	—
81180	7C00, B800, F400, 3100, 6D00, A900, E500, 2000	—	—	—
24310	7CB0	F431	6DA0	E520
41380	7CB0, F430, 6DA0, E520, F870, E960, DA50, CB40	—	—	—

The generated file should repeat the pattern for 256 lines. Figure 17 shows an example of the beginning of the 4421 pattern file. Because the 4421 pattern contains data in the I0, Q0, I1, and Q1 sections, the pattern file for this mode is four columns wide. Also, because each section contains only one value, that value is simply repeated for the entirety of the column. For sections containing more than one value, the pattern in the corresponding column cycles through the values instead of just repeating the one value.



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31928,-3023,28073,-6880
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Figure 17. Example Short Test Pattern File

In the HSDC Pro application, click the *Load External Pattern File* button and load in the pattern file. Click the *Send* button.

The next step is to enable the short pattern test in the DAC. In the DAC38RF8x GUI, select the *Low Level View* tab. Scroll down in the list of registers to the DAC38RF8x section and then select register 0x10C. Write a 1 to bit 12 of this register to enable the short pattern test.

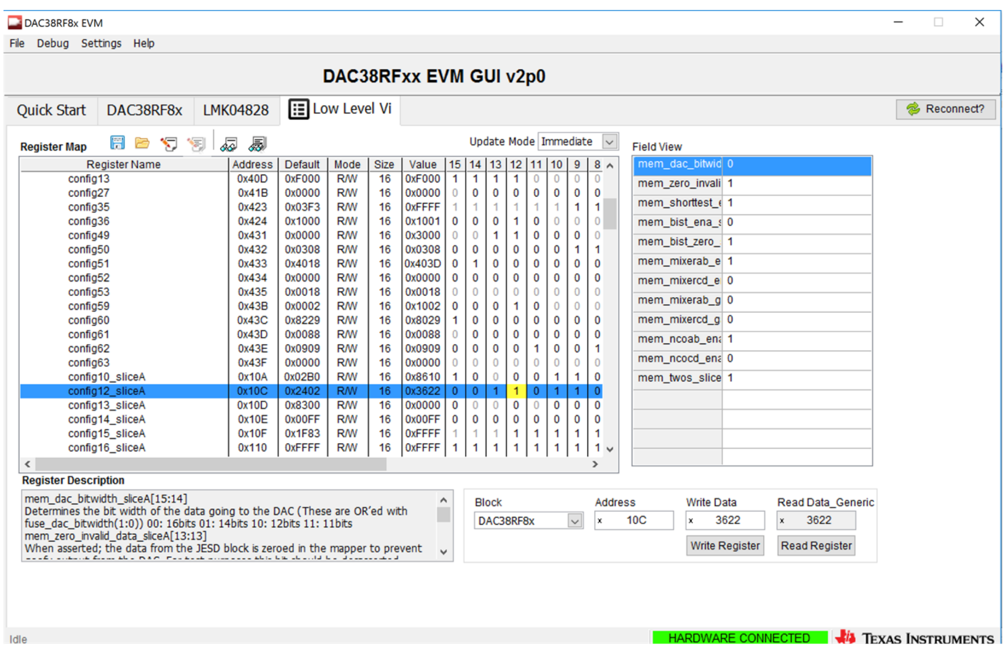

Figure 18. DAC38RF8x EVM GUI *Low Level View* Tab Short Test Enable Register

2.8 JESD204B Short Pattern Test Results

To read the alarm pin, scroll down and select register 0x16C. In the *Write Data* box, type the value 0000 and click the *Write Register* button. This write clears any alarms that may have been inadvertently triggered in the setup process. Next click the *Read Register* button. If the value in the register remains a zero, the test is passing and the configuration is correct. If the value changes to a 1, the alarm signal has been detected and the user's setup could have issues.

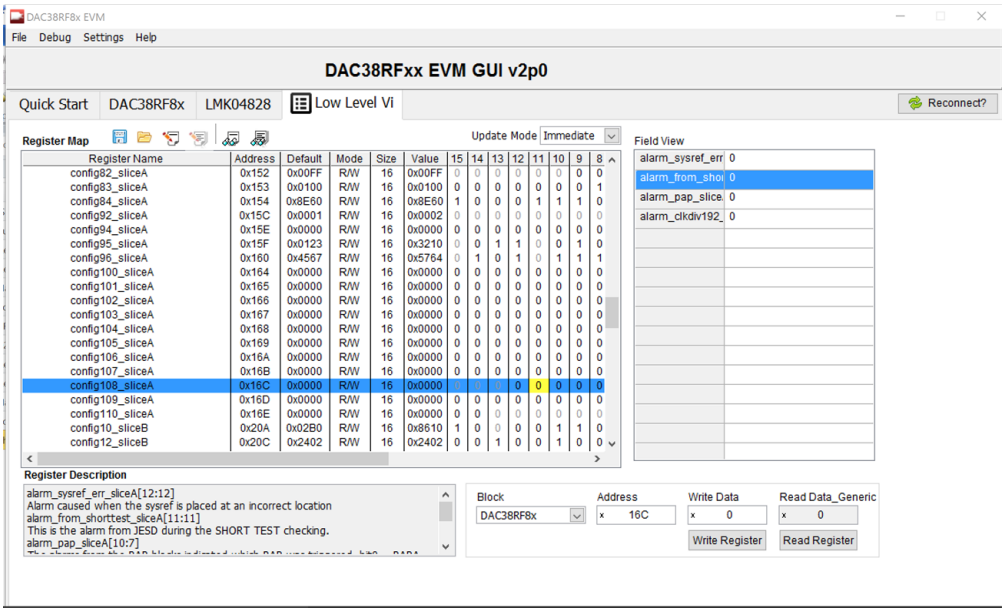

Figure 19. DAC38RF8x EVM GUI *Low Level View* Tab Short Test Alarm Register

NOTE: The register values in the GUI do not automatically update and can only be checked by using the *Read Register* button. Also the short pattern test alarm must be cleared manually between each reading using the write register tool. Disabling the short pattern test through the short test enable register does not clear the alarm pin.

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