DAC3xJ8x Device Initialization and SYSREF Configuration

Version 1.0

Kang Hung Hsia

12/31/2015

[Type the abstract of the document here. The abstract is typically a short summary of the contents of the document. Type the abstract of the document here. The abstract is typically a short summary of the contents of the document.]

Acrynoms

DAC – Digital to Analog Converter

CW – Constant Wave (or sine wave)

Multi-frame (K) – the number of Frames in the Multi-Frame in JESD204B specification.

Frame (F) – the number of Octets in a Frame in JESD204B specification.

QMC – quadrature modulator correction signal processing block.

JESD204B TX – JESD204B transmitter. In a JESD204B system of FPGA/ASIC and the DAC3xJ8x device, this is referred to the FPGA/ASIC.

JESD204B RX - JESD204B receiver. In a JESD204B system of FPGA/ASIC and the DAC3xJ8x device, this is referred to the DAC3xJ8x.

LMFC – local multi-frame clock. It is a JESD204B sub-clock indicating the boundary of multi-frame.

S2P – serial to parallel conversion. This refers to the data packing on the JESD204B RX.

P2S – parallel to serial conversion. This refers to the data packing on the JESD204B TX.

SYSREF – system reference clock. This refers to the reference needed in JESD204B subclass 1 system where the reference clock is used to align LMFC.

DAC3xJ8x – a family of JESD204B subclass 1 DAC devices.

Introduction

The DAC38J84 family of devices (DAC3xJ8x) is a family of complex, mix signal, high performance digital-to-analog converter (DAC) devices with JESD204B Receiver block (JESD204B RX) for high speed serial to parallel (S2P) data transfer. It also includes various digital signal processing blocks such as interpolation filters, mixers, and quadrature modulator correction filters. Due to the operating nature of these digital blocks, the DAC3xJ8x has various divided down clocks running internally, including the local multi-frame clock (LMFC) for JESD204B data transfer.

The DAC3xJ8x is part of JESD204B system, and the JESD204B system implements high speed parallel to serial (P2S) on the JESD204B TX device and S2P transfer on the JESD204B RX device. The packing of the data would depend on the frame and multiple frames of octets, depending on the S2P or P2S transfer. If one cycle of these high speed data transfers after the P2S stage is misaligned and delayed in time, a relatively larger amount of data may be shifted in time after the S2P process, therefore resulting a much larger latency variation.

In order to achieve the overall system synchronization, the alignment of the DAC3xJ8x's local multi-frame cycle (LMFC) with the overall system multi-frame clock is critical. Without alignment, the relative latency of the data transfer from JESD204B TX device to the DAC3xJ8x JESD204B RX side will vary. The DAC3xJ8x is a JESD204B, Subclass 1 device that uses an external system reference clock (SYSREF) signal as a common reference for multiple devices. The ultimate goal of using a global distributed SYSREF for LMFC is to ensure all the JESD204B devices (include TX and RX) are aligned upon initialization. The overall latency of the JESD204B data transfer can be deterministic, which may also be important for system designers wish to implement multiple device synchronization in the system.

JESD204B Subclass 1 Overview

With JESD204B Subclass 1, SYSREF is source synchronous to the device clock and should come from the same clock source. It can be a one-shot pulse, gapped periodic, or periodic signal. In the case of a gapped or periodic signal, the SYSREF must be an integer multiple of the local multi-frame clock (LMFC) to prevent SYSREF from occurring in the middle of a multi-frame.

System designer can implement deterministic latency between a JESD204B TX and JESD204B RX device when the internal LMFC clocks are aligned to the edge of the device clock when the SYSREF is sampled high. This should also align/reset all the internal clocks of the TX and RX devices. Furthermore, you can achieve multiple device synchronization by ensuring that the deterministic latency is the same for each TX-to-RX link in your group of devices.

The clock chip will generate the SYSREF signal that meets the setup and hold times of the device clock and must be distributed to each group of TX and RX devices with matched trace lengths to ensure proper alignment of the signals. System designers should use a clock chip, such as the LMK04828, capable of generating both the SYSREF and the device clocks to minimize the skew between the signals. The timing signals required for subclass 1 are shown below in Figure 2.
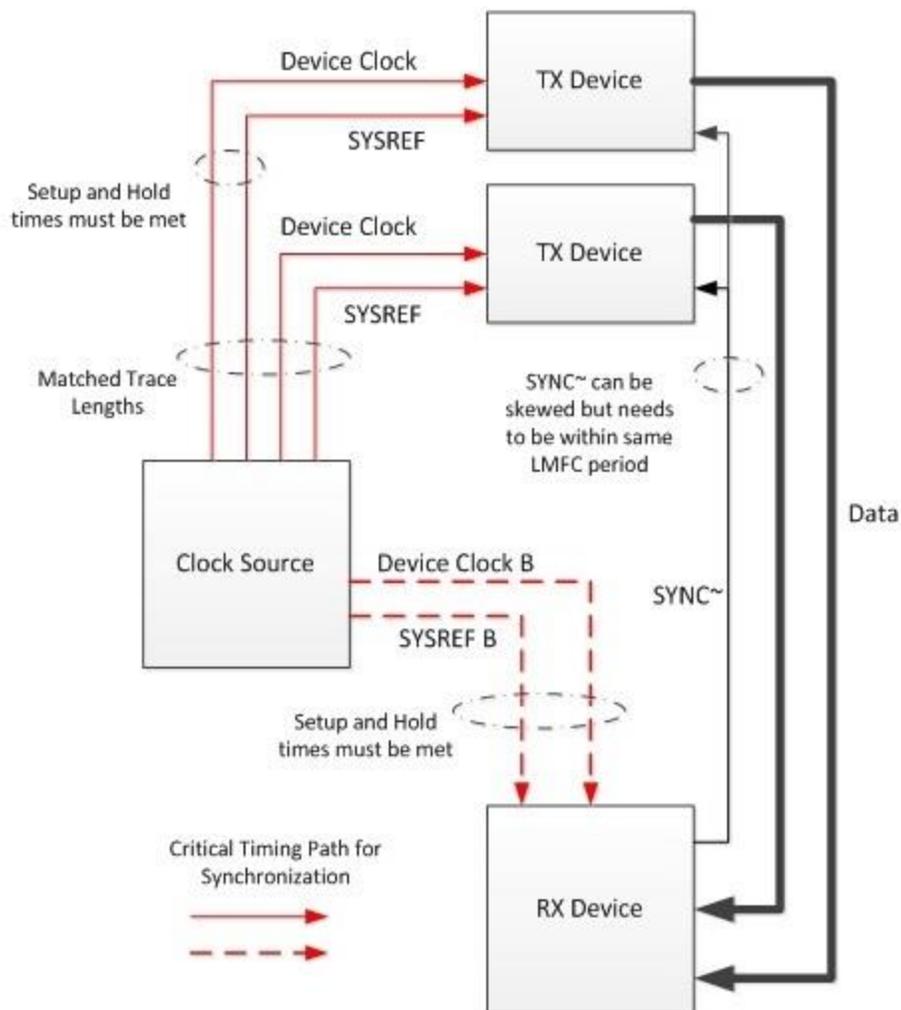
It is not mandatory for the clock chip to generate the exact same SYSREF for all TX and RX devices, but the clock chip should generate different SYSREFs in such a way that there is a deterministic relationship between when SYSREF is sampled high in all of the devices. In this case, the latency is deterministic but not minimized.

Device Clock Edge used for Frame
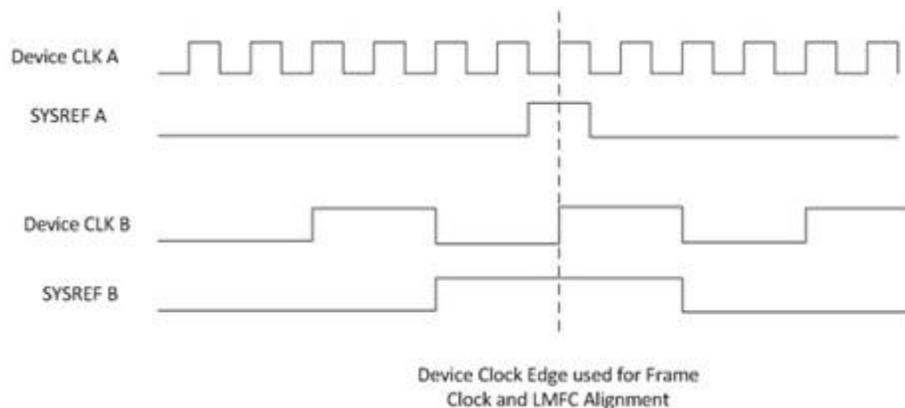Clock and LMFC Alignment

Figure 3: Multiple devices using different SYSREF and device clocks with a deterministic relationship (copy from blogpost https://e2e.ti.com/blogs_/b/analogwire/archive/2014/10/24/jesd204b-understanding-subclasses-part-1)

Once the system completes LMFC alignment, future SYSREF pulses can be a reference to check the alignment of the local frame and multiframe clocks. Be sure to turn SYSREF off during normal operation, as a periodic SYSREF signal runs at a sub-harmonic of the sampling clock and may create unwanted spurs. If the SYSREF signal is coupled onto the DAC3xJ8x output, the frequency spectrum of the DAC3xJ8x output will typically show two CW spurs that are on both side of the main signal output. The distance of the spurs to the main signal is at the SYSREF frequency, due to the modulation from the noise coupling.

The DAC3xJ8x is a subclass 1 device and only uses the ~SYNC signal in the code group synchronization (CGS) process. The ~SYNC is not a critical timing signal for subclass 1 JESD204B system. The DAC3xJ8x has one pair of LVDS signal (SYNCBp/n) and two pairs of CMOS signals (SYNCA and SYNCB) that can represent the ~SYNC of up to two JESD204B links (Link 0 and/or Link1). Upon the triggering of SYSREF to the internal digital blocks, the respective ~SYNC signals will be in logic LOW to start the link initialization process.

LMFC and SYSREF Period

To calculate the LMFC of various JESD204B link configuration, refer to the following equation.

$$LMFC(Hz) = \frac{SERDES\ Line\ Rate\ (bps)}{10\ F\ K}$$

Where F = number of frames per multi-frame

Where K = number of octets per frame

If periodic SYSREF signal is used thorough the system, the SYSREF frequency must be an integer factor of the LMFC.

$$SYSREF(Hz) = \frac{SERDES\ Line\ Rate\ (bps)}{10\ n\ F\ K}$$

Where n = positive integers of 1, 2, 3, …

DAC3xJ8x Clock Divider and JESD204B Logic

Clock Divider and JESD204B Logic Core Descriptions

The DAC3xJ8x has a clock divider block and a JESD204B logic block. The clock divider is to provide divided-down clocks for all the digital logics such as JESD204B logic, FIR filter logics for the interpolation filters, and complex mixers. Figure TBD shows the simplified clock divider structure. The source of the clock divider comes from the DACCLK, and the clock divider can be reset by the SYSREF signal.
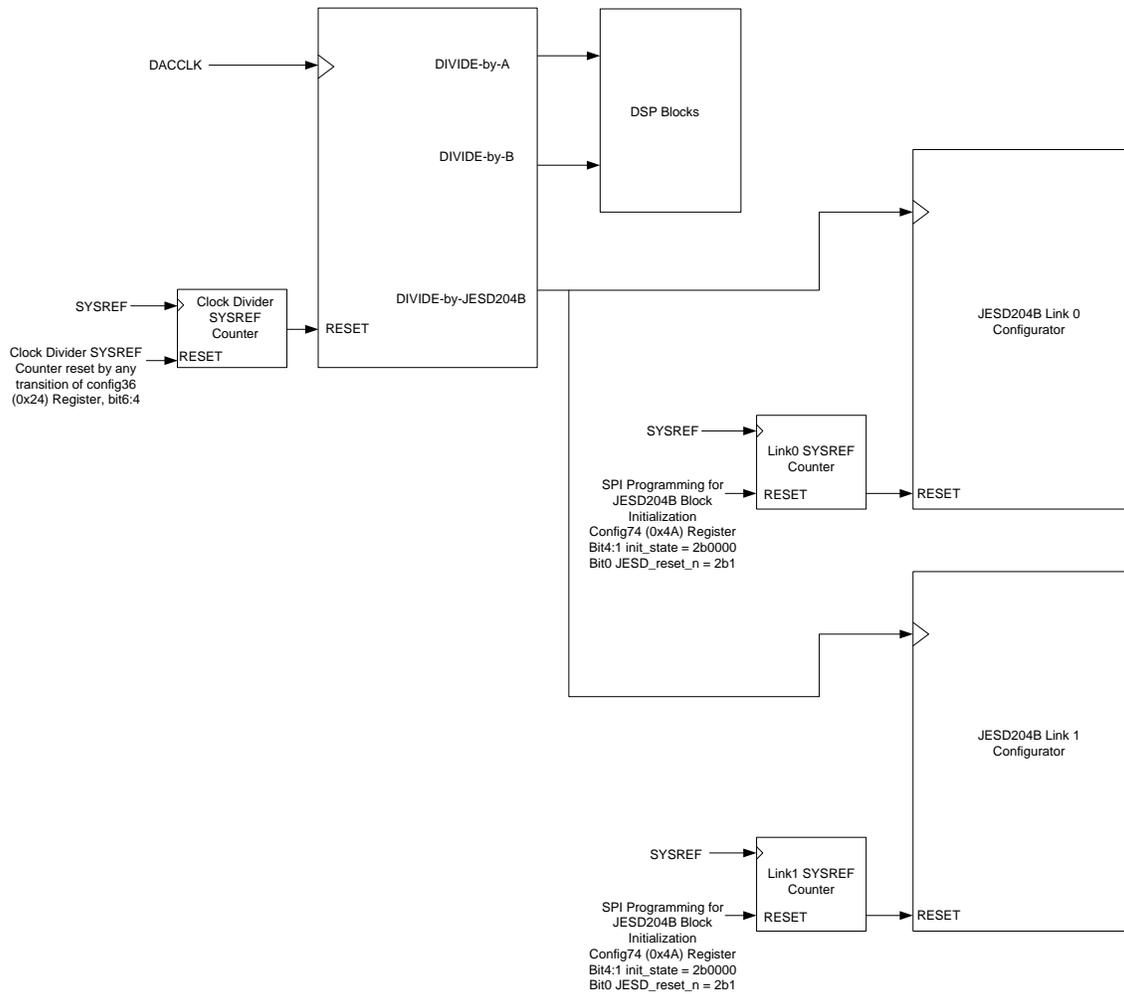
Figure 1. Clock Divider and JESD204B Simplified Circuit Diagrams

The JESD204B logic block will operate on one of the divided-down clocks from the clock divider. The DAC3xJ8x JESD204B only supports up to two independent links (i.e. Link1 and Link0). If only one link is used, then the default link should be link0. Therefore, only sysref_mode_link1 and sysref_mode_link0 should be configured. Both sysref_mode_link3 and sysref_mode_link2 should be set to 2b'000.

Both the clock divider and JESD204B block are the essential blocks for the JESD204B link initialization. After both blocks are initialized through the triggering of SYSREF pulse, the JESD204B link initialization will start. Basically, the DAC3xJ8x will issue a sync request to the JESD204B TX (default configuration behavior is to pull the LVDS SYNCB pair from logic HIGH to logic LOW). The JESD204B TX will start the CGS stage, which is the beginning of the JESD204B link start-up.

Clock Divider and JESD204B Logic Core Initializer

The clock divider and JESD204B block initializers require SYSREF signal to provide correct initialization for the DAC3xJ8x device operation. They can be armed to register all SYSREF pulses or to register only the first, the second, or the third pulse. The exact configuration for the clock

divider depends on config36, bit6:4 cdrvserv_sysref_mode, while the configuration for the JESD204B block depends on config92, bit6:4 sysref_mode_link1, and config92, bit2:0 sysref_mode_link0.

For the clock divider, the start of the clock divider reset pulse count is based on any SPI register transition of config36 (0x24) Register, bit6:4. Basically, upon programming of the cdrvser_mode_sysref register, the clock divider reset counter for SYSREF will start and determine which SYSREF pulse to use. TI recommends user to initialize the clock divider logic before the JESD204B link0 and link1 logic since the link0 and link1 logic blocks derive their clock from the main clock divider.

For the Link0 and Link1 logic block, the start of the SYSREF pulse count for the initializer will be based on the time instance when JESD204B block is initialized through config74, init_state = 2b'0000 and config74, jesd_reset_n = 2b'1. These register writes allows the JESD204B block initializers to start and begin counting the SYSREF edges. Note that the JESD204B blocks can be initialized at a later time by deterministic SYSREF pulses. The SYSREF pulse to the clock divider and to the JESD204B logic block do not have to be the same. They just have to have the same relationship even after certain period of time. Basically, the SYSREF pulses have to occur at the expected time without any time delay or phase shift.
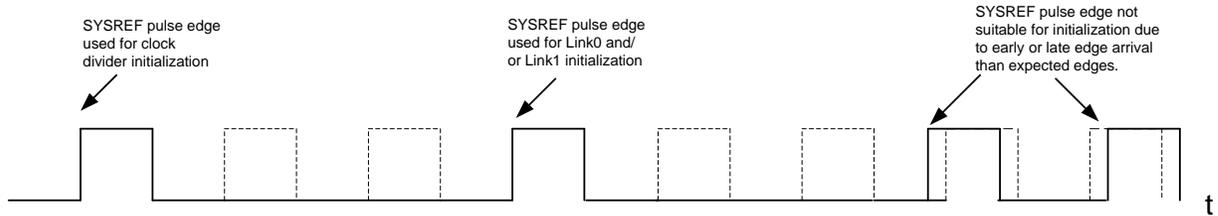

Figure 2 SYSREF pulses used for clock divider and link0/link1 initialization with deterministic relationship.

Register Name: config36 – Address: 0x24, Default: 0x0000

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config36	0x24	15:13	reserved	Reserved	000
		12:7	reserved	Reserved	000000
		6:4	cdrvser_ sysref_mode	Determines how SYSREF is used to sync the clock dividers in the device. 000 = Don't use SYSREF pulse 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses.	000
		3:2	reserved	Reserved	00
		1:0	reserved	Reserved	00

Register Name: config92 – Address: 0x5C, Default: 0x1111

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config92	0x5C	15	err_cnt_ clr_link3	A transition from 0≥1 causes the error_cnt for link3 to be cleared.	0
		14:12	sysref_ mode_link3	Determines how SYSREF is used in the JESD synchronizing block. 000 = Don't use SYSREF pulse 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses. 101 = Skip two SYSREF pulses then use only the next one 110 = Skip two SYSREF pulses then use all pulses.	001
		11	err_cnt_ clr_link2	A transition from 0≥1 causes the error_cnt for link2 to be cleared.	0
		10:8	sysref_ mode_link2	Determines how SYSREF is used in the JESD synchronizing block. 000 = Don't use SYSREF pulse 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses. 101 = Skip two SYSREF pulses then use only the next one 110 = Skip two SYSREF pulses then use all pulses.	001
		7	err_cnt_ clr_link1	A transition from 0≥1 causes the error_cnt for link1 to be cleared.	0
		6:4	sysref_ mode_link1	Determines how SYSREF is used in the JESD synchronizing block. 000 = Don't use SYSREF pulse 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses. 101 = Skip two SYSREF pulses then use only the next one 110 = Skip two SYSREF pulses then use all pulses.	001
		3	err_cnt_ clr_link0	A transition from 0≥1 causes the error_cnt for link0 to be cleared.	0
		2:0	sysref_ mode_link0	Determines how SYSREF is used in the JESD synchronizing block. 000 = Don't use SYSREF pulse 001 = Use all SYSREF pulses 010 = Use only the next SYSREF pulse 011 = Skip one SYSREF pulse then use only the next one 100 = Skip one SYSREF pulse then use all pulses. 101 = Skip two SYSREF pulses then use only the next one 110 = Skip two SYSREF pulses then use all pulses.	001

Register Name: config74 – Address: 0x4A, Default: 0x001E

Register Name	Addr (Hex)	Bit	Name	Function	Default Value
config74	0x4A	15:8	lane_ena	Turn on each SerDes lane as needed. Signal is active high. bit15 : SerDes lane7 enable bit14 : SerDes lane6 enable bit13 : SerDes lane5 enable bit12 : SerDes lane4 enable bit11 : SerDes lane3 enable bit10 : SerDes lane2 enable bit9 : SerDes lane1 enable bit8 : SerDes lane0 enable	0x00
		7:6	jesd_test_seq	Set to select and verify link layer test sequences. The error for these sequences comes out the lane alarms bit0. 1= fail and 0 = pass. 00 : test sequence disabled 01 : verify repeating D.21.5 high frequency pattern for random jitter 10 : verify repeating K.28.5 mixed frequency pattern for deterministic jitter 11 : verify repeating ILA sequence	00
		5	dual	Turn on "DUAL DAC" mode. This disables the clocks to the C and D data paths, reducing the power of the DIG block.	0
		4:1	init_ state	Put the JESD block into "INIT_STATE" mode when high. During this mode the JESD can be programmed and its outputs will stay at zero. NOTE: See the JESD description of the correct startup sequence.	1111
		0	jesd_ reset_n	Reset the JESD block when low. NOTE: See the JESD description of the correct startup sequence.	0

Clock Divider SYSREF Counter reset by any transition of config36 (0x24) Register, bit6:4

For link 0 and link 1 configuration, the pulse count start after the following JESD204B Initialization Register:

init_state = 2b'1111 and jesd_reset_n = 2b'0

init_state = 2b'1111 and jesd_reset_n = 2b'1

init_state = 2b'0000 and jesd_reset_n = 2b'1

SYSREF Gating

Once the overall system establishes DAC3xJ8x JESD204B RX link to the system JESD204B TX link, the SYSREF signal to the DAC3xJ8x may be turned off to save power consumption and also reduce noise coupled into the DAC3xJ8x output. If cdrvser_sysref_mode, sysref_mode_link1, and sysref_mode_link0 are set to register only single rising edge of SYSREF, the SYSREF signal may be turned off at any time after the link is established. TI recommend to set clock divider and JESD204B block initializer to register single SYSREF pulse if possible to prevent false re-initialization due to potential SYSREF glitches or noise coupling. Also, since the clock divider provides the JESD204B clock, TI recommends system designers to initialize the clock divider using either the first or second pulse, and then initialize the JESD204B block using either the

second or the third pulse. Basically, the initialization of the JESD204B block is staggered behind the initialization of the clock divider.

Some system designers may prefer continuous SYSREF signal present at all time to ensure stable system synchronization. Typically in this situation, the clock divider and JESD204B block are set to register all SYSREF pulses. If at any time the SYSREF signal need to be disabled, system designer need to further plan additional transient behaviors depending on the network between the SYSREF driver and SYSREF receiver. The easiest approach would be first to set cdrvser_sysref_mode, sysref_mode_link1, and sysref_mode_link0 to all zeros to prevent clock divider and JESD204B logic from re-initialized due to the transients of disabling SYSREF. After programming these initializers to all zeros, disabling SYSREF will not affect these digital core blocks. The approach to prevent transient behaviors from false triggering the SYSREF receiver are described in both sections of AC Coupled Approach and DC Coupled Approach.

SYSREF Initialization for DSP Blocks

Various DSP blocks on the DAC3xJ8x such as NCO, mixer, and QMC may be initialized by SYSREF as an option. This is one of the best options to achieve deterministic initialization to multiple device DSP blocks.

11.0   Syncing the design

The syncing in the DAC38J84 is generalized like the DAC3484, however it is much simpler. There are no brute force handoffs across a FIFO. The only sync from the input side of things is from the JESD block. This sync only fires off one pulse at the completion of the ILA sequence. It can be used to sync NCOs of different chips. The **SYSREF** can also be used but is trickier because of the clock dividers and JESD block. Both of these blocks will have to be programmed to not look at the **SYSREF** if it is going to be used to sync other blocks. The same AUTOSYNC structure used in the DAC3484 is also used for the mixer, qmc and qmoffset blocks. There is also a *mem_sif_sync* that can be used to sync the design through the SIF port, although multiple chips cannot be aligned using this type of syncing.
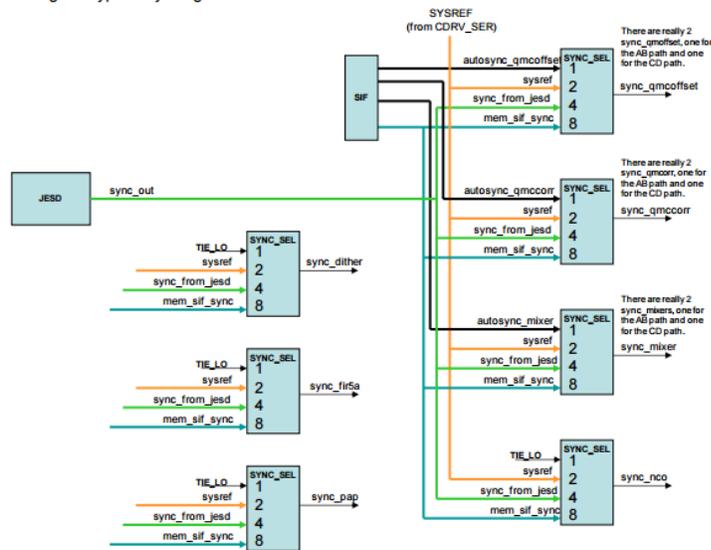

Figure 13 DIG block syncing hookup

The most suitable initialization SYSREF signal for these DSP blocks is a single pulse SYSREF. Using these DSP block would require the JESD204B link to be established, therefore the initialization of these DSP block would come after the clock divider and JESD204B block initialization. TI recommends setting the clock divider and JESD204B block to register only single pulse based SYSREF or to disable registering SYSREF after link establishment. This will prevent the JESD204B link from false re-initialization when the DSP blocks are being initialized with SYSREF pulses.

Using periodic SYSREF pulses to initialize these DSP blocks may cause periodic interruption to the DSP operation. For instance, if the NCO accumulator is initialized by the SYSREF with periodic pulses, then the NCO frequency must be integer multiple of the SYSREF period. Otherwise, the NCO accumulator cannot cycle through the counter completely before the next SYSREF reset. Use the SYSREF initialization feature with caution.
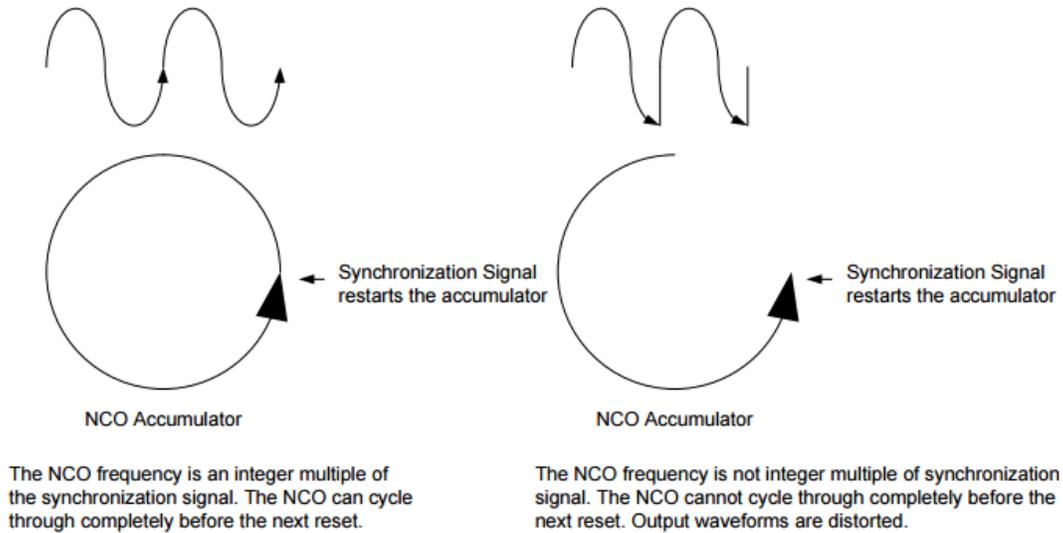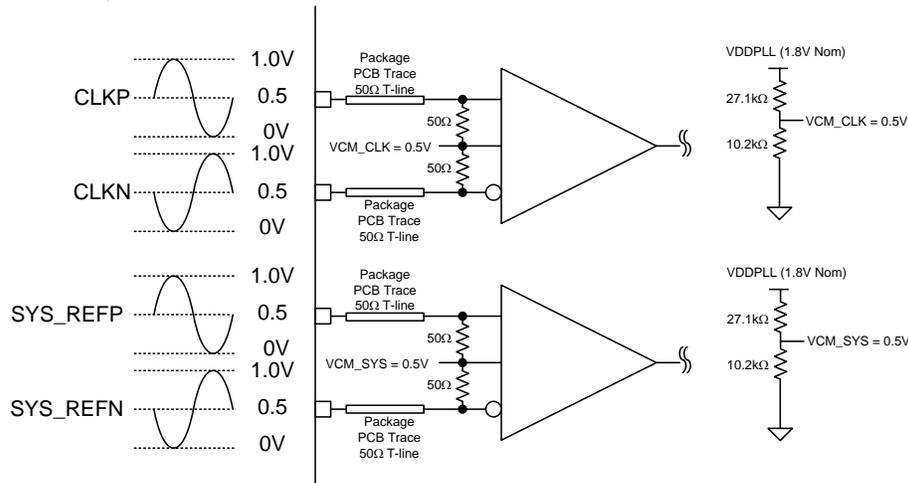

Figure 33. NCO Accumulator Operation with Repetitive Synchronization Signals
(copy from SLAA584, figure 33)

DAC3xJ8x DACCLK and SYSREF Receivers

The DAC3xJ8x DACCLK and SYSREF receivers have delay matched receiver design given the external clock and SYSREF inputs have identical driver behavior and are AC coupled. The internal resistor divider networks set the common mode voltage of the DACCLK and SYSREF receivers at 0.5V nominal.

Each input leg of the receiver has on-chip 50ohm termination that is tied to the respective VCM node. Based on the DAC3xJ8x datasheet, the minimum swing for each leg is 400mVpp of |Vid|.

Since the input presented at each pin cannot swing below ground, the maximum swing for each leg can theoretically be 1Vpp of |Vid|.

To achieve high clock signal performance, both the DACCLK and SYSREF receivers do not have any hysteresis mechanism build-in. Therefore, if any of the digital core initializers are actively looking for SYSREF while the SYSREF receiver inputs are both set at VCM, these digital circuits may register false SYSREF triggering, mainly from noise disturbance near receiver threshold. If any digital block initializers are actively registering SYSREF signal, a differential voltage of 100mVpp must be present at SYSREF receiver to avoid false triggering due to noise disturbance.

The timing relationship between the DACCLK and SYSREF signal is very stringent in a JESD204B system. Therefore, the signal path network of the DACCLK and SYSREF signals must be as similar as possible to ensure that the signal relationship is maintained from the launch of the signal, through their respective channels to the DACCLK and SYSREF input receivers. The SYSREF timing requirements depend on whether deterministic latency of the JESD204B link is required. If deterministic latency is required, then the SYSREF signal must meet setup and hold requirements relative to the DACCLK signal. If deterministic latency is not required, then the SYSREF signal may be supplied as an asynchronous signal resulting in latency variation in the orders of multiple multi-frame period.

TI recommends AC coupling for the SYSREF interface as described in section "AC Coupled Network". For certain instances, DC coupled SYSREF interface may also be implemented with discretion. Please see section "DC Coupled Network" for detail.

AC Coupled Approach

The AC coupled network ensures both the DACCLK and SYSREF signal timing are well matched and controlled, given the DACCLK and SYSREF drivers are identical in behavior. Due to this reason, TI recommends this network for applications requiring deterministic latency across the DAC3xJ8x device or multiple DAC3xJ8x devices synchronization.
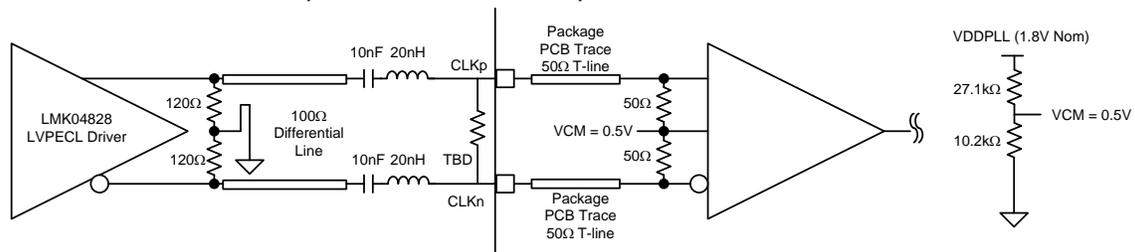
The AC coupled network requires series capacitors to allow the common mode voltage on both the SYSREF driver and SYSREF receiver to establish independently. Therefore, the series capacitors, along with the DAC3xJ8x SYSREF receiver on-chip 50ohm termination, forms a high pass response to isolate the common mode voltage of the driver and receiver. The high pass corner is the typical first order response with cut-off frequency and time constant as follow:

$$Fc = \frac{1}{2\pi RC} \qquad \tau = RC$$

Compatible SYSREF Signals for AC Coupled Networks

The AC coupled network allows the implementation of the typical three types of SYSREF signals: periodic, gapped periodic, or one shot pulse. Periodic SYSREF signal is the most ideal situation for overall system synchronization because this maintains constant, steady bias for both the driver and receiver and also allows consistent SYSREF pulses for device synchronization. When implementing gapped periodic or one shot pulse, however, system designers must pay special attention to the SYSREF driver and the overall AC coupled network. The ideal SYSREF driver for gapped periodic or one shot pulse is that the driver must maintain common mode bias between idle period and active period. This behavior maintains the charge of the series capacitor and will not impact the SYSREF waveform at the receiver side. The trade-off is mainly based on the concern for double sideband spurs and additional power consumptions due to active SYSREF driver. Refer to Table TBD for detail.

|	Periodic	Gapped Periodic/One Shot
Benefits	Constant, steady bias for both driver and receiver. Consistent, timely SYSREF pulses for device synchronization. Active SYSREF signaling prevents potential false SYSREF triggering at the receiver due to noise disturbance.	No risk for double sideband spurs due to active SYSREF driver. Saves system power consumption by disabling SYSREF driver. Useful for initializing various DSP blocks such as QMC and Mixer in multiple DAC3xJ8x device synchronization scenario. Clock Divider and JESD204B blocks must be programmed to not register SYSREF after JESD204B link establishment to avoid false re-initialization of the link.
Drawbacks	Potential double sideband spurs modulated onto the DAC output spectrum. Additional power consumption from active SYSREF driver. Difficult to implement DSP block initialization due to the cyclic nature of SYSREF. For instance, the NCO frequency may not be correct due to continuous reset of SYSREF pulses.	SYSREF driver must be pre-biased at its own VCM to avoid transients during active state. SYSREF receiver may register false SYSREF triggering during SYSREF driver idle state. If any digital block initializers are actively registering SYSREF signal, a differential voltage of 100mVpp must be present at SYSREF receiver to avoid noise disturbance.

SYSREF Driver Constraints for Gapped Periodic or One Shot SYSREF

As long as the SYSREF driver can maintain its own VCM, and ensure the VCM does not change between idle and active state, system designer may implement gapped periodic or one-shot SYSREF for AC coupled network. The TI TINA SPICE simulation below shows a typical LVPECL driver interfacing with the DAC3xJ8x SYSREF receiver in AC coupled fashion. The driver has a typical VOH of 2.21V and VOL of 1.25V, and the VCM of the driver at steady state is 1.73V. The AC coupling capacitor is the typical 100nF value with on-chip 50ohm resistor at the SYSREF receiver. The time constant is in the range of 5us. The driver has been pre-biased at 1.73V for 100us of simulation time and started to toggle immediately after 100us. At the receiver side after the AC coupling capacitor, the toggling remains smooth and no transients were observed due to the driver pre-bias at VCM.
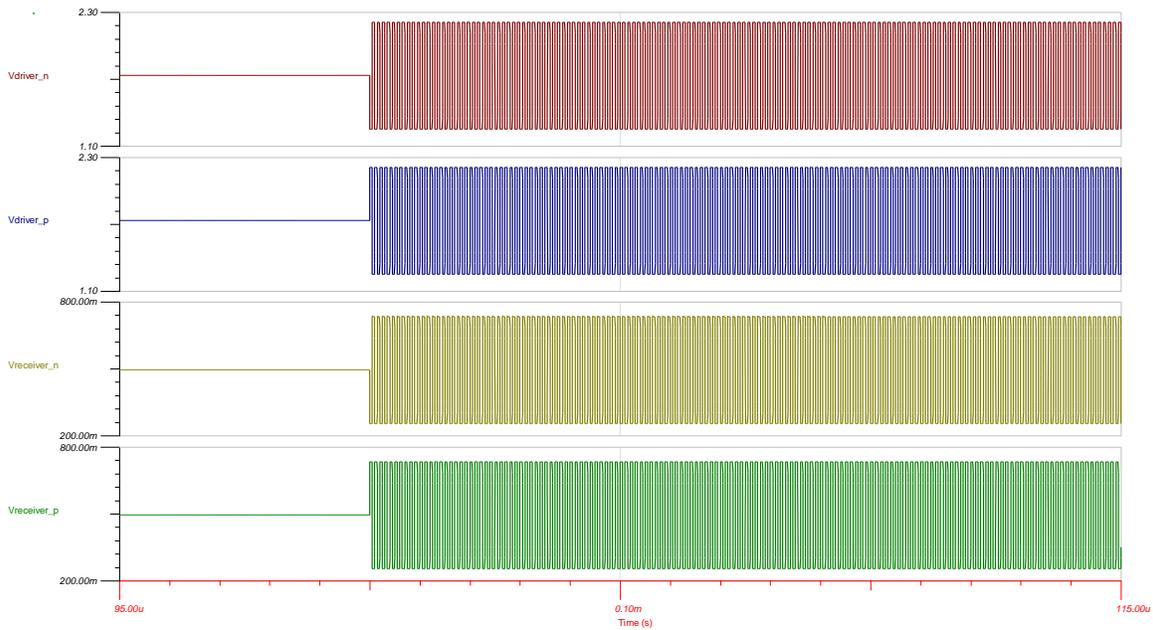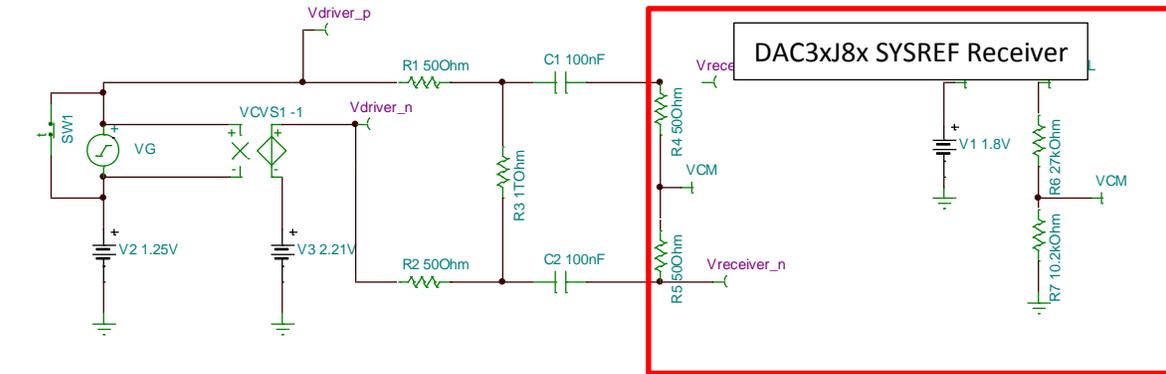
If the SYSREF driver cannot maintain common mode voltage between idle period and active period, then the charge of the series capacitor will be disturbed in between the period. Since the voltage delta across a capacitor cannot change instantaneously, the SYSREF waveform at the receiver side may rise above or fall below (depending on the initial voltage delta across the cap) such that the initial waveforms may impact the receiver behavior due to the variation of the VCM on both legs of the receiver input.

For instance, consider the SYSREF driver that will transition to one leg at VOH and another at VOL during idle time and transition to VCM during active time. Upon triggering of the active state for the SYSREF, it may take a couple of time constants for the VCM to settle. During the initial stage, the SYSREF may not register the SYSREF signal correctly.
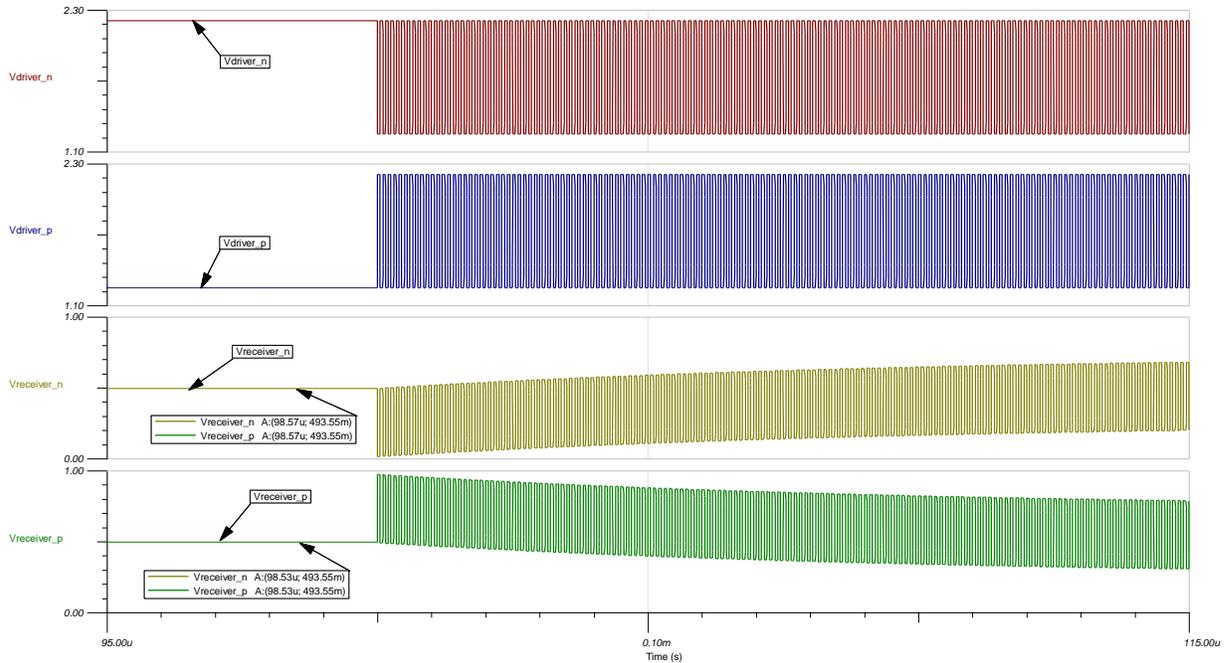
For situations similar to the one described above where the SYSREF driver having a pre-bias of either differential logic HIGH or differential logic LOW, system designer may consider adding a set of parallel L+R network to balance out the differential driver at VCM. The inductor basically provides a DC short to balance out the VCM, and the resistor is used to tune out the voltage delta between the two legs if the sink and source current are different. With this implementation, the designers need to consult with the SYSREF driver manufacturer for such recommendation and evaluate the impact of such network to the operating lifetime of the SYSREF driver. The SYSREF driver can be tuned to be pre-biased with symmetrical VCM for smooth transition before and after the driver active stage. Also, the AC coupling capacitor value may also be increased to maintain VCM stability longer due to larger amount of charges in the capacitor.
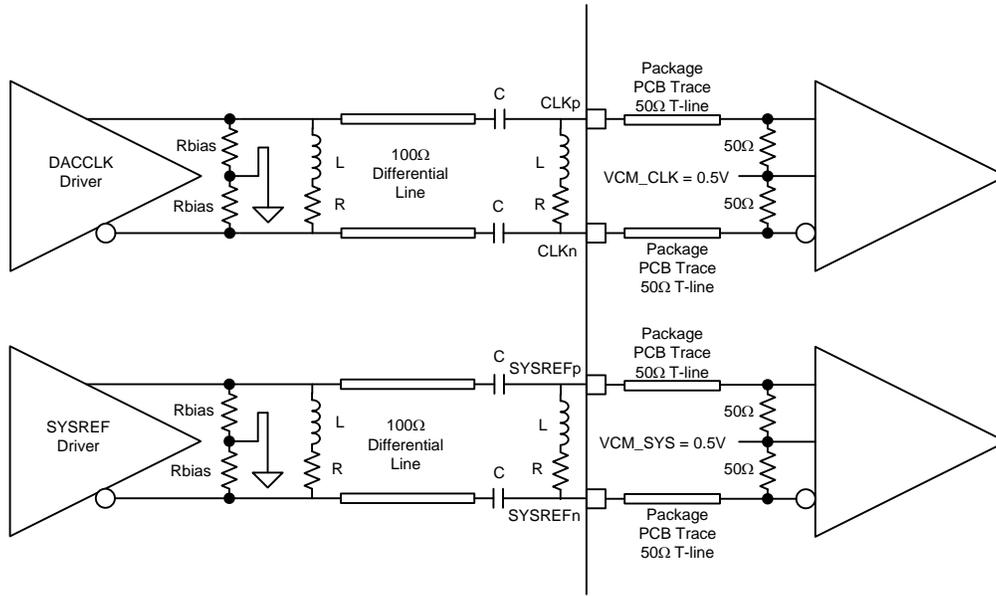
Moreover, both the DACCLK and SYSREF receiver path may have such implementation to form a part of a matched bandpass network. The PCB layout of both paths may be matched, but the exact bandpass frequency and components may not match since the DACCLK is usually a much higher frequency than SYSREF. This may be an option if the DACCLK port is being used as a slow reference clock for the DAC3xJ8x on-chip PLL path.

Digital Block Initializer Configuration for AC Coupled Network

Regardless of the SYSREF signal type, both the clock divider and JESD204B block initializer should register only a single pulse of SYSREF. As mentioned in the clock divider and JESD204B block section, since the clock divider provides the JESD204B clock, TI recommends system designers to initialize the clock divider using either the first or second pulse, and then initialize the JESD204B block using either the second or the third pulse. Basically, the initialization of the JESD204B block is staggered behind the initialization of the clock divider. If there are concerns regarding the common mode voltage stability during the initial SYSREF driver idle to active transition, initialize the clock divider using the second pulse and then initialize the JESD204B using the third pulse. The overall JESD204B link initialization requires least three gapped SYSREF pulses in this case.

	First Pulse Only	Second Pulse Only	Third Pulse Only
Clock Divider (Config36 0x24 Register)	0x20	**0x30**	N/A
JESD204B Block (Config92 0x5C Register)	Single Link: 0x0002 Dual Link: 0x0022	Single Link: 0x0003 Dual Link: 0x0033	**Single Link: 0x0005 Dual Link: 0x0055**

Indicate Recommended Setting

Clock Divider SYSREF Counter reset by any transition of config36 (0x24) Register, bit6:4

For link 0 and link 1 configuration, the pulse count start after the following JESD204B Initialization Register:

init_state = 2b'1111 and jesd_reset_n = 2b'0
init_state = 2b'1111 and jesd_reset_n = 2b'1
init_state = 2b'0000 and jesd_reset_n = 2b'1

Various DSP blocks such as NCO and QMC may be initialized by SYSREF if needed. As mentioned earlier, the most suitable initialization SYSREF signal for these DSP blocks is a single pulse SYSREF. Since the clock divider and JESD204B blocks already registered single pulse during link initialization and would ignore all other pulses, re-issuing of SYSREF to these DSP blocks will not trigger false link re-initialization.

Hysteresis Setup for AC Coupled Network

If these DSP blocks are programmed to initialize with SYSREF, then the respective initializer will constantly register any SYSREF pulses. Depending on system requirement, these DSP block initializer may not be turned off and will have to be programmed to be initialize with SYSREF at all time. This may be the case for systems requiring multi-DAC3xJ8x devices synchronization. The main concern in this particular setup is that both SYSREF receiver input legs are self-biased at VCM. Any noise disturbance on the receiver input will false trigger the initializers.

To avoid false triggering of SYSREF due to noise disturbance to the SYSREF receiver input, designers may add a pull-up and pull-down network to create hysteresis. The following network introduces 100mVpp differential to the SYSREF receiver. The equivalent AC load is slightly less than 100ohm differential since the pull-up/pull-down network are fairly large value when compared to on-chip 100ohm termination. Since SYSREF is a low speed signal, the impact to SYSREF terminal signal integrity is minimum.
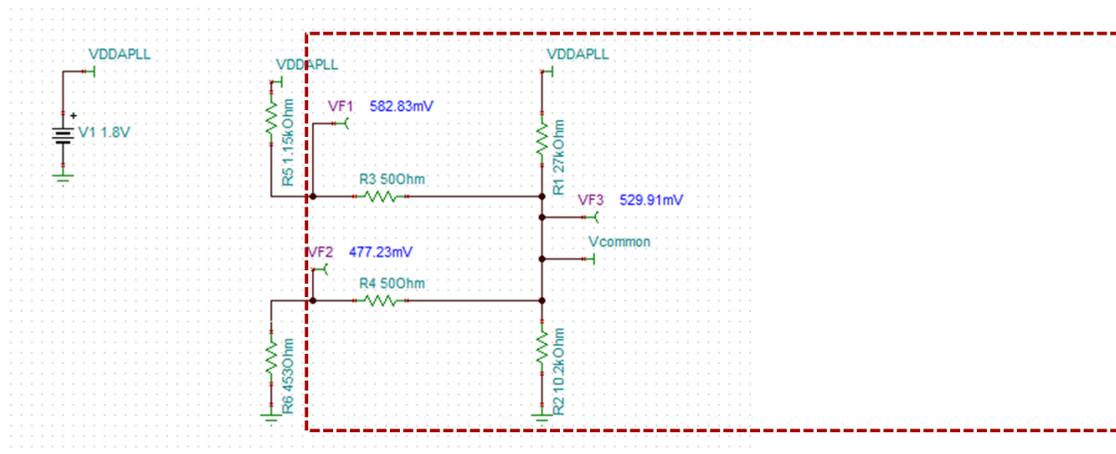

Typical Start-up Procedure for AC Coupled SYSREF Network

1. Power up the FPGA/ASIC and start the JESD204B transmitter system.
2. Power DAC3xJ84 and Provide DACCLK. For periodic SYSREF, the SYSREF may be provided at anytime as long as the SYSREF driver can maintain stable VCM and minimum transients during JESD204B link establishment.

3. Reset DAC3xJ8x by toggling the RESETB pin from logic HIGH to logic LOW and then back to Logic HIGH.
4. Program DAC3xJ8x per applications need.
    1. Clocking Configurations Registers: On-chip PLL: config49 (0x31) to config51 (0x33)
    2. SERDES Parameter: config59 (0x3B) to config63 (0x3F)
    3. JESD204B parameters: config70 (0x46) to config98 (0x62)
    4. Various DSP blocks: enable the blocks through config0 (0x00) to config2 (0x02) and program respective filter coefficients from config 8 (0x08) to config25 (0x19). DSP block initializers are set from config30 (0x1E) to config32 (0x20).
5. Check alarm_from_pll, alarm_rw0_pll, and alarm_rw1_pll (if applicable) in config108, 0x6C to see if the on-chip PLL and SERDES PLLs are locked. If not, please check the DAC programming and DACCLK.
6. Program config74 (0x4A) to initialize JESD204B block of the DAC (i.e. init_state = 2b'1111 and jesd_reset_n = 2b'0). The SYNCB should be in logic HIGH at this point.
7. Alarm_sysref_err in config0x6c are active at this point.
8. Program Config36 (0x24) = 0x30 => clock divider use sysref skip one pulse and then use next
9. Program Config92 (0x5c) = 0x0005 => use skip two pulses and then use next. Ignore link1, link2, and link3 since they are not used.
10. Clear sysref alarm at this point. Repeat step 7 to 10 again if error persists.
11. Program Config74 (0x4A) to initialize JESD204B block of the DAC (0x4A = 0x0F1F. init_state = 2b'1111 and jesd_reset_n = 2b'1).
12. Program Config74 (0x4A) to initialize JESD204B block of the DAC (0x4A = 0x0F01. init_state = 2b'0000 and jesd_reset_n = 2b'1).
13. Clear alarm_sysref_err in config108, bit13 for link1 (if needed), and bit12 for link0 at this point. Repeat step 7 to 13 again if error persists.
14. If periodic SYSREF is present or if gapped periodic SYSREF is triggered, the LVDS SYNCB should be in logic Low.
15. SYSREF may be disabled as long as VCM remains stable. This can be done at much later time to prevent possible transient pulses affecting the link initialization.
16. Please check for alarms in registers config100 (0x64) to config109 (0x6D) and also ALARM CMOS pin. If error is observed, please repeat steps 6 to step 16 again to ensure correct SYSREF is provided for LMFC alignment.
Check for standard JESD204B errors, FIFO errors, and LOS errors. If these errors are observed, TI recommends to repeat steps 6 to 15 to ensure optimal initialization.
    1. For the JESD204B errors, JESD204B standard requires at least resync upon code synchronization error, 8b/10b not in table error, and 8b/10b disparity error.
    2. The end user will need to decide how to response to other JESD204B errors.
17. If DAC3xJ8x is error free, enable TXENABLE and start DAC output transmission.

DC Coupled Approach
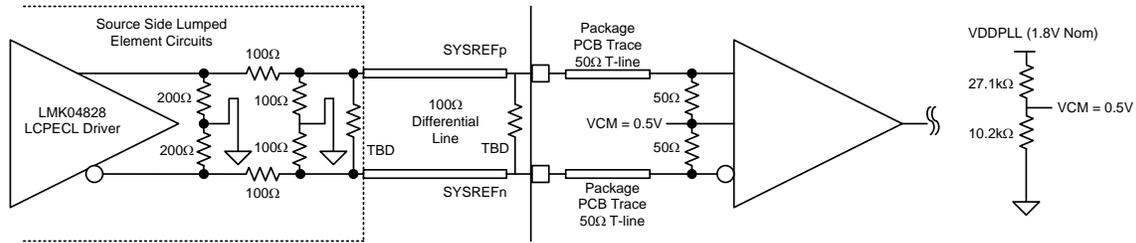
System design may implement DC coupled network for the SYSREF receiver with discretions. The primary reason to implement DC coupled network is to utilize pulsed SYSREF without concerns from SYSREF driver pre-bias and RC time constant. Due to various scenarios and driver interface types, this section highlights an example based on DAC3xJ8x EVM design. The concern for DC coupled network is mainly driven by the fact that the DACCLK and SYSREF may have different coupling network and different driver behavior, and difference in behavior may cause slight mismatch in the overall propagation delay between the DACCLK path and SYSREF path.

The ideal scenario for DC coupled approach is to provide DC coupled network for both the DACCLK and SYSREF paths. However, other limitations arise such as the clock driver amplitude and phase noise performance. For instance, the DAC3xJ8x EVM has the DACCLK AC coupled while the SYSREF is DC coupled. The main reason to keep the DACCLK AC coupled is that the LVPECL driver on the LMK04828 side can achieve the best phase noise performance in this condition. DC coupling would require LCPECL driver, which does not have as high of phase noise performance as AC coupling with LVPECL driver. We typically recommend high clock swing drivers such as LVPECL to allow the DAC to achieve the best noise performance.

If DACCLK path has the LVPECL, AC coupled network while the SYSREF path has the LCPECL, DC coupled network, system designer must ensure that under these conditions, the delay of the DACCLK path and the delay of the SYSREF are matched. This would involve the IBIS modeling of the clock driver delay propagation and associated PCB trace delay simulation. Physical measurements may be needed to ensure matched delay. In the EVM scenario, both the digital and analog delay feature of the LMK04828 can compensate the potential propagation delay difference.

Regarding the SYSREF input bias on default EVM setup, LMK04828 drives the SYSREF in DC coupled fashion with LCPECL driver. The common mode is divided down to 0.5V through resistor divider. The LMK04828 driver can be programmed such that during idle state, the SYSREF driver will output VOH and VOL on the positive and negative leg of the driver, respectively. The idle state can be continuous SYSREF mode with driver power down or in pulsed SYSREF mode with the pulses finished. This creates 0.55V and 0.45V on the positive and negative input of the SYSREF receiver. The 100mV difference is sufficient to prevent unintended assertions.

The major benefit of DC coupled approach is elimination of potential delay due to RC time constant. Since DC coupling does not have capacitors to charge up, the SYSREF pulses can trigger the initialization blocks immediately. System design may implement pulsed SYSREF signal freely once the concern of propagation delay is compensated. Start-up procedures for DC coupled network remains the same as start-up procedures for AC coupled network except that periodic SYSREF is removed from this scenario.

Typical Start-up Procedure for DC Coupled SYSREF Network

1. Power up the FPGA/ASIC and start the JESD204B transmitter system.
2. Power DAC3xJ84 and Provide DACCLK.
3. Reset DAC3xJ8x by toggling the RESETB pin from logic HIGH to logic LOW and then back to Logic HIGH.
4. Program DAC3xJ8x per applications need.
   1. Clocking Configurations Registers: On-chip PLL: config49 (0x31) to config51 (0x33)
   2. SERDES Parameter: config59 (0x3B) to config63 (0x3F)
   3. JESD204B parameters: config70 (0x46) to config98 (0x62)
   4. Various DSP blocks: config0 (0x00) to config2 (0x02) and respective coefficients from config 8 (0x08) to config25 (0x19). DSP block initializers are set from config30 (0x1E) to config32 (0x20).
5. Check alarm_from_pll, alarm_rw0_pll, and alarm_rw1_pll (if applicable) in config108, 0x6C to see if the on-chip PLL and SERDES PLLs are locked. If not, please check the DAC programming and DACCLK.
6. Program config74 (0x4A) to initialize JESD204B block of the DAC (i.e. init_state = 2b'1111 and jesd_reset_n = 2b'0). The SYNCB should be in logic HIGH at this point.
7. Alarm_sysref_err in config0x6c are active at this point.
8. Program Config36, 0x24 = 0x30 => clock divider use sysref skip one pulse and then use next
9. Program Config92, 0x5c = 0x0005 => use skip two pulses and then use next. Ignore link1, link2, and link3 since they are not used.
10. Clear sysref alarm at this point. Repeat step 7 to 10 again if error persists.
11. Program Config74 (0x4A) to initialize JESD204B block of the DAC (0x4A = 0x0F1F. init_state = 2b'1111 and jesd_reset_n = 2b'1).
12. Program Config74 (0x4A) to initialize JESD204B block of the DAC (0x4A = 0x0F01. init_state = 2b'0000 and jesd_reset_n = 2b'1).
13. Clear alarm_sysref_err in config108, bit13 for link1 (if needed), and bit12 for link0 at this point. Repeat step 7 to 13 again if error persists.
14. If periodic SYSREF is present or if gapped periodic SYSREF is triggered, the LVDS SYNCB should be in logic Low. Disable SYSREF with known logic level present at SYSREF port.
15. Please check for alarms in registers config100 (0x64) to config109 (0x6D) and also ALARM CMOS pin. If error is observed, please repeat steps 6 to step 16 again to ensure correct SYSREF is provided for LMFC alignment.
    Check for standard JESD204B errors, FIFO errors, and LOS errors. If these errors are observed, TI recommends to repeat steps 6 to 15 to ensure optimal initialization.
    1. For the JESD204B errors, JESD204B standard requires at least resync upon code synchronization error, 8b/10b not in table error, and 8b/10b disparity error.
    2. The end user will need to decide how to response to other JESD204B errors.
16. If DAC3xJ8x is error free, enable TXENABLE and start DAC output transmission.