DIGITAL POST-CORRECTION OF ANALOG-TO-DIGITAL CONVERTER

[1]PRADIP MANE, [2]P.L.PAIKRAO

[1]M.Tech, [2]Assistant Professor, Electronics & Telecommunication Engineering Department,
GCOE Amravati, Maharashtra, INDIA
E-mail: [1]manepradip18491@gmail.com, [2]plpaikrao@gmail.com

Abstract— As the rapid change in the wireless communication system and mobile video devices, the integrated chip with less power consumption and maximum conversion efficiency is needed. ADC and DAC are playing an important role in these applications. The aim of this paper is to verify a post-correction method which is used for improving the performance of ADC. Which effectively minimize both static nonlinearities and memory effects. Refer to this model, one post-correction method is described and verified. Based on the post-correction, this method is used to modify the output signals which have been converted from analog to digital format by adding a correction term. Simulation results show excellent performance using this method.

Keywords— Volterra Series, THD, SiNAD, SFDR, Post-Correction Model, ADC.

I. INTRODUCTION

The analog-to-digital converter (ADC) take a important role in communication systems and various applications, such as electronic devices, instruments and sensor networks. As current trend is to move more and more of the functionality of a communication system into the digital domain in order to provide an increased flexibility and reduced cost, the industry has consistently asked the performance of ADCs. For high data rate and a high dynamic range, ADCs become nonlinear, which causes mismatches and distortion to the input signal and thus degrades the performance of the system[5].
With the continuous increment of CMOS technology, digital circuit can be made with very low power consumption and low cost. So that the digital calibration become popular in ADC calibration "black-box" based digital post-corrections have attracted significant attention.

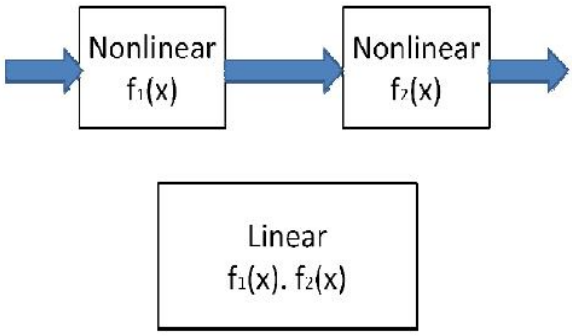

Figure 1

The basic concept of this paper is that when nonlinear system of these is to apply an inverse nonlinear function of same sysem then the output system become linear. Same concept is apply to the digital output of the ADC to generate a compensation signal that is then subtracted from the original output in order to restore signal fidelity. This digital correction unit treats the ADC as a black-box, so that it does not require detailed knowledge of the internal circuits of the ADC, while also independent of ADC architectures.
Some research works have already demonstrated this calibration approach by various behavioral models including

1) Hammerstein model
2) Volterra series model
3) Decoupled Wiener model
4) Adaptive digital filter

In these works, researchers verify their algorithms based on the calibration performances using different simulation tools.
The design of post-correction of ADC is going through different difficulties in terms of size, cost and power consumption. For demonstration of how the algorithm works, it is necessary to realize hardware implementation that will disclose more practical problems which are occurs in circuits such as computational complexity, latency, bit-precision and digital noise.

II. TERMS IN ADC

Total Harmonic Distortion(THD):
THD is defined as: Nonlinearity in the data converter results in harmonic distortion when analyzed in the frequency domain. Such distortion is observed as "spurs" in the FFT at harmonics of the measured signal as illustrated in Figure 10. This distortion is referred to as *total harmonic distortion (THD)*,

$$\mathrm{THD} = 20\log\left(\frac{\sqrt{V_2^2 + V_3^2 + \ldots + V_n^2}}{V_1}\right)$$

Signal-to-noise and distortion (SiNAD):

SiNAD offers a more complete picture by including the noise and harmonic distortion in one specification. SiNAD gives a description of how the measured signal will compare to the noise and distortion. You can calculate the SiNAD ratio using following Equation

$$\text{SiNAD} = 20\log\left(\frac{V_1}{\sqrt{V_2^2 + V_3^2 + \ldots + V_n^2 + V_{noise}^2}}\right)$$

Effective Number of Bits (ENOB):

The effective number of bits is related to the SINAD of the ADC. In (1.5) the relation between the number of bits *b* and the SINAD of an *ideal* ADC was given. For a practical converter the SINAD will be lower. The effective number of bits should be interpreted as the number of bits required in an ideal converter to achieve a certain SINAD.

Spurious-Free Dynamic Range (SFDR):

The difference (in dB) between the amplitude of the fundamental and the largest harmonic or spur (from dc to half of sampling rate)

III. PROPOSED METHOD

Error correction of ADCs has received increasing attention during the last two decades. Several methods have been proposed and evaluated during this time, e.g., [HSP00, LASH02a, IHK91, Mou89, TL97, Hum02, RI87, Iro86]. These methods have in common that the ADC to be corrected is treated as a closed entity, i.e., internal signals and states of the ADC are not available, and the calibration and correction methods must operate *outside* of the converter. Moreover, the correction is dependent on the output signal $x(n)$ of the ADC to be corrected. That is, the correction is an operation incorporated *after* the ADC, hence the name post-correction.

We are mainly concerned with look-up table correction methods. These are, as the name suggests, methods that produce a corrected ADC output value through the use of a look-up table where pre-calculated values are stored. A distinction between *static* and *dynamic* correction is made. If the correction for a sample $x(n)$ is a function *only* of the value $x(n)$, i.e., not depending on past or future samples, signal derivatives, signal frequency, etc., then the correction is said to be static. Else, it is said to be dynamic.

Static Correction

The basic assumption behind static correction is that the quantization performed in the ADC is inaccurate in the sense that the quantization regions $\{Sj\}M-1$ $j=0$ deviate from the ideal regions. In a uniform quantizer this corresponds to the quantization regions failing to be of equal size. A static look-up table correction scheme would then map every possible output state *xi* into a corrected state *si* through the use of an *M*-size table. An alternative equivalent structure is to let the table contain *correction terms* $\{\varepsilon j\}M-1$ $j=0$, which are added to the output to form $si = xi+\varepsilon i$. This is also a more practical way to implement a correction table, since the word length of the table is utilized more efficiently. The two alternatives are depicted in Figure 2(a) and Figure 2(b), respectively. The table is said to be addressed, or indexed, with the present sample *xi* only.

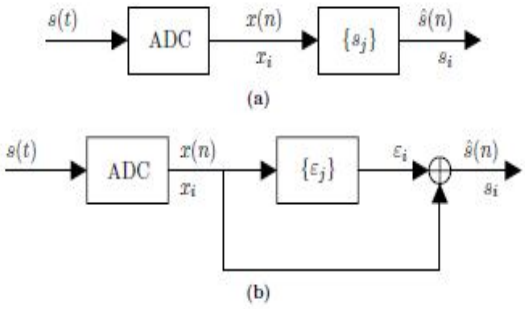

Figure 2: Two types of static correction tables. In 2(a) the ADC output $x(n) = xi$ is replaced by the table entry *si*, while in 2(b) the corrected output is produced by adding a correction term εi to the ADC output *xi*.

It is obvious that this scheme will produce the same corrected value *si* for a given ADC output xi regardless of the signal dynamics (e.g., regardless of signal history). Thus, it is of significant importance that the quantization regions *S* stay constant in the intended range of operation for the ADC. This is the method proposed, for example, in [Iro86] and [HSP00]. In the latter it was demonstrated that static correction may improve performance for some frequencies, while deteriorating it for other frequencies. This can be interpreted as the quantization regions changing with signal frequency, hence making the correction table useless for signal frequencies where the regions have changed.

Dynamic Correction

Since the error behavior of practical ADCs is dynamic in general, successful error correction over a wider frequency range depends on the correction scheme being dynamic as well.

1. State-Space Structures

One way to introduce dynamics into the correction scheme is to adopt a state-space structure. The look-up table is extended to two dimensions, as illustrated in Figure 3 The current sample, $x(n)$, and the previous sample, $x(n-1)$, are used to address the table so that the ADC operation becomes $(x(n) = xi, x(n-1) = xj) \Rightarrow \hat{s}(n) = xi + \varepsilon i, j$. This method is referred to as *state-space correction* and is proposed in, for example, [IHK91] and [TL97]. The correction is undoubtedly dependent on signal dynamics, since the corrected value for a sample $x(n) = xi$ is potentially

different for different values of the previous sample $x(n-1)$.

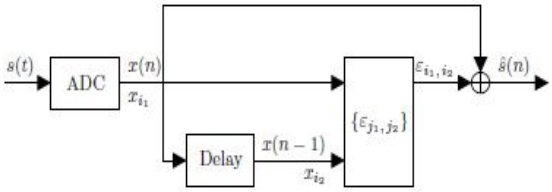

Figure 3 two dimensional state space correction table

2. Phase-Plane Structures

As an alternative to state-space correction, the phase-plane correction, described in, for example, [RI87] and [Mou89], can be used. Similar to the state-space case, the correction is in this case based on a two-dimensional

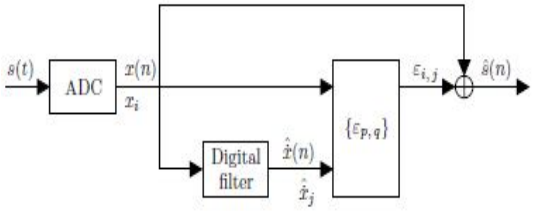

Figure 4 Two-dimensional phase-plane correction table.

The filter calculates an estimate of the signal slope for each sample. The estimate is represented with a binary word ˆ˙*xj* of finite precision (say *b*2 bits, not necessarily equal to *b*) and is used as part of the table index.

IV. SIMULATION RESULTS

In order to validate the proposed method, following software are used

1) QUESTASIM-6.4
2) Xilinx ISE Design Suite 12.2

It can also be seen that a purely corrected sine wave signal can almost reach the noise floor, which is hard to achieve in most digital correction performance. It is reasonable to believe that the implementation accuracy for both post-correction model and online model extraction can satisfied the demand of industrial requirement

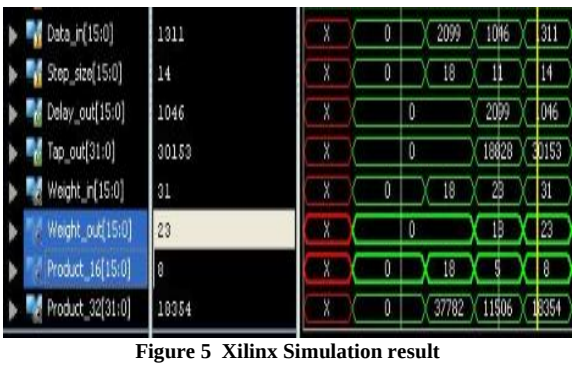

Figure 5 Xilinx Simulation result

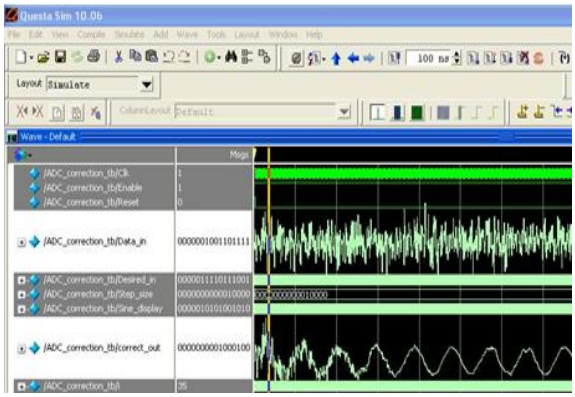

Figure 6 QUESTASIM Simulation result

CONCLUSION

Errors generated from channel mismatches are a main problem in realizing wide-band ADCs with acceptable output resolutions. In this paper a post-correction method has been proposed to compensate for the nonlinearities of ADCs, The post-correction block can be made as a standalone module or an add-on element to linearized various types of ADCs, which is very important for future integrated digital circuit design.

REFERENCE

[1] (Wenhui cao, cgao Yu, and anding Zhu university college DULBIN) *"Digital Post-correction of Analog-To-Digital Converter with Real-time FPGA Implementation" 2015 IEEE*

[2] (Tsung-Heng Tsai, *Member, IEEE, Paul J. Hurst, Fellow, IEEE, and Stephen H. Lewis, Fellow, IEEE)* "Correction of Mismatches in a Time-Interleaved Analog-to-Digital Converter in an Adaptively Equalized Digital Communication Receiver*" Ieee Transactions On Circuits And Systems—i: Regular Papers, Vol. 56, No. 2, February 2009*

[3] (Hassan Hani Slim , Peter Russer)*"Digital Automatic Calibration Method for a Time-Interleaved ADCs System used in Time-Domain EMI Measurement Receiver" 2011 IEEE*

[4] (Shahzad Saleem, Student Member, IEEE, and Christian Vogel, Senior Member, IEEE) "Adaptive Blind Background Calibration of Polynomial-Represented Frequency Response Mismatches in a Two-Channel Time-Interleaved ADC" *Ieee Transactions On Circuits And Systems—i: Regular Papers, Vol. 58, No. 6, June 2011*

[5] (Yashar Hesamiafshar, Sanaz Momeni) "A New DFT based Approach for Gain Mismatch Detection and Correction in Time-Interleaved ADCs" *Microelectronics Research Lab Urmia University, 2010 IEEE*

[6] C. Schmidt, J. E. Cousseau, J. L. Figueroa, R. Wichman and S. Werner "ADC post-compensation using a Hammerstein model"*Proc. of the Argentine School of Micro-Nanoelectronics Technology and Applications, catalog, pp. 71-76*

[7] X.Hu, H. Ma, J. Peng and C. Tian "State-of-the-art in Volterra series modeling for ADC nonlinearity"*Second Asia International Conference on Modelling & Simulation, pp. 1043-1047*

[8] L.Peng, G. C. Sun, H. H. Deng and M. Chen "A Wiener model based Post-calibration of ADC nonlinear distortion" *pp. 366-370.*

[9] Y. Chiu, C. W. Tsang and B. Nikolic "Least mean square adaptive digital background calibration of pipelined

analog-to-digital converters" *vol. 51, pp. 38-46, Jan., 2004.*

[10] J. Peng, H. Ma and C. Tian "Modeling of ADC nonlinearity by time-delay-based power series"*Second Asia International Conference on Modelling & Simulation, pp. 1048-1053*

[11] S. Haykin Adaptive Filter Theory *1996, Prentice-Hall*

★★★