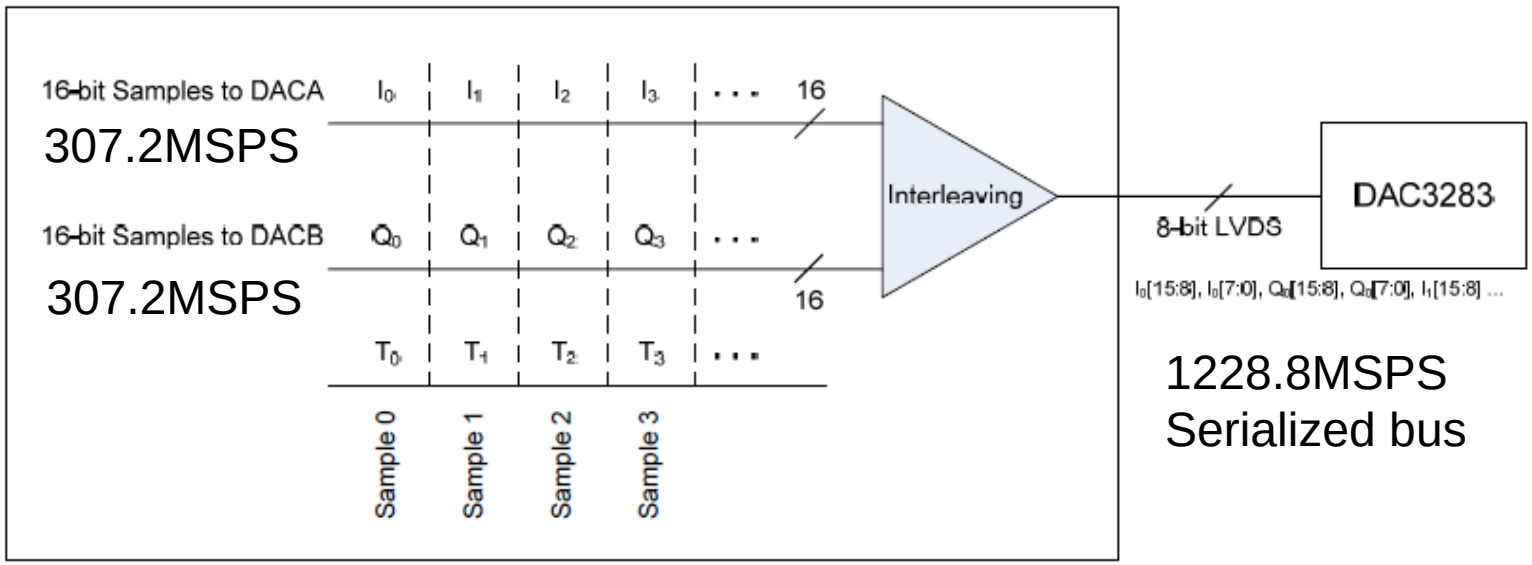
DAC3282/3 Byte Wide DDR Clocking

4-Time Interleave Example

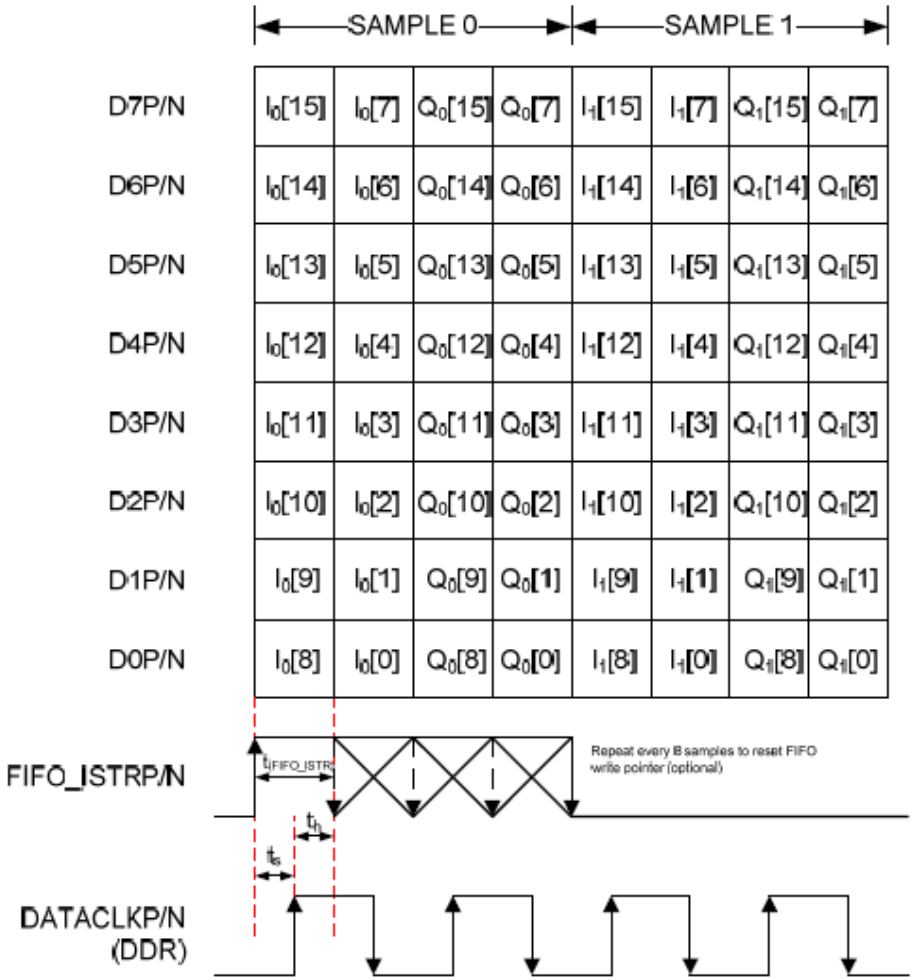


F_{DAC} = 614.4MHz, 2x interpolation

F_{DATA} = 307.2MSPS @ 2 buses of 16 bits

F_{DATA} after interleaving = 1228.8MSPS @ 1 bus of 8 bits. (DATACLK = 614.4MHz)

Data Clock and DAC Clock relationship



DATACLK = ½ data rate (after interleave)

DATACLK = 2 * DACCLK for 1x int

DATACLK = 1 * DACCLK for 2x int

DATACLK = ½ * DACCLK for 4x int

Maximum Clock Speed

f_{CLK}	Maximum output update rate	1x Interpolation	312.5	MSPS
		2x Interpolation	625	
		4x Interpolation	800	

Need to be aware of maximum clock speed at various interpolation settings.