

ADC1x Dx xxx(RF)

Virtex-4

Cypress uC

Expansion

Power

FRONT END

PLL

EXT_CLK_SELECT removed from the schematic

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ADC1xDxxxx(RF)RB Reference Board

REFERENCE DESIGN

Board ID:	SV600863
EVM Assembly	Variant
ADC10D1500RB	-001
ADC12D1600RB	-002
ADC12D1600RFRB	-003
ADC12D1800RB	-004
ADC12D1800RFRB	-005
ADC12D2000RFRB	-006
ADC12D800RFRB	-007

SPECIAL NOTES

These schematics reflect the current state of product development. This design had NOT yet been fully tested at the time these schematics were generated.


Since this product is in development, the user of this document is strongly advised to check for the latest revision.

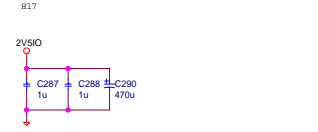
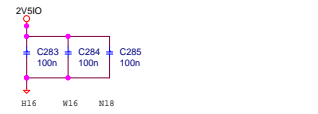
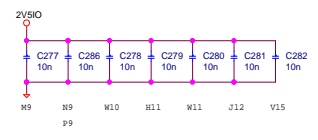
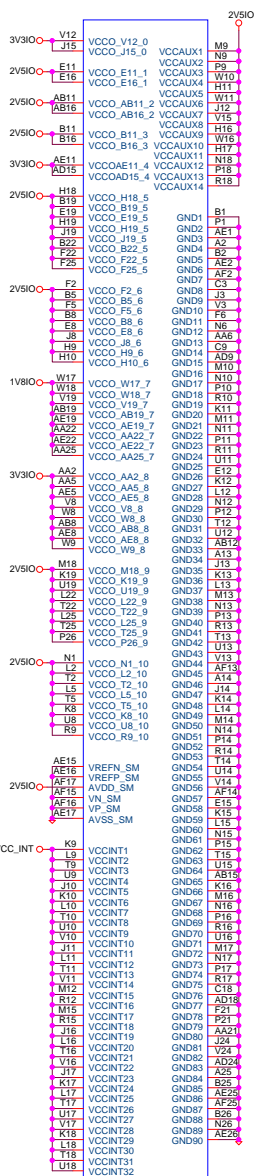
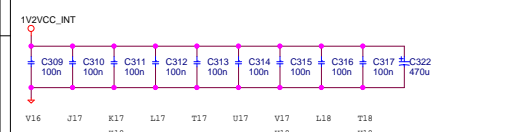
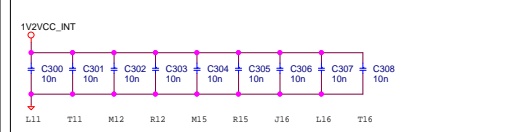
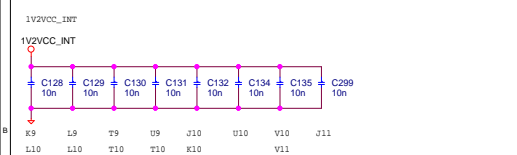
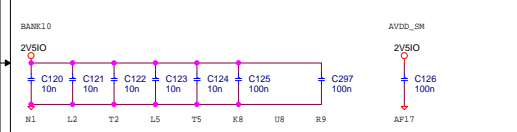
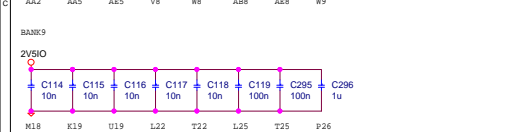
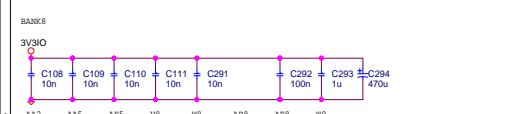
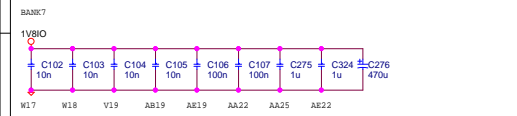
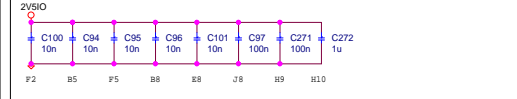
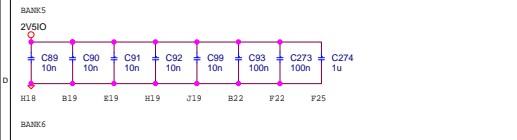
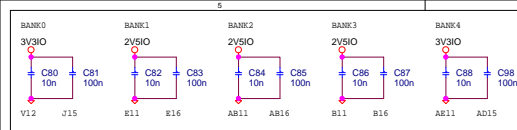
Texas Instruments reserves the right to make changes to this product.

ALL parts labeled "NA" are NOT ASSEMBLED.

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BANK #	BANK SUPPLY	INTERFACE
1	2V5IO	USI-1 Header
2	2V5IO	Test Headers, Temp. Sensor
3	2V5IO	ADC DCLK
4	3V3IO	Cypress, LEDs, 100 MHz oscillator
5	2V5IO	ADC Q-Channel (LVDS)
6	2V5IO	Clock generator
7	1V8IO	ADC Control
8	3V3IO	Cypress, LEDs
9	2V5IO	ADC I-Channel (LVDS)
10	2V5IO	Logic Analyzer Header

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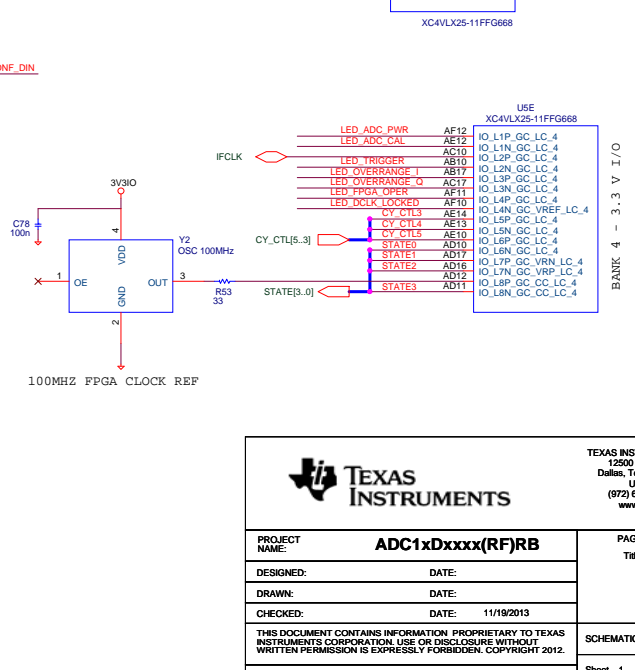
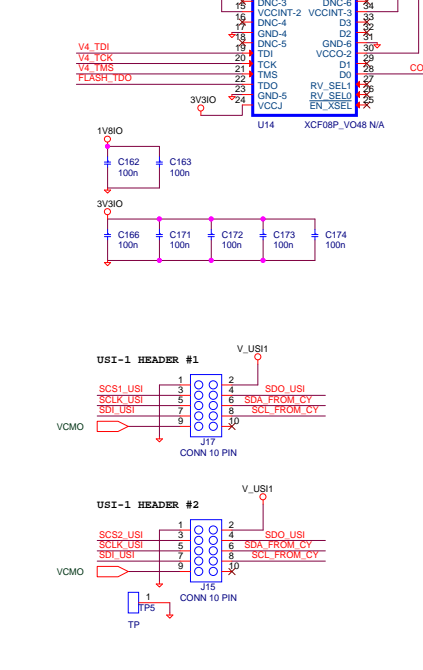
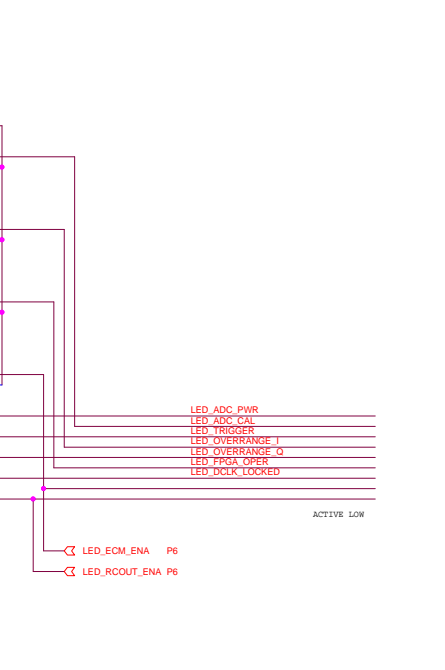
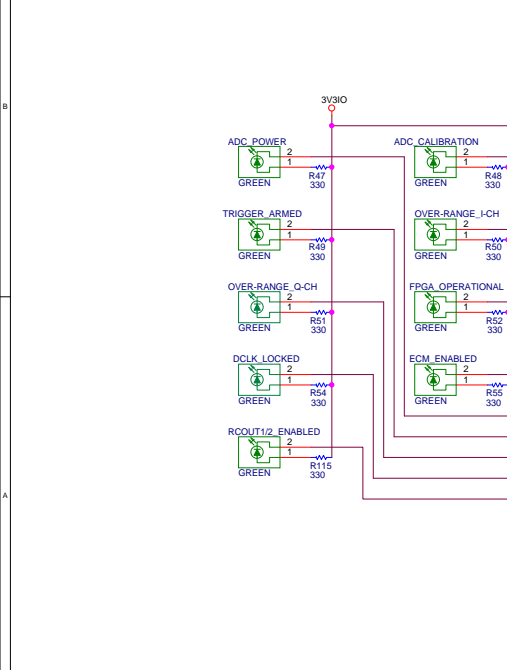
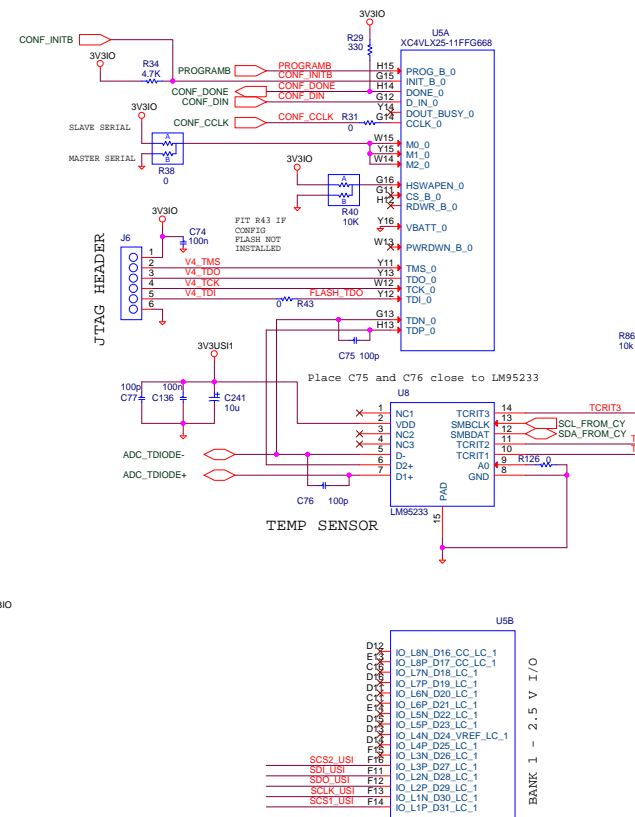
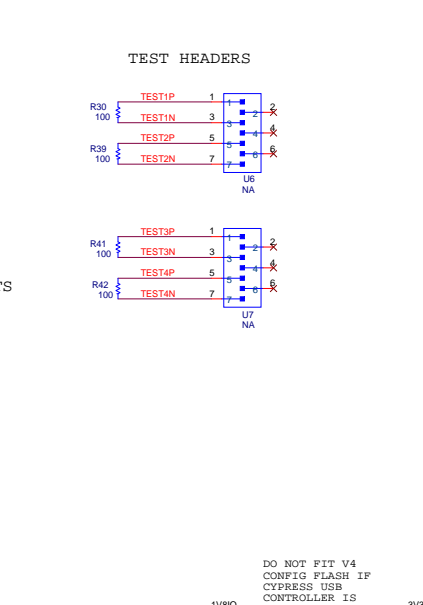
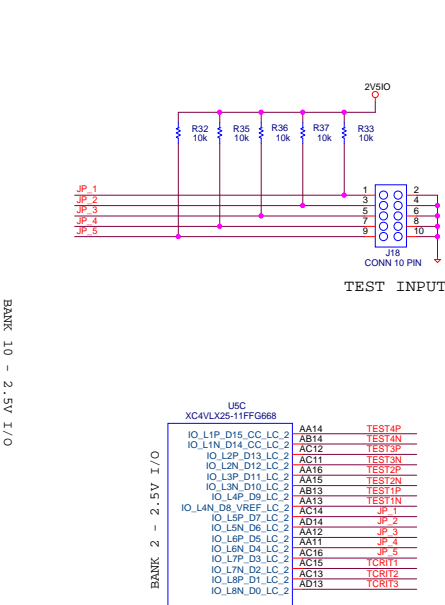
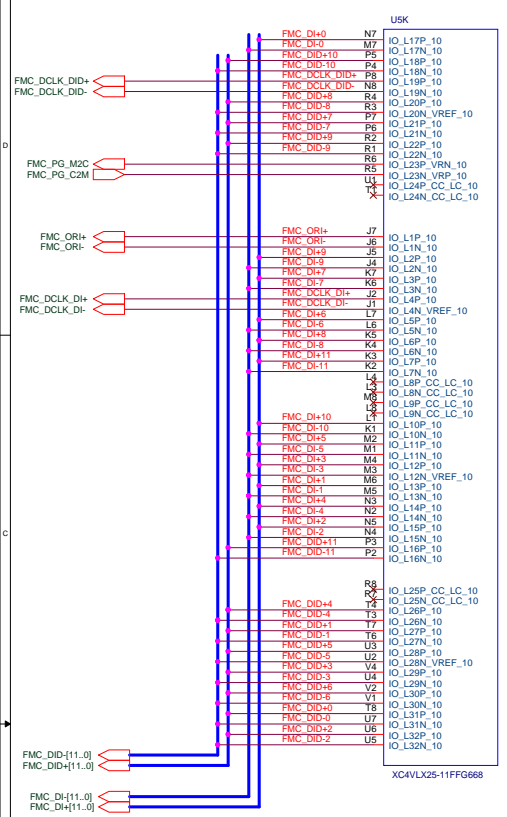
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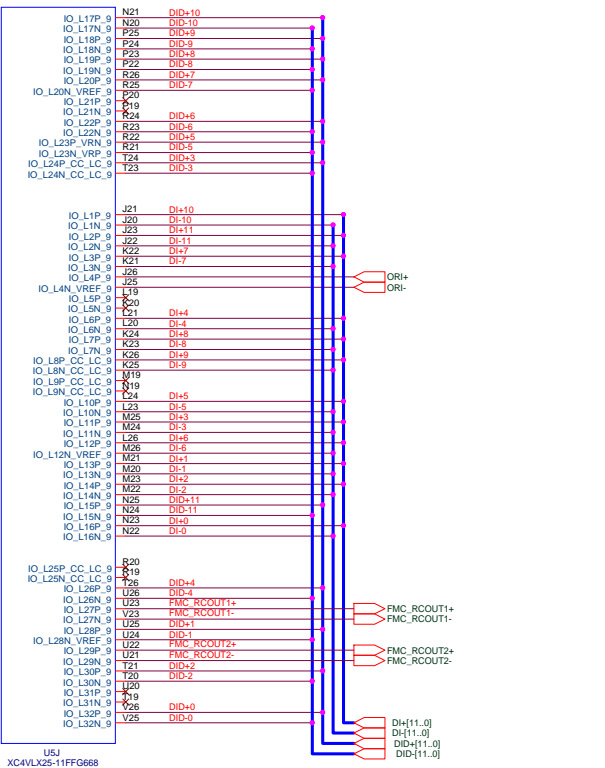
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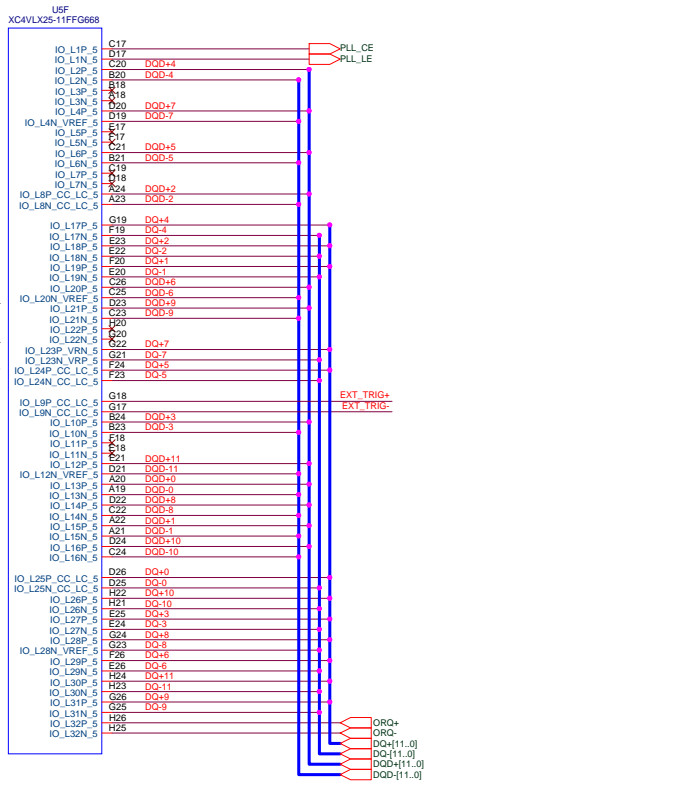
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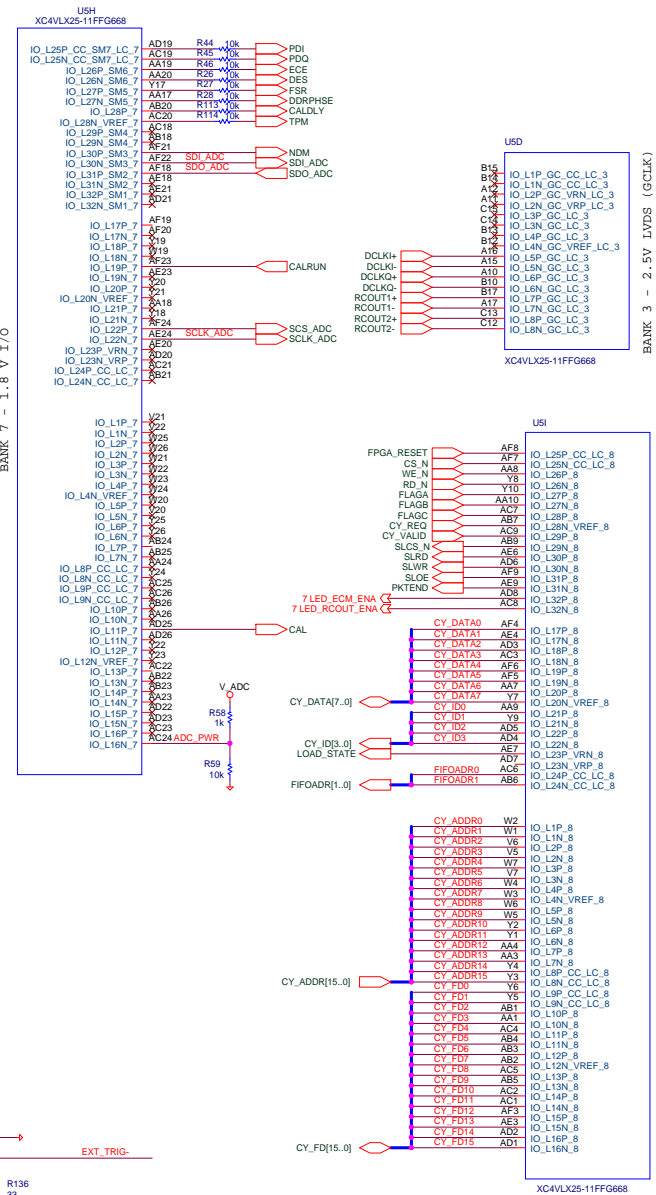
BANK 9 - 2.5 V I/O (LVDS)



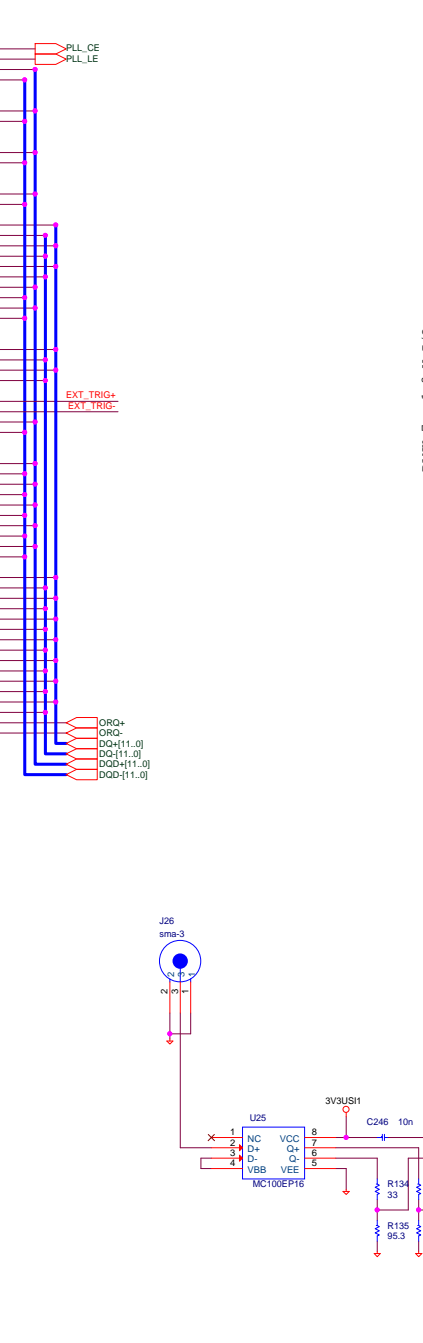
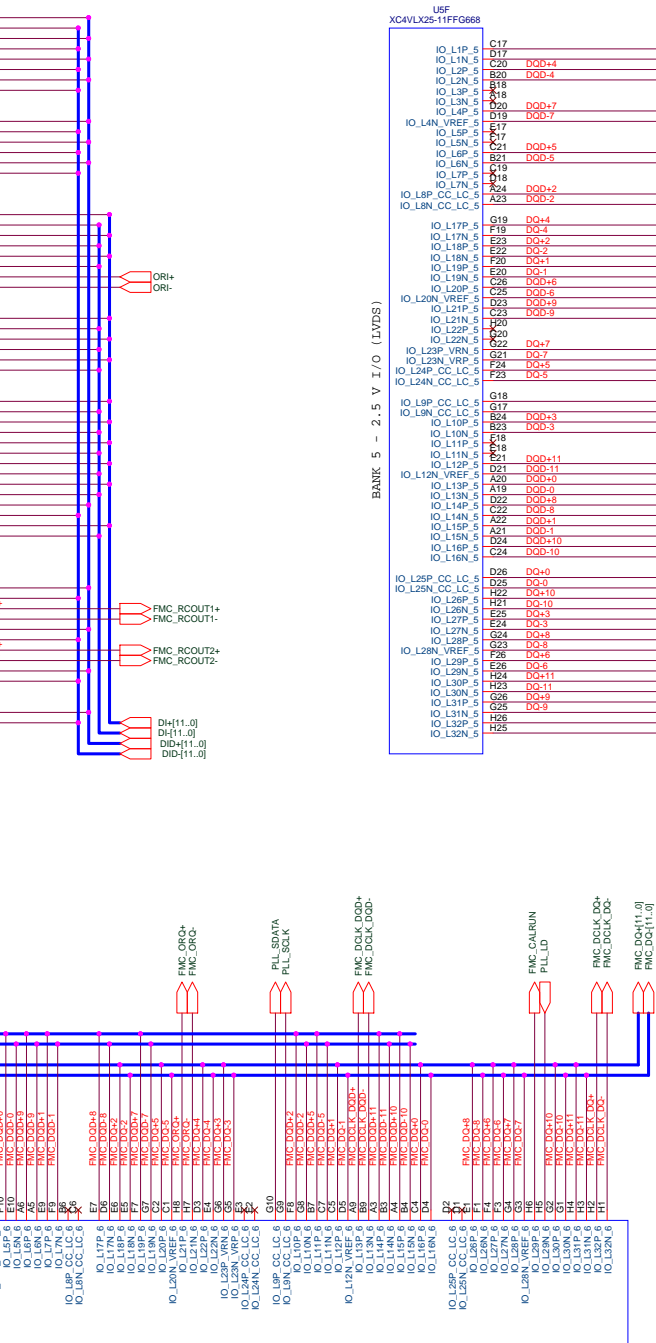
BANK 5 - 2.5 V I/O (LVDS)



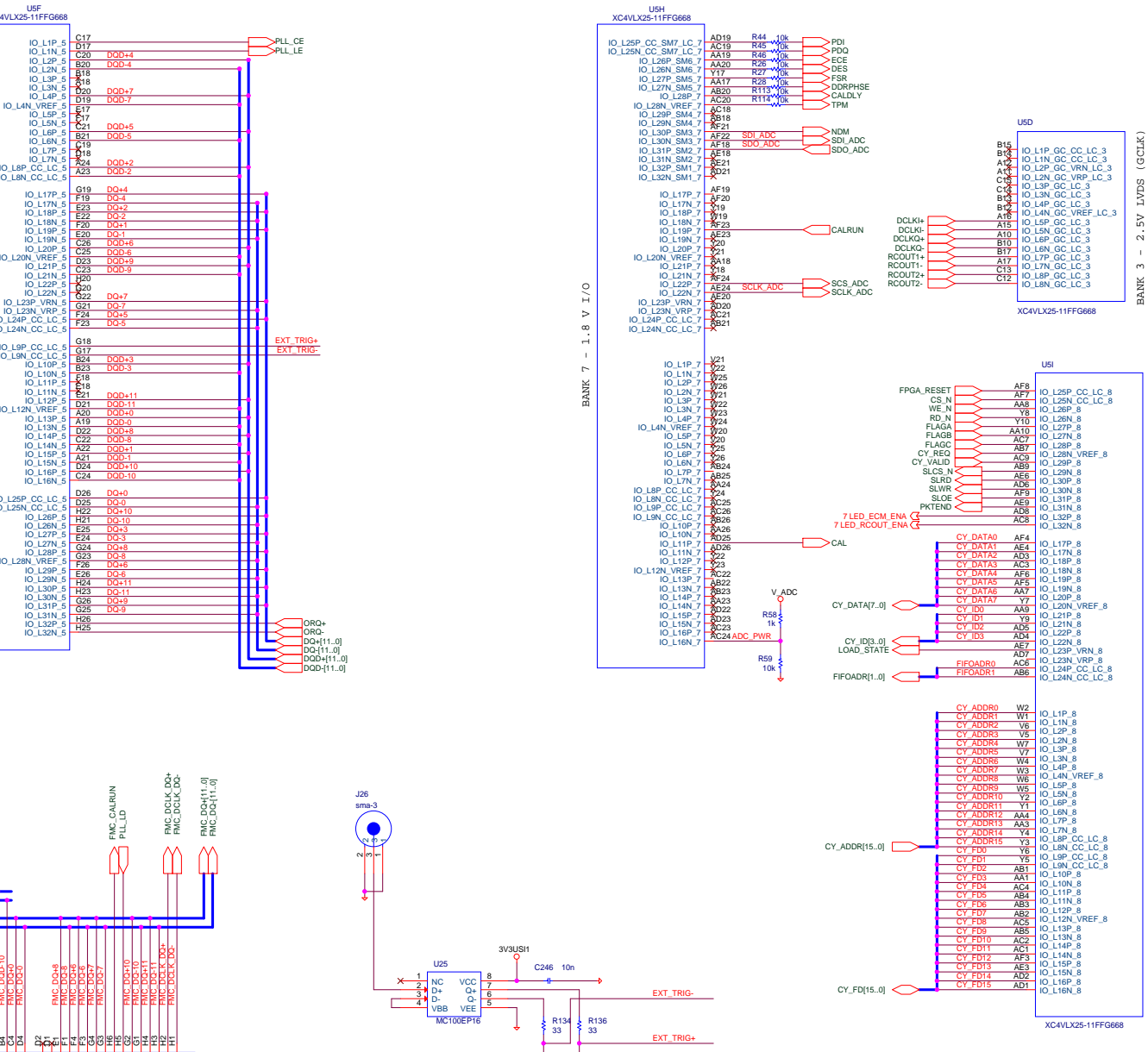
BANK 7 - 1.8 V I/O



BANK 6 - 2.5V I/O



BANK 3 - 2.5V I/O (CCLK)



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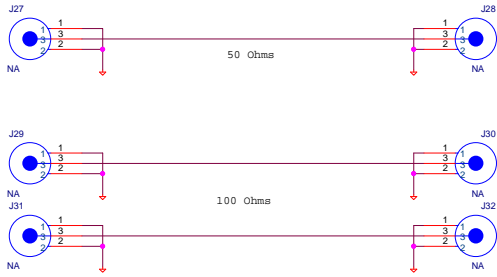
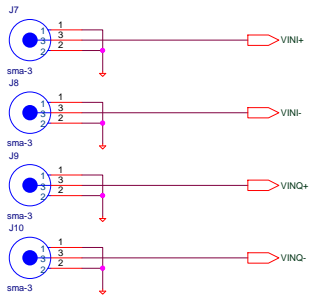
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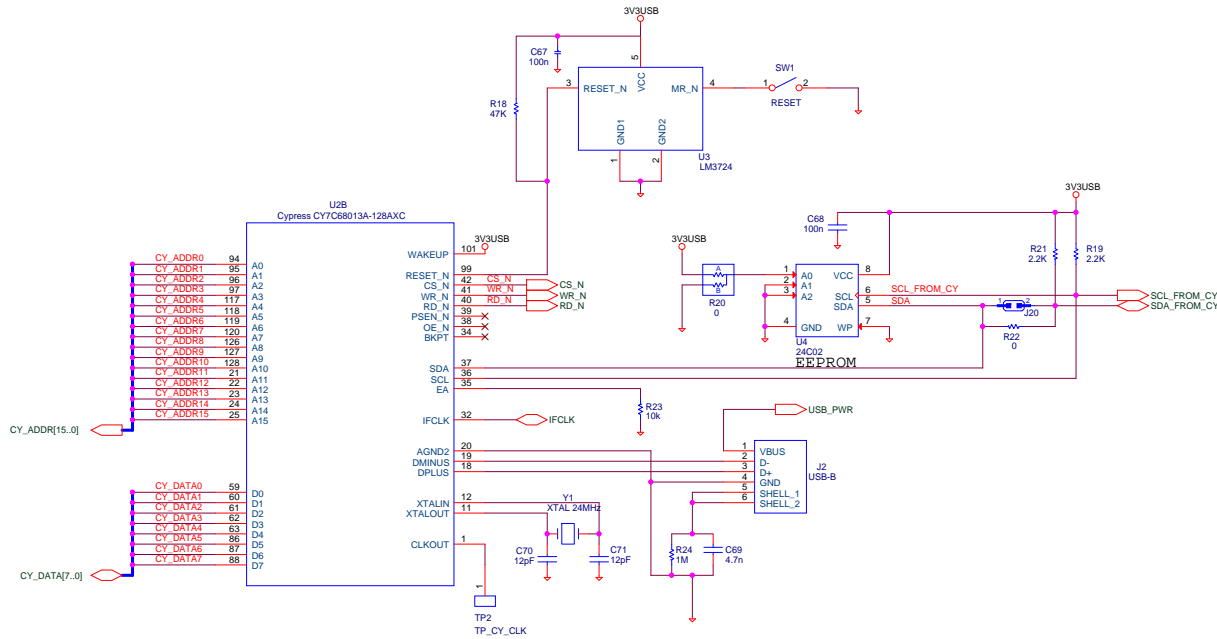
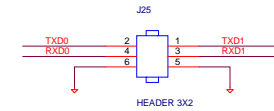
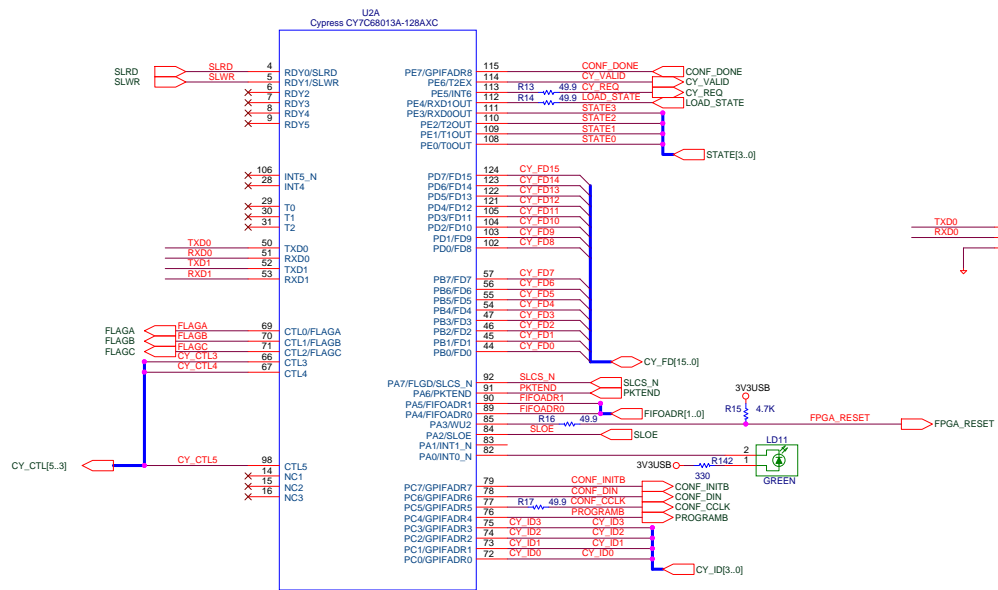
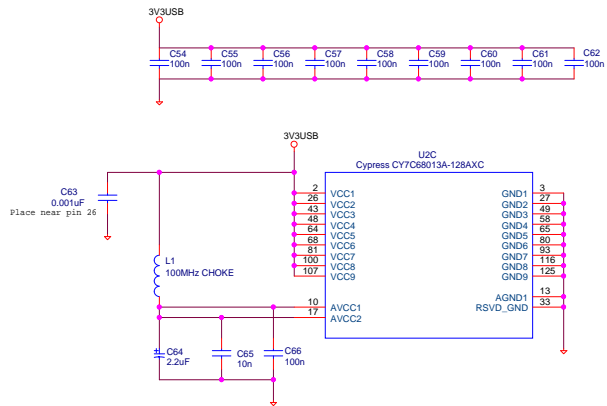
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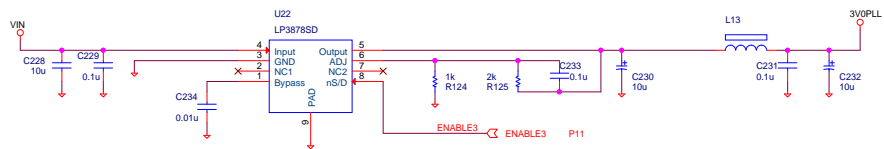


Impedance test connectors

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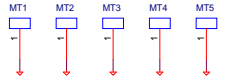
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3V0PLL - LMX2531 CLOCK GENERATOR SUPPLY




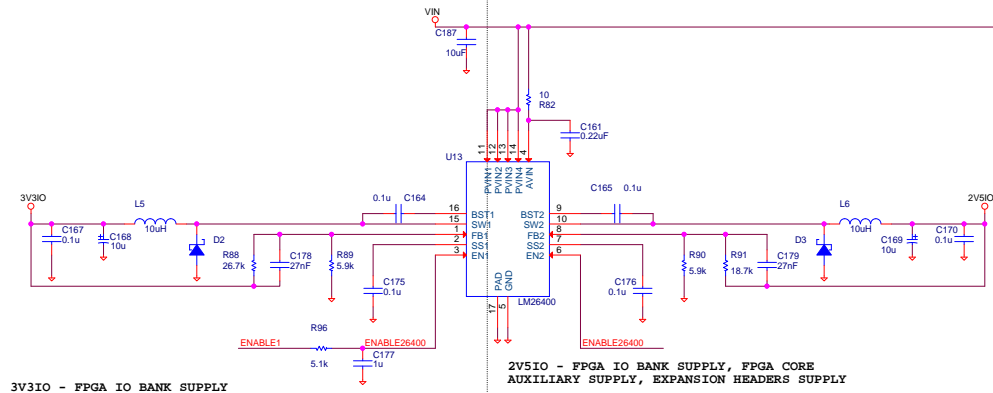
BOARD MOUNTING HOLES



HOLES FOR FMC CONNECTOR

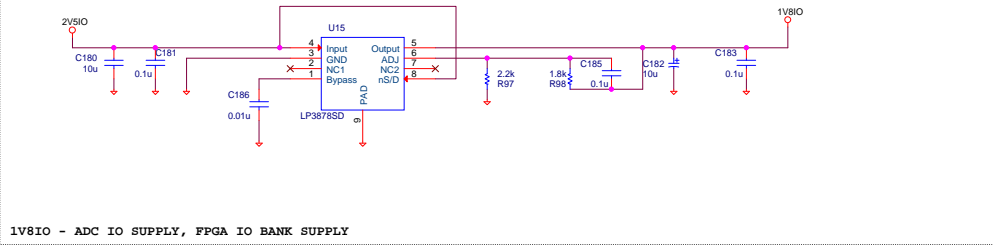


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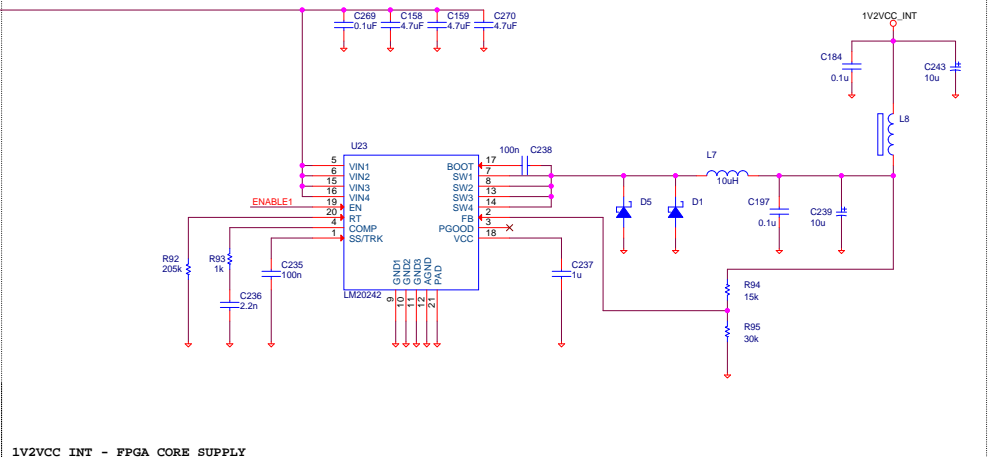


3V3IO - FPGA IO BANK SUPPLY

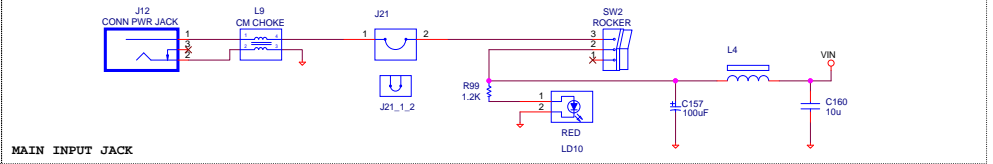
2V5IO - FPGA IO BANK SUPPLY, FPGA CORE AUXILIARY SUPPLY, EXPANSION HEADERS SUPPLY



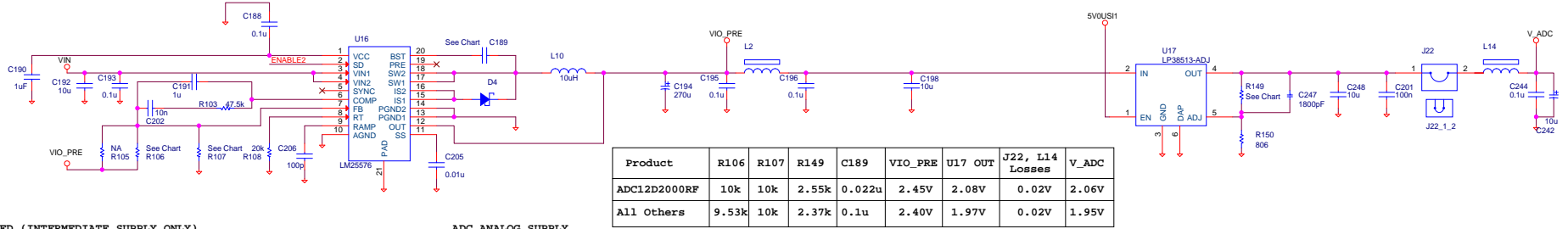
1V8IO - ADC IO SUPPLY, FPGA IO BANK SUPPLY



1V2VCC_INT - FPGA CORE SUPPLY

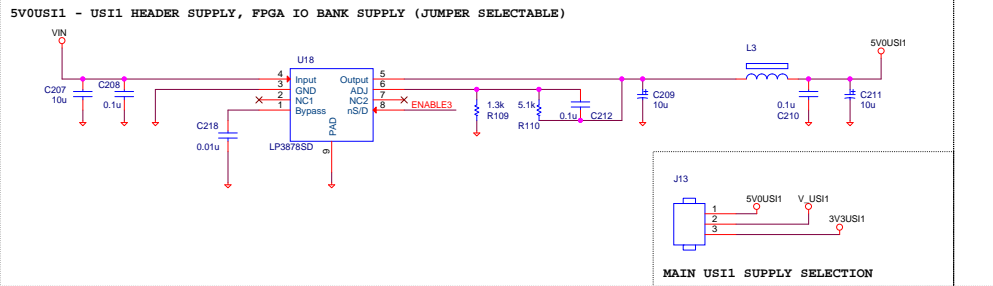


MAIN INPUT JACK



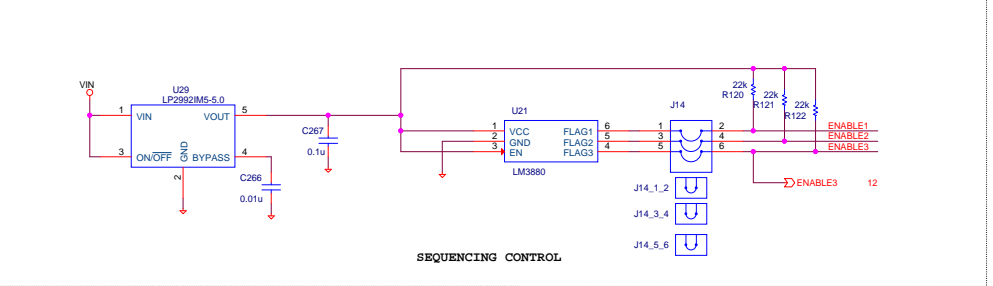
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ADC ANALOG SUPPLY

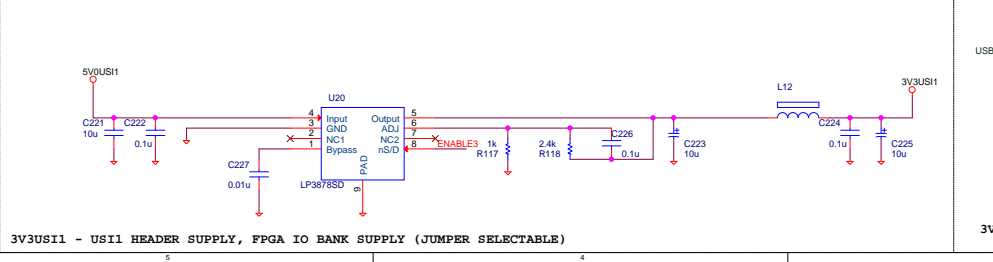


5V0US11 - US11 HEADER SUPPLY, FPGA IO BANK SUPPLY (JUMPER SELECTABLE)

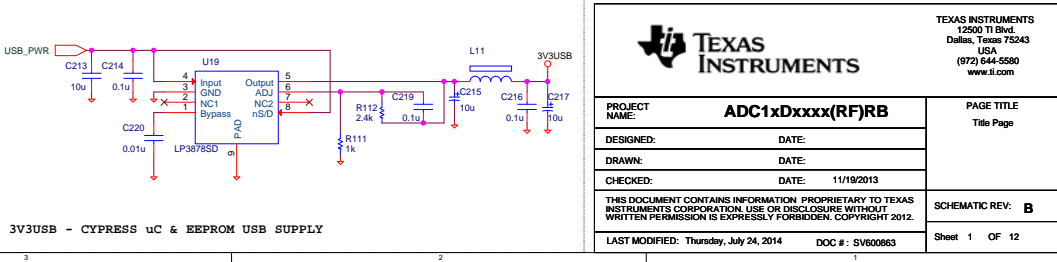
MAIN US11 SUPPLY SELECTION



SEQUENCING CONTROL



3V3US11 - US11 HEADER SUPPLY, FPGA IO BANK SUPPLY (JUMPER SELECTABLE)



3V3USB - CYPRESS uC & EEPROM USB SUPPLY

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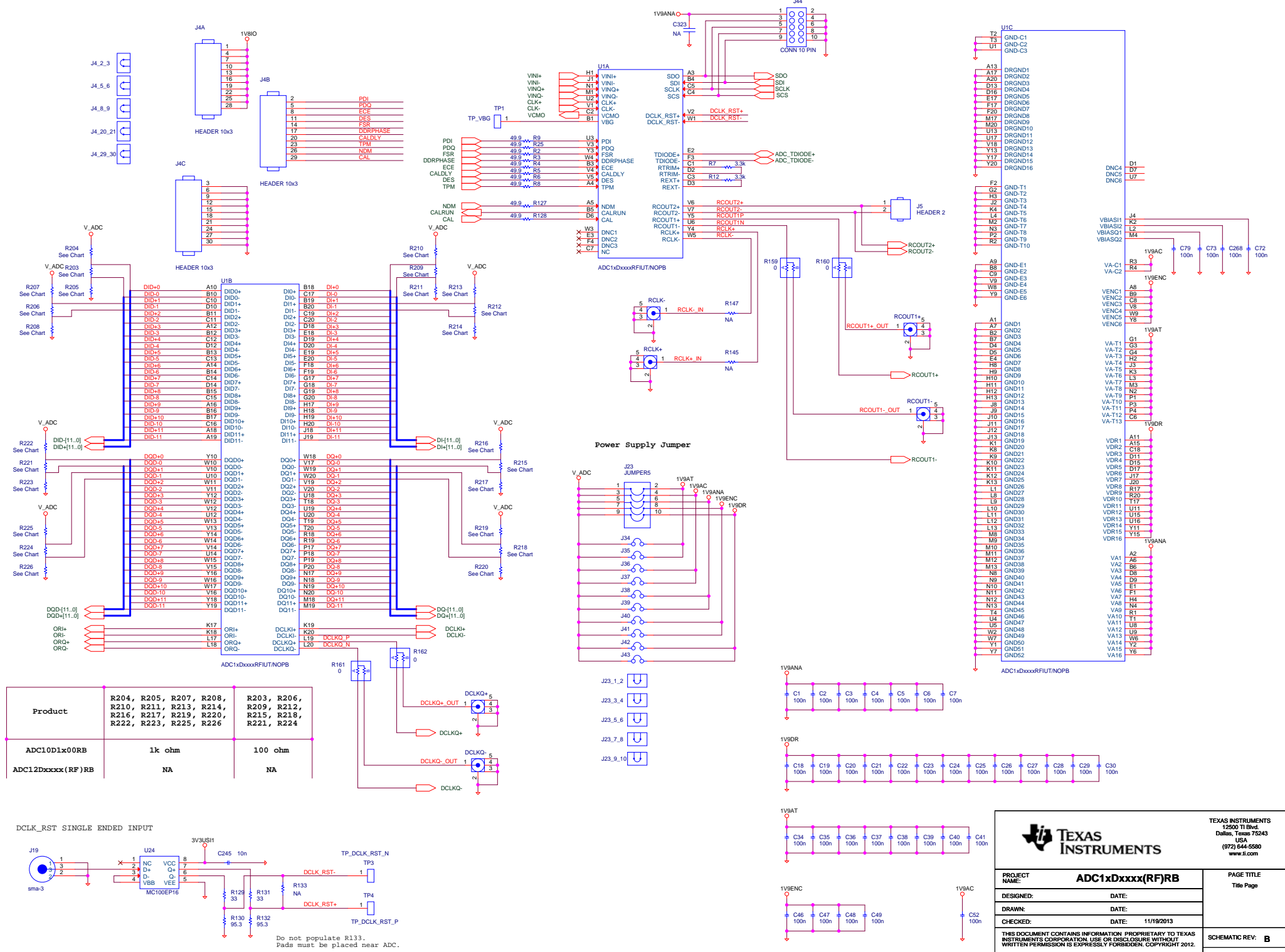
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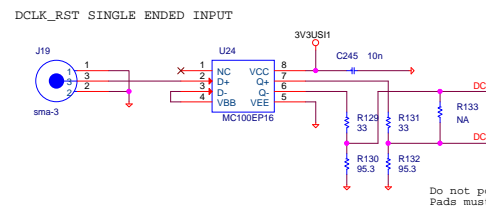
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Product	R204, R205, R207, R208, R210, R211, R213, R214, R216, R217, R219, R220, R222, R223, R225, R226	R203, R206, R209, R212, R215, R218, R221, R224
ADC10D1x00RB	1k ohm	100 ohm
ADC12Dxxx(RF)RB	NA	NA



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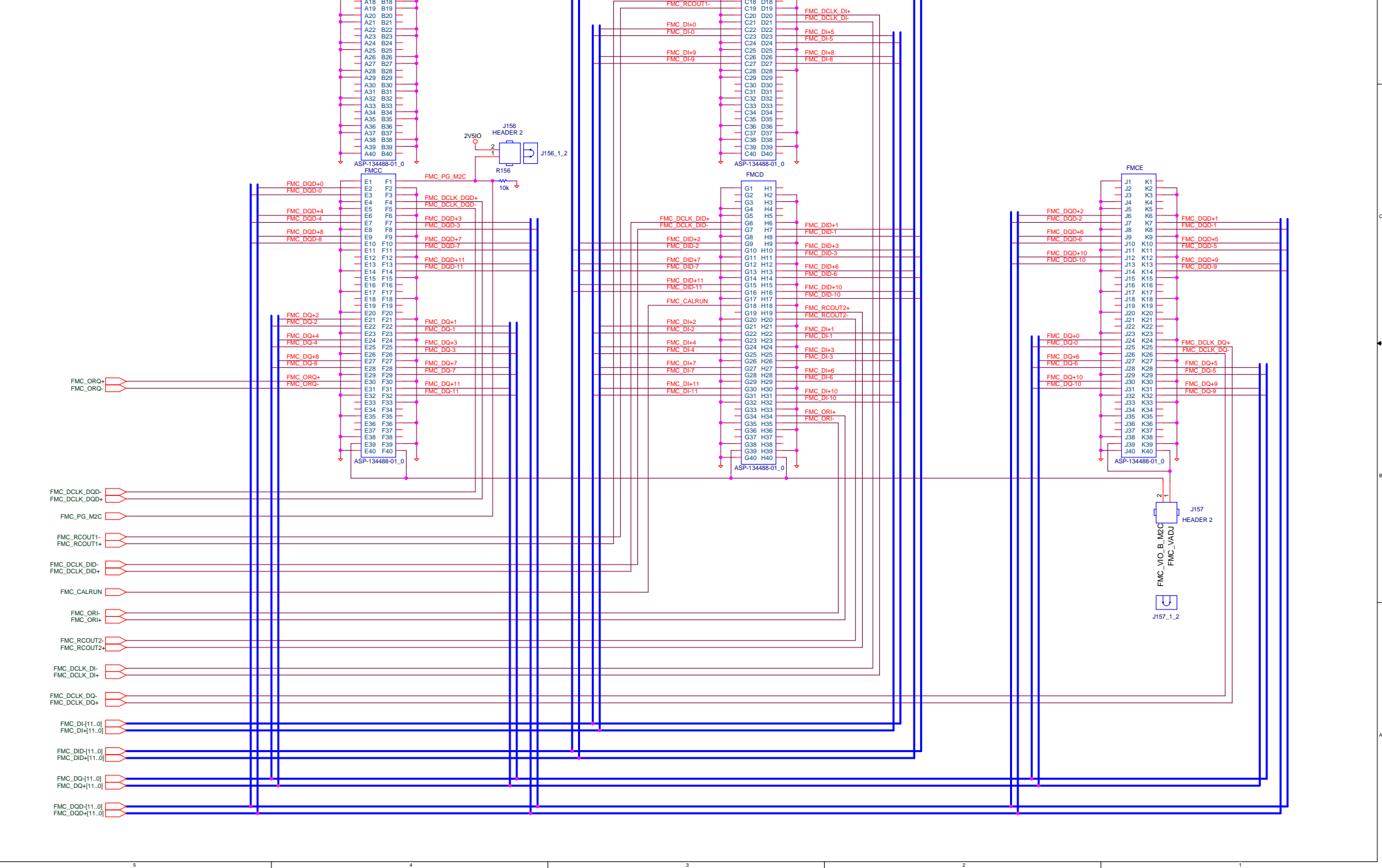
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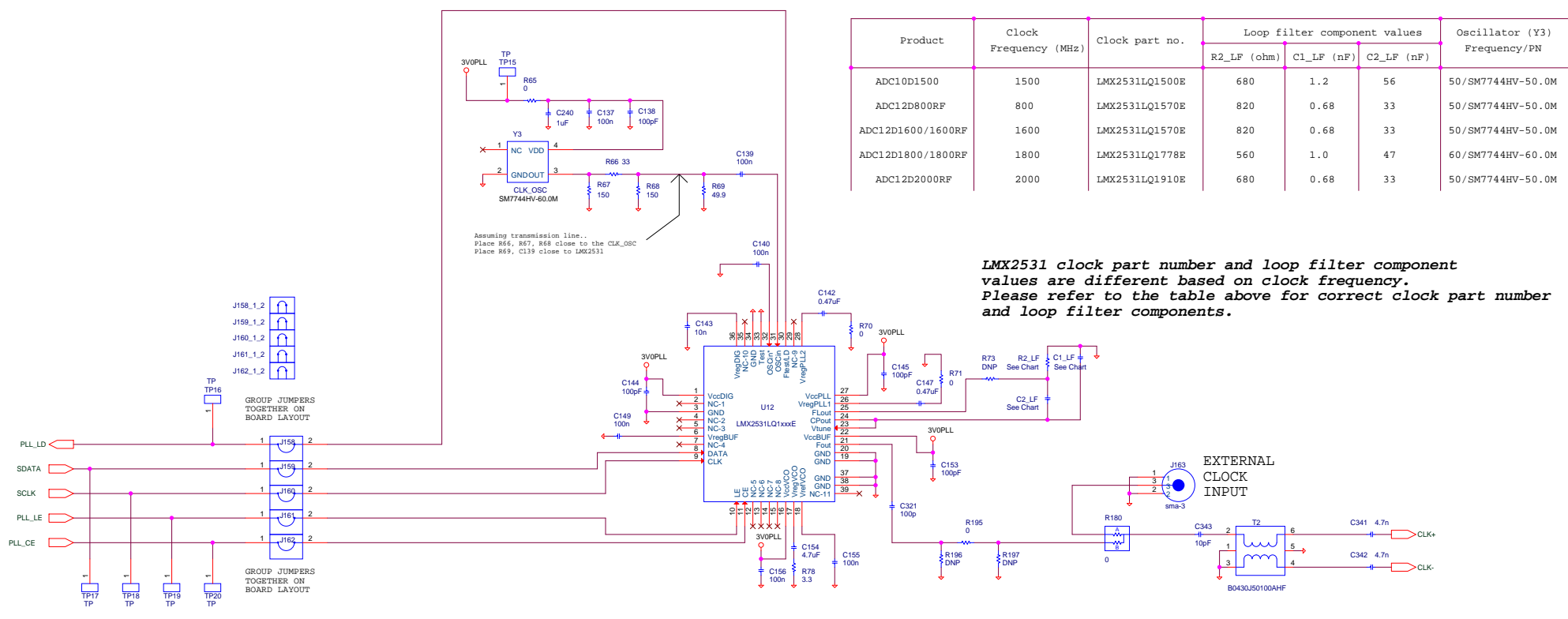
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Product	Clock Frequency (MHz)	Clock part no.	Loop filter component values			Oscillator (Y3) Frequency/PN
			R2_LF (ohm)	C1_LF (nF)	C2_LF (nF)	
ADC10D1500	1500	LMX2531LQ1500E	680	1.2	56	50/SM7744HV-50.0M
ADC12D800RF	800	LMX2531LQ1570E	820	0.68	33	50/SM7744HV-50.0M
ADC12D1600/1600RF	1600	LMX2531LQ1570E	820	0.68	33	50/SM7744HV-50.0M
ADC12D1800/1800RF	1800	LMX2531LQ1778E	560	1.0	47	60/SM7744HV-60.0M
ADC12D2000RF	2000	LMX2531LQ1910E	680	0.68	33	50/SM7744HV-50.0M

LMX2531 clock part number and loop filter component values are different based on clock frequency. Please refer to the table above for correct clock part number and loop filter components.

LAYOUT NOTE: FOR CLOCK ROUTING DO NOT USE VIAS (LMX2531 FOUT, EXT CLK) ALL THE WAY TO VIAS AT SOCKET EDGE. AVOID STUBS AND CHOOSE SERIES COMPONENTS TO BE 0402 SIZE WHERE POSSIBLE.

LAYOUT NOTE: Use as short traces as possible from LMX2531-Fout (pin 21) and External Clock Input to VIAs at socket edge



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