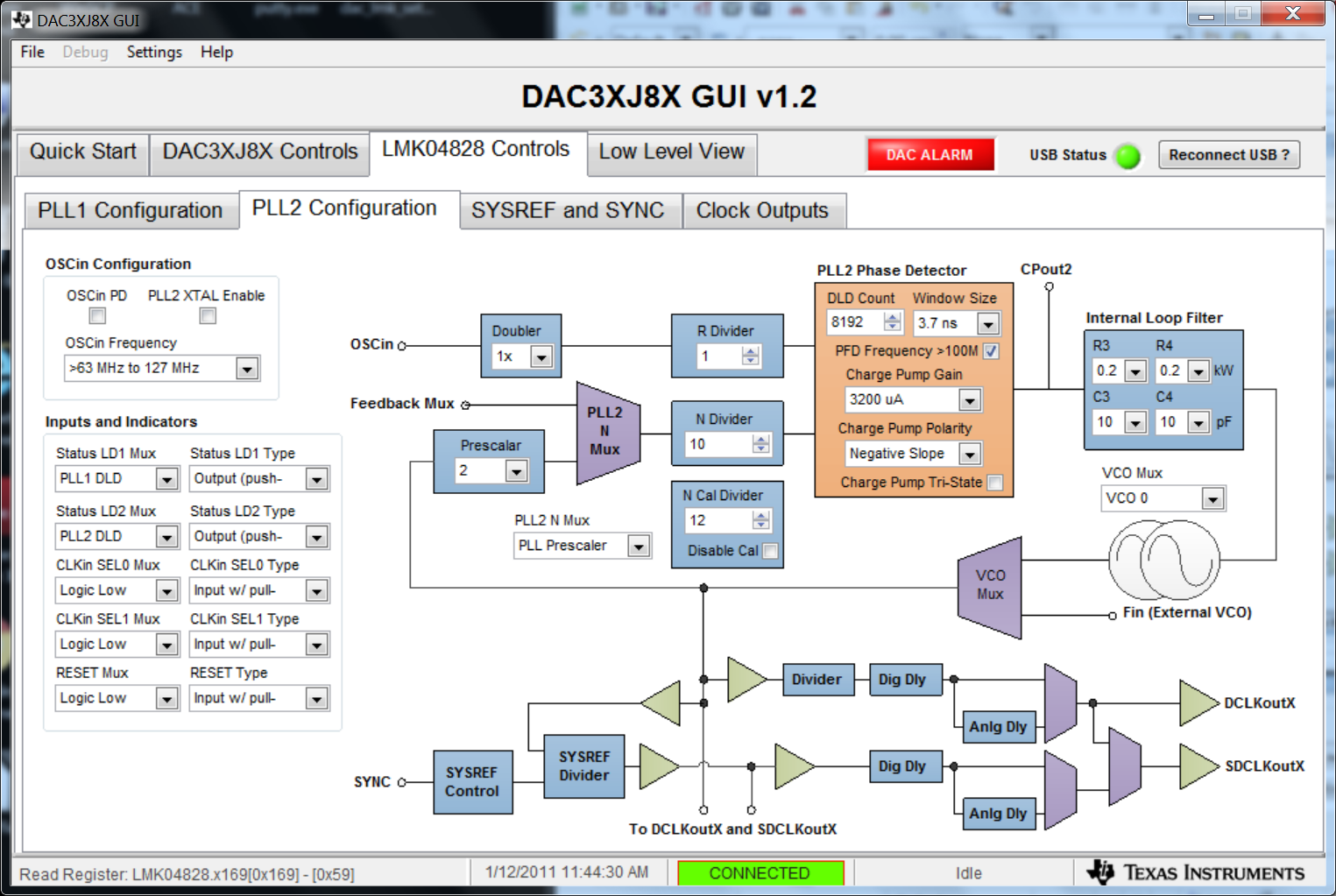
Dear Jim

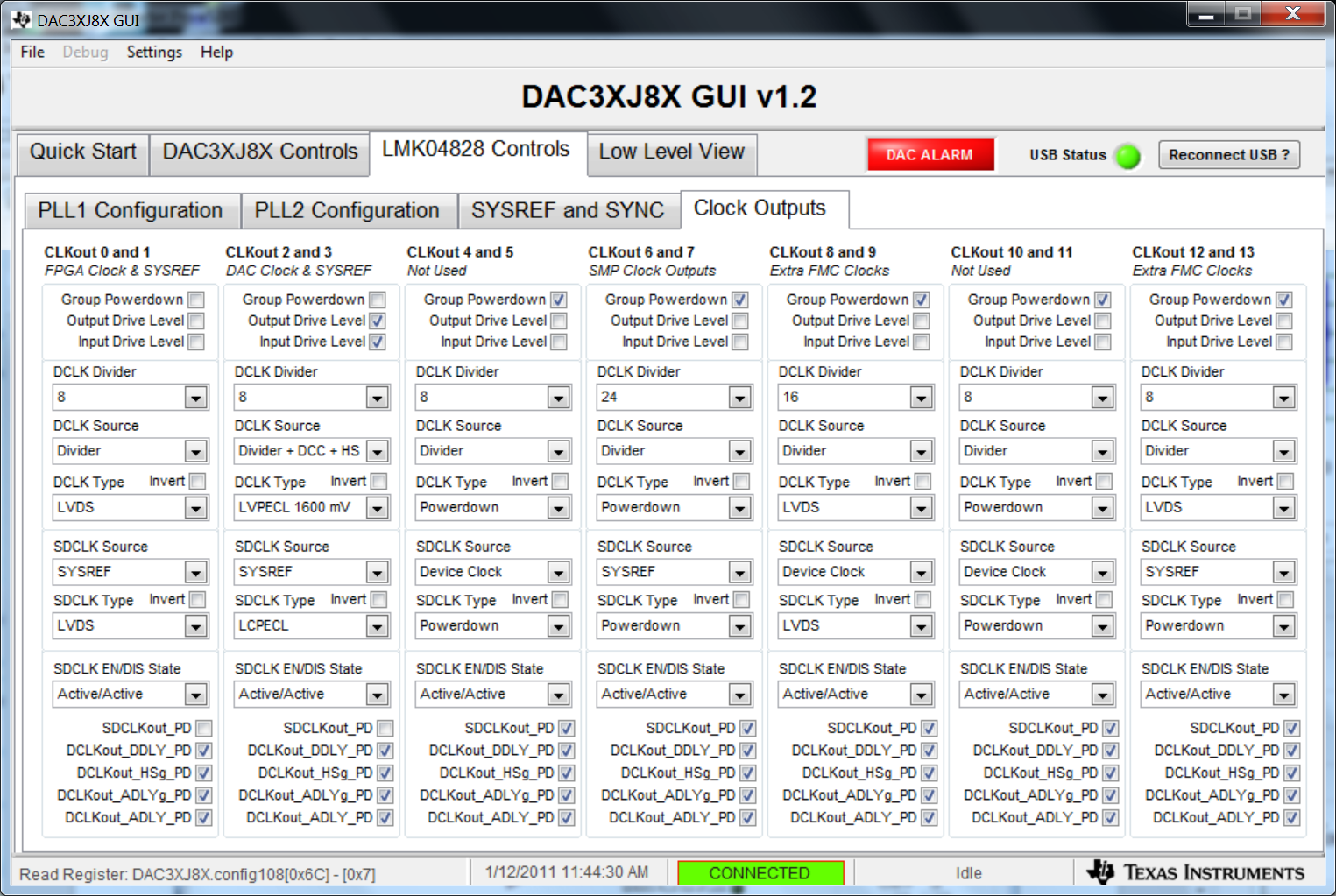
With your recommendation, I tried to set the GUI for the DAC as follows:

LMK04828, PLL1 bypassed and PLL2 receives the **OSCin** with the following set as in the picture. The signal delivered to the PLL is 134.4 MHz coming from J17 (after implement the configuration option of *Clock Generator using External Reference* that is R177, C206, and C121 should be uninstalled and R185, R186, and C92 should be installed).

The VCO frequency designed to 134.4 \* 18 = 2419.2 MHz that is using VCO0 (2370 to 2630 MHz) using PLL2 Prescaler =2 and PLL2 N Divider =9. I believe that the Charge pump Tri-State should be left unmarked and to lower the Charge Pump Gain to 100uA the VCO frequency is stable and the **PLL2 locked led lit**.

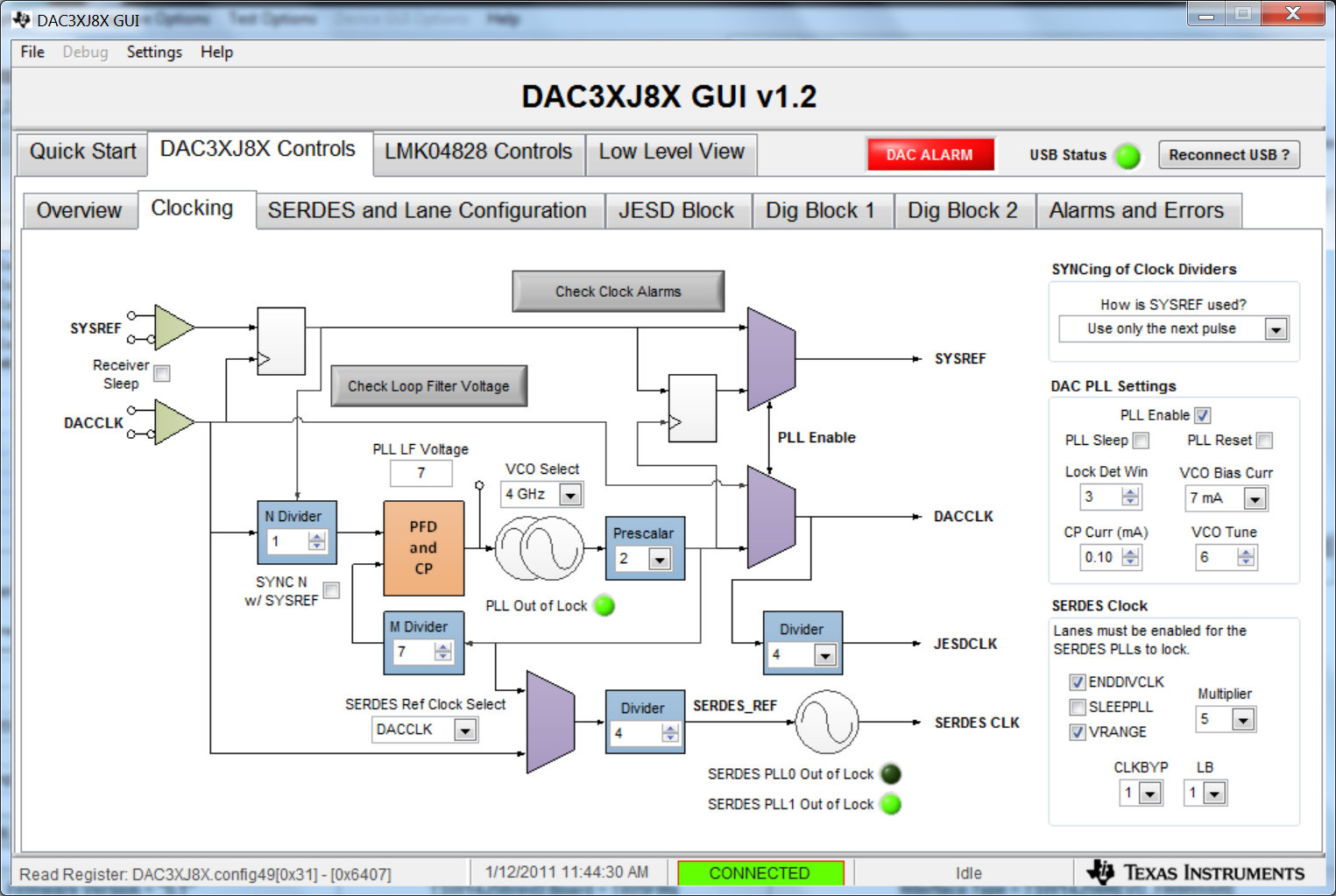


CLKout0 tuned to VCO0 /18 = 134.4 MHz , CLKout2 tuned to VCO0 /9 = 268.8 MHz and CLKout1 and 3 provides in accordance the SYSREF. (DCLKout0 Divider =18 and DCLKout2 Divider =9)



**The DAC operated using it's internal PLL:**

VCO Freq = 268.8 \* M\_Divider \* DAC\_VCO\_Prescaler / N\_Divider = 268.8 \* 8 \*4 / 2 = 4300.8 MHz , using L-band VCO (3.7 – 4.66 GHz). As a result the DACCLK (DAC Output Rate) = 4300.8 /4 = 1075.2 MHz . **The PLL OUT OF Lock is lit !!!!** (The PLL Enable check box is checked)



The LMF = 222 , the serdes rate is 5.376 Gbps.