TSW14J56 EVM Megacore Firmware

FPGA Design Document

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Revision 1.0

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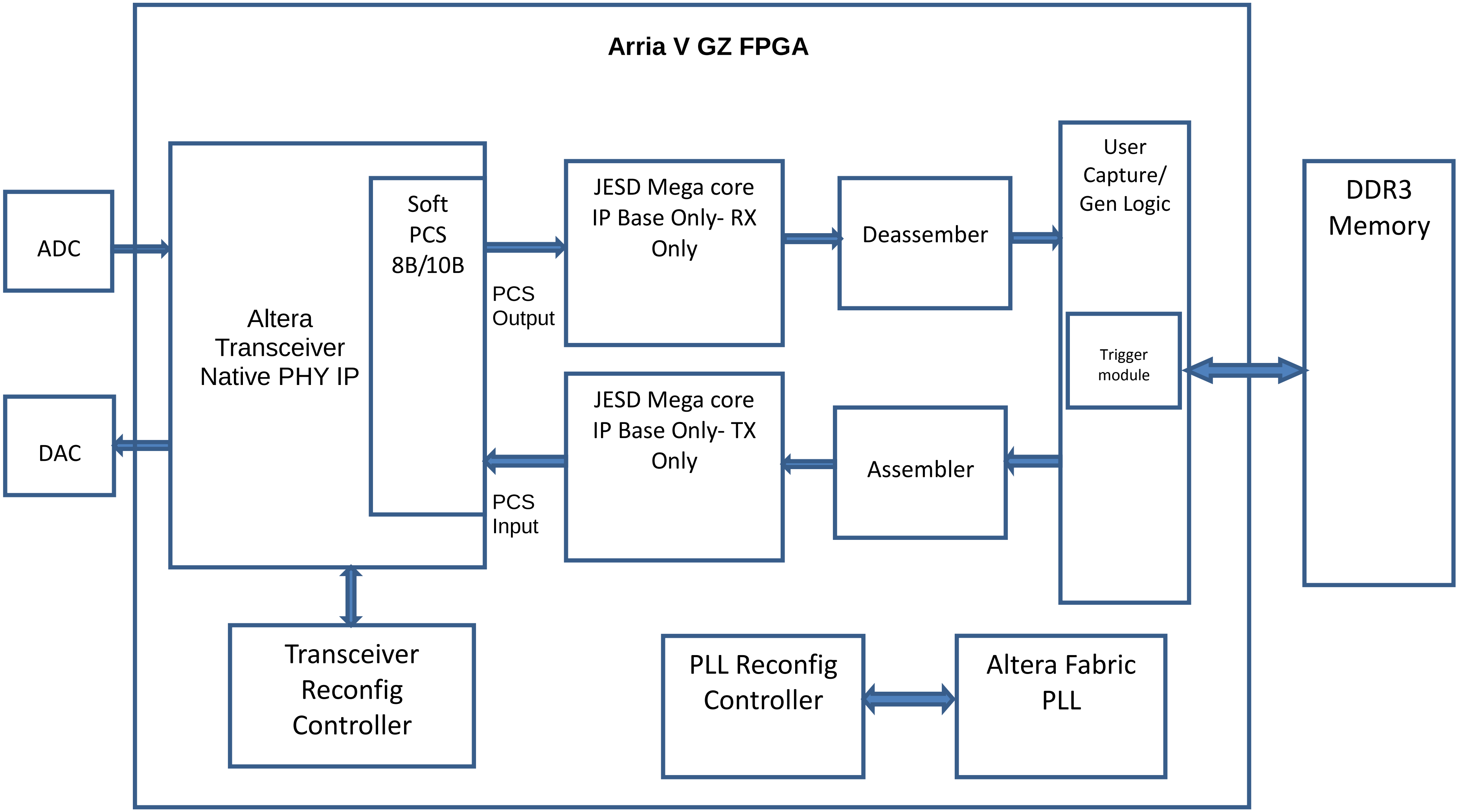
BLOCK DIAGRAM



FIRMWARE ARCHITECTURE

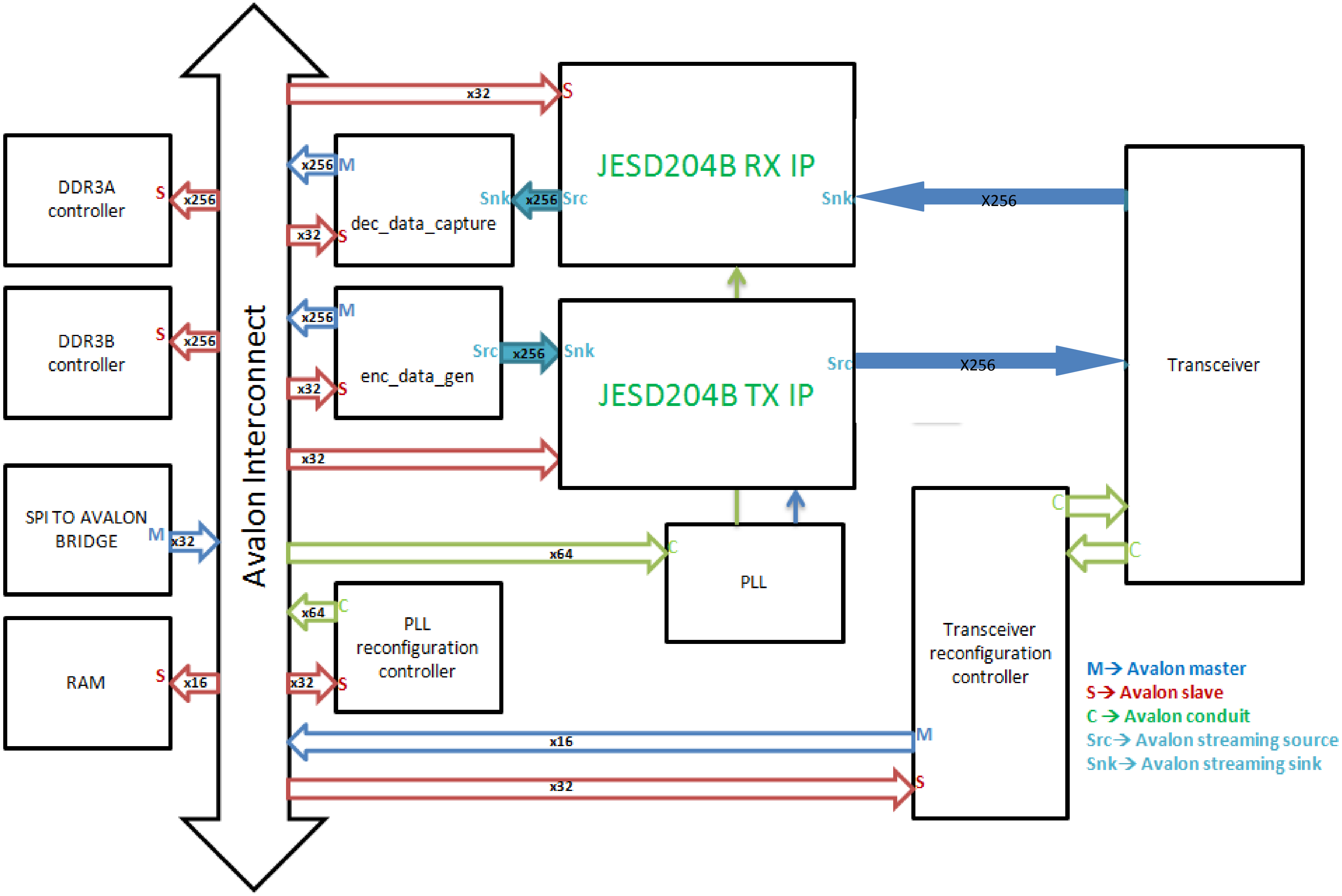


Figure 1: Architecture of TSW14J56 firmware

Overview

TSW14J56 is a hardware platform that can be used to evaluate the performance of TI's JESD204B devices. Examples of devices than can be used with TSW14J56 are ADS42JBx9 family, ADC12J4000 and ADC16DX370. The devices are evaluated by connecting their EVMs as daughter cards to the FMC port on TSW14J56 and using the HSDCPRO software to send or capture data. To enable TSW14J56 to work, the board includes a USB to SPI port, DDR3 memory and an Arria V GZ FPGA. Inside the FPGA, there are interface controllers for connecting the FPGA to DDR3 memory and other external peripherals through SPI. Also present are serdes transceivers for interfacing to the data converter under evaluation, JESD204B IP, Reconfiguration controllers to dynamically switch between supported modes and PLL's for internal clock management.

Architecture:

The FPGA architecture is divided in to modules as shown below.

1. DDR3 memory controller IP
2. SPI to Avalon Master Bridge IP
3. JESD204B Megacore IP TX/RX
4. Arria V Gz Native PHY transceiver IP TX/RX
5. Assembler & Deassembler (Transport layer)
6. enc_data_gen module
7. dec_data_capture module
8. trigger module
9. framesoftrst

DDR3 memory controller IP

The firmware contains two independent instances of the DDR3 memory controller. Each controller interfaces to 4Gb of external memory and is used to read and write data into the memory. The interface is quarter rate with an output width of 256bits. It can support clock speeds up to 800MHz. Both controllers share a common PLL and DLL to help minimize FPGA resource usage. A 100MHz external reference clock is provided via differential pair pins [G20 G21] to the PLL inside the controllers. Three output pins are used to indicate the state of the memory controller: local_cal_fail, local_init_done, local_cal_success

Local_cal_fail: when high, indicates that the memory calibration failed. This signal is connected to LED D8 on TSW14J56. D8 should be turned on during normal operation.

Local_init_done: when high indicates that the memory startup sequences all checked out successfully. This pin is connected to LED D7 on TSW14J56. D7 should be turned off during normal operation

Local_cal_success: when high, indicates that memory calibration was successful. This pin is connected to LED D6 on TSW14J56. D6 should be turned off during normal operation.

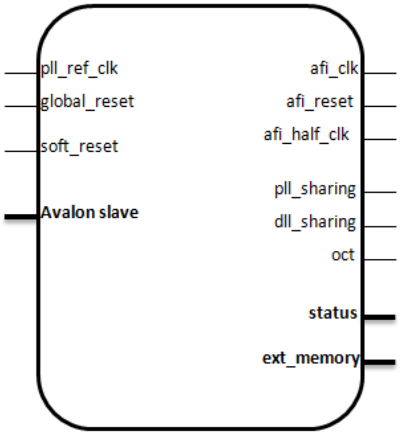
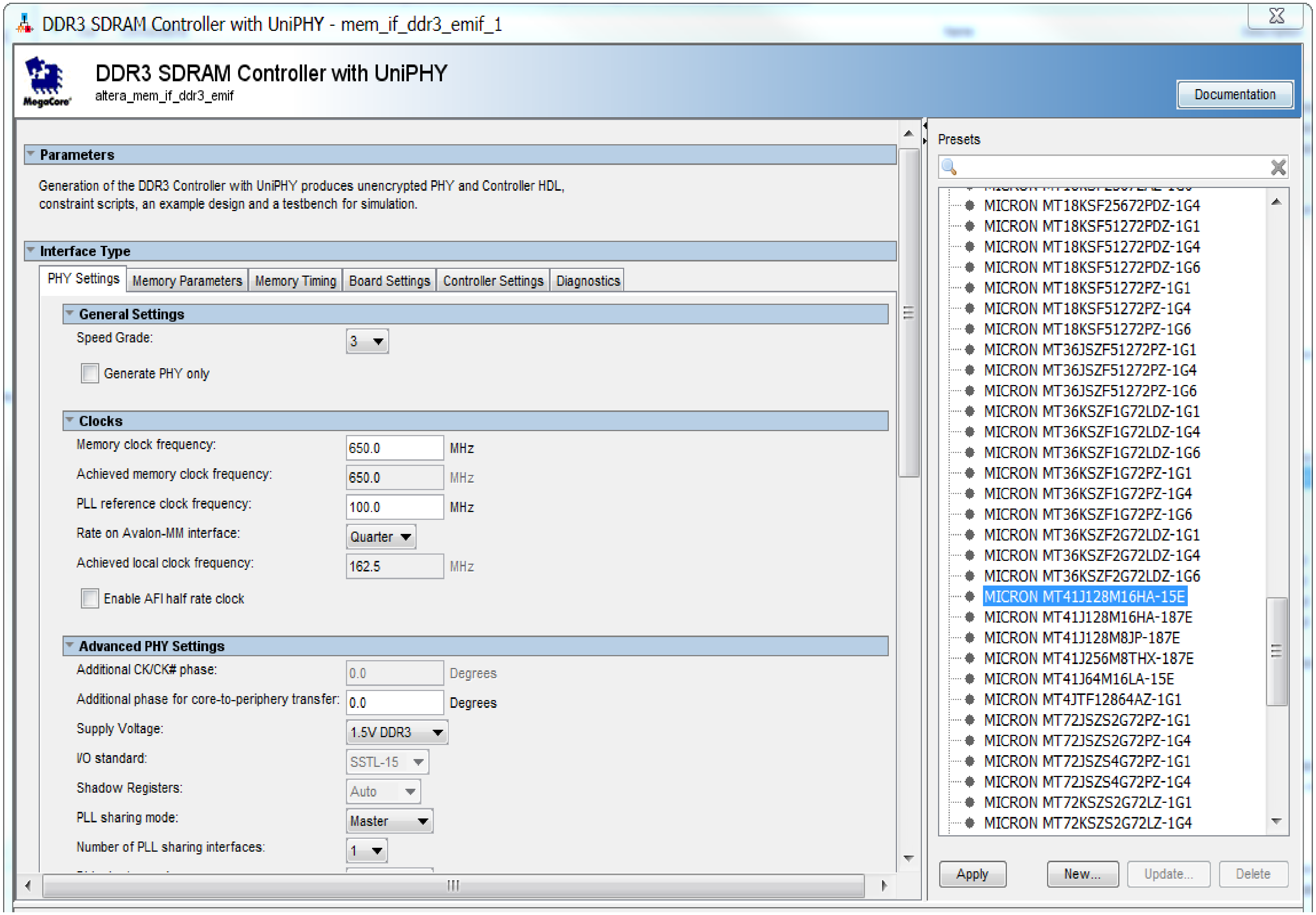


Figure 2: DDR3 memory controller interface

To setup the memory controller:

- Open the user interface (UI) for the DDR3 memory controller (shown in figure 3) from QSYS or Megawizard
- Apply the default settings for MICRON MT41J128M16HA-15E from the preset window on the left of the UI.
- Set the desired memory clock frequency and the reference input clock frequency on the PHY settings tab of the UI. A memory interface clock frequency of 650MHz generated from a 100MHz external reference clock is shown in figure 3.
- On the Memory interface tab set the following parameters:
    - Total Interface width = 32, DQ/DQS group size = 8, Row address width = 14, Column address width = 10, Bank address width = 3
- On the controller settings tab set the burst size to 8 (max?). For this design, data is written to and read from the memory in bursts to maximize the read and write efficiency.



DDR3 SDRAM Controller with UniPHY - mem_if_ddr3_emif_1

DDR3 SDRAM Controller with UniPHY
altera_mem_if_ddr3_emif

Parameters

Generation of the DDR3 Controller with UniPHY produces unencrypted PHY and Controller HDL, constraint scripts, an example design and a testbench for simulation.

Interface Type

General Settings

Speed Grade: 3

□ Generate PHY only

Clocks

Memory clock frequency: 650.0 MHz

Achieved memory clock frequency: 650.0 MHz

PLL reference clock frequency: 100.0 MHz

Rate on Avalon-MM interface: Quarter

Achieved local clock frequency: 162.5 MHz

□ Enable AFI half rate clock

Advanced PHY Settings

Additional CK/CK# phase: 0.0 Degrees

Additional phase for core-to-periphery transfer: 0.0 Degrees

Supply Voltage: 1.5V DDR3

I/O standard: SSTL-15

Shadow Registers: Auto

PLL sharing mode: Master

Number of PLL sharing interfaces: 1

Presets

- MICRON MT18KSF25672PDZ-1G4
- MICRON MT18KSF51272PDZ-1G1
- MICRON MT18KSF51272PDZ-1G4
- MICRON MT18KSF51272PDZ-1G6
- MICRON MT18KSF51272PZ-1G1
- MICRON MT18KSF51272PZ-1G4
- MICRON MT18KSF51272PZ-1G6
- MICRON MT36JSZF51272PZ-1G1
- MICRON MT36JSZF51272PZ-1G4
- MICRON MT36JSZF51272PZ-1G6
- MICRON MT36KSZF1G72LDZ-1G1
- MICRON MT36KSZF1G72LDZ-1G4
- MICRON MT36KSZF1G72LDZ-1G6
- MICRON MT36KSZF1G72PZ-1G1
- MICRON MT36KSZF1G72PZ-1G4
- MICRON MT36KSZF1G72PZ-1G6
- MICRON MT36KSZF2G72LDZ-1G1
- MICRON MT36KSZF2G72LDZ-1G4
- MICRON MT36KSZF2G72LDZ-1G6
- MICRON MT41J128M16HA-15E
- MICRON MT41J128M16HA-187E
- MICRON MT41J128M8JP-187E
- MICRON MT41J256M8THX-187E
- MICRON MT41J64M16LA-15E
- MICRON MT4JTF12864AZ-1G1
- MICRON MT72JSZS2G72PZ-1G1
- MICRON MT72JSZS2G72PZ-1G4
- MICRON MT72JSZS4G72PZ-1G1
- MICRON MT72JSZS4G72PZ-1G4
- MICRON MT72KSZS2G72LZ-1G1
- MICRON MT72KSZS2G72LZ-1G4

Figure 3: User interface to configure external DDR3 memory

The interface between the DDR3 memory and the JESD204B IP is shown in figure 4. The 256bits wide data interface of the JESD204B IP is split in two halves of 128 bits each before it is connected to the memory interface. This is done in order to provide sufficient bandwidth to support high serdes data rates.

Part of the 256bits wide data from the JESD204B IP to the memory may not be valid depending on the value of the JESD204B core parameter M programmed into the firmware. This range of valid data and the corresponding M values are shown in figure 4. For instance, when the M register of the IP is set to 1, only the first 64bits out of the 256bits of data to the IP are valid data. The IP will ignore all the invalid bits at its interface.

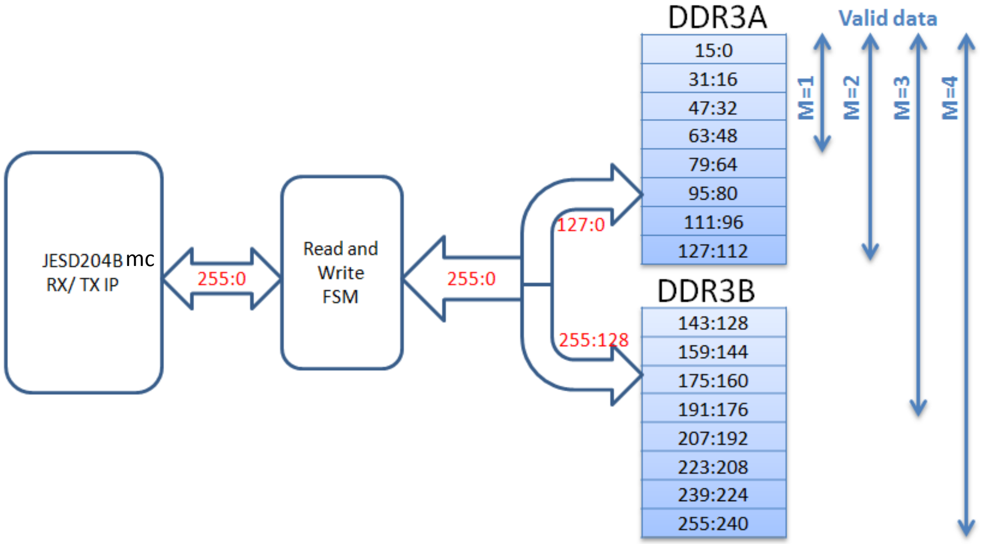


Figure 4: Interface between DDR3 memory controller and the JESD204B IP in non-transceiver mode

In transceiver mode, when receive and transmit are used simultaneously, data is stored in the external memory as shown in figure 5. This mode achieves half the available memory bandwidth when compared to the non-transceiver mode in figure 4. Details of the DDR3 memory controller can be found in [3].

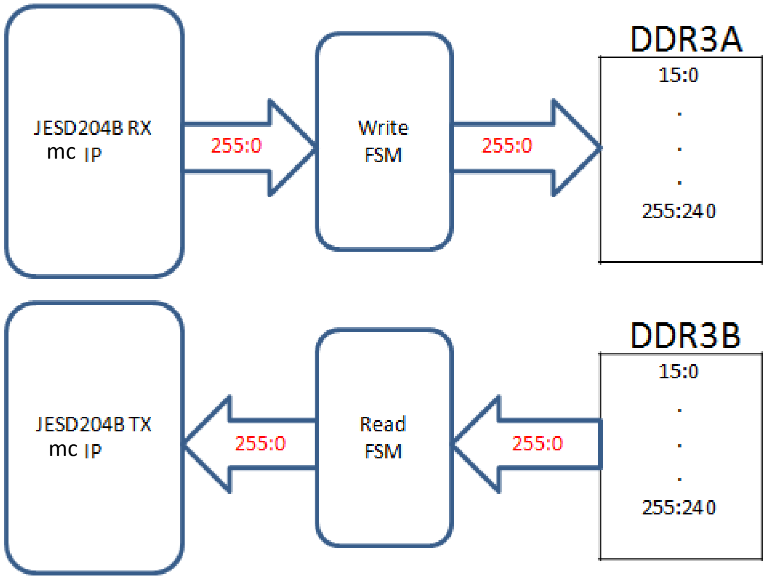


Figure 5: Interface between DDR3 memory controller and the JESD204B IP in transceiver mode

SPI to Avalon Master Bridge IP

This interface is clocked at 100MHz. The behavior of the SPI to Avalon master bridge is explained in figure 7. Before software sends (or reads) user data to (or from) the FPGA, it formats the data so that it can be transferred through the Avalon interconnect to its intended destination. The data must include the address of the slave component the data is being sent to, a read or write command, the SOP byte, EOP byte and the Escape character.

The firmware includes two SPI to Avalon Master bridges. Each SPI master bridge uses an address to communicate with any slave component connected to it. One SPI master is used for configuring the firmware in different modes by reading and writing to internal registers. The second SPI master is dedicated for reading and writing to the external DDR3 memory. The appendix gives details of each slave component and their addresses and how they are accessed through this SPI master bridge.

Details on the operation of the SPI to Avalon master core can be found in [1]

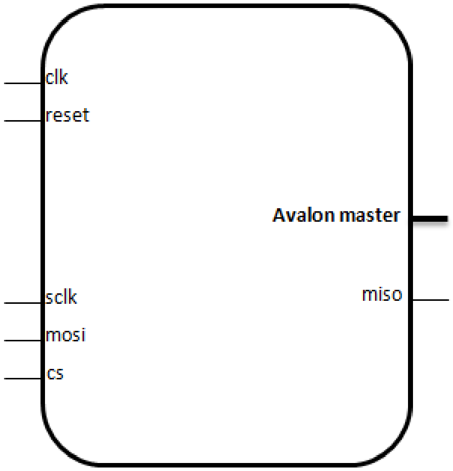


Figure 6: Interface signals of the SPI to Avalon Master Bridge

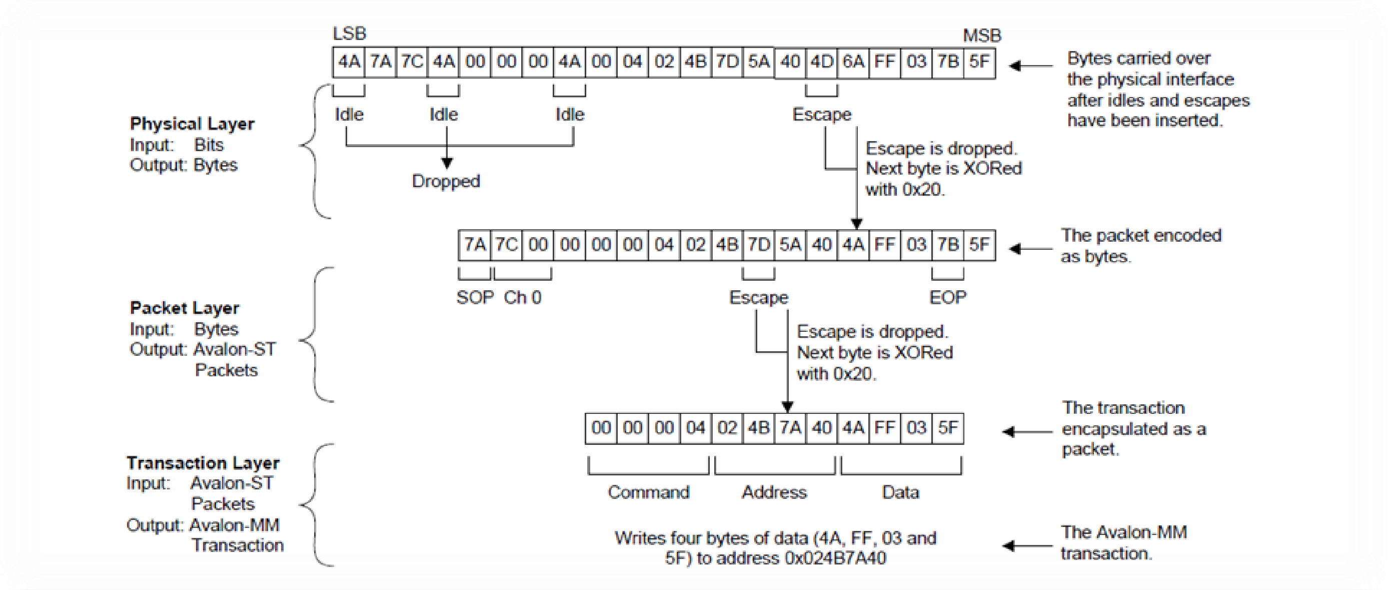

LSB
MSB
4A 7A 7C 4A 00 00 00 4A 00 04 02 4B 7D 5A 40 4D 6A FF 03 7B 5F
Bytes carried over the physical interface after idles and escapes have been inserted.
Physical Layer
Input: Bits
Output: Bytes
Idle
Idle
Idle
Escape
Dropped
Escape is dropped. Next byte is XORed with 0x20.
7A 7C 00 00 00 00 04 02 4B 7D 5A 40 4A FF 03 7B 5F
The packet encoded as bytes.
Packet Layer
Input: Bytes
Output: Avalon-ST Packets
SOP
Ch 0
Escape
EOP
Escape is dropped. Next byte is XORed with 0x20.
00 00 00 04 02 4B 7A 40 4A FF 03 5F
The transaction encapsulated as a packet.
Transaction Layer
Input: Avalon-ST Packets
Output: Avalon-MM Transaction
Command
Address
Data
Writes four bytes of data (4A, FF, 03 and 5F) to address 0x024B7A40
The Avalon-MM transaction.

Figure 7: Flow of data through the SPI to Avalon Master bridge

JESD204B Megacore IP TX/RX

This IP implements the JESD204B link layer with the BASE alone enabled. The IP core has a number of internal registers that must be configured correctly to enable it to work. In TSW14J56, these internal registers are programmed through the SPI interface from a PC running the HSDCPRO software. The HSDCPRO software reads the required configuration values from the device initialization (ini) file and writes them to their respective register address. These configuration parameters and their offset addresses are given in the Appendix. The main purpose of this IP is to apply the JESD CGS and ILAS sequence with the Deserialized data from the Transceiver IP. The data coming out of the JESD Megacore IP is formatted in the Transport layer and only then samples are obtained.

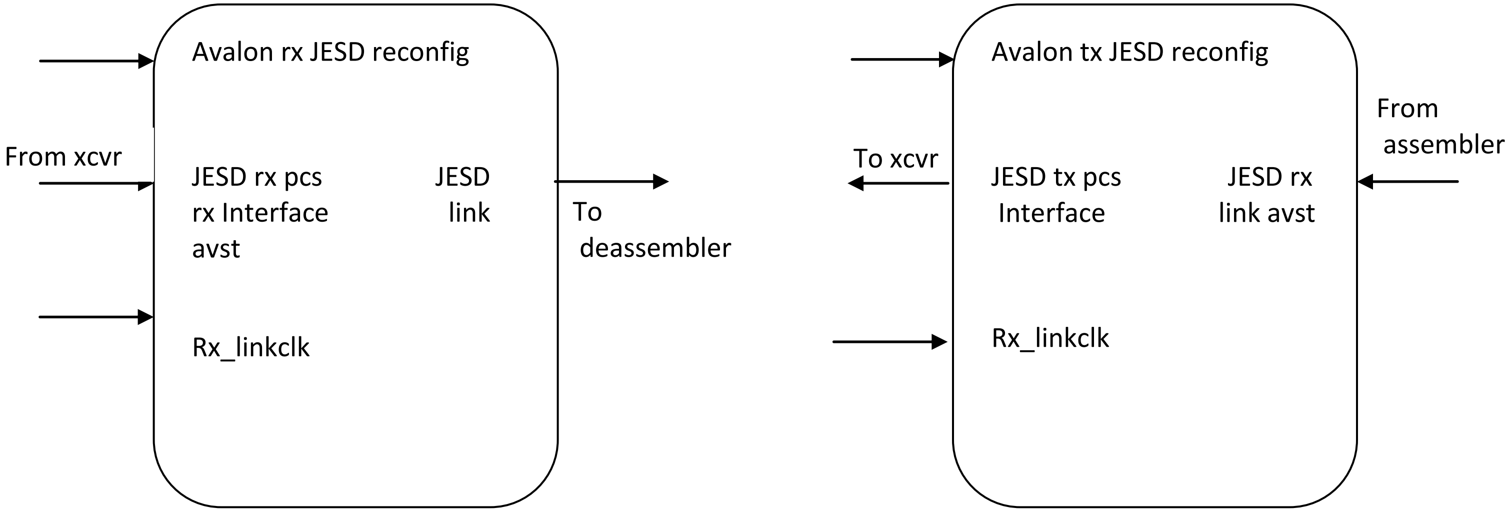
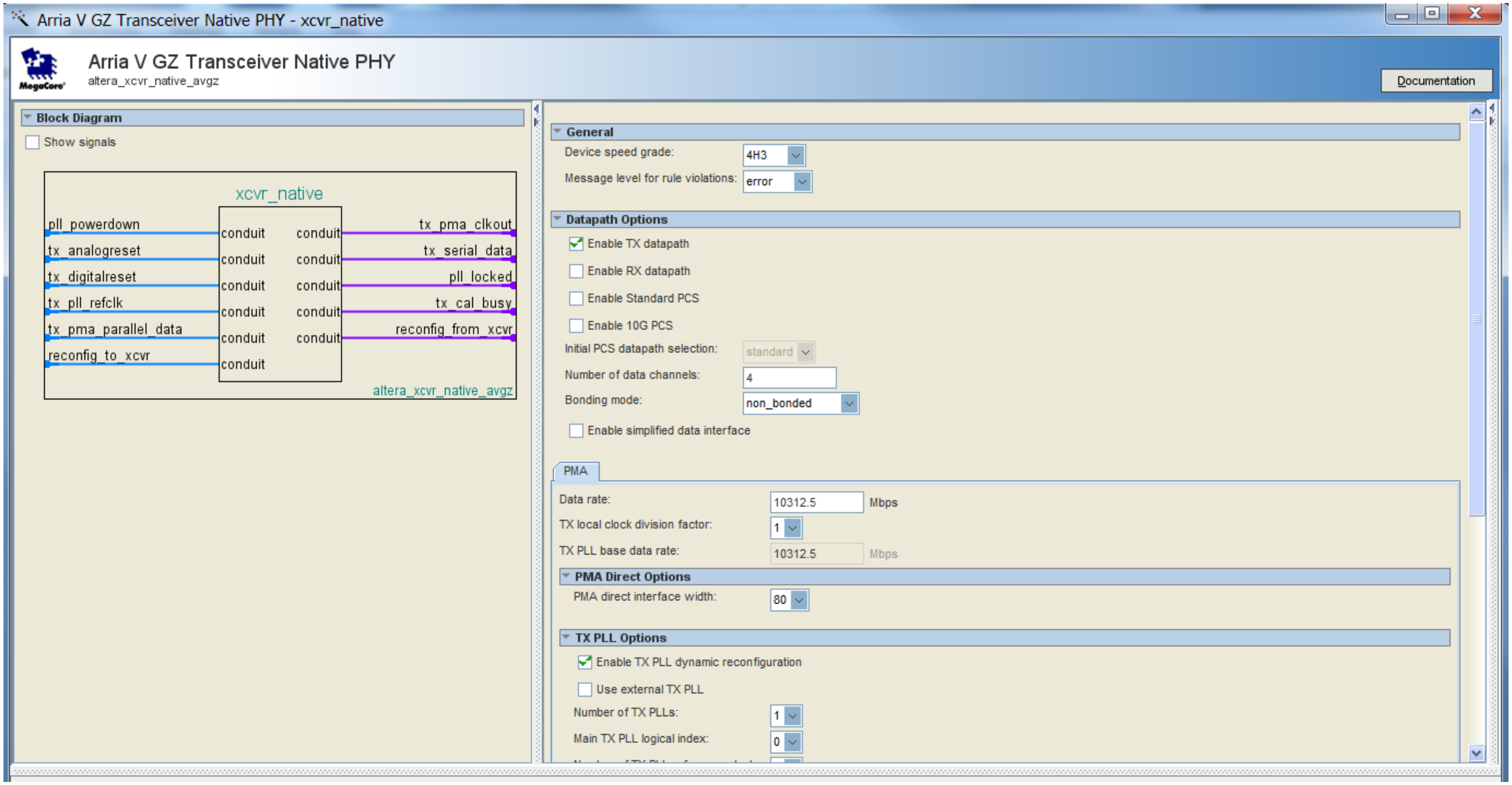


Figure 8: Interface to JESD204B TX/RX IP's

Arria V GZ Native PHY transceiver IP TX/RX

The Arria V GZ FPGA (5AGZME1) contains up to 12 high speed transceivers. However, a maximum of 10 transceivers can be run simultaneously because the transceiver in either channel 1 or 4 is used as a central clock divider instead of a transceiver channel. The data rate supported by the transceivers can be extended to 12.5Gbps (in the fastest device speed grade) with the Native PHY IP. The user interface (UI) for the Native PHY IP is shown above in figure 10.



General

Device speed grade: 4H3

Message level for rule violations: error

Datapath Options

☑ Enable TX datapath

□ Enable RX datapath

□ Enable Standard PCS

□ Enable 10G PCS

Initial PCS datapath selection: standard

Number of data channels: 4

Bonding mode: non_bonded

□ Enable simplified data interface

PMA

Data rate: 10312.5 Mbps

TX local clock division factor: 1

TX PLL base data rate: 10312.5 Mbps

PMA Direct Options

PMA direct interface width: 80

TX PLL Options

☑ Enable TX PLL dynamic reconfiguration

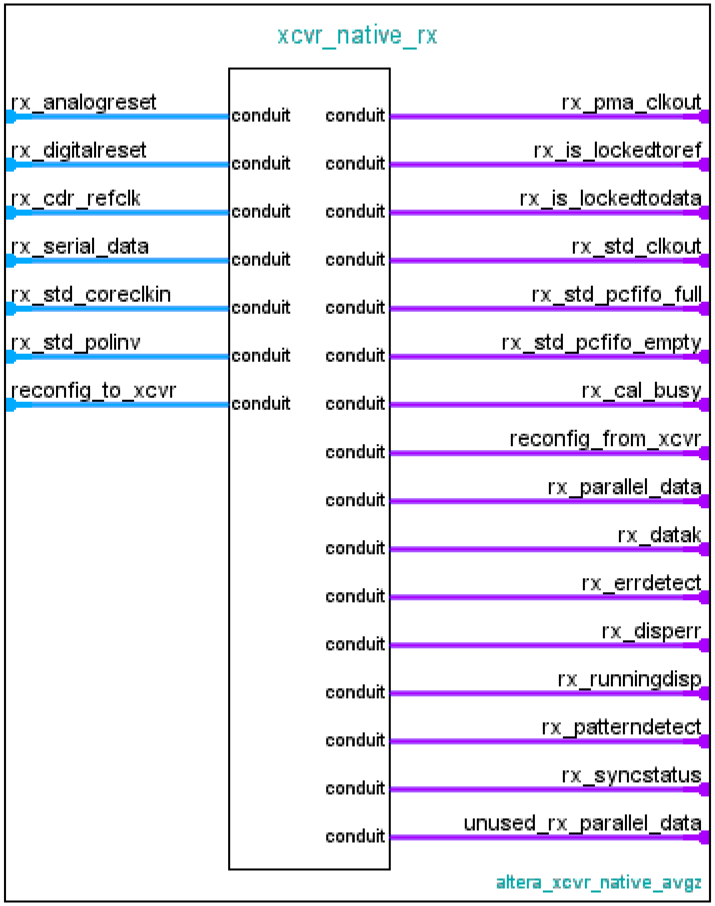
□ Use external TX PLL

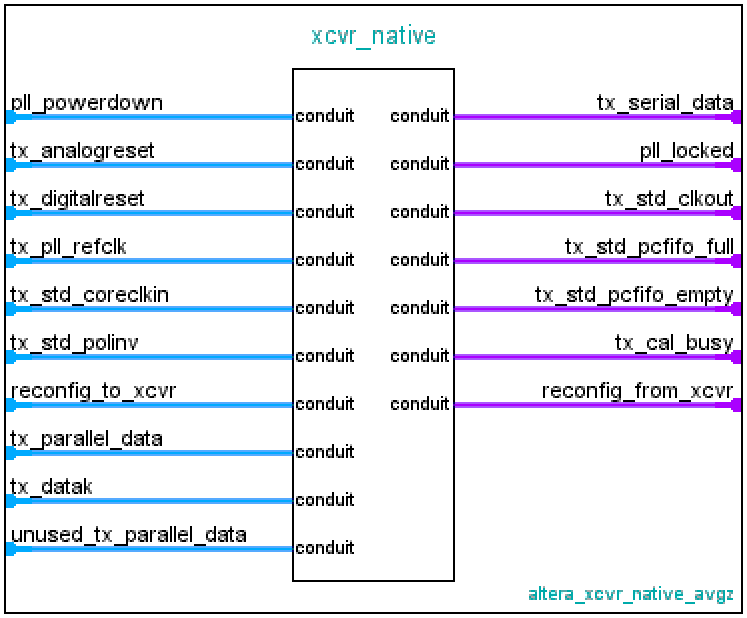
Number of TX PLLs: 1

Main TX PLL logical index: 0

Figure 10: User interface for the Native PHY transceiver IP

The Native PHY is used in standard PCS mode. The PCS part is included in the transceiver in contrast to its predecessor(In MTI firmware the PCS 8B/10B is included in the JESD MTI core). The 256 bit parallel PCS bus is connected to the JESD Megacore module.





Other differences from the former firmware include enabling lane polarity control option.

Assembler & Deassembler (Transport layer)

The transport layer in the JESD204B IP core consists of an assembler at the TX path and a deassembler at the RX path.

The transport layer provides the following services to the application layer (AL) and the DLL:

- The assembler at the TX path:
- maps the conversion samples from the AL (through the Avalon-ST interface) to a specific format of non-scrambled octets, before streaming them to the DLL.
- reports AL error to the DLL if it encounters a specific error condition on the Avalon-ST interface during TX data streaming.
- The deassembler at the RX path:
- maps the descrambled octets from the DLL to a specific conversion sample format before streaming them to the AL (through the Avalon-ST interface).
- reports AL error to the DLL if it encounters a specific error condition on the Avalon-ST interface during RX data streaming.

The Altera provided Assembler Deassembler source code is modified to make sure no 0s are included in the 256 bit bus to and from the transport. This is implemented through a shift register which shifts data based on a counter value. This counter value thereshold is based on the L and F parameters.

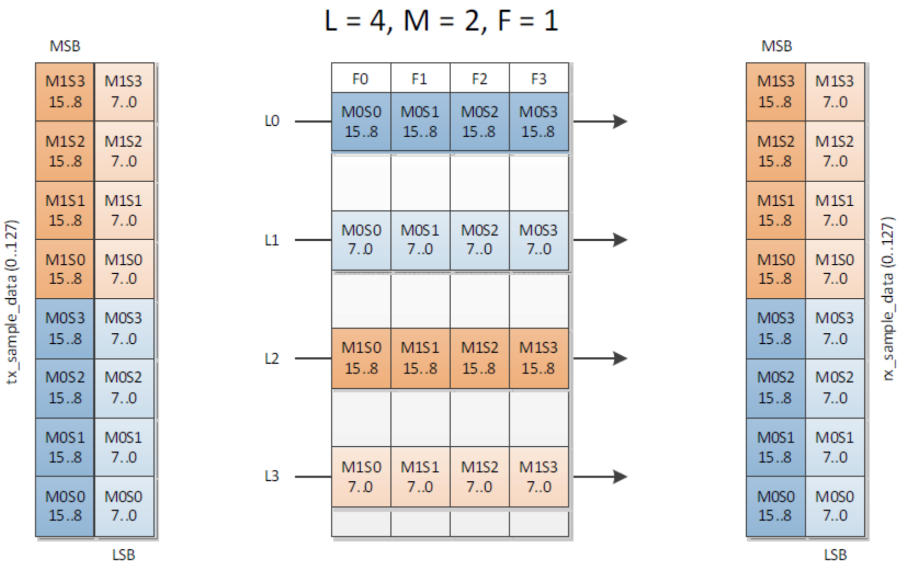


Figure 3: Data formatting in LMF = 421 mode

enc_data_gen module

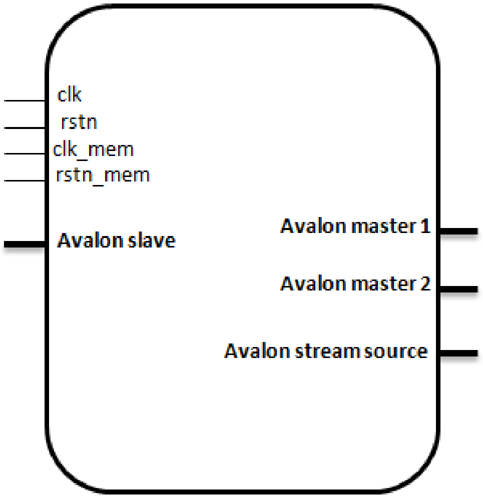


Figure 4: Interface to *enc_data_gen* module

The *enc_data_gen* module is used to read data from the DDR3 memory and send it to the JESD204B TX IP. Several control signals exist that are used to control the behavior of this module. The values of these signals are set via software through the USB to SPI port on TSW14J56 and they are described in Table 2.

Table 1: Signals for controlling the behavior of the transmit firmware

*Offset Address	Size	Description
0x20000	32	[0]- read start [1]- read loop [2]- read stop [3]- xcvr mode [31:4] data length

*register address = offset address + base address, base address= 0x0

This module transitions between two states, IDLE and AVST_READY as shown in figure 15.

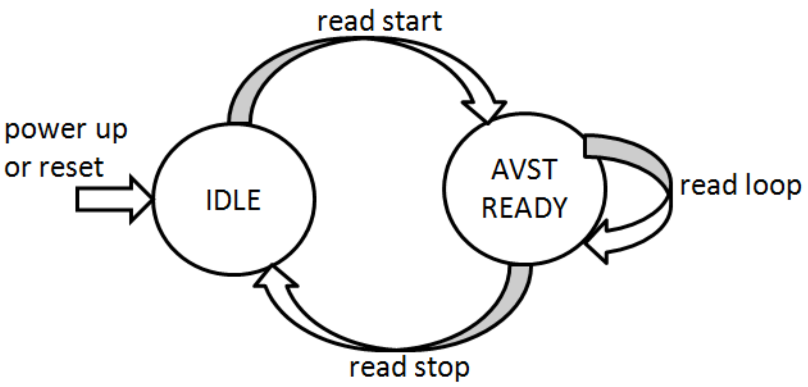


Figure 5: State transitions in *enc_data_gen* module

read start: This bit is set high to trigger reading data from DDR3 memory. When set the *enc_data_gen* module exists the IDLE state to the AVST_READY state.

read loop: When set high forces the memory address counter to wrap around to zero. This puts the memory read operation in an infinite loop.

read stop: when set forces the *enc_data_gen* module into idle state. In idle state, the address counter is reset to zero, read enable signals are de-activated and the data interface to the JESD204B IP holds the last data read from the memory.

xcvr mode: This bit puts the module into transceiver mode when set high. When in transceiver mode, both transmit and receive run simultaneously and data (width = 256) will only be read from DDR3B. In non-transceiver mode, data (width = 256) is read from both DDR3A (width = 128) and DDR3B (width = 128).

data length: sets the maximum length of the memory address counter. The value of the data length register is 1/4th the number of samples per channel. Thus, to read 65536 samples per channel from memory, data length register must be set to 16384.

dec_data_capture module

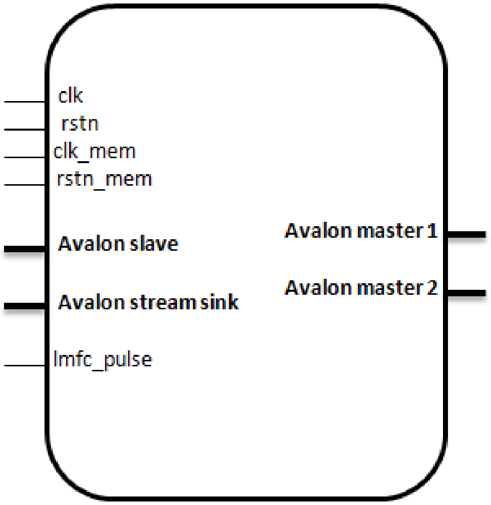


Figure 6: Interface signals for *dec_data_capture* module

This module takes user data from the JESD204B RX IP and writes it into DDR3 memory. The interface is shown in figure 16. The signals that control the behavior of this module are described below in table 3.

Table 2: Signals for controlling the behavior of the receive firmware

*Offset Address	Size	Description
0x20000	32	[0]- capture start [1]- capture done [3]- xcvr mode [31:4] data length

*register address = offset address + base address, base address= 0x400000

capture start: when set high, signifies the start of data capture from the JESD interface into the DDR3 memory. It causes the *dec_data_capture* module to transition from the IDLE state to LMFC WAIT state. The state transitions for this module are shown in figure 17.

capture done: This bit is set high when the length of data written to memory equals the value specified in the data length register. It indicates the end of data capture.

xcvr mode: This bit puts the module in transceiver mode when set high. When in transceiver mode, data (width = 256) will only be written to DDR3A. In non-transceiver mode, data (width = 256) is written to both DDR3A (width = 128) and DDR3B (width = 128).

Data length: sets the length of data to capture from the JESD204B RX IP and store in memory. The value of the data length register is 1/4th the number of samples per channel. Thus, to capture 65536 samples per channel from an ADC, the data length register must be set to 16384.

As shown in figure 17, at power up or reset, the dec_data_capture module enters the IDLE state.

In the IDLE state;

- the data interface (avst_data) to the JESD204B IP is held at its previous value
- the write enable signal to the memory interface is de-asserted.
- Memory address counter is forced to zero

When the capture start bit is set to high, the state will transition from IDLE to LMFC WAIT.

In the LMFC WAIT state;

- The module waits for *lmfc pulse* signal to go high. *lmfc pulse* is an output from the JESD204B RX IP and it is used to align the start of data capture to the local multi frame clock
- All the signals keep their values from the IDLE state

When *lmfc pulse* goes high, the state will transition from LMFC WAIT to AVST READY.

In AVST READY state;

- The write enable signal to the DDR3 memory is asserted
- Sampled data at the data interface of the JESD204B RX IP is stored in memory
- Memory address counter is incremented in steps of the write burst size. In TSW14J56, the burst size is 8.

When the memory address counter reaches the value set in the data length register, the capture done bit is set high to indicate the end of data capture and the state transitions to IDLE.

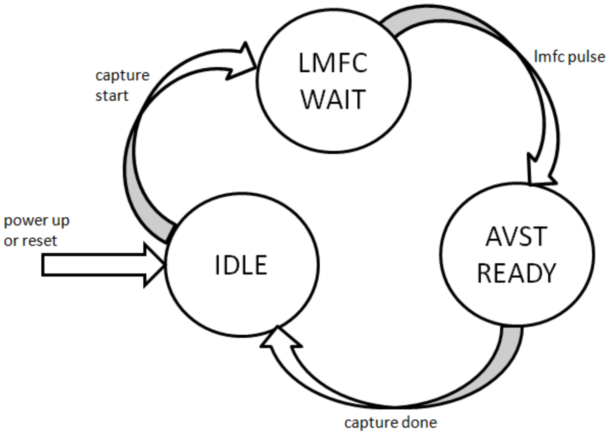


Figure 7: State transitions for *dec_data_capture* module

Trigger module

The trigger mode in TSW14J56 has two options namely:

1. Normal Trigger mode
2. SYSREF based trigger mode

Normal Trigger mode

In this mode there when capture or gen module is in IDLE state waiting for an external trigger to be received. After the external trigger rising edge is detected the capture or generation immediately starts. In case of capture module it enters LMFC WAIT state and starts the capture after LMFC pulse. The external trigger is sampled with respect to the frame clock.

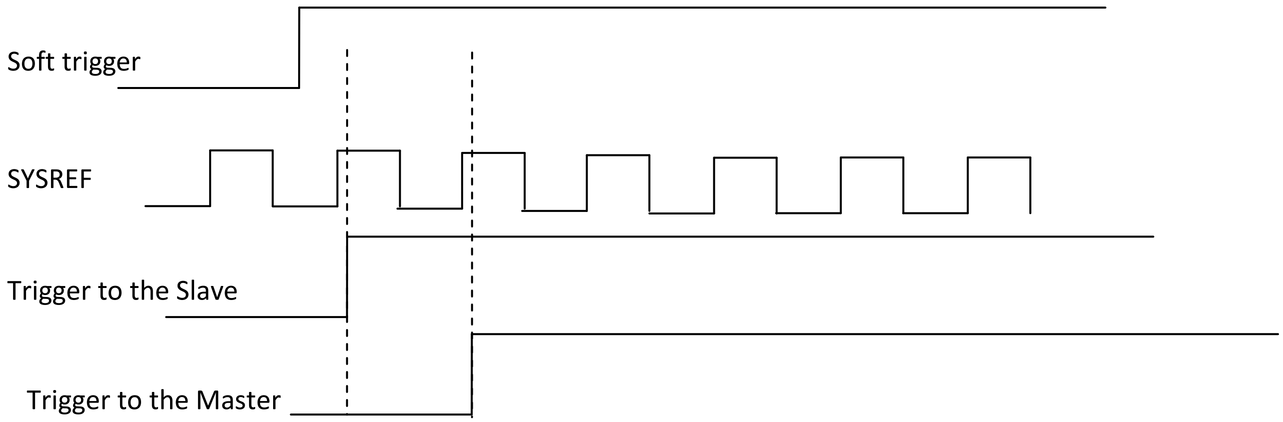
SYSREF based trigger mode

In the SYSREF based trigger mode there are two sub modes (i) Master triggering mode (ii) Slave triggering mode.
In general this mode is used to synchronize two ADC or DAC setups based on a common continuous SYSREF signal in both the setups.
The trigger generating setup is called master setup and trigger receiving setup is called slave setup

Below the two of the submodes are explained in detail

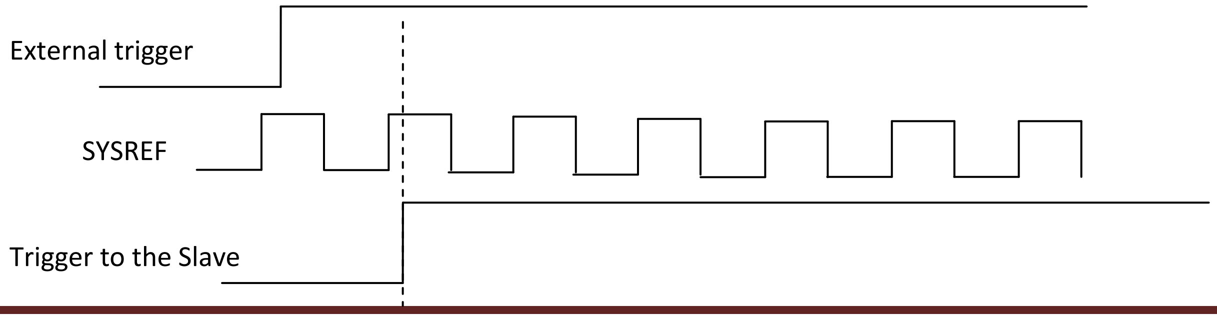
(i)Master triggering mode

In master mode the trigger pin is configured as an output. The trigger generation is by toggling a bit in the dedicated trigger register. This toggling is done by the software through through the USB to SPI port on TSW14J56. The rising edge of the toggled signal is sent to the trigger module. The output from this trigger module for slave triggering starts at the first rising edge of the SYSREF signal. The output signal from the trigger module for initiating capture or generation, starts at the second rising edge of the SYSREF signal.



(ii)Slave triggering mode

In Slave mode the trigger pin is configured as input. Module waits for the external trigger and generates the trigger aligned to the first encountered SYSREF rising edge. The rising edge of this SYSREF aligned trigger starts the capture or generation.



The signals that control the triggering in capture module (dec_data_capture) are listed in table 4 below

*Offset Address	Size	Description
0x20004	32	[0]- X [1]- X [2]- X [3]-trigger status [6:4]- Delay clk [7]- ext trig mode en [8]-Trig sel [9]- master / slave [10]- soft trig tog bit [11]- sysref rise/fall [12]- out trigger pol [13]- SYSREF trig en [16:14]- sysref cnt [31:17]-XX

Table 4: Signals for controlling the triggering in dec_data_capture

*register address = offset address + base address, base address= 0x400000
The signals that control the triggering in generation module (enc_data_gen) are listed in table 5 below

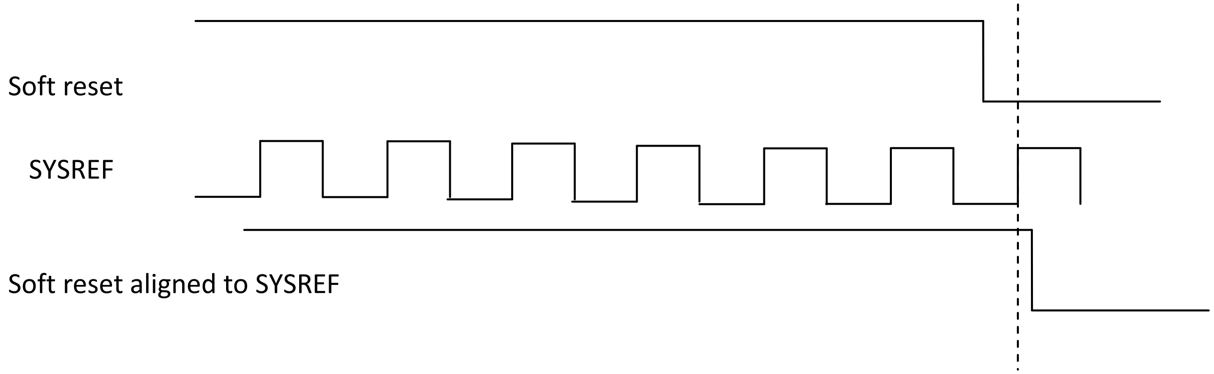
*Offset Address	Size	Description
0x20004	32	[0]- X [1]- X [2]- X [3]-trigger status [6:4]- Delay clk [7]- ext trig mode en [8]-SYSREF trig en [11:9]- sysref cnt [12]- sysref rise/fall [13]- out trigger pol [14]- master/slave [15]- soft trig tog bit [31:16]-XX

*register address = offset address + base address, base address= 0x000000

In the current firmware most of the parameters out trigger pol, sysref cnt, sysref rise/fall are hardcoded.

framesoftrst

This module is confined to the JESD RX side. The JESD RX Megacore module during reconfiguration is set in reset state. The reset state is controlled by software through the USB to SPI port on TSW14J56. The deassertion of this reconfig reset was randomn. This module was included in order to make sure the deassertion occurs only at the rising edge of SYSREF rising edge. This mechanism helped in achieving consistent LMFC clock generation from the JESD RX Megacore.



Clocking architecture

The core of the FPGA can be divided broadly into 2 regions: the fabric, and the transceivers. Each region contains a PLL that is used to generate clocks needed in that region. The PLL for the FPGA fabric is commonly referred to as the fPLL. Likewise, the PLL used to generate the high speed clock for the transceivers is known as the CMU PLL. In TSW14J56, both the fPLL and the CMU PLL share a common reference clock as shown in figure 12. This common reference clock can be provided through the FMC port to differential pair pins [U23,U24] on the FPGA or can also be provided through differential pair pins [N23,N24] on the FPGA via an SMA connector. There are 3 clock domains present in the firmware and these are illustrated in figure 12.

a) All configuration interfaces are clocked at 100MHz. This includes the SPI core, the PLL reconfiguration controller and the transceiver reconfiguration controller

b) The JESD204B IP is clocked at lane rate/40 where lane rate is the serdes data rate.

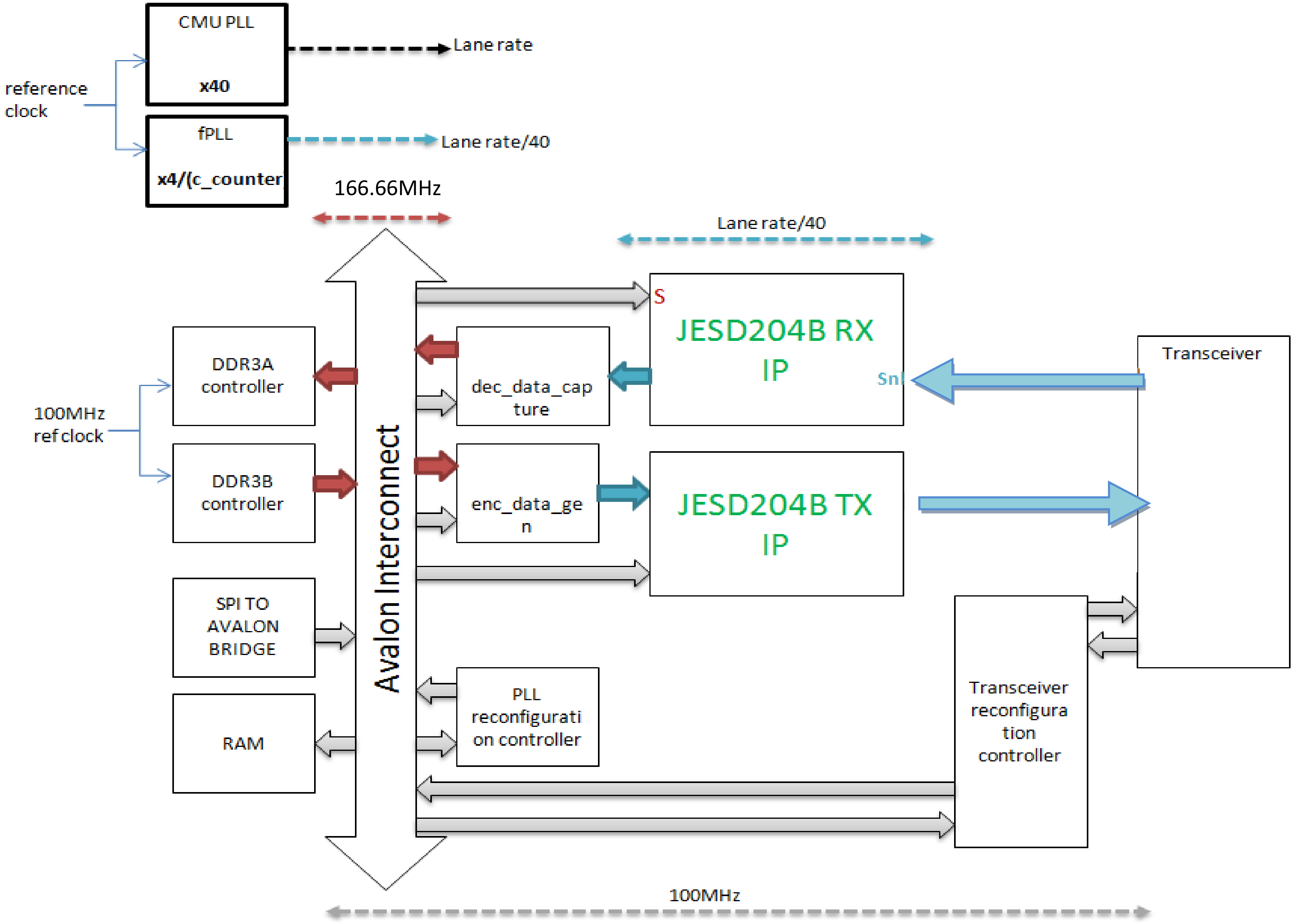


Figure 8: Clocking architecture of JESD204B firmware

c) The data interface to the memory interface is clocked at a fixed 166.66MHz. Since the controller is quarter rate, the external memory runs at 4x166.67= 666.667M

fPLL

As mentioned earlier, the fPLL generates the clock required for the FPGA fabric. This clock is used mainly as the device clock to the JESD204B IP. Figure 13 shows how the fPLL generates the device clock from the reference clock provided at pins [U23,U24]. The reference clock is multiplied by 4 and then divided down with the C-counter. The value of the C-counter is programmable and can be dynamically re-configured to support different device clock frequencies.

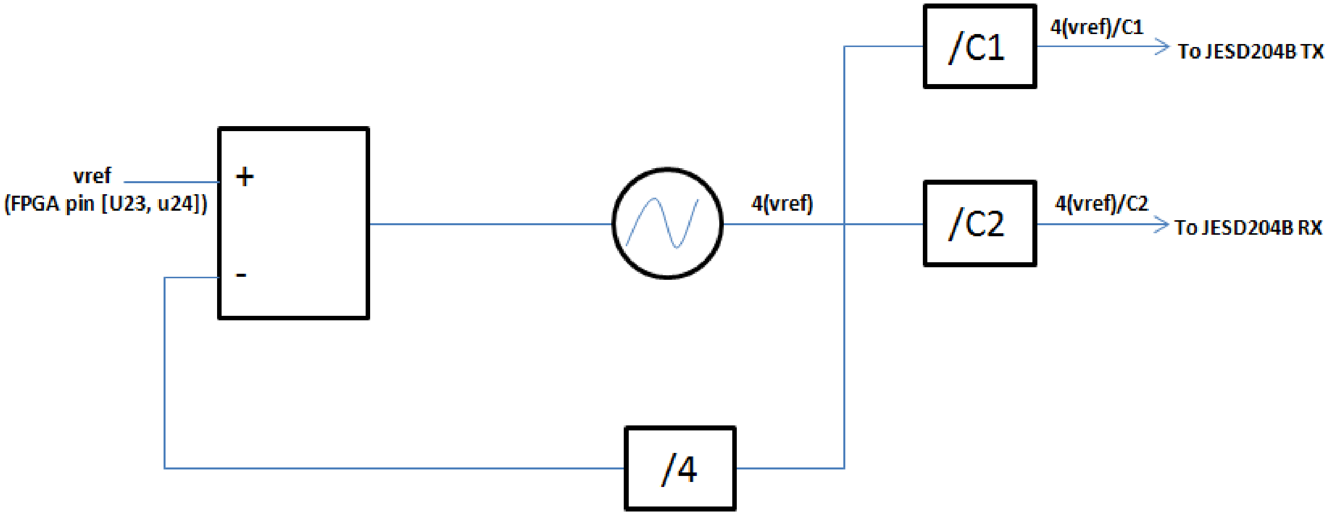


Figure 9: JESD204B device clock generation by fPLL

Understanding C-counter re-configuration

The value used to configure the C-counter consists of three bytes: an address byte, a high count byte and a low count byte. The address byte for the C1 counter shown in figure 13 above is 0x04 and the address byte for the C2 counter is 0x08. The outputs of the C1 and C2 counters are used as the device clocks to the JESD204B transmitter and JESD204B receiver blocks respectively. The C counter reconfiguration value is illustrated below for C1 (transmit) and C2 (receive):

For transmit (C1):

04	HIGH COUNT	LOW COUNT

For receive (C2):

08	HIGH COUNT	LOW COUNT

In both transmit and receive, the sum of HIGH COUNT and LOW COUNT gives the actual C counter value.

For example, to configure the C counter to decimal 20 (0x14) in the receiver firmware, the hex value 0x 080A0A or 0x08080C etc may be used. Likewise, to configure the C counter in the transmit firmware to 20, either 0x040A0A or 0x04080C etc can be used as well. HIGH COUNT and LOW COUNT cannot be zero. The Avalon read and write commands that are used to achieve fPLL reconfiguration can be found in the Appendix. Details of the C-counter reconfiguration can also be found in [6]

CMU PLL

This PLL generates the high speed serdes clock required by the high speed transceivers.

By default, the CMU PLL is set to multiply the reference clock provided at pins [U23,U24] by 40. This default multiplier can be dynamically changed by streaming a mif file. The HSDCPRO software can be used to stream the mif file to change the CMU PLL settings. MIF files for CMU PLL re-configuration are automatically generated after running the Assembler in Quartus II software. To start reconfiguration, the contents of the MIF file are first written to RAM. In TSW14J56, this RAM is dual port with dimensions of 16×128 and base address of 0x801100. After writing the MIF file to RAM, the transceiver reconfiguration controller is then triggered with a series of Avalon write commands to begin the reconfiguration process. The steps used to reconfigure the CMU PLL can be found in the Appendix.

Details of how to stream a MIF file to change the default settings of the CMU PLL can be found in [7]

The CMU PLL can span the frequency range from 0.611GHz to 10.3125GHz (lower speed grade device: 5AGZME1E3H29C4) or 0.611GHz to 12.5GHz (higher speed grade device: 5AGZME1E2H29C3).

References

[1] "Embedded Peripherals IP User Guide", *Altera Corporation, ch. 18, pg. 18-1, June 2011.*

[2] "Avalon Interface Specifications", *Altera Corporation, May 2013.*

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[4] "JESD IP Core User Guide", *Altera Corporation, June 2014.*

[5] "Altera Transceiver PHY IP Core User Guide", *Altera Corporation, ch. 14, pg 14-1, December 2013.*

[6] "Implementing Fractional PLL Reconfiguration with Altera PLL and Altera PLL Reconfig Megafunctions", *Altera Corporation, AN-661, November 2013.*

[7] "Using the Transceiver Reconfiguration Controller for Dyanmic Reconfiguration in Arria V and Cyclone V Devices", *Altera Corporation, AN-676, December 2013.*

Revision log

Revision	Modification details	Date of release
Rev1.0	Initial draft	2nd Dec 2014