Tapped Inductor Bandpass Filter Design

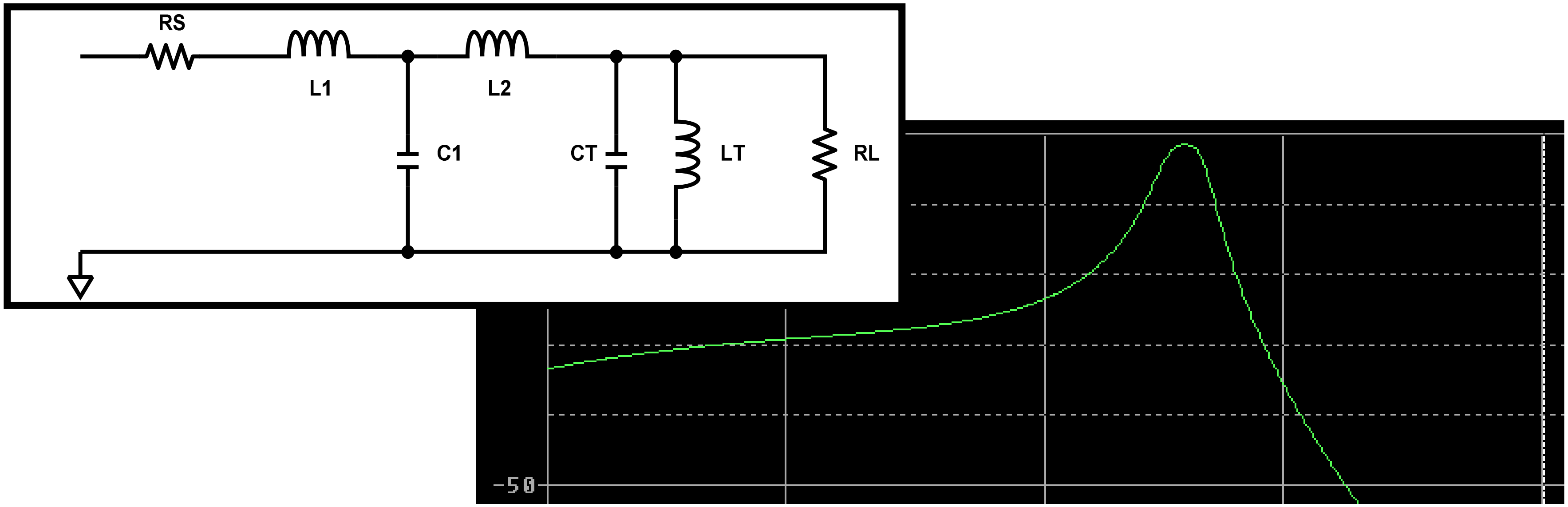
High Speed Signal Path Applications

7/21/2009 v1.6

PowerWise

National Semiconductor

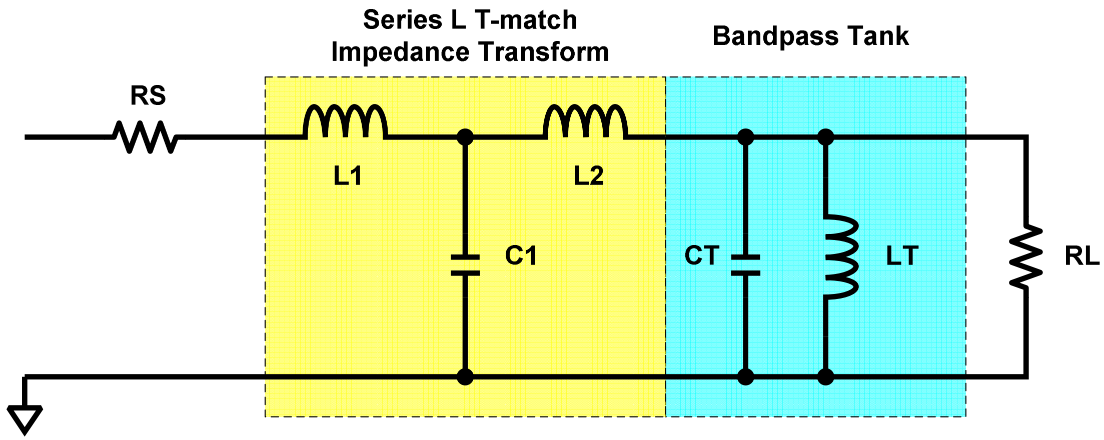
Tapped Inductor BP Filter



- 1st order (6 dB/oct) LOW frequency roll-off
  - Shunt LT
- 4th order (24 dB/oct) HIGH frequency roll-off
  - Series L1, L2 – Shunt C1, CT
- Called “Tapped Inductor” because filter uses a series-L T-match impedance transform

PowerWise National Semiconductor

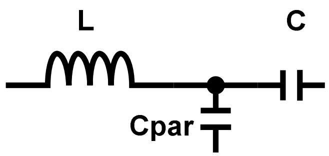
Tapped Inductor BP Filter



- Tank provides 1st order Bandpass profile
- Impedance transform matches R_L to R_S at center frequency and increases high frequency roll-off to 4th order

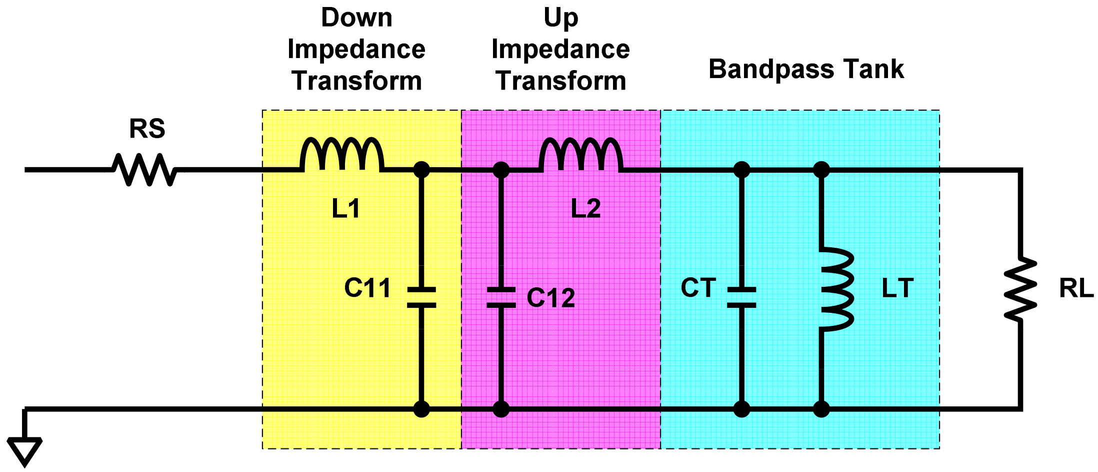
Pros / Cons

- Why is this architecture good?
  - Avoids capacitors in series branches which are very susceptible to shunt parasitics
  - Provides best harmonic tone rejection with lowest possible filter complexity
  - Good noise rejection despite shallow roll-off at low frequencies
  - Relatively easy to design filters up to 300 MHz with 3dB Q~5 (Q = Fo/BW)
  - Design procedure provides flexible matching of R_L to R_S



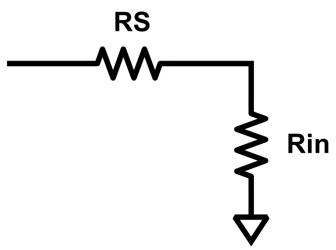
- Drawbacks?
  - Shallow low frequency roll-off may limit noise performance
  - For large R_S, R_L, and large Q's → C1 becomes prohibitively small
  - Wider passband requires shallower stopband (tradeoff)

Theory



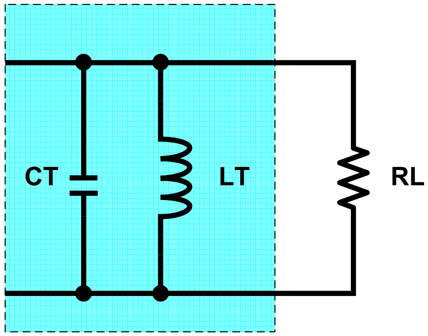
- Filter can be broken into parts for analysis
  - Bandpass Tank
  - T-match split into Up/Down impedance transforms
  - Each section characterized by Wo and Q
  - Design procedure works from load up to source

Theory: Filter Loss and Impedance Matching



- Impedance Matching
  - Power transfer maximized and reflections minimized when $R_S = R_{in}$
  - R_{in} is equivalent resistance looking into T-match
- Filter Loss
  - Related to R_S, R_L, and Q's used in design
  - Certain configurations can cause voltage gain

Theory: Bandpass Tank



- **LC Bandpass Tank**
  - **Impedance should equal R_L at center frequency due to parallel cancellation of L_T and C_T**
  - **Sets the center frequency and influences the BW**

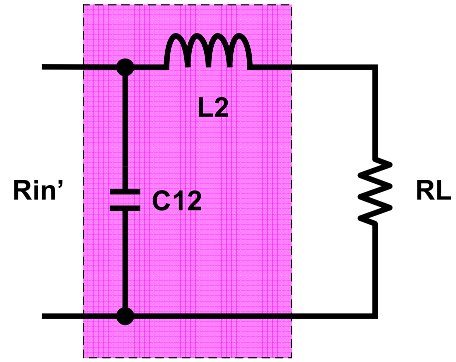
- **Design procedure**
  - **Choose filter center frequency F_0**
  - **Choose suitable Q_T**
  - **Choose R_S and R_L based on source/driver requirements and passband loss**
  - **Solve for C_T using Q equation**
  - **Solve for L_T using F_0 equation**

$$Q_T = 2\pi f_0 \cdot R_L C_T$$

$$f_0 = \frac{1}{2\pi\sqrt{L_T C_T}}$$

Theory: Up Impedance Transform

- **Up Impedance Transform**
  - When properly designed, impedance looking into network will be real and > R_L at center frequency
  - Q_U must be high enough to isolate C_{12} from the tank to preserve the tank center frequency



$$Q_U = 2\pi f_0 \frac{L_2}{R_L}$$

- **Design procedure**
  - Choose desired Q_U
  - Solve for L_2 using Q equation
  - Solve for L_2'
  - Solve for C_{12} using F_0 equation
  - Solve for R_{in}'

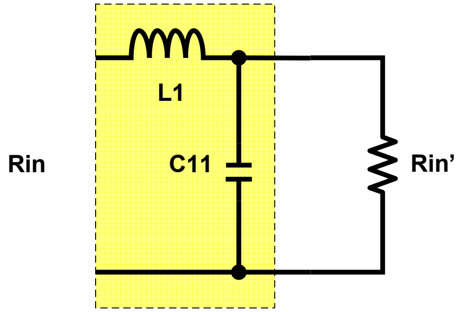
$$L_2' = L_2\left(\frac{1+Q_U^2}{Q_U^2}\right)$$

$$f_0 = \frac{1}{2\pi\sqrt{L_2' C_{12}}}$$

$$R_{in}' = R_L\left(1+Q_U^2\right)$$

Theory: Down Impedance Transform

- **Down Impedance Transform**
  - **When properly designed, impedance looking into network will be real and Rin < Rin' at center frequency**



- **Design procedure**
  - **Choose desired Q_D**
  - **Solve for C_{11} using Q equation and R_{in}' from Up Transform design procedure**
  - **Solve for C_{11}'**
  - **Solve for L_1 using F_0 equation**
  - **Solve for R_{in}**

$$Q_D = 2\pi f_0 \cdot R_{in}' C_{11}$$

$$C_{11}' = C_{11}\left(\frac{Q_D^2}{1+Q_D^2}\right)$$

$$f_0 = \frac{1}{2\pi\sqrt{L_1 C_{11}'}}$$

$$R_{in} = R_{in}'\left(\frac{1}{1+Q_D^2}\right)$$

PowerWise

National Semiconductor

Theory: Effect of Q

- Effect of Q
  - After load/source/frequency are set, Q's are the only design knobs
  - Closely related to Bandwidth of filter
  - Higher Q typically results in less loss and a narrower filter but makes filter more sensitive and harder to tune on the actual board
- Choosing Q_T
  - Intuitive trend is $Q_T \sim F_o/BW$ but the results are not simple
- Choosing Q_U
  - Set > 3 to prevent ripples in passband
- Choosing Q_D
  - Use equation for impedance matching: $$\frac{R_L}{R_S} = \frac{1+Q_U^2}{1+Q_D^2}$$
  - OR Set $Q_U < Q_D < 12$ for relaxed component values and possible voltage gain increase

PowerWise National Semiconductor

Theory: Tips

- For $R_L=4R_S$ → $Q_T=5$, $Q_D=2.34$, $Q_U=5$
  - Impedance matched, Gain ~ 0 dB
- For $R_L=4R_S$ → $Q_T=6$, $Q_D=3$, $Q_U=10$
  - Gain > 0 dB
- For $R_L=R_S$ → $Q_T=6$, $Q_D=3$, $Q_U=3$
  - Loss ~ 6dB
  - Can't increase Q_U much because R_{in} becomes too small (Avoid)
- Setting low Q_D or Q_U for wide BW can cause deep ripples in passband due to poor impedance transform.
- Increased gain can occur when $R_L>2R_S$. Set $Q_D>1.5Q_U$ only under this condition.
- Very large R_L can cause prohibitively small C_1 and large L1, L2

Theory: Tips

- Large Q_T allows for narrower and flatter bandpass but the quality is very sensitive to $(C_{11}+C_{12})$. Variations cause significant misshaping. Difficult to tune frequency.
- Small Q_T allows for easier tuning without misshaping by changing C_T OR $(C_{11}+C_{12})$. Easier to tune with C_T because it is usually much bigger.
- True bandwidth depends on both the tank and T-network.
- Filter voltage gain at center frequency:

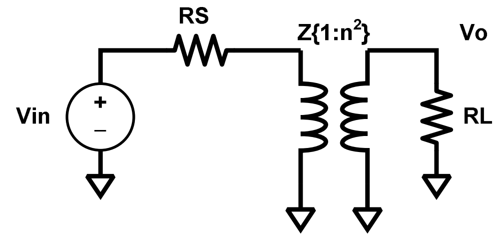
$$\left.\frac{V_{out}}{V_{in}}\right|_{f=f_0} \sim 20\log\left(\frac{R_{in}}{R_S+R_{in}}\right)+10\log\left(\frac{R_{in}^{'}}{R_S}\right)+10\log\left(\frac{R_L}{R_{in}^{'}}\right) \qquad R_{in}=\left(\frac{1+Q_U^2}{1+Q_D^2}\right)R_L$$

  - For gain > 0 dB: $R_L/R_S>1$ and $R_S<<R_{in}$
  - An impedance matched filter ($R_{in}=R_S$) has ~0 dB gain for $R_L=4R_S$

PowerWise® National Semiconductor

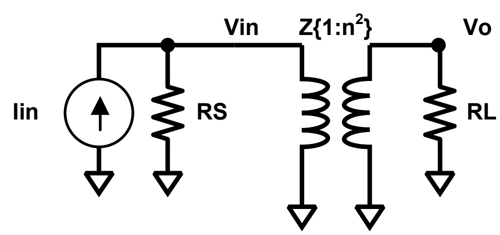
Theory: Tips

- **Voltage output Amplifier**
  - **Filter impedance Xform modeled as Transformer with coil ratio of 1:n (therefore an impedance ration of 1:n^2)**



$$\left.\frac{V_{out}}{V_{in}}\right|_{f=f_0} = \frac{n \cdot R_L}{R_L + n^2 \cdot R_S} \qquad n^2 = \frac{1+Q_U^2}{1+Q_D^2}$$

  - **If R_L=4*R_S, n=2, then G_V=1**
    - **Impedance is also matched because $R_S = R_L/n^2$**
    - **For a R_S,R_L voltage divider, G_V=0.8 (-2dB)**
    - **The LC network achieves a voltage gain of 2dB**
- **Current output Amplifier**
  - **No series R loss, G_V = n**
  - **Amplifier requires large R_S, R_L for large amplifier gain**
  - **If R_L=R_S, n=1, then G_V=1**
    - **Impedance is matched, $Q_U = Q_D$**
  - **If R_L=R_S, n=2, then G_V=2**
    - **Impedance not matched, risk more ripple in passband**

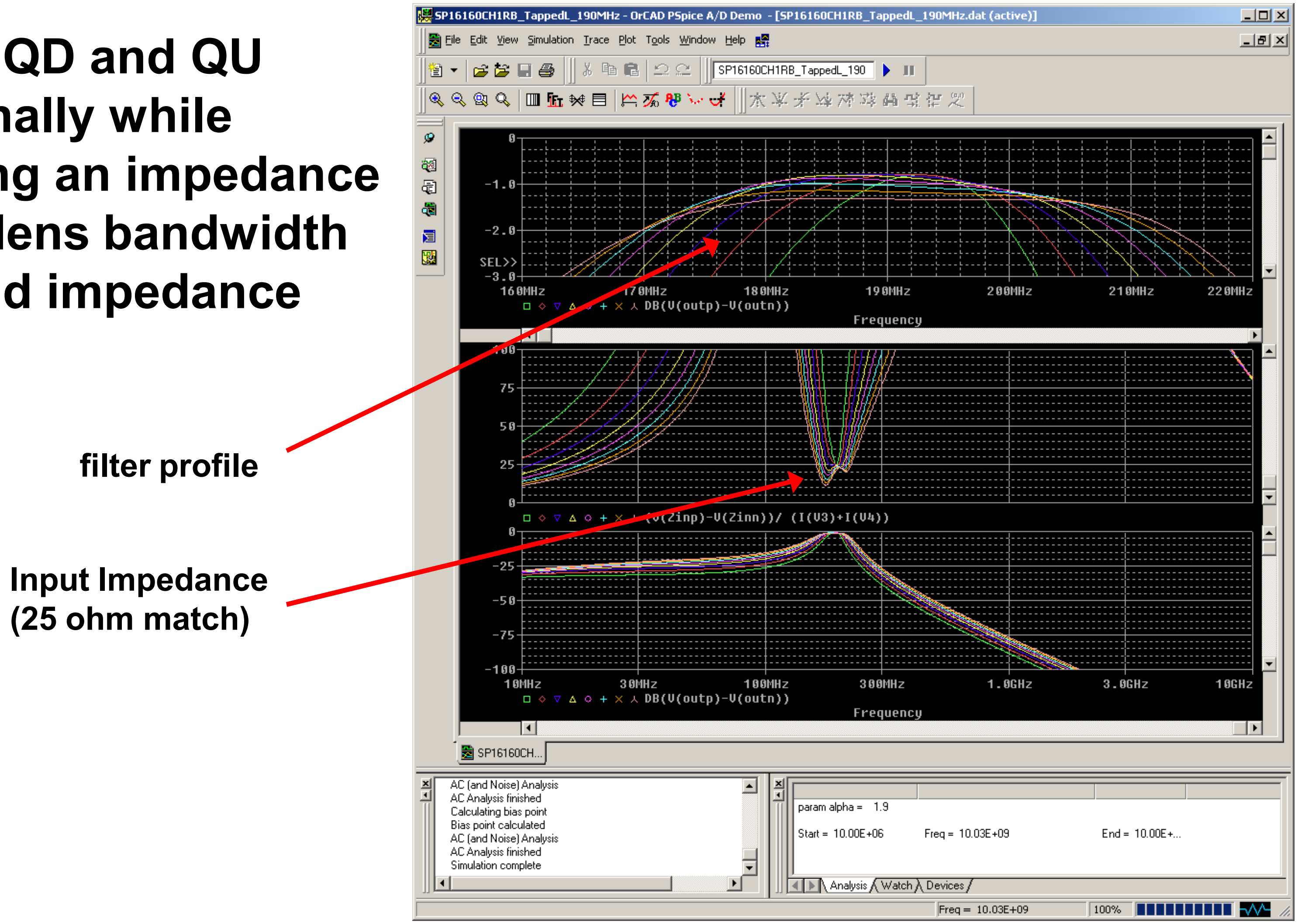


PowerWise

National Semiconductor

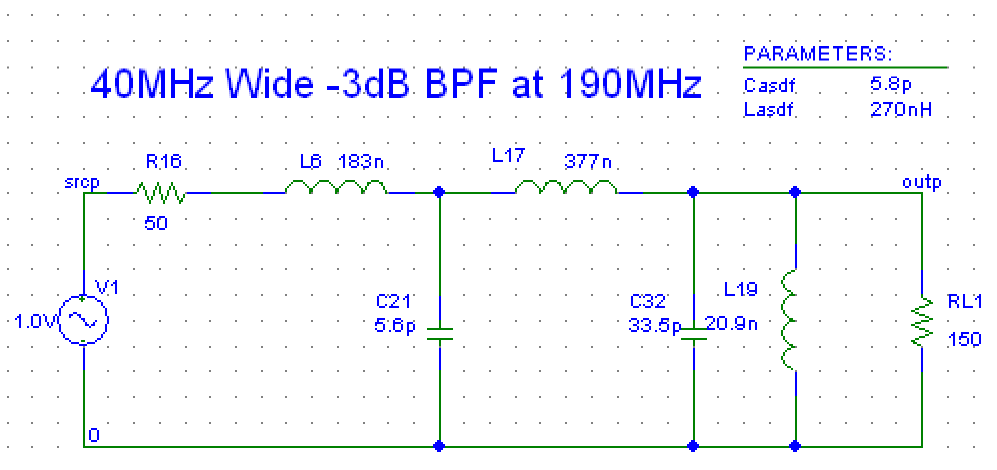
Theory: Tips

- **Reducing QD and QU proportionally while maintaining an impedance match widens bandwidth of filter and impedance match**

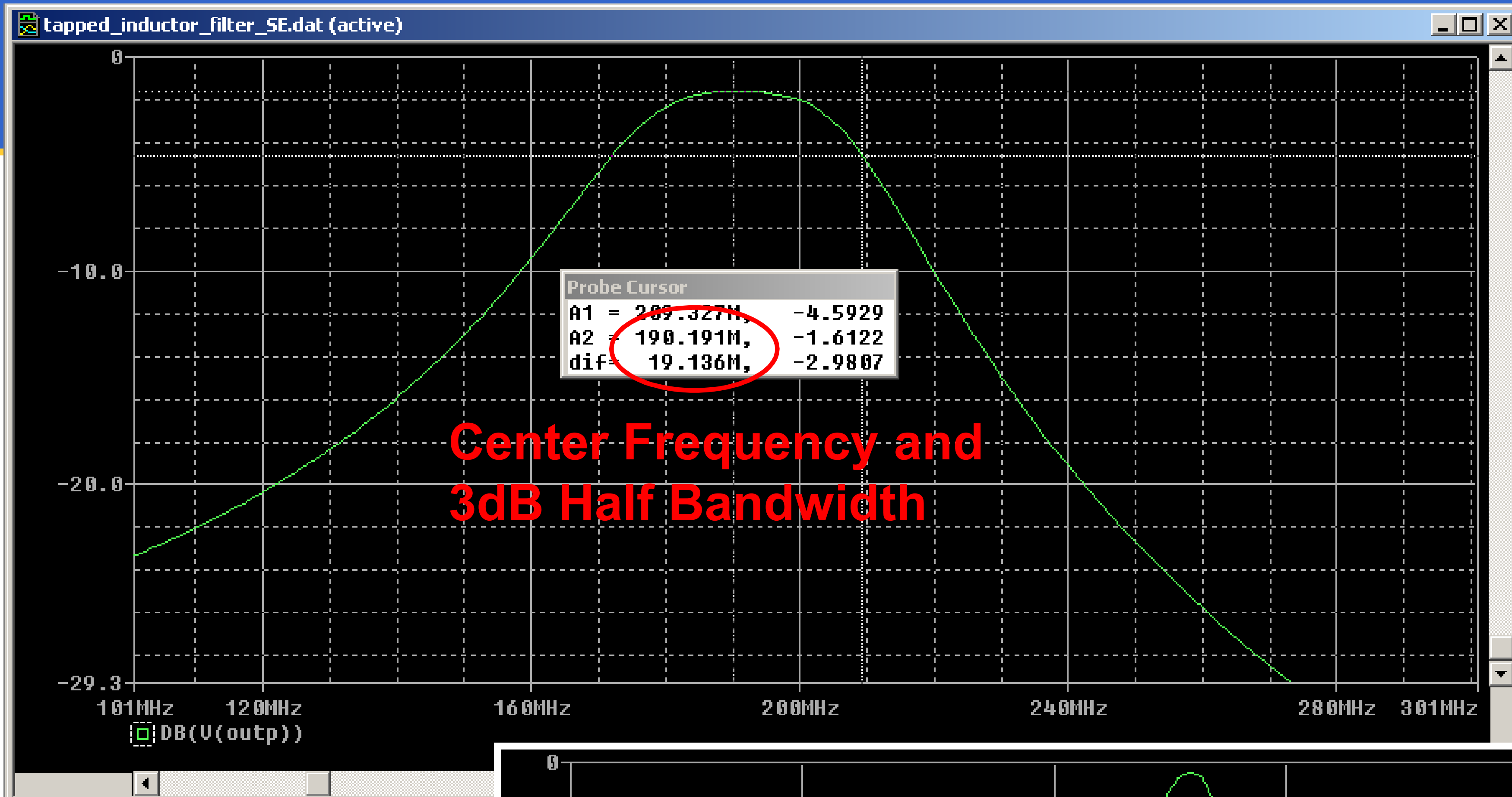


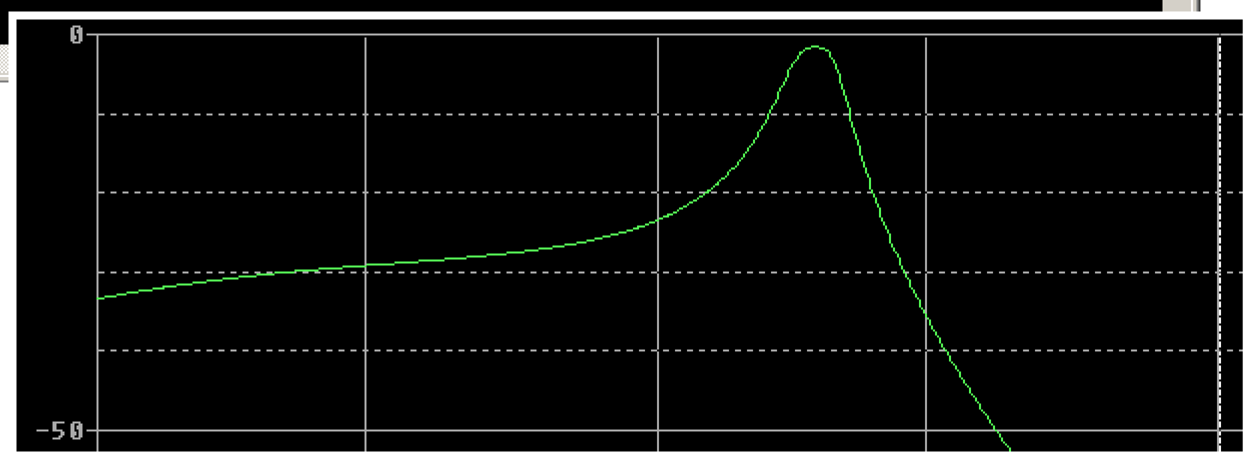
Example

- F_0=190MHz, 30MHz -1dB Bandpass Filter
- R_S=50, R_L=150



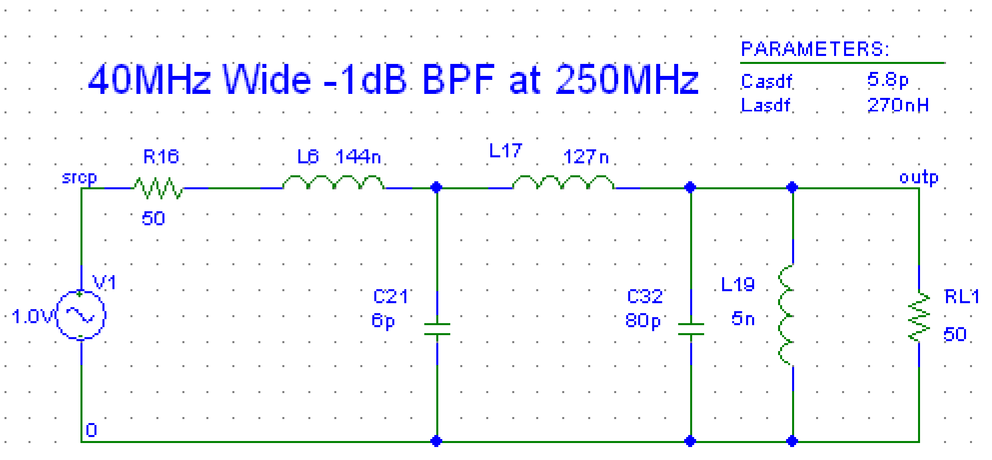
	A	B	C	D	E
1					
2	Filter Characteristics				
3	Wo	BW	Q		
4	1.90E+08	3.00E+07	6.333333333		
5					
6	Source/Load				
7	RS	RL			
8	50	150			
9					
10	Tuned Tank				
11	QT	L3	C3		
12	6	2.09E-08	3.35E-11		
13					
14	Upward Impedance Xform				
15	Q2	Rin'	L2'	L2	C12
16	3	1500	4.18774E-07	3.77E-07	1.68E-12
17					
18	Downward Impedance Xform				
19	Q1	Rin	C11'	L1	C11
20	7	30	3.83039E-12	1.83E-07	3.91E-12


tapped_inductor_filter_SE.dat (active)
0
-10.0
-20.0
-29.3
101MHz
120MHz
160MHz
200MHz
240MHz
280MHz
301MHz
DB(V(outp))
Probe Cursor
A1 = 209.327M, -4.5929
A2 = 190.191M, -1.6122
dif= 19.136M, -2.9807
Center Frequency and
3dB Half Bandwidth


0
-50

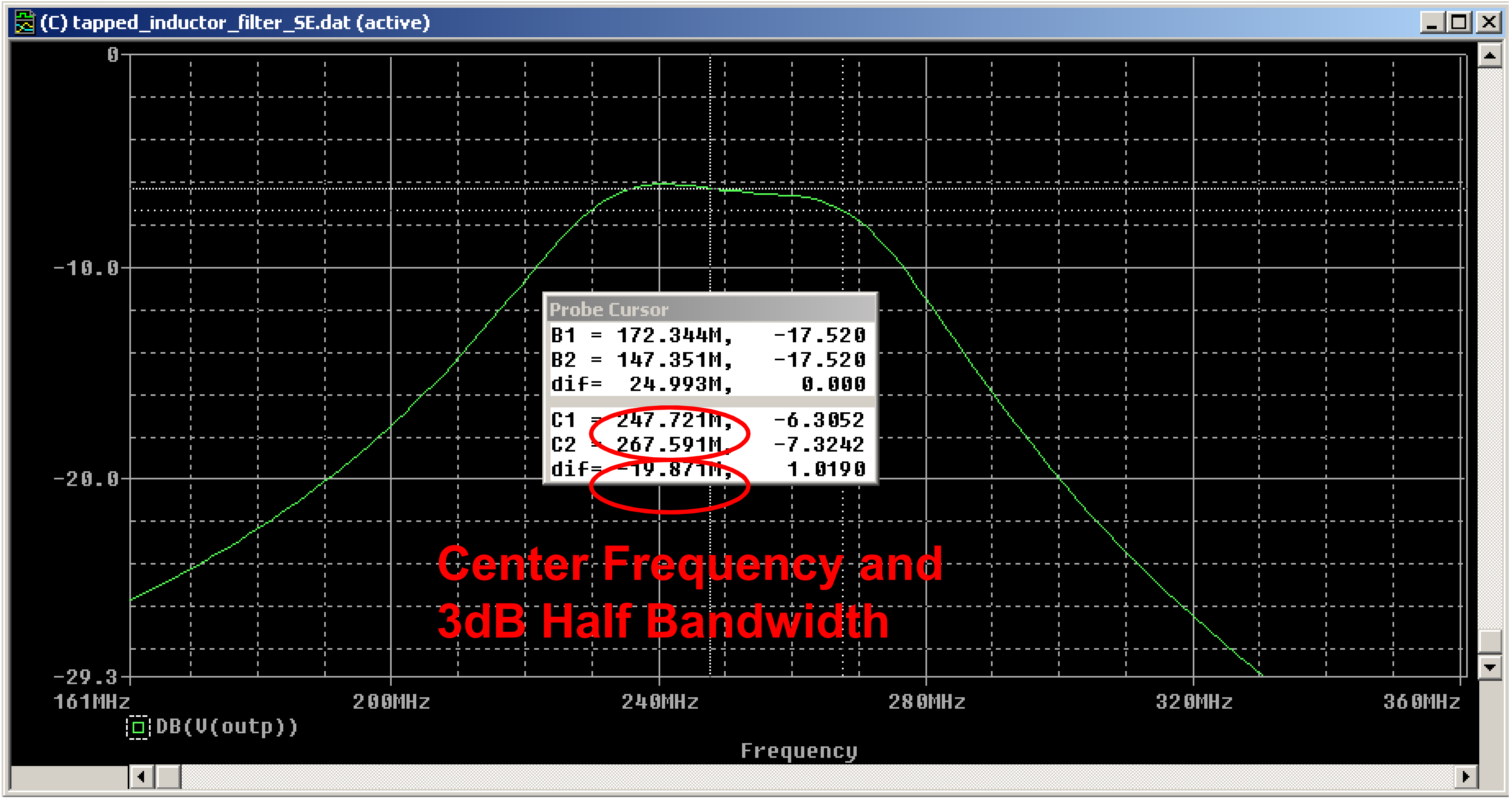
Example

- F_0=250MHz, 40MHz -1dB Bandpass Filter
- R_S=50, R_L=50



	A	B	C	D	E
1					
2	Filter Characteristics				
3	Wo	BW	Q		
4	2.50E+08	4.00E+07	6.25		
5					
6	Source/Load				
7	RS	RL			
8	50	50			
9					
10	Tuned Tank				
11	QT	L3	C3		
12	6.25	5.09E-09	7.96E-11		
13					
14	Upward Impedance Xform				
15	QU	Rin'	L2'	L2	C12
16	4	850	1.35264E-07	1.27E-07	3.00E-12
17					
18	Downward Impedance Xform				
19	QD	Rin	C11'	L1	C11
20	4	50	2.81927E-12	1.44E-07	3.00E-12

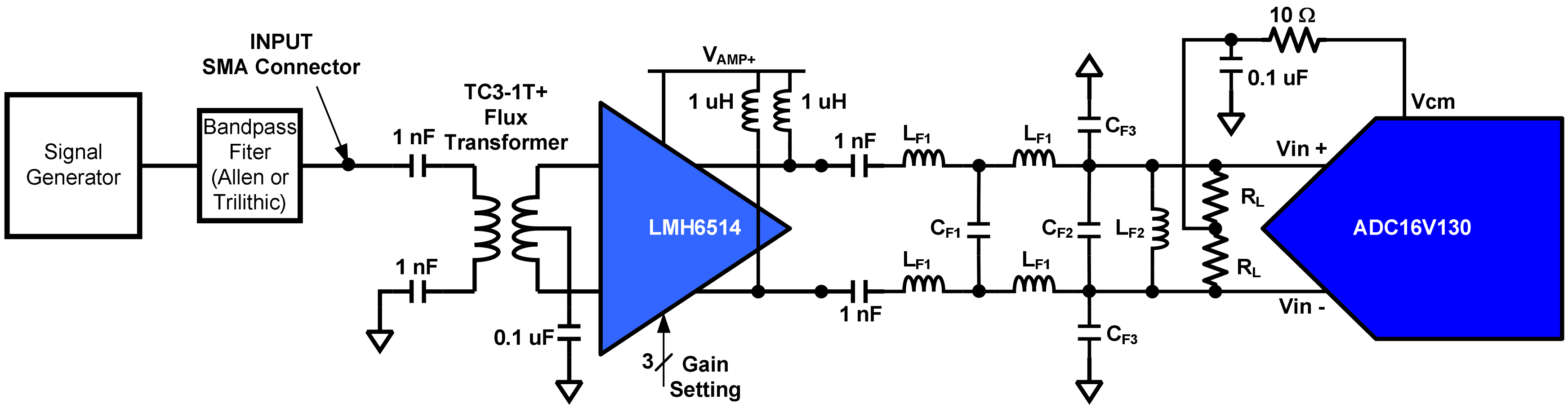
Example



POWERWISE

National Semiconductor

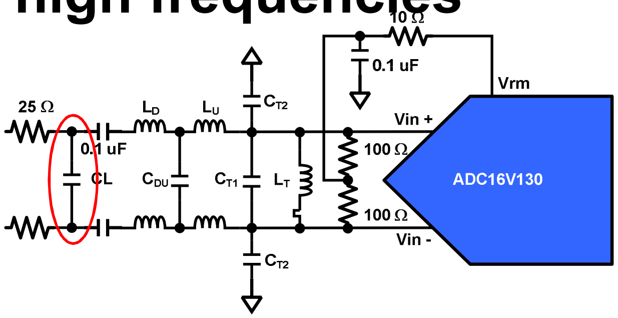
Architecture Example

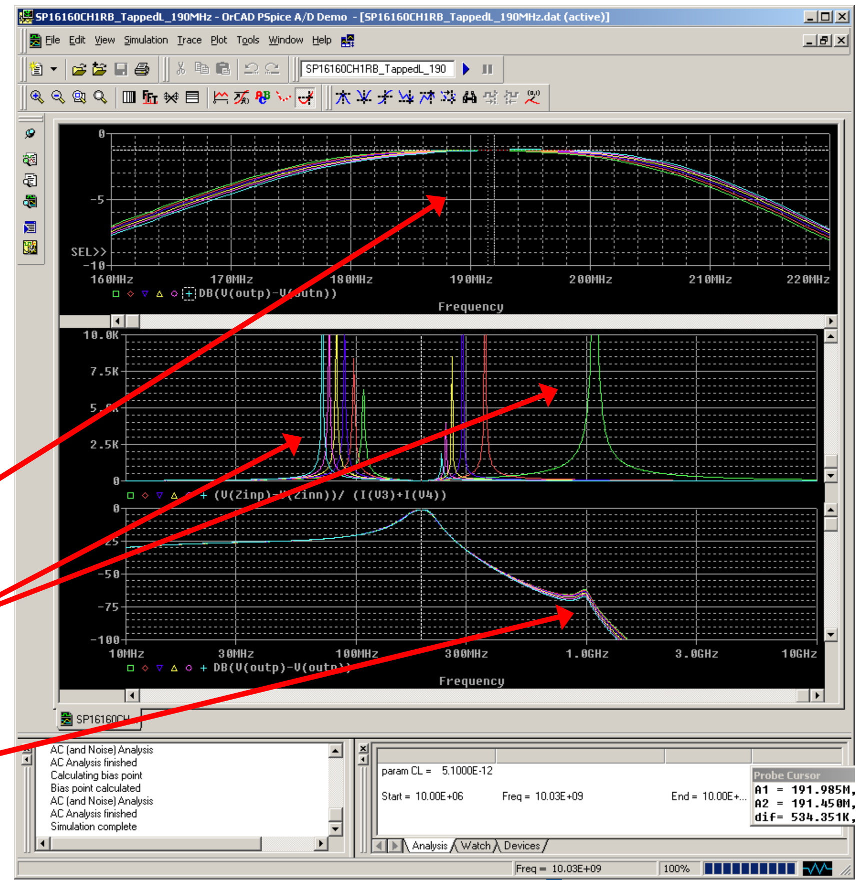


- Differential implementation
- Additional large series caps for AC coupling
- ADC sets input common mode through load resistors
- Tank caps separated into common mode and differential loads for better charge kickback suppression from ADC

Practical Issues

- **Input impedance matching good in bandwidth, but has peaking at certain frequencies**
- **Insert a small cap (CL) after the series output R's of DVGA to reduce impedance resonance at high frequencies**





Solid filter profile

Impedance resonances (swept CL, green: CL=0.1pF)

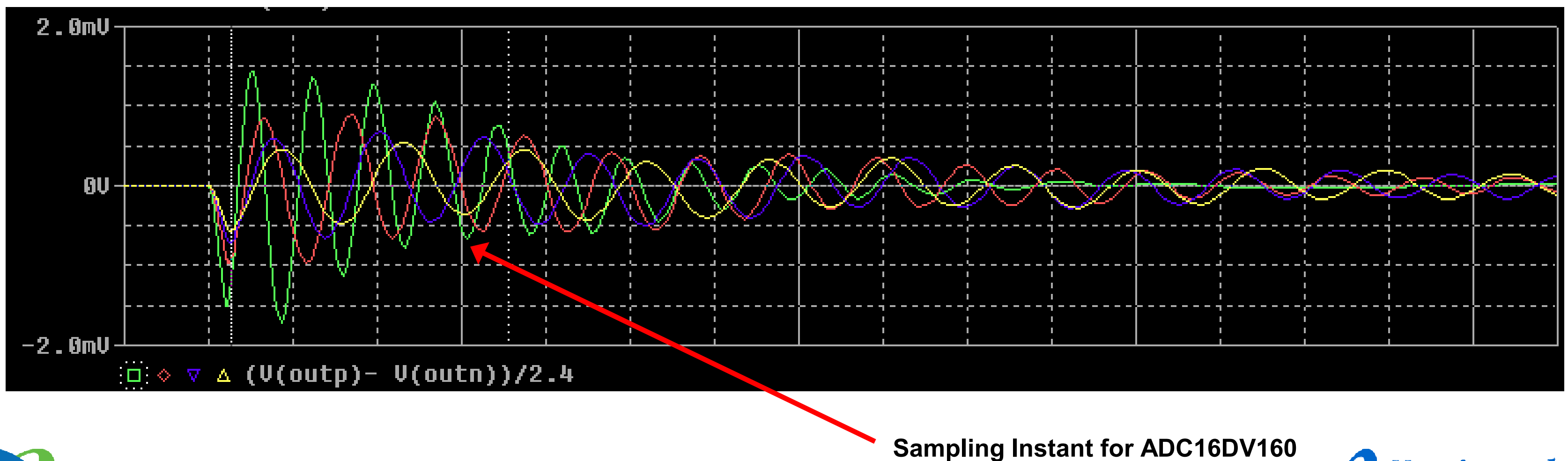
Peaking due to bond wire inductance

POWERWISE

National Semiconductor

Practical Issues

- **Charge kickback from ADC resonates with bond wire inductance and LC tank (observed in simple model simulation)**
  - **Lower tank Q decays faster but bigger initial spike**
  - **Higher tank Q decays slower but smaller initial spike**
- **Differential and CM error depends on whether sampling instant lands on maximum or minimum of kickback ringing**
  - **Can create seemingly illogical SFDR variations across signal frequency, amplitude, sampling rate, common-mode capacitance, etc.**



References

- T.H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits," Cambridge University Press, 2004, pp. 92-99. (Impedance matching)

National
Semiconductor