ADS8860 Key Specs

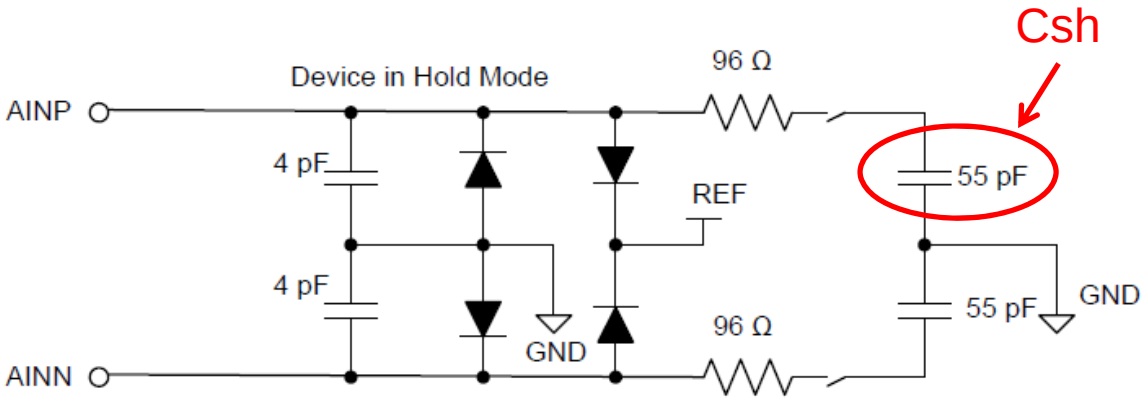


Figure 45. Input Sampling Stage Equivalent Circuit

AINN is at or near GND so almost all sampled charge will be on AINP S/H capacitor. For REF Pin model can treat this as a single-ended input ADC.

16Bit ADC with FSR= 4.5V

$$1LSB = \frac{4.5V}{2^{16}} = 68.66uV$$

1MSPS:

tacq = 290ns min

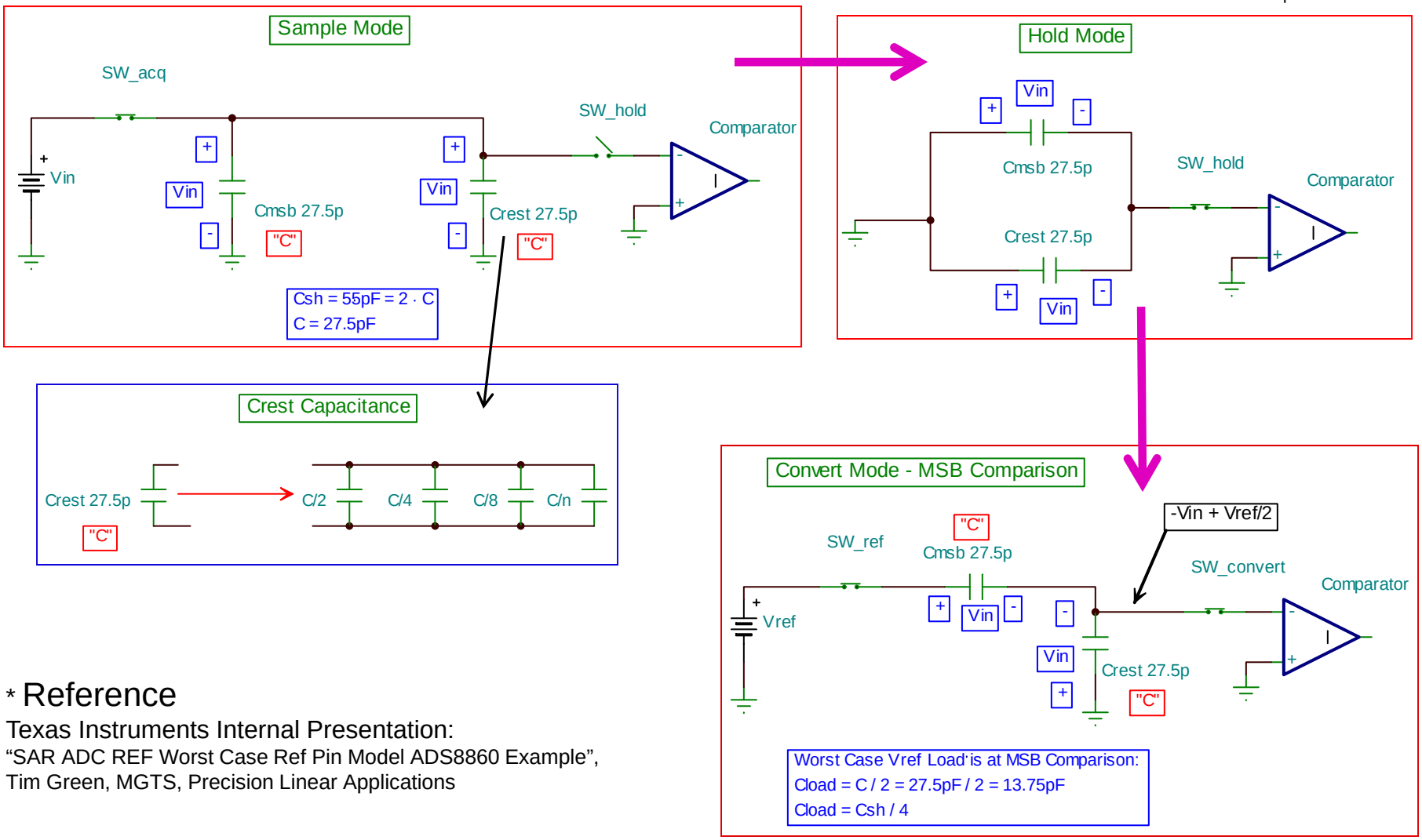
tconv = 710ns max

*** Reference:**
Texas Instruments Internal Presentation,
"SAR ADC REF Worst Case Ref Pin Model ADS8860 Example",
Tim Green, MGTS, Precision Linear Applications

EXTERNAL REFERENCE INPUT					
V_{REF}	Input range		2.5	5	V
	Reference input current	During conversion, 1-MHz sample rate, mid-code		300	µA
	Reference leakage current			250	nA
C_{REF}	Decoupling capacitor at the REF input		10	22	µF

Simple ADC Architecture and Vref Loading – based on

SAR ADC Operation



* Reference

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