https://cloudcycle.atlassian.net/wiki/spaces/TM/pages/edit-v2/722239494

ADC ESD Calculations

RTD Differential filter set to 226Hz. Should be around 10x greater than sampling rate.

With 6.2k resistors this gives a cap value of 56nf

Select common mode cap to be 10x smaller - 5.6nf

Select reference cut off to be approximatley equal to the differential frequency cut off

Sinc3 filter gives better noise performance than the low latency filter but has a 3 cycle latency at the data output.

PT1000 RTD

Temperatures -20 to 80 Degrees C

921.6 to 1309 ohms

with 500uA and a gain of 2 the range is:

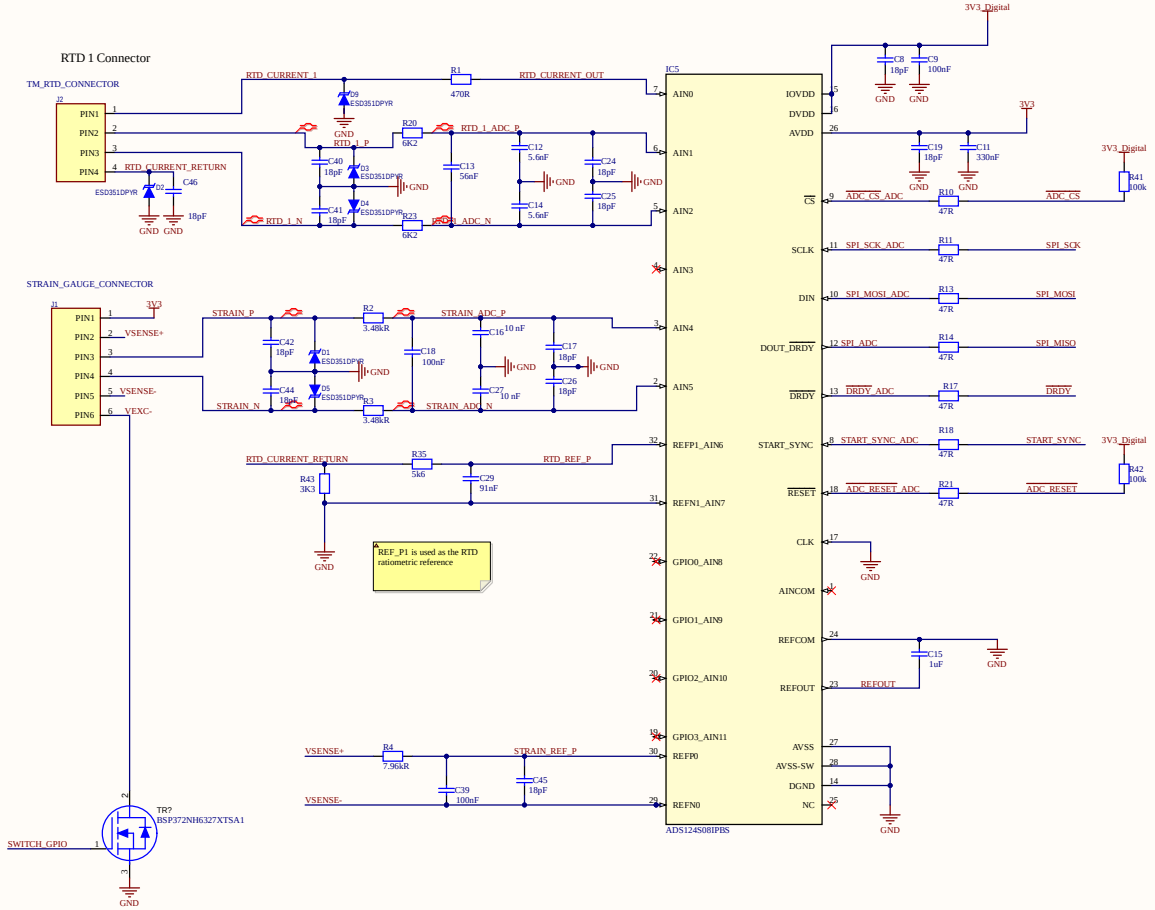
0.92 to 1.3V

Rref = 3300 ohms

= max voltage of 1.65V

Within PGA Range and IDAC Compliance range

## RTD 1 Connector




SPI Clock polarity and Phase:

CLOCK_POL = 0
CLOCK_PHASE = 1

Analog Settling time:

33nf x 4.99K = 0.00016s

17.3 time constants to settle for 24 bit resolution:

#NAME?

REF_P1 is used as the RTD ratiometric reference

Using internal oscillator so tieing CLK to gnd

VEXC- and REFN0 wil be internally connected to GND through an internal low side switch. As VEXC- and REFN0 are in the same path and the measurement is ratiometric the resistances of the switch will not affect the measurement.

REF_P0 is used as the strain gauge ratiometric reference

Recommended reference resistor is <10 PPM.

Currently set to 0.01% so at 30 degrees we will have an error of 0.003 degrees. Cost is high.

Cheaper resistor that is 0.05%, at 30 degrees will have an error of 0.015 degrees.

Class A RTD will have a tolerance of +/- 0.21 degrees at 30 degrees.

Self heating error = (0.0005^2 * 1116) / 0.0025 = 0.11 degrees error

= 0.015 + 0.21 + 0.11 = 0.335 degrees error at 30 degrees

### Other Considerations

When selecting the corner frequency of the RC filters, make sure to account for both the noise signals present in the environment, and the timing constraints of the application. In many cases, the signal produced by the RTD may be treated as essentially a dc signal. The analog filter must be allowed to completely settle after activating the current source, but before the sensor measurement takes place. On high-resolution applications, when initially biasing the RTD, the user may have to wait several time constants for the filter to settle. For example, when performing a 20-bit resolution measurement, after initially biasing the sensor, the user must wait up to 14 RC filter time constants for the measurement to settle within ½ an LSB. Table 1 shows the required RC filter time constants to settle to ½ LSB resolution.

**Table 1. Required RC Filter Time Constants to Settle to ½ LSB Resolution**

| Resolution (Bits) | Time Constants to ½ LSB |
|---|---|
| 16 | 11.78 |
| 18 | 13.17 |
| 20 | 14.56 |
| 22 | 15.94 |
| 24 | 17.33 |

#### 9.3.6.1.2 Data Conversion Time for the Low-Latency Filter

The amount of time required to receive data from the ADC depends on more than just the nominal data rate of the device. The data period also depends on the mode of operation and other configurations of the device. When the low-latency filter is enabled, the data settles in one data period. However, a small amount of latency exists to set up the device, calculate the conversion data from the modulator samples, and other overhead that adds time to the conversion. For this reason, the first conversion data takes longer than subsequent data conversions.

Table 13 shows the conversion times for the low-latency filter for each ADC data rate and various conversion modes.

**Table 13. Data Conversion Time for the Low-Latency Filter**

| NOMINAL DATA RATE(1) (SPS) | FIRST DATA FOR CONTINUOUS CONVERSION MODE OR SINGLE-SHOT CONVERSION MODE(2) | | SECOND AND SUBSEQUENT CONVERSIONS FOR CONTINUOUS CONVERSION MODE | |
|---|---|---|---|---|
| | $t_{RM}$(3) | NUMBER OF $t_{MOD}$ PERIODS(3) | $t_{RM}$(4) | NUMBER OF $t_{MOD}$ PERIODS(4) |
| 2.5 | 406.504 | 104065 | 400 | 102400 |
| 5 | 206.504 | 52865 | 200 | 51200 |
| 10 | 106.504 | 27265 | 100 | 25600 |
| 16.6 | 60.254 | 15425 | 60 | 15360 |
| 20 | 56.504 | 14465 | 50 | 12800 |
| 50 | 20.156 | 5160 | 20 | 5120 |
| 60 | 16.910 | 4329 | 16.66 | 4264 |
| 100 | 10.156 | 2600 | 10 | 2560 |
| 200 | 5.156 | 1320 | 5 | 1280 |
| 400 | 2.656 | 680 | 2.5 | 640 |
| 800 | 1.406 | 360 | 1.25 | 320 |
| 1000 | 1.156 | 296 | 1 | 256 |
| 2000 | 0.656 | 168 | 0.5 | 128 |
| 4000 | 0.406 | 104 | 0.25 | 64 |

(1) Valid for the internal oscillator or an external 4.096-MHz clock. Scales proportional with $f_{CLK}$.
(2) Conversions start at the rising edge of the START/SYNC pin or on the seventh SCLK falling edge for a START command.
(3) Time does not include the programmable delay set by the DELAY[2:0] bits in the gain setting register. The default setting is an additional 14 $t_{MOD}$, where $t_{MOD} = t_{CLK} \times 16$.
(4) Subsequent readings in continuous conversion mode do not have the programmable delay time.

Mech parts

FID1 FID2 FID3

LOGO1
LOGO

SN1
SERIAL_NO

| | | |
|---|---|---|
| CLOUDCYCLE | | TITLE: Drum Temperature Module DVT |
| DRAWN: J. Craig | CKD: Schematic Checked By | PRINT DATE: 15/01/2024 |
| | | Sheet: ADC.SchDoc |
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