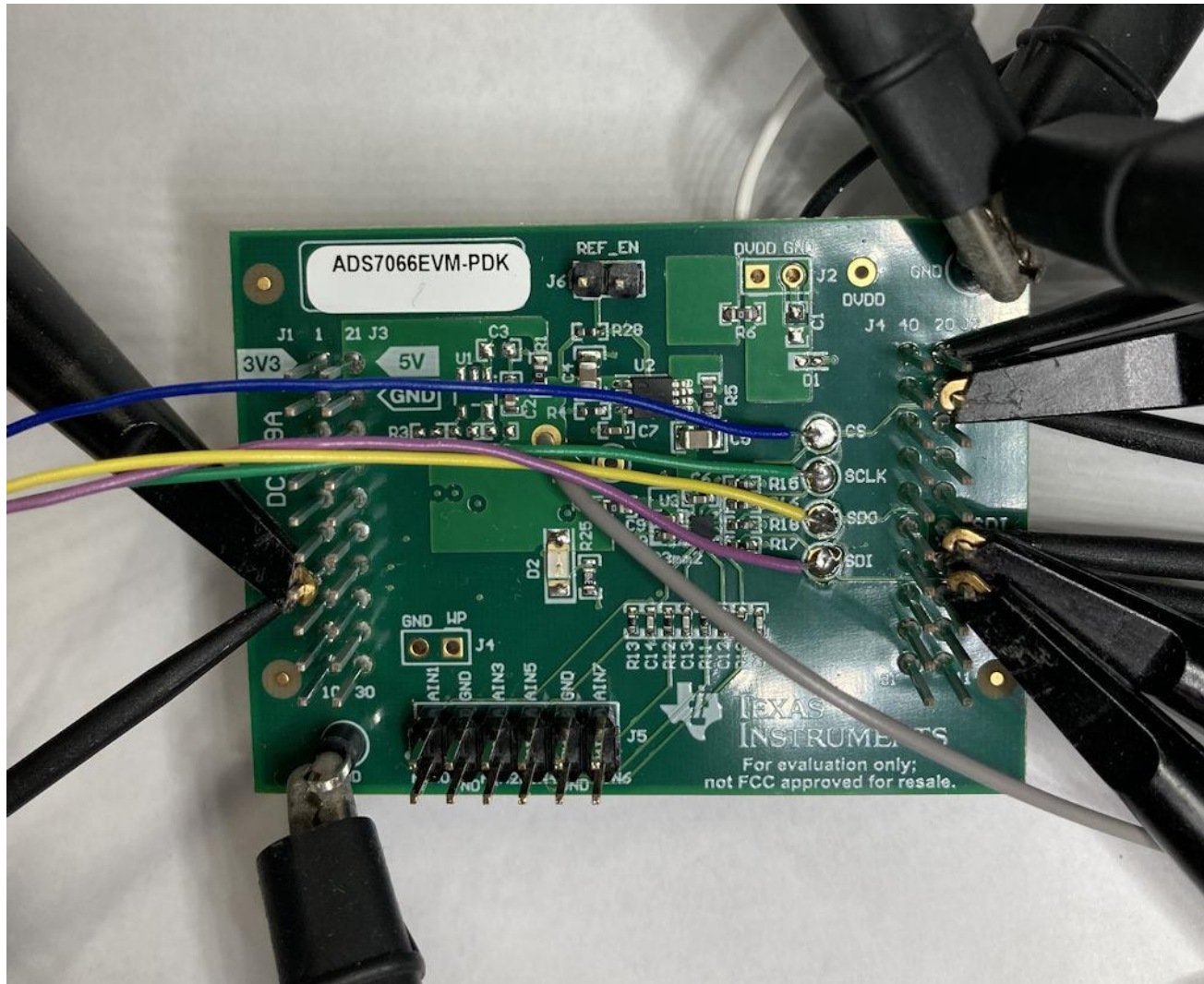
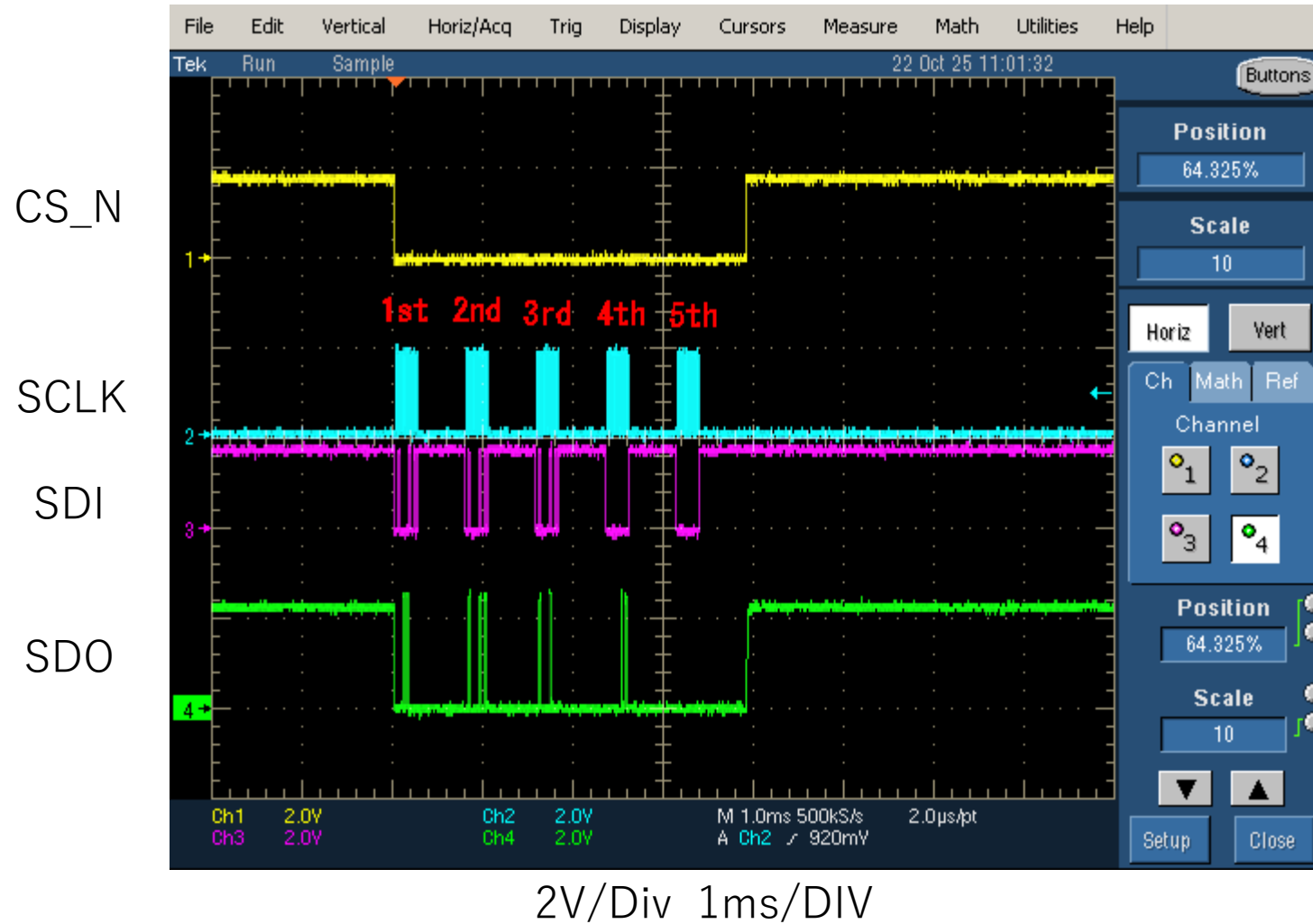


measurement environment



Using the official evaluation board.
The ADC is driven by an external
FPGA.

Oscilloscope observation of SDI and SDO of a **single** ADC



Repeatedly wrote the following 24-bit frames:

1st frame: 08018C (hex)

2nd frame: 08018C

3rd frame: 08018C

4th frame: 000000

5th frame: 000000

Here,

08018C indicates

GENERAL_CFG

(Internal ref ON, $2 \times V_{ref}$)

000000 indicates

NOP

It was confirmed that writing 08018C enables the reference voltage output.

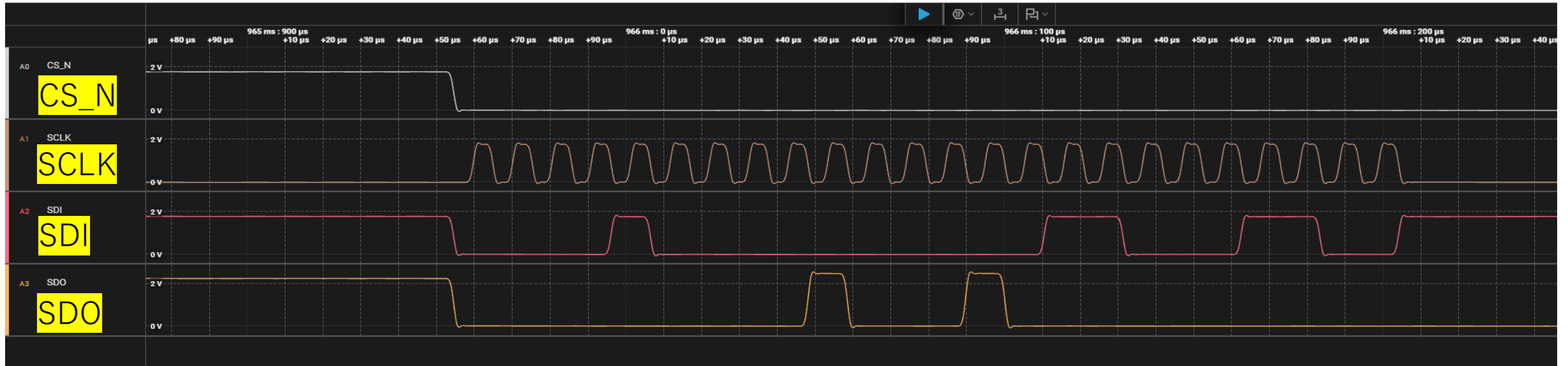
This shows the SDI and SDO signals of a single ADC.
The waveform represents five frames captured using an analog logic analyzer.



The SCLK frequency is 100 kHz, and the sampling is 2.5 MS/s.

It works fine up until the second frame, so in a daisy chain configuration, the second ADC works fine, but the third ADC doesn't.

This is the waveform of the 1st frame captured with an analog logic analyzer.



The SCLK frequency is 100 kHz, and the sampling frequency is 2.5 MHz.

SDI is supposed to be latched on the rising edge of SCLK.

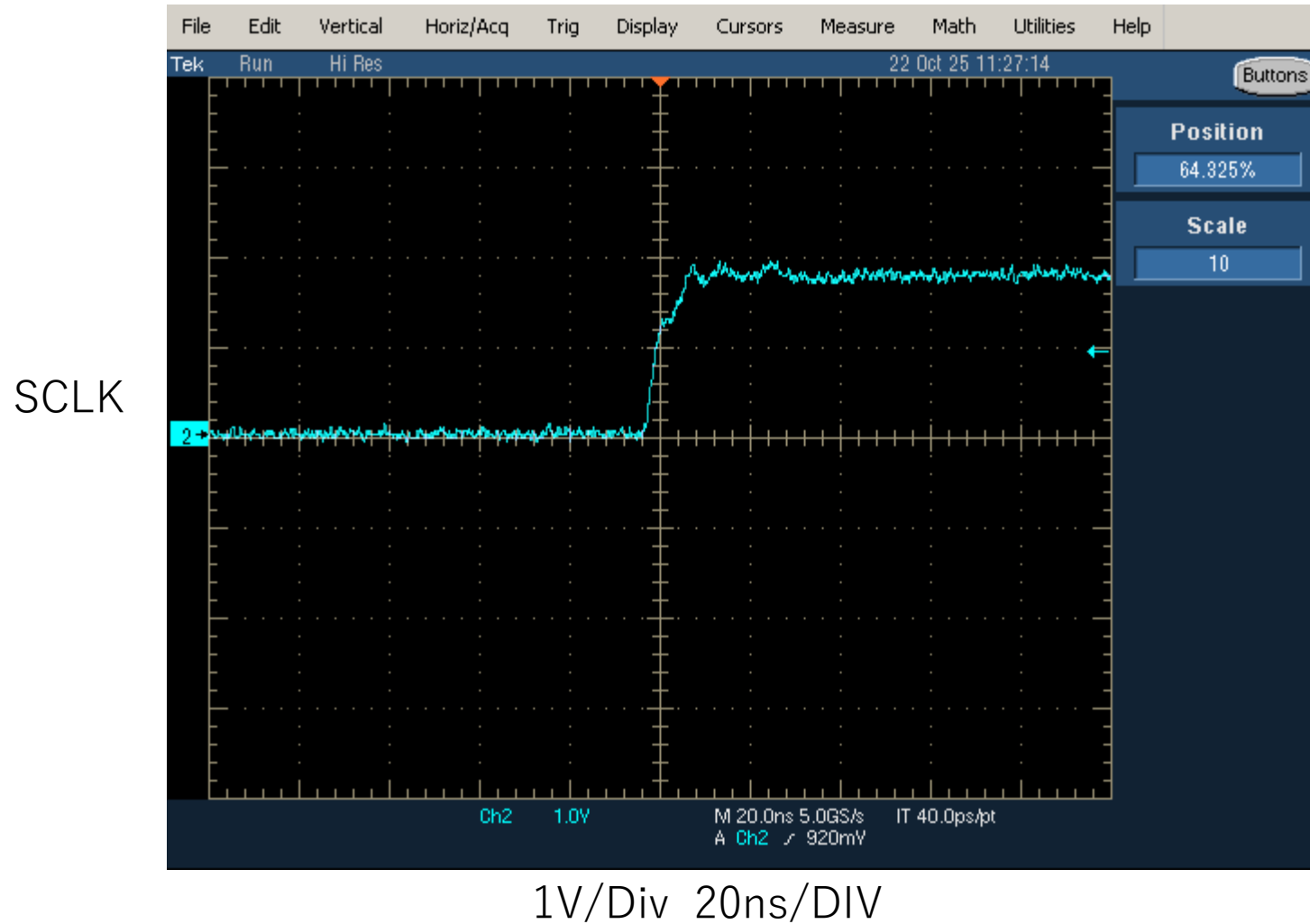
Since SDI does not change around the rising edge of SCLK, sufficient setup and hold times are ensured.

Power-up waveform of the ADC



1V/Div 1ms/DIV

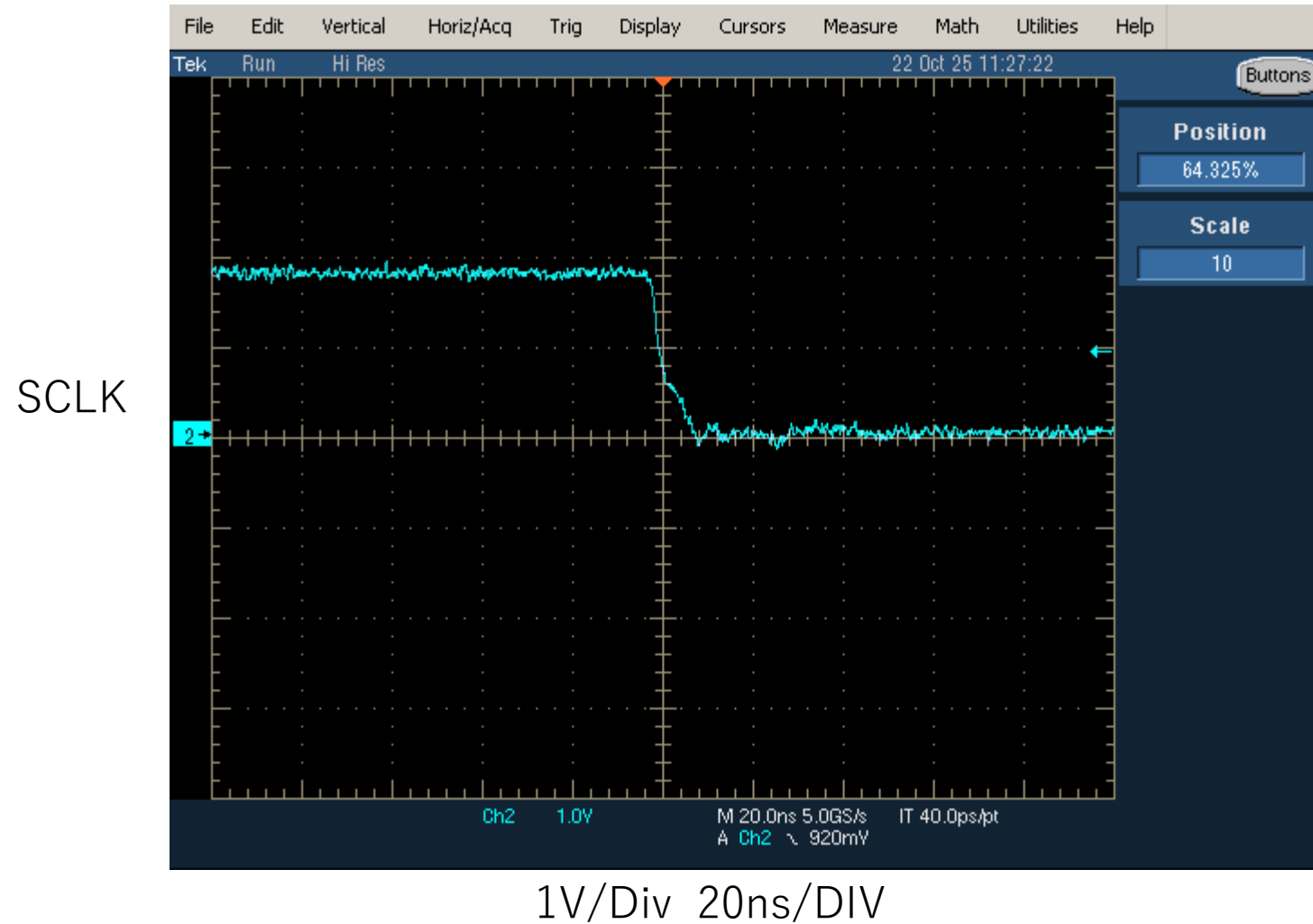
This is the rising-edge waveform of SCLK.



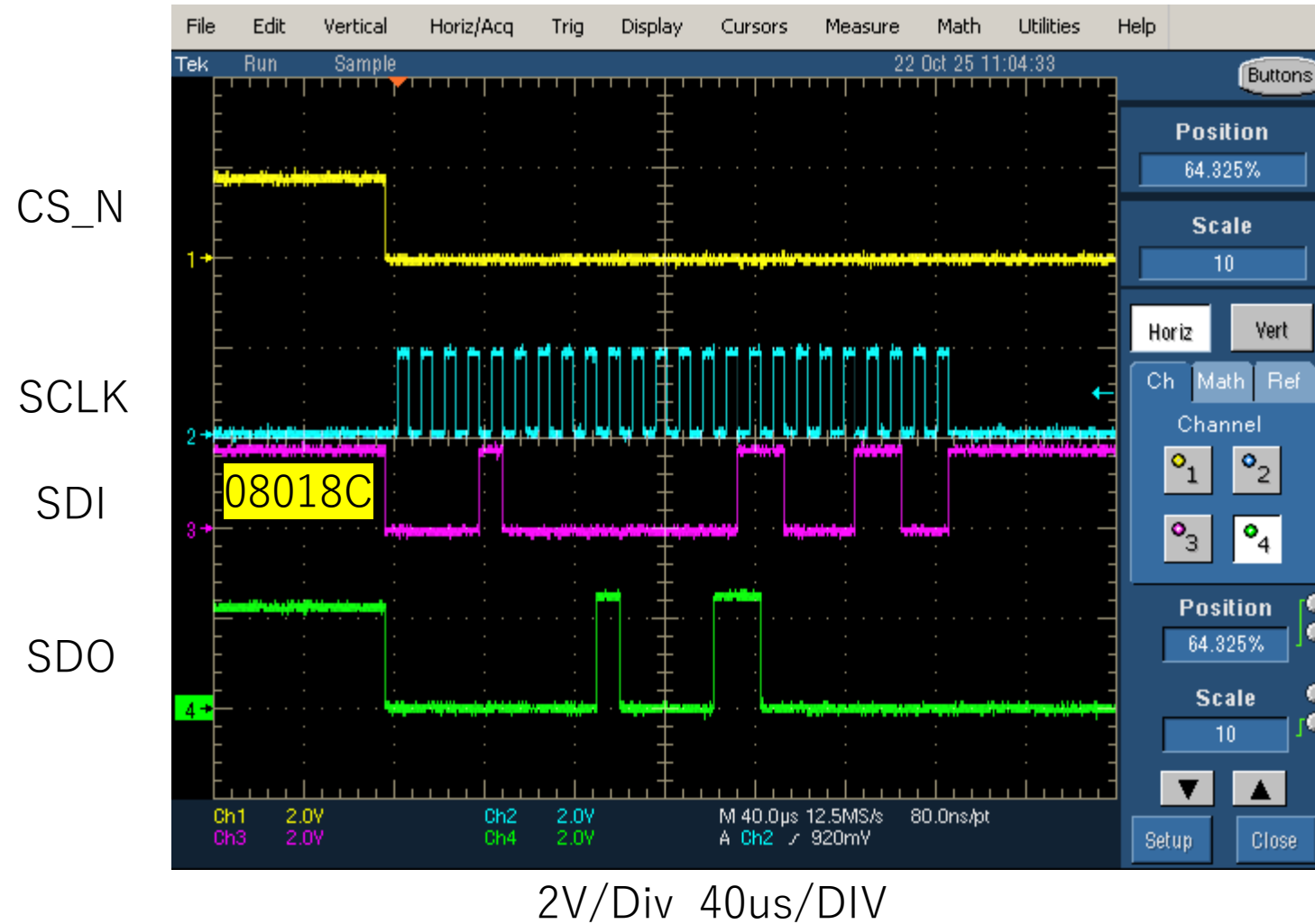
The in-house developed board and the official evaluation board use different signal input paths, but the same issue occurs on both.

Even when varying the SCLK slew rate and the damping resistor, data corruption occurs on the SDO of the 3rd frame.

This is the falling-edge waveform of SCLK.



This is an enlarged view of the 1st frame.



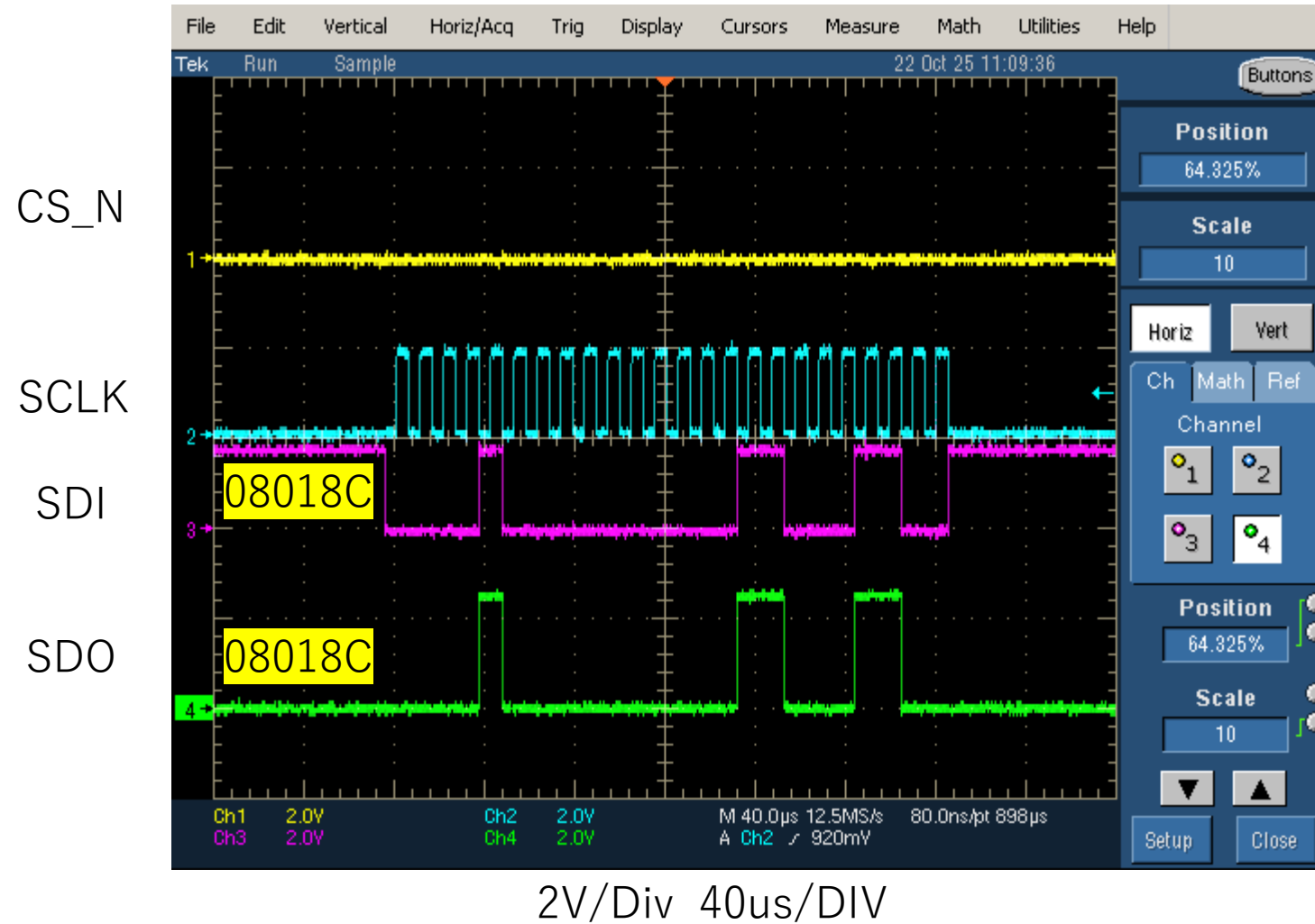
08018C is applied to the SDI input during the 1st frame.

Garbage data ? appears on the SDO.

The SCLK frequency is 100 kHz.

SDI is supposed to be latched on the rising edge of SCLK.
Since SDI does not change around the rising edge of SCLK, sufficient setup and hold times are ensured.

This is an enlarged view of the 2nd frame.

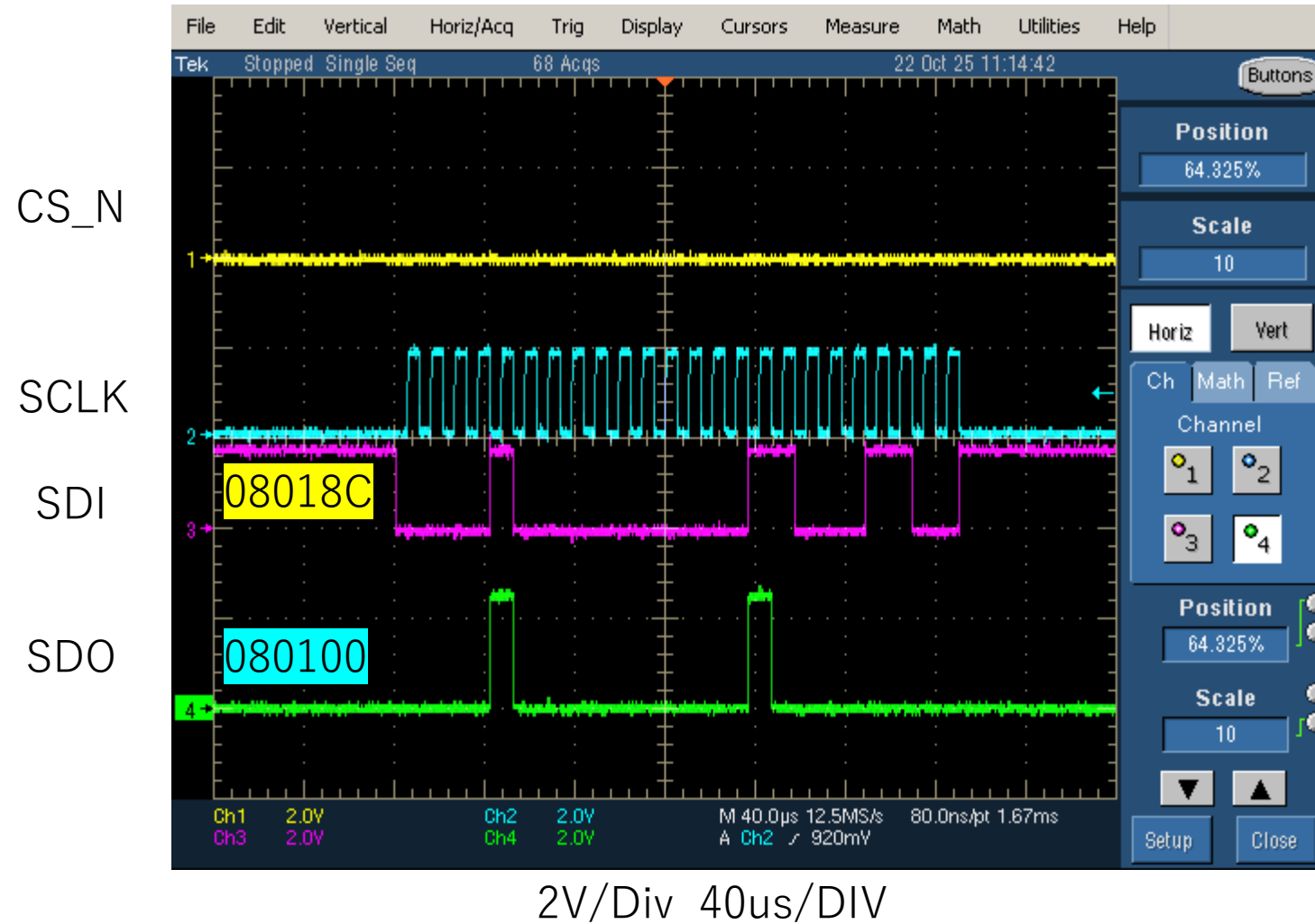


08018C is applied to the SDI input during the 2nd frame.

08018C is output from the SDO. It is the data written in the 1st frame.

This behavior is correct.

This is an enlarged view of the 3rd frame.



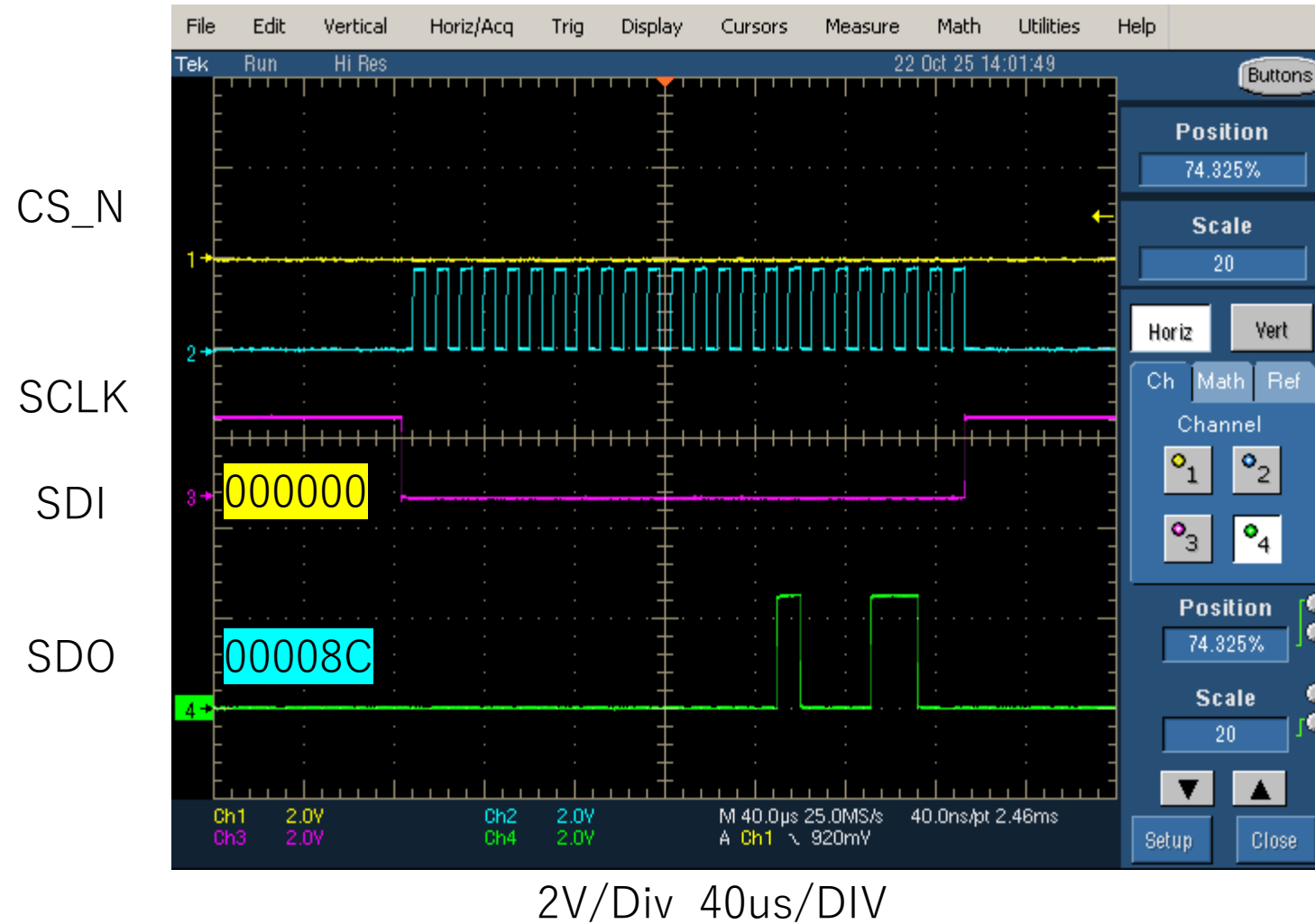
08018C is applied to the SDI input during the 3rd frame.

080100 is output from the SDO.
This behavior is incorrect.

When daisy-chained, the SDO of the 2nd frame is correct, but the SDO of the 3rd frame becomes corrupted. Therefore, the second ADC in the daisy chain operates correctly, whereas the third ADC operates incorrectly.

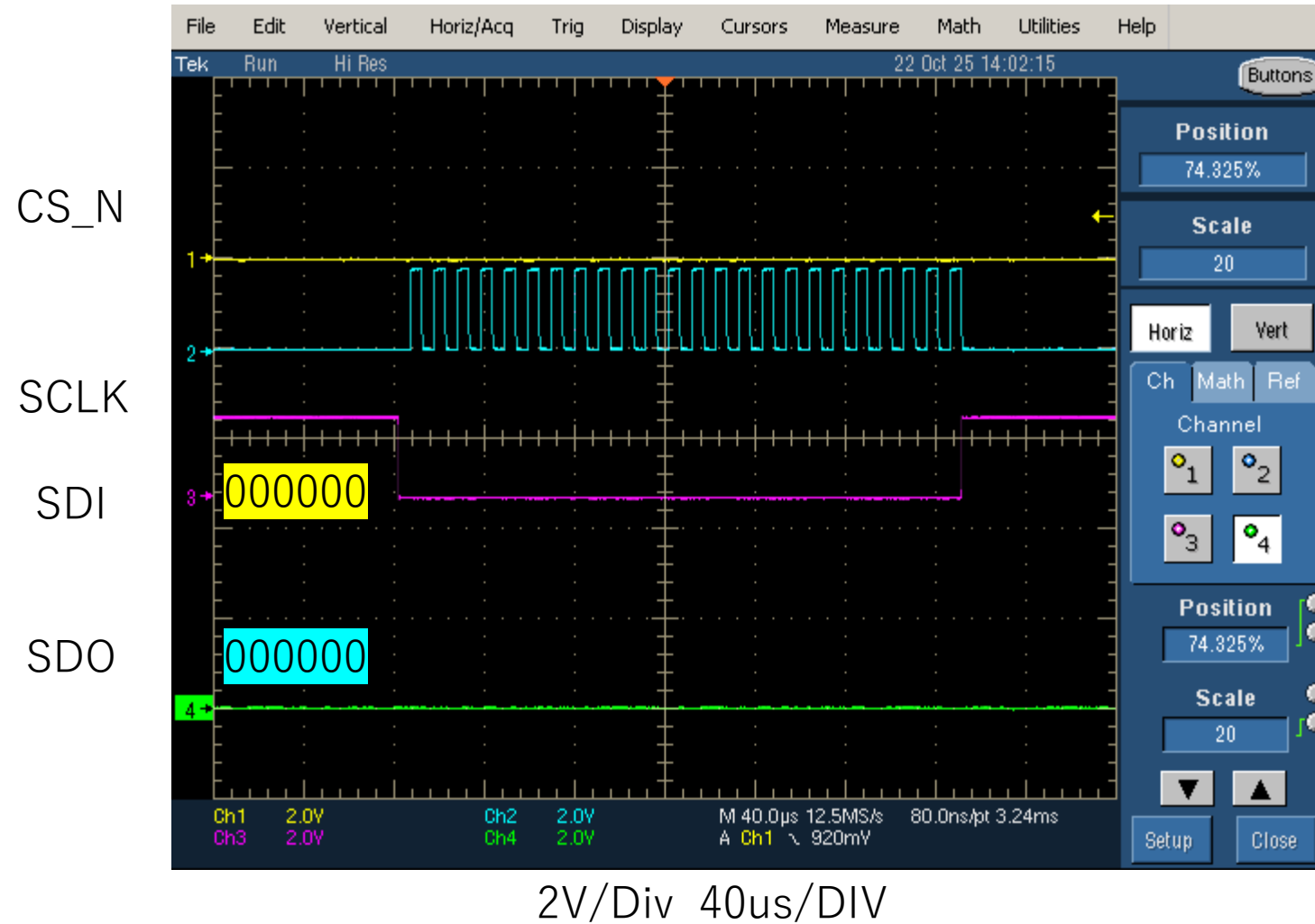
These are measurements from a single ADC, which leads to the conclusion that daisy chaining more than three ADCs is not possible.

This is an enlarged view of the 4th frame.

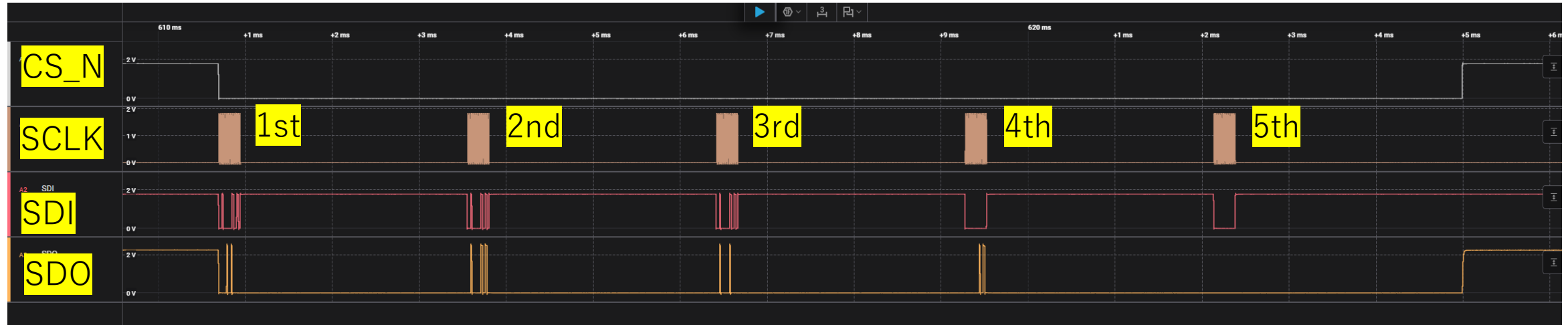


SDO should be 000000.

This is an enlarged view of the 5th frame.



This shows the SDI and SDO signals of a single ADC.
Increased the wait time between frames.



The result is unchanged.

Summary

- This is not a daisy-chain issue, as the SDO issue occurs even with a single ADC.
- Since the correct data appears in the second frame even when writing other command frame, it's unlikely to be a latching issue.
- The analog waveforms and power also appear to be normal.

Questions

- Is it acceptable to write 08018C after power-up? Is any specific configuration required before doing so?
- Is it correct to continuously send 08018C? However, if continuous write operations are not possible, the daisy chain cannot be used.
- Could the change in data in the third frame be caused by some internal operation within the ADC?
- Is it necessary to insert a fairly long wait after writing the 08018C data?
- Is there really no command to switch to daisy-chain mode?