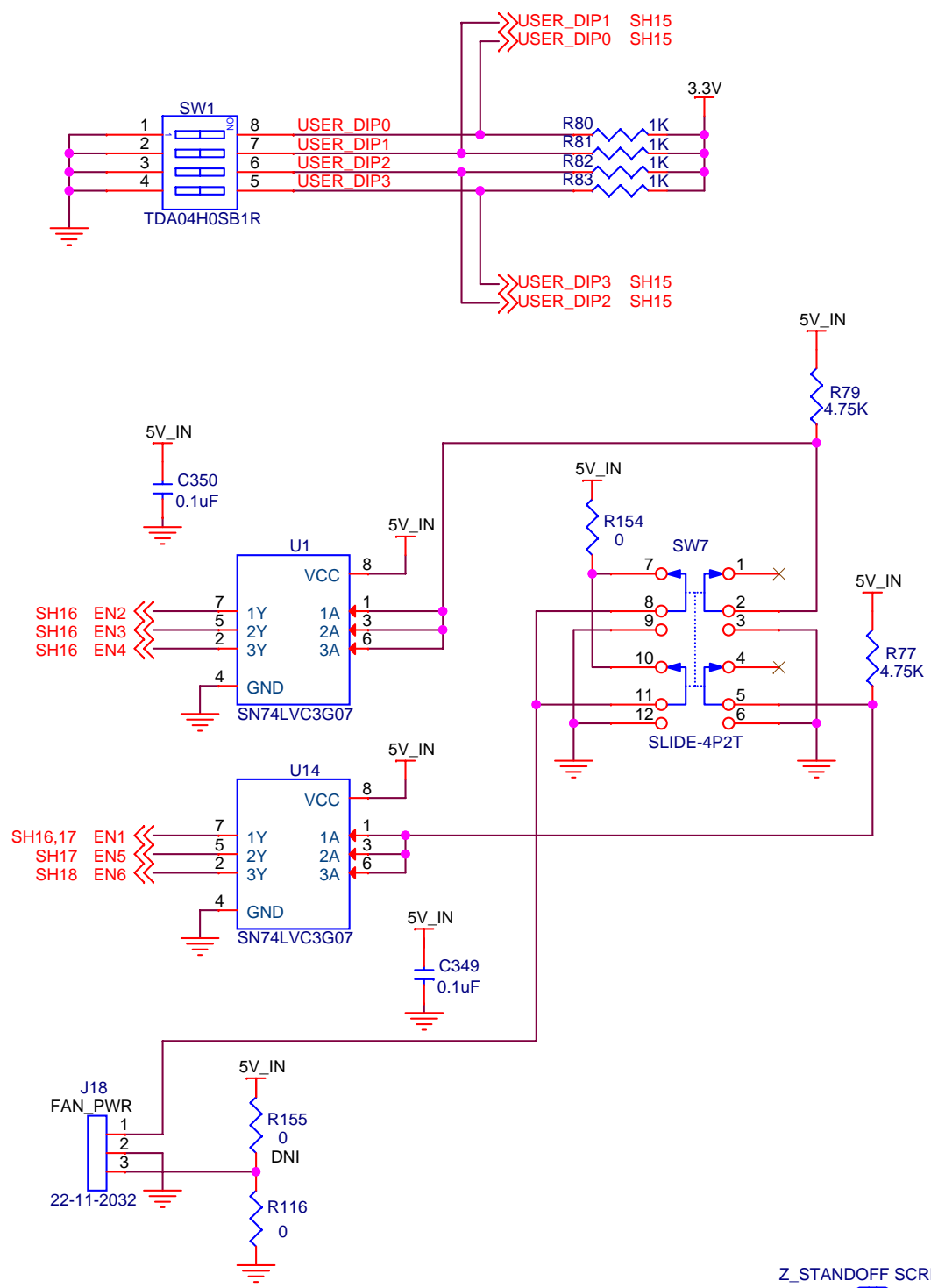
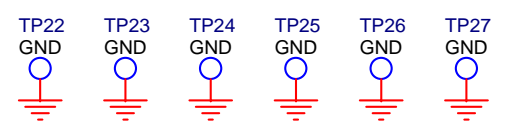
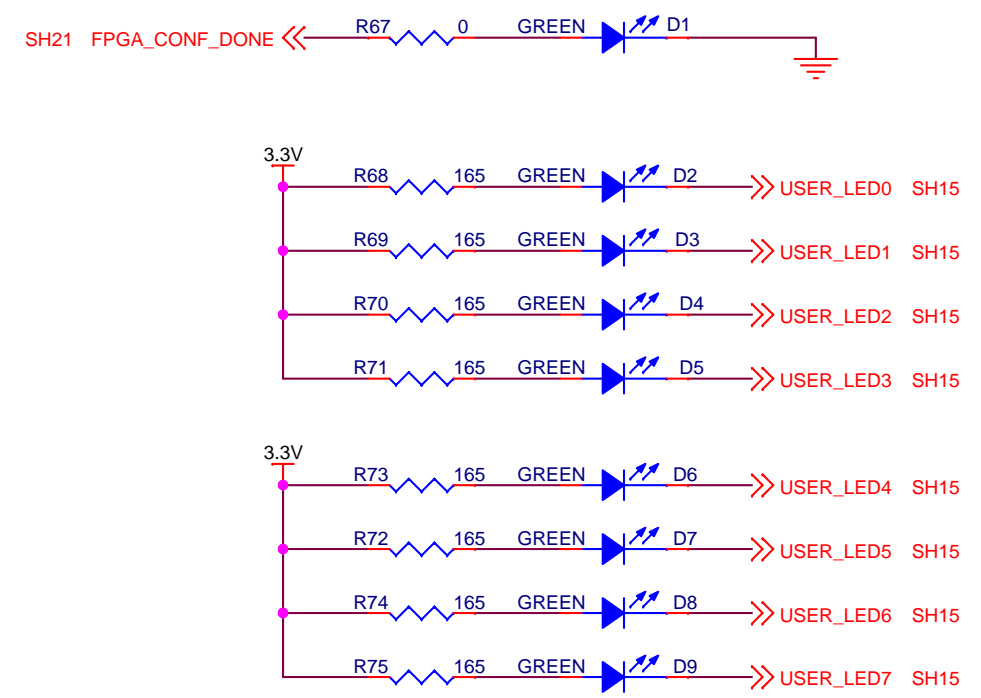


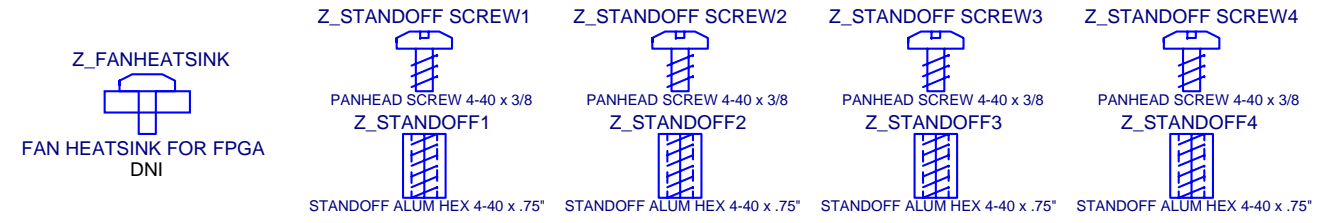
# Buttons & Switches



# LEDs



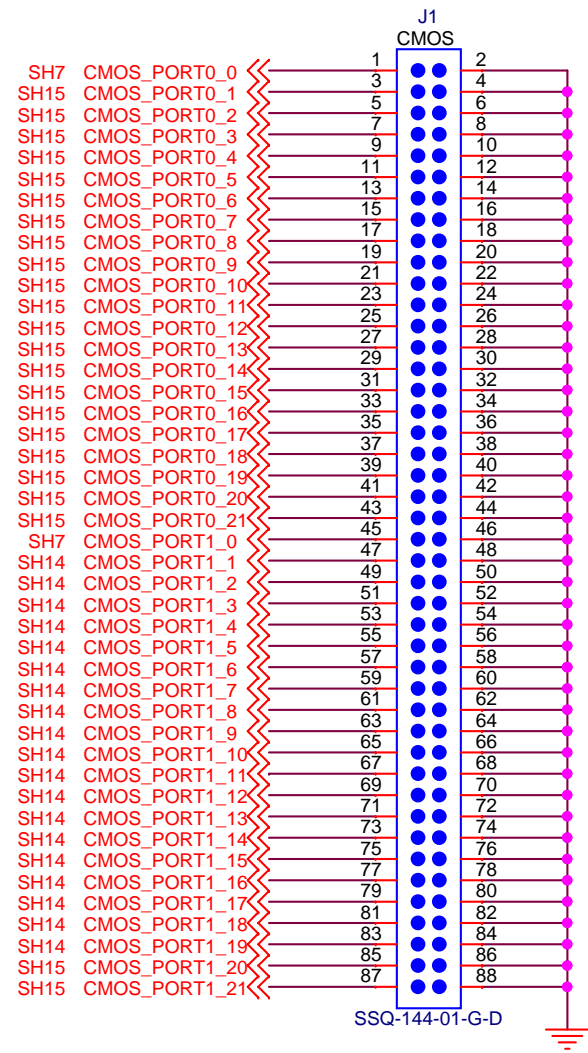
# MECHANICAL PARTS



Title		
<b>BUTTONS, SWITCHES, LEDS</b>		
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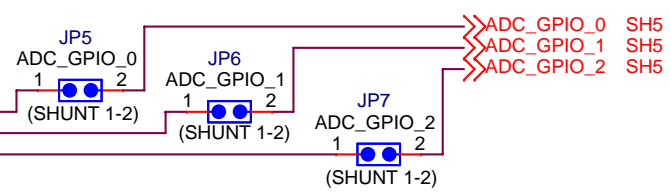
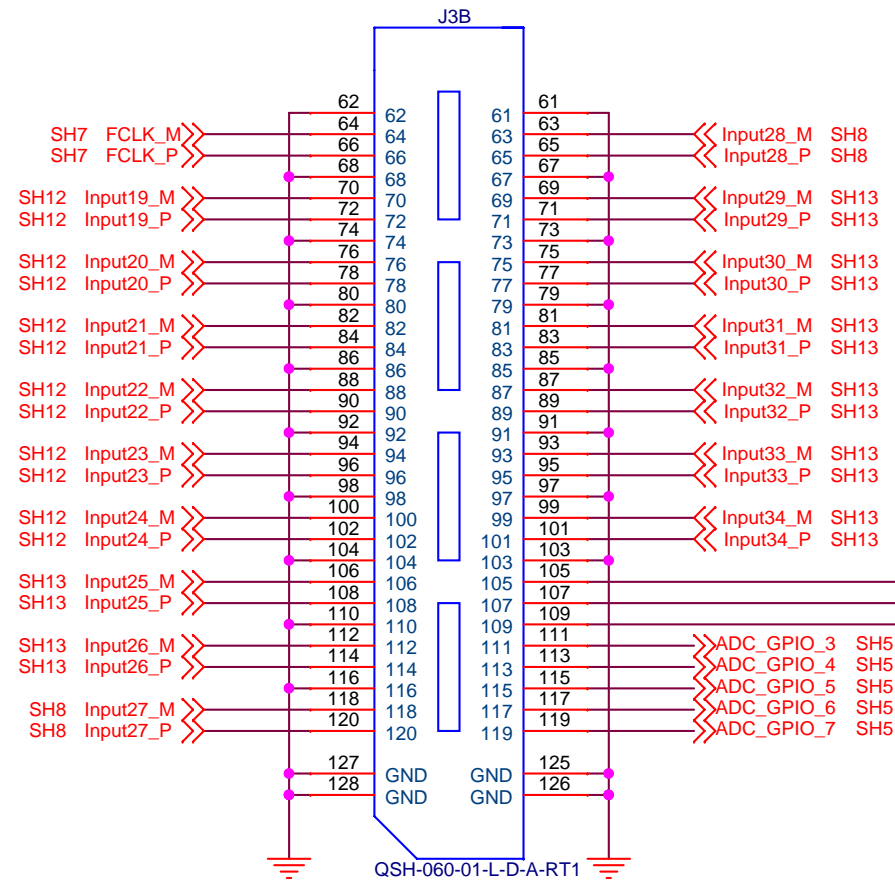
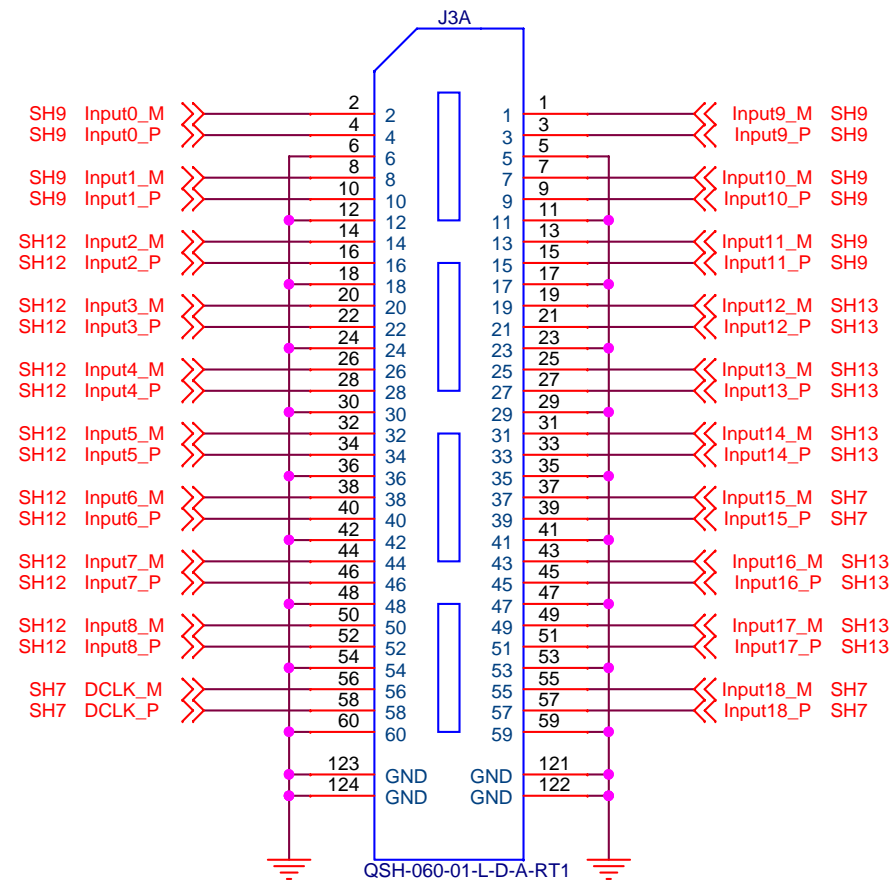
Drawn: P. LARSON  
 Engineer: J. SETON

# CMOS Header

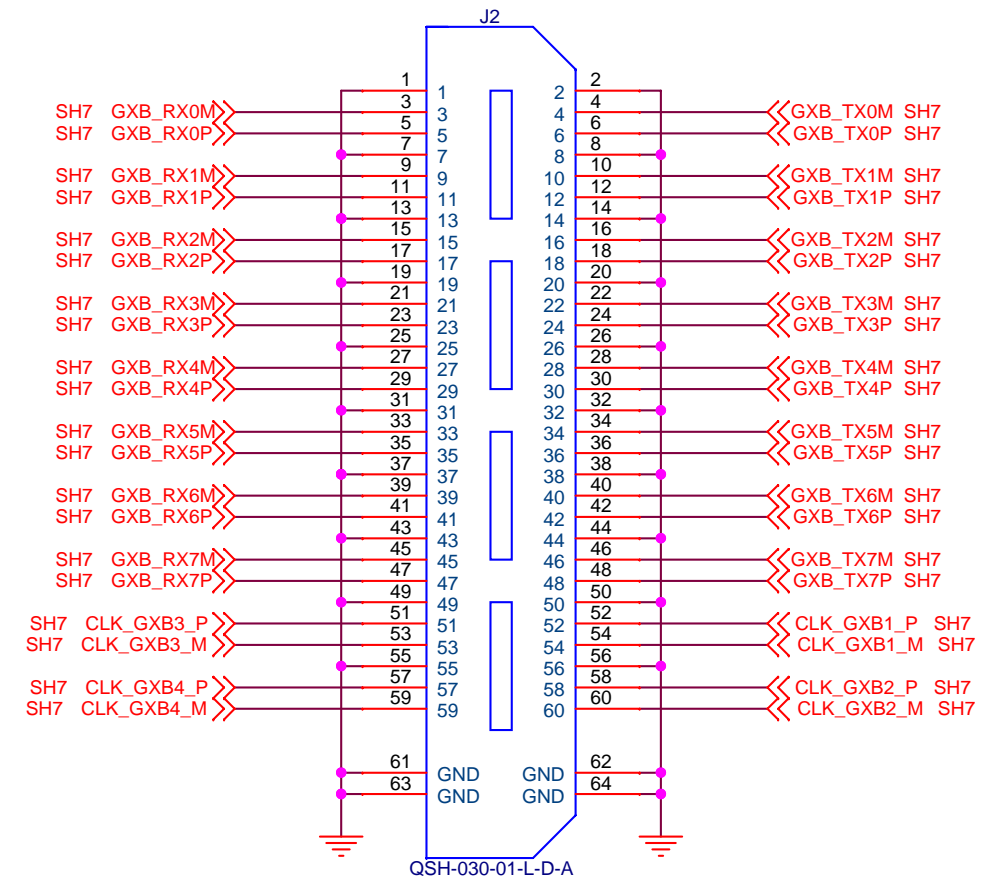


Title		
<b>CMOS Header</b>		
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# ADC Interface



# JESD

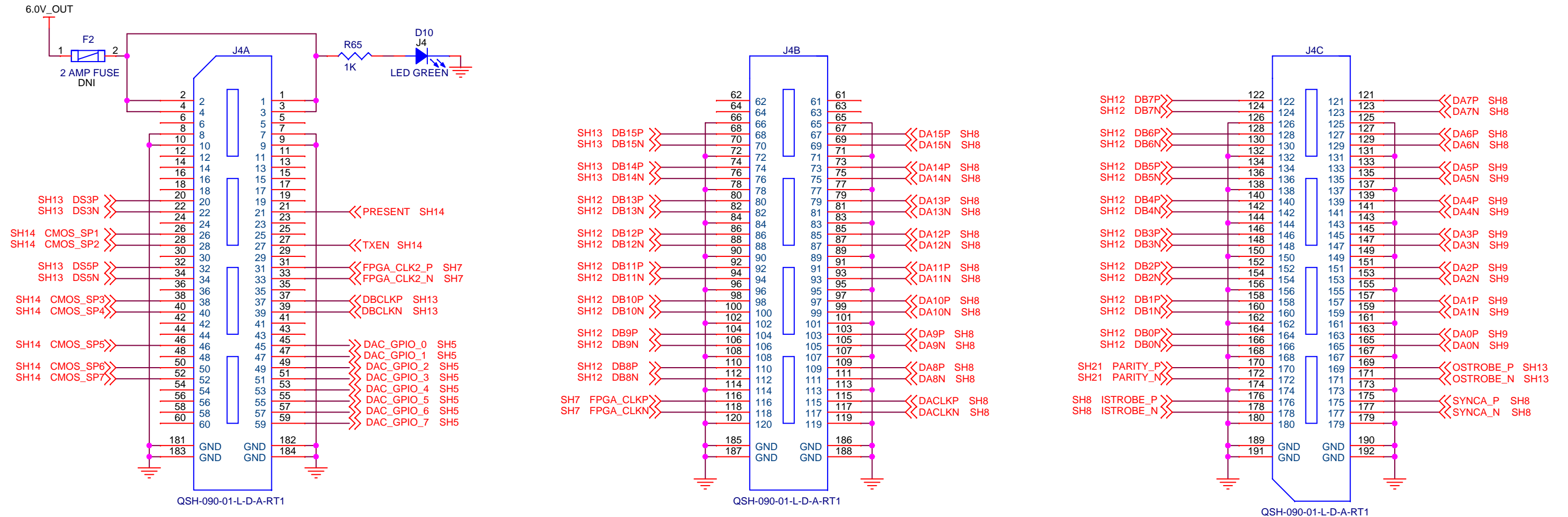


**TEXAS INSTRUMENTS**

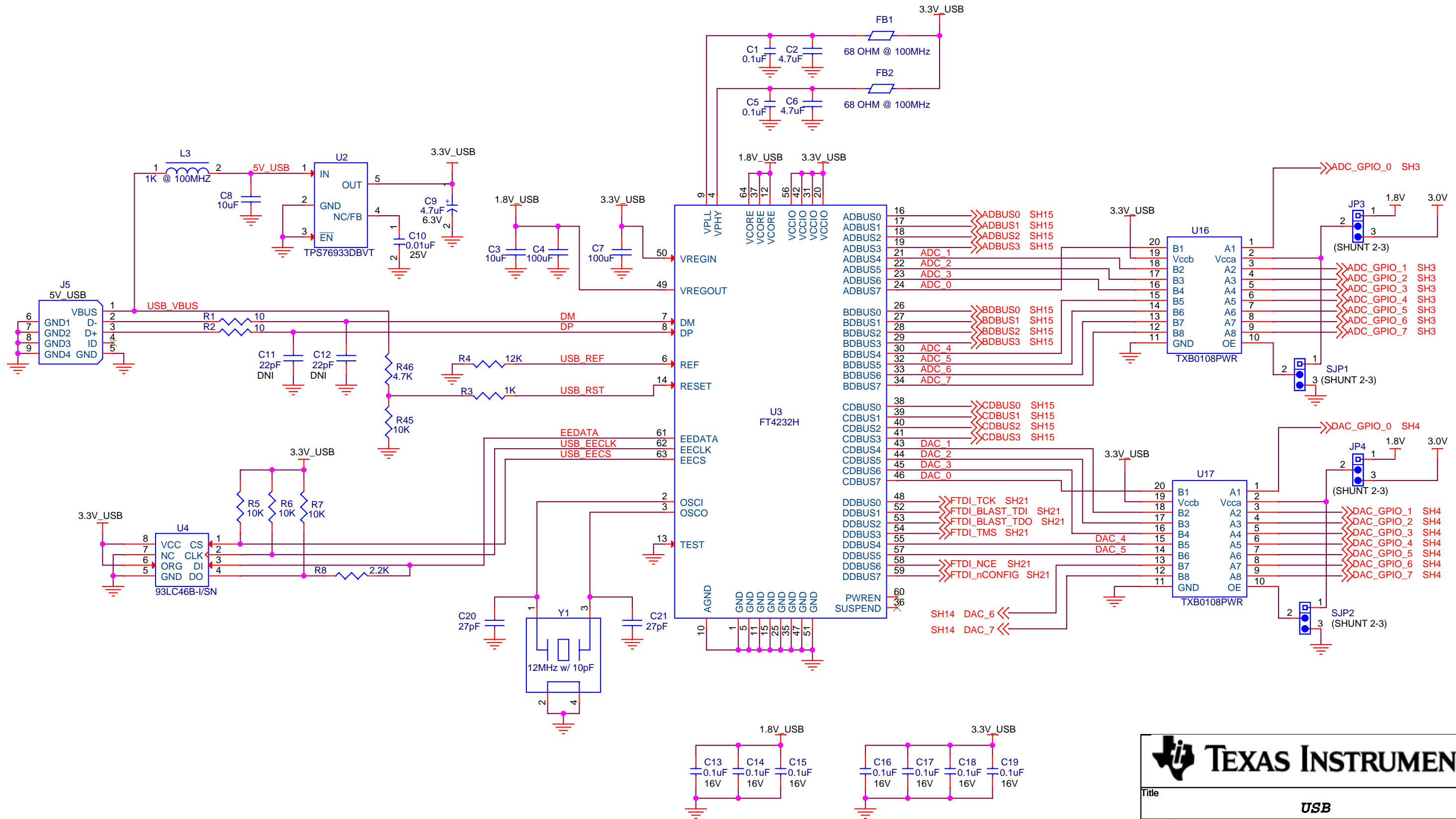
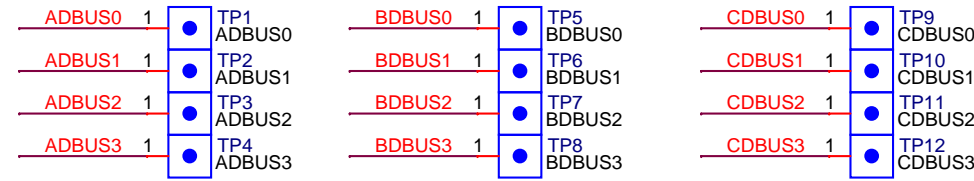
Title: **ADC & JESD INTERFACE**

Size: <b>B</b>	Document Number: <b>TSW1400</b>	Rev: <b>D</b>
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# DAC Interface

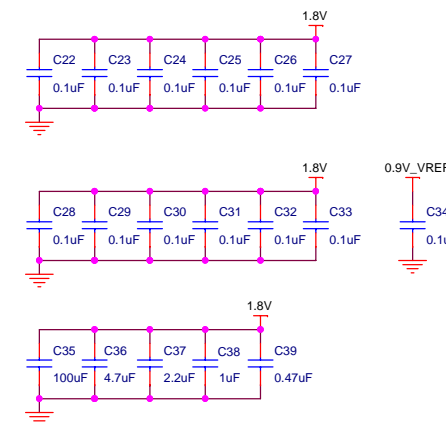
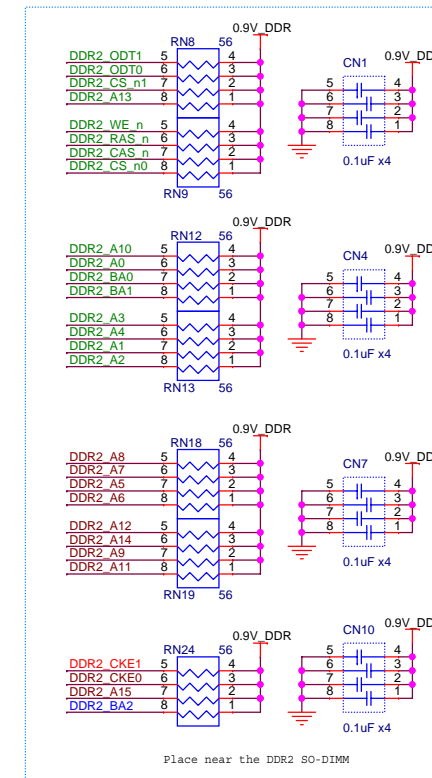


# USB

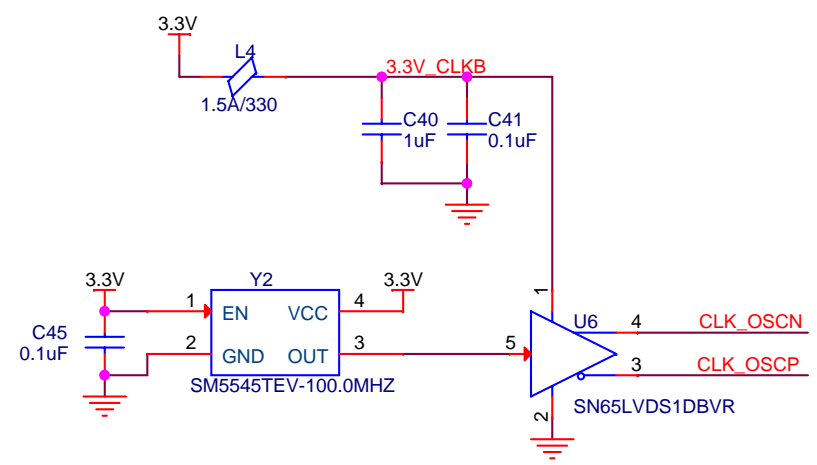
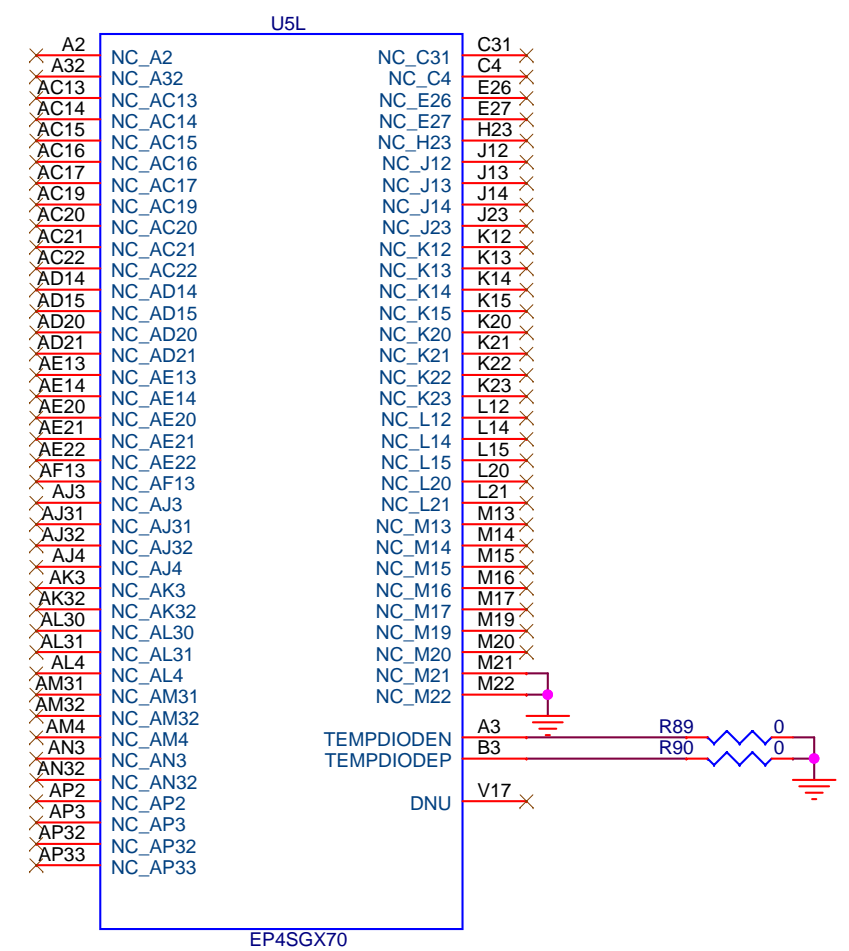


**TEXAS INSTRUMENTS**  
 Title: **USB**  
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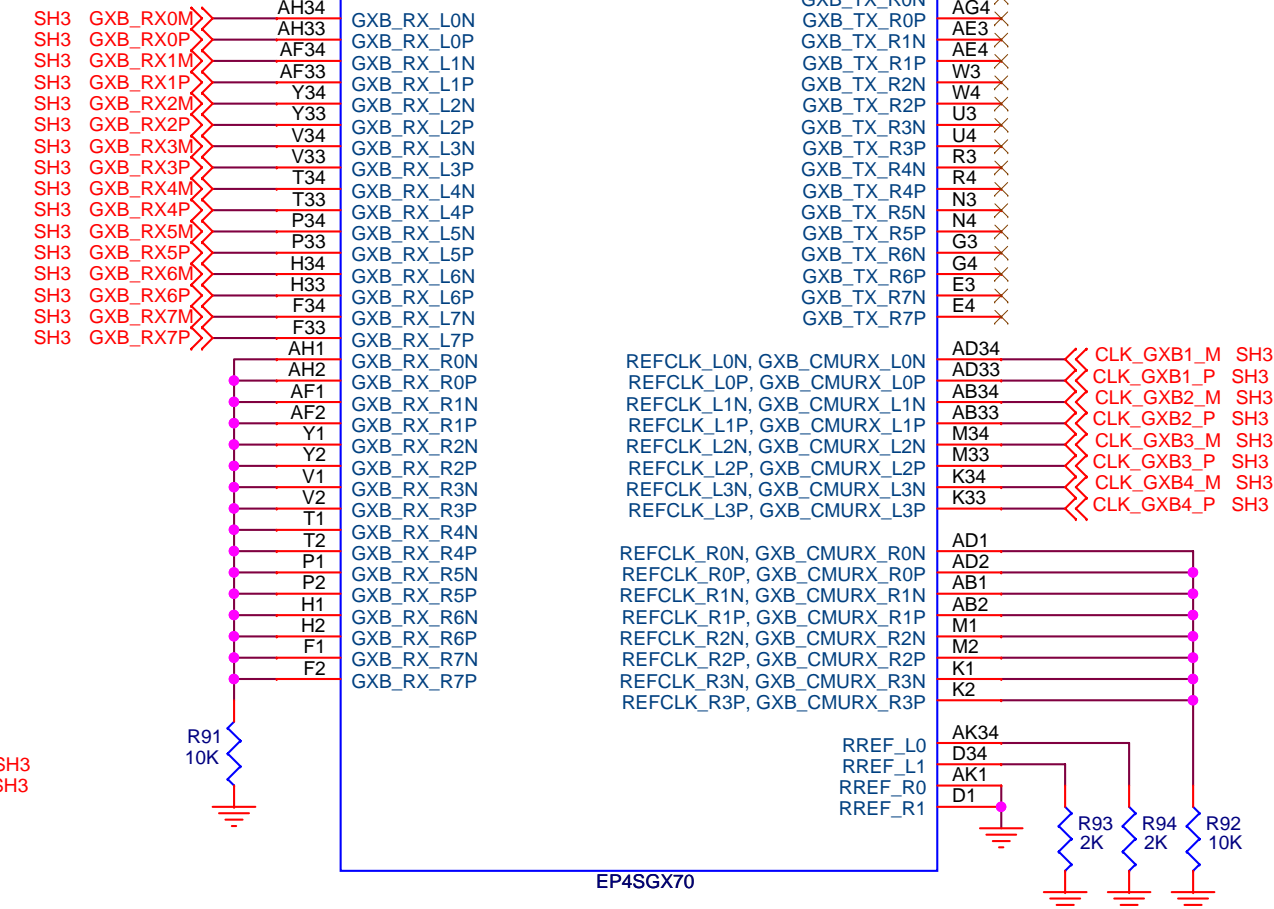
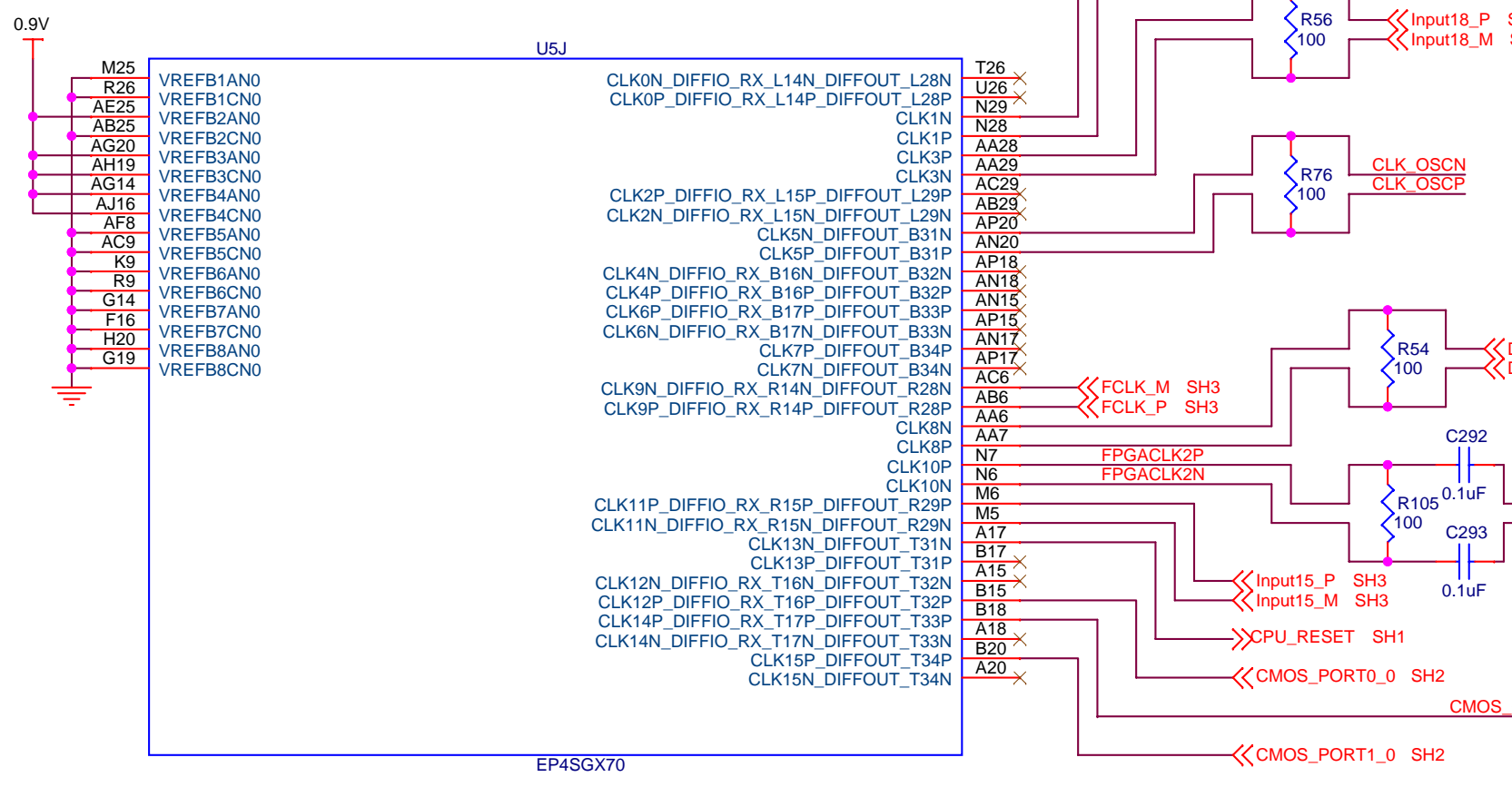
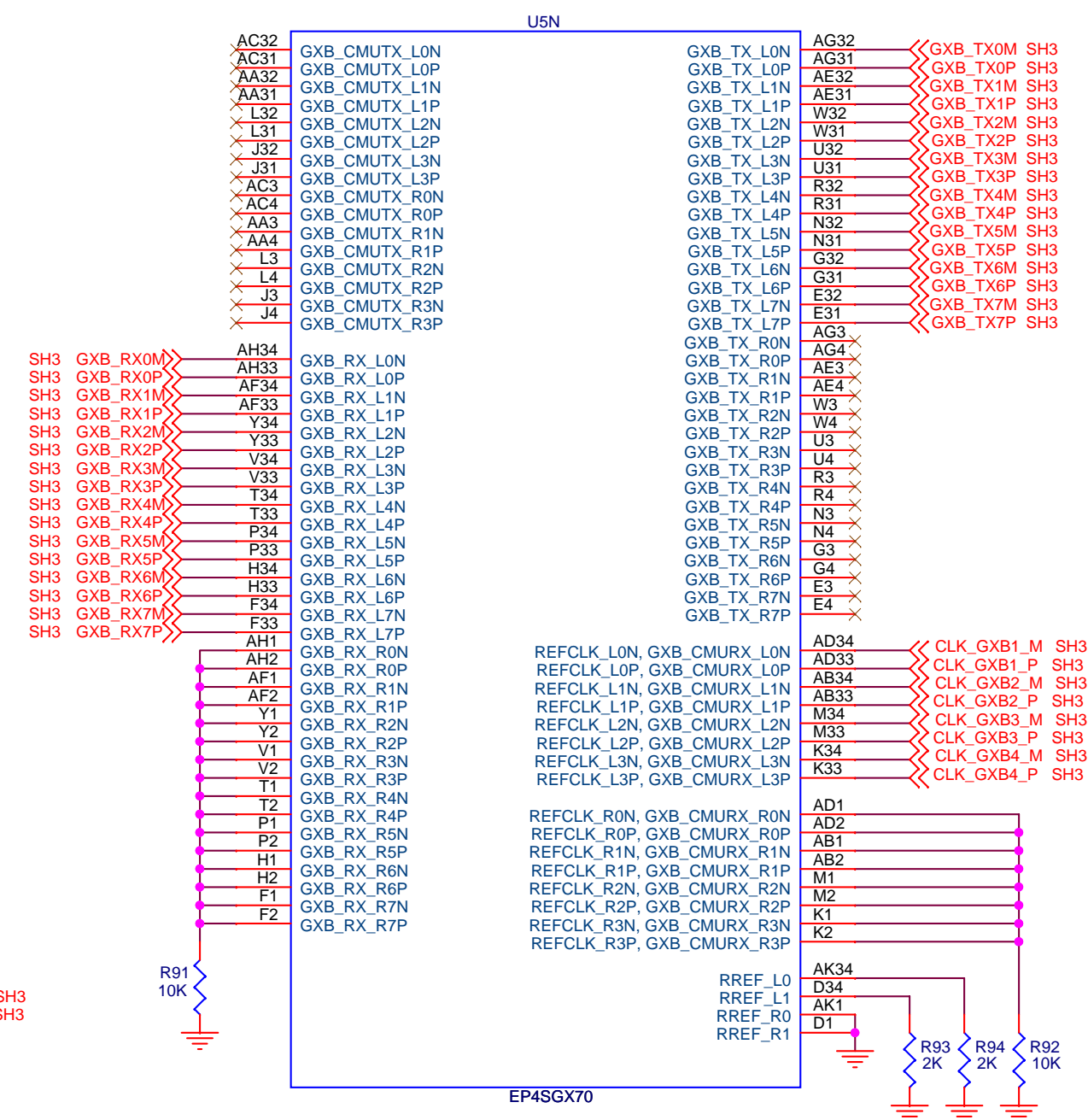
# DDR2 SO-DIMM







# BANK QL



**TEXAS INSTRUMENTS**

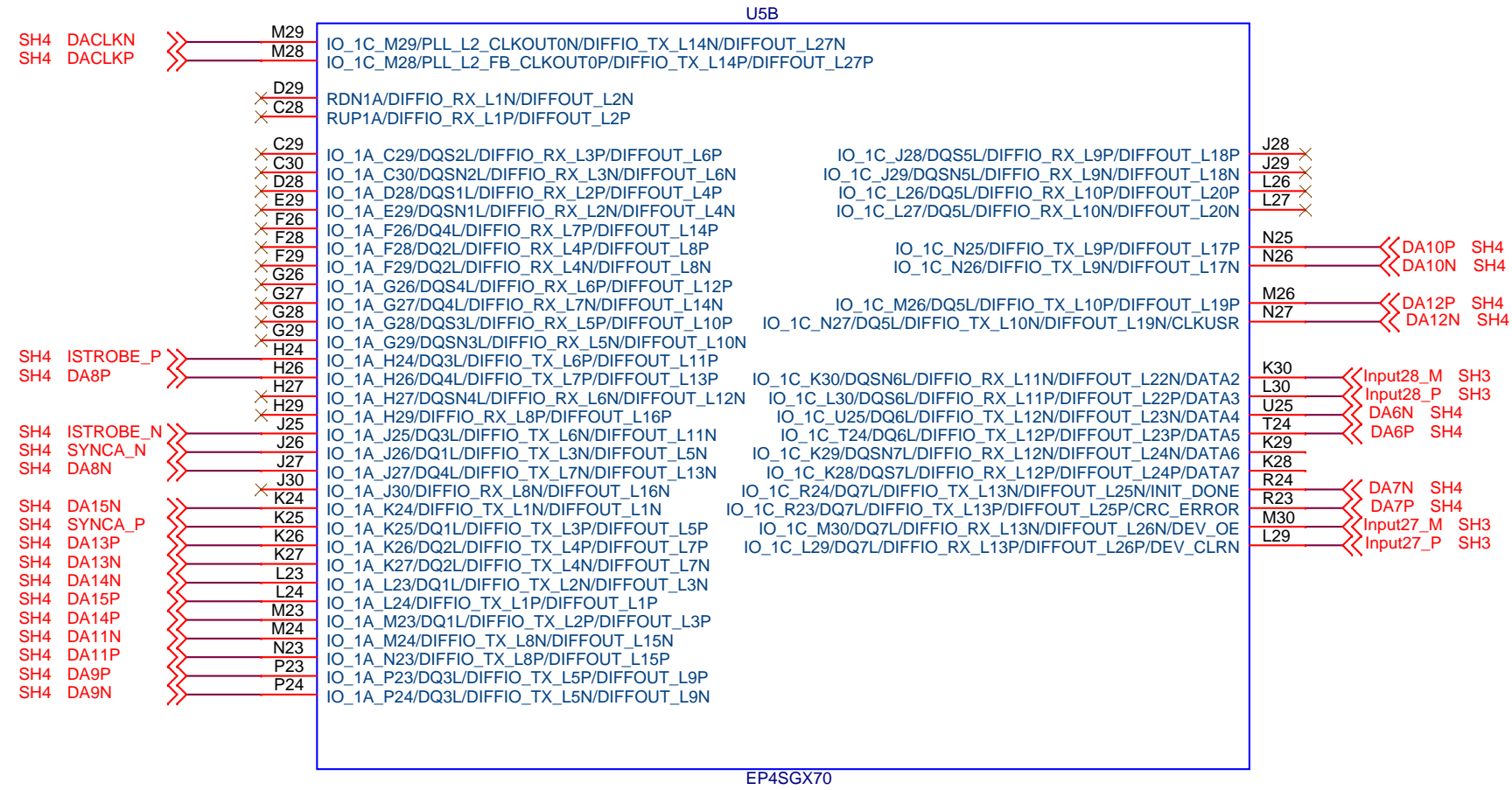
Title: **Bank QL**

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# BANK1

## 2.5V



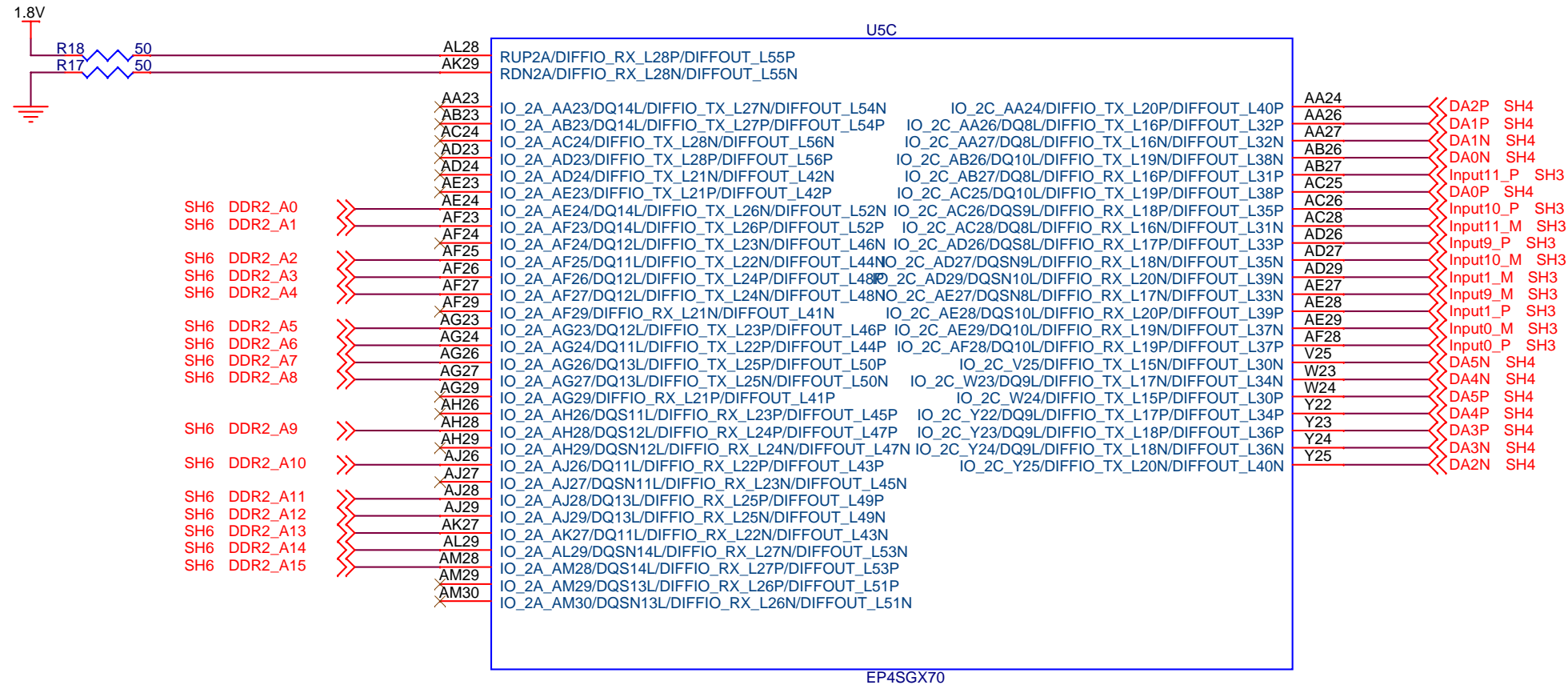
Title		
<b>Bank1</b>		
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# BANK2

1.8V

2.5V



**TEXAS INSTRUMENTS**

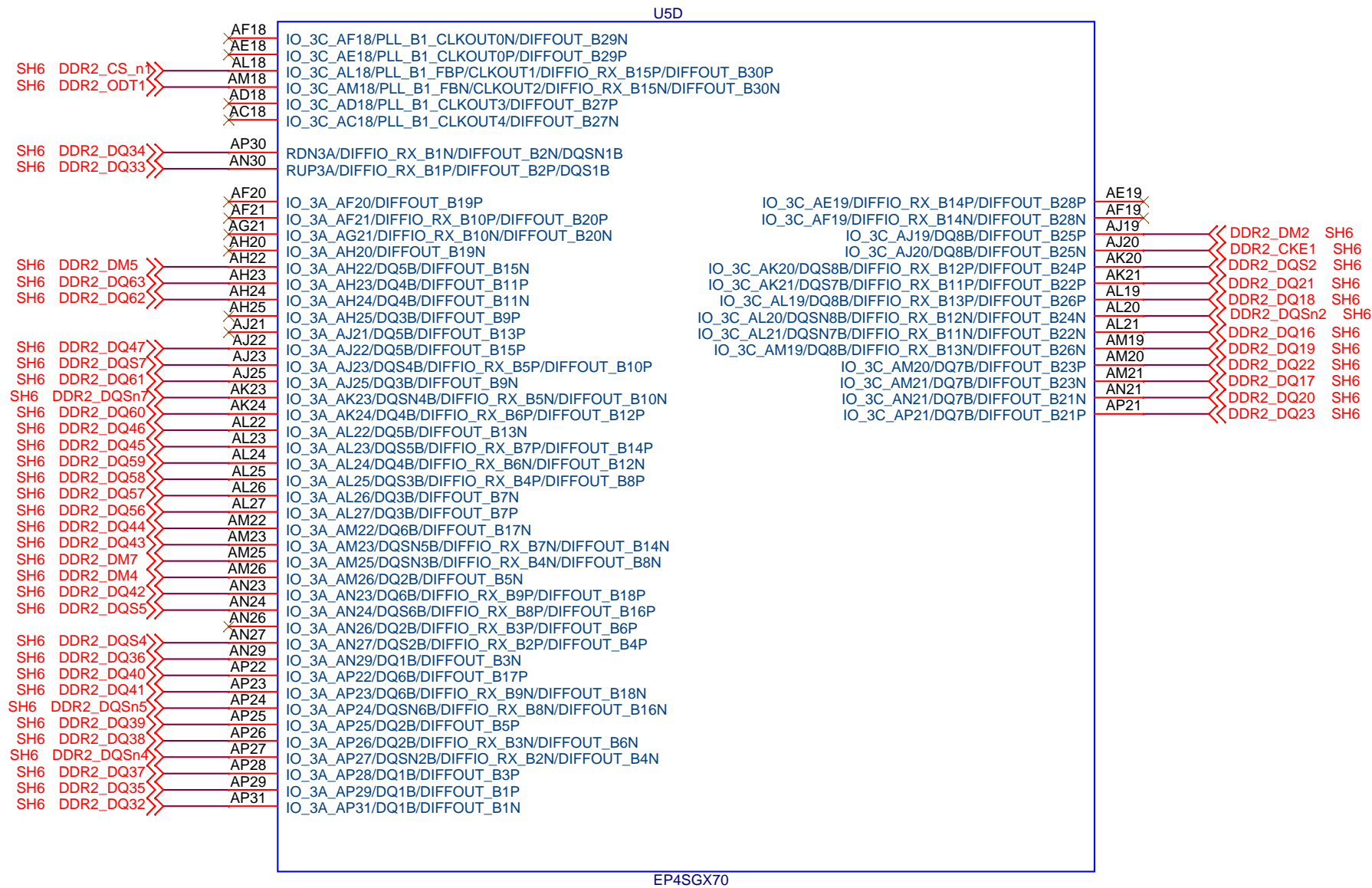
Title: **Bank2**

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# BANK3

## 1.8V

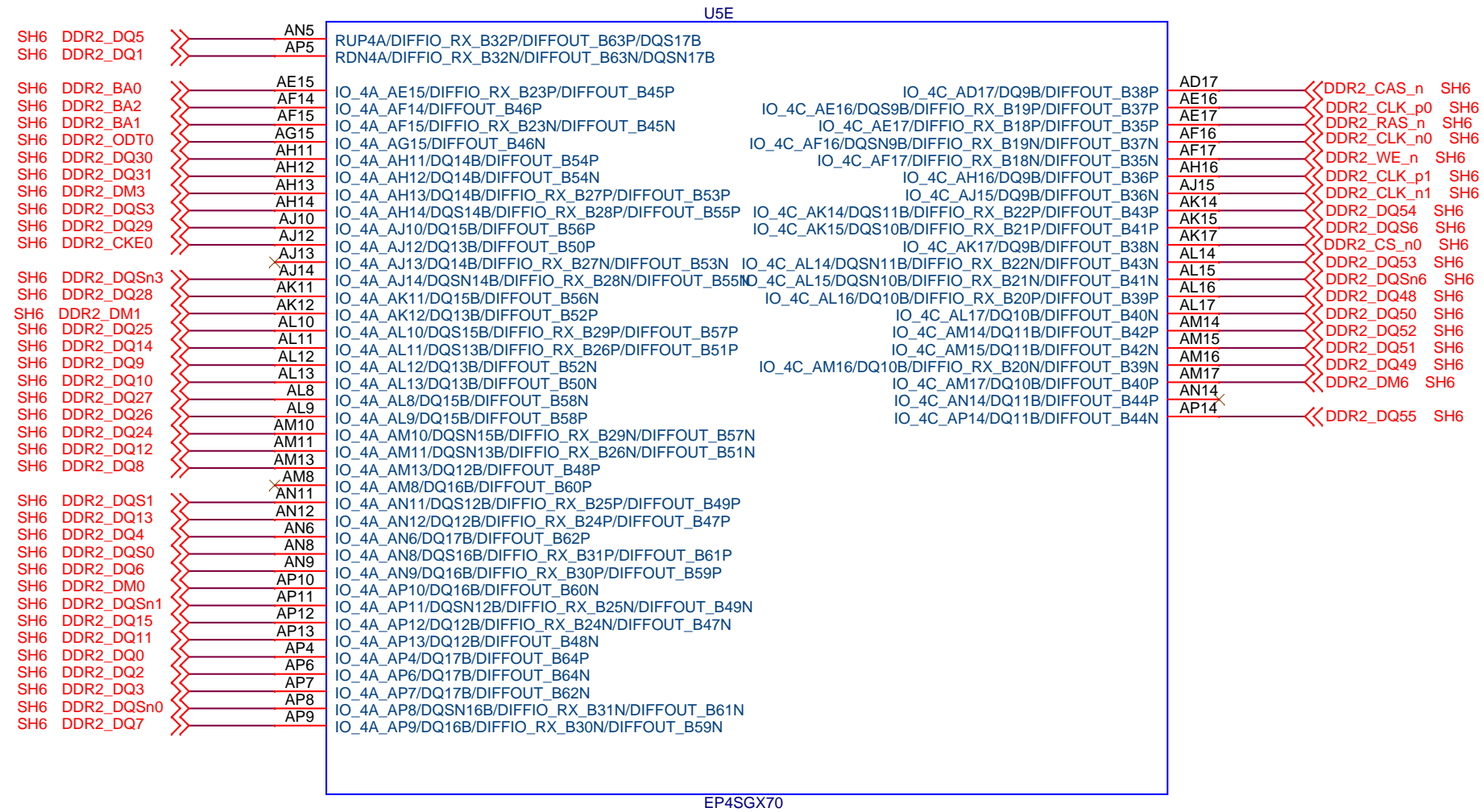


**TEXAS INSTRUMENTS**

Title		
<b>Bank3</b>		
Size	Document Number	Rev
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# BANK4

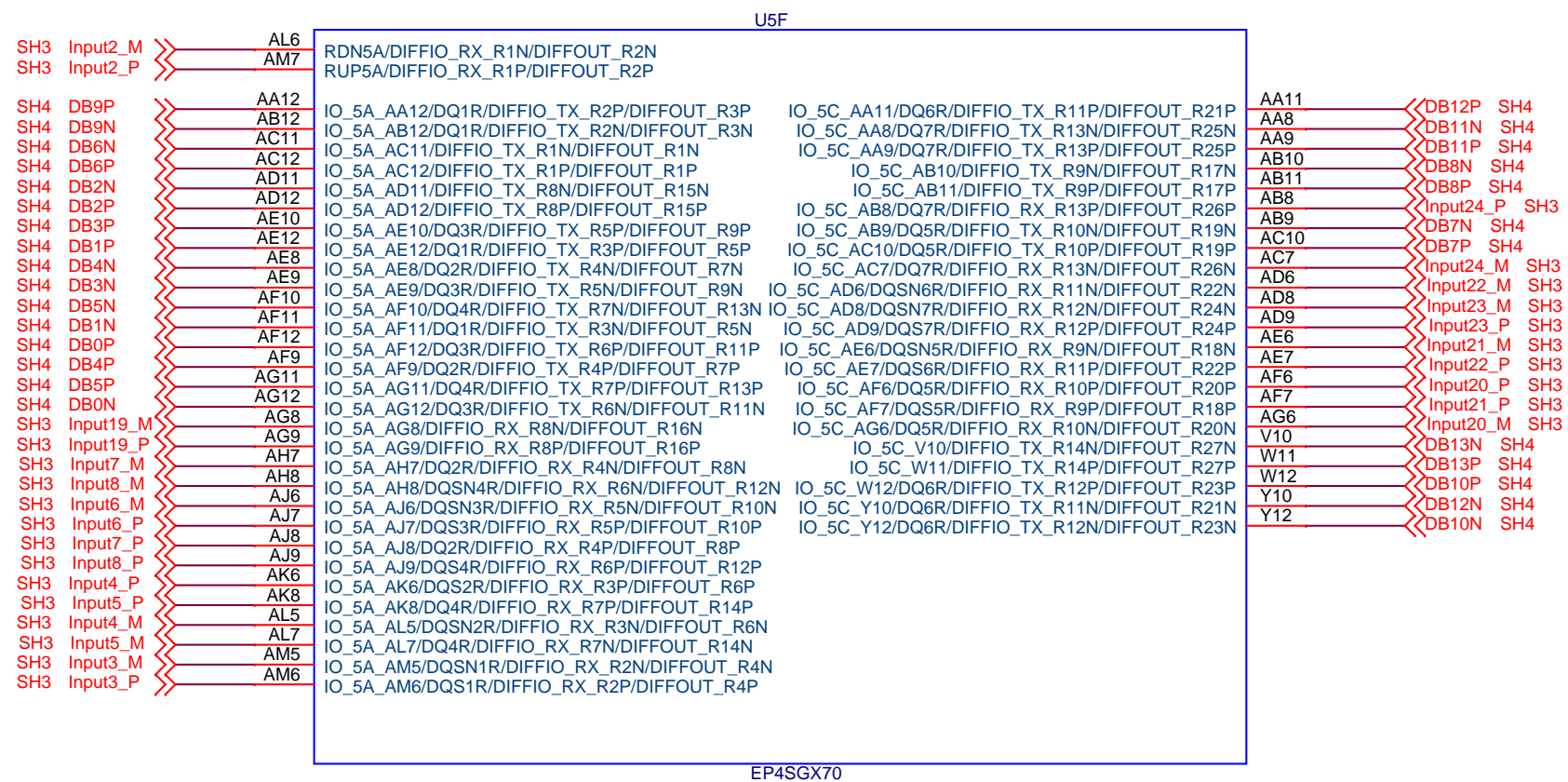
## 1.8V



**TEXAS INSTRUMENTS**

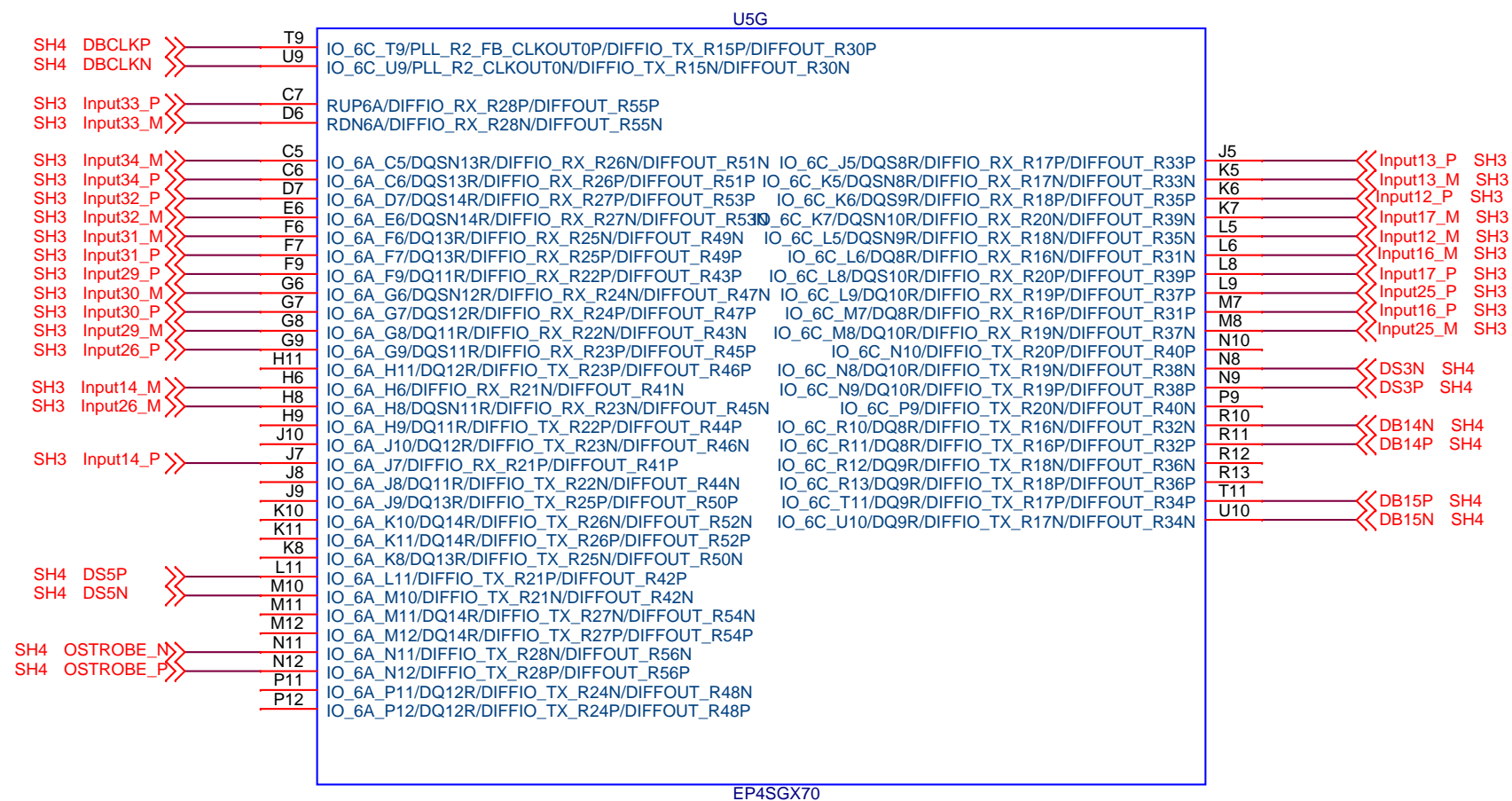
Title		
<b>Bank4</b>		
Size	Document Number	Rev
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# BANK5 2.5V



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<b>Bank5</b>		
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# BANK6 2.5V

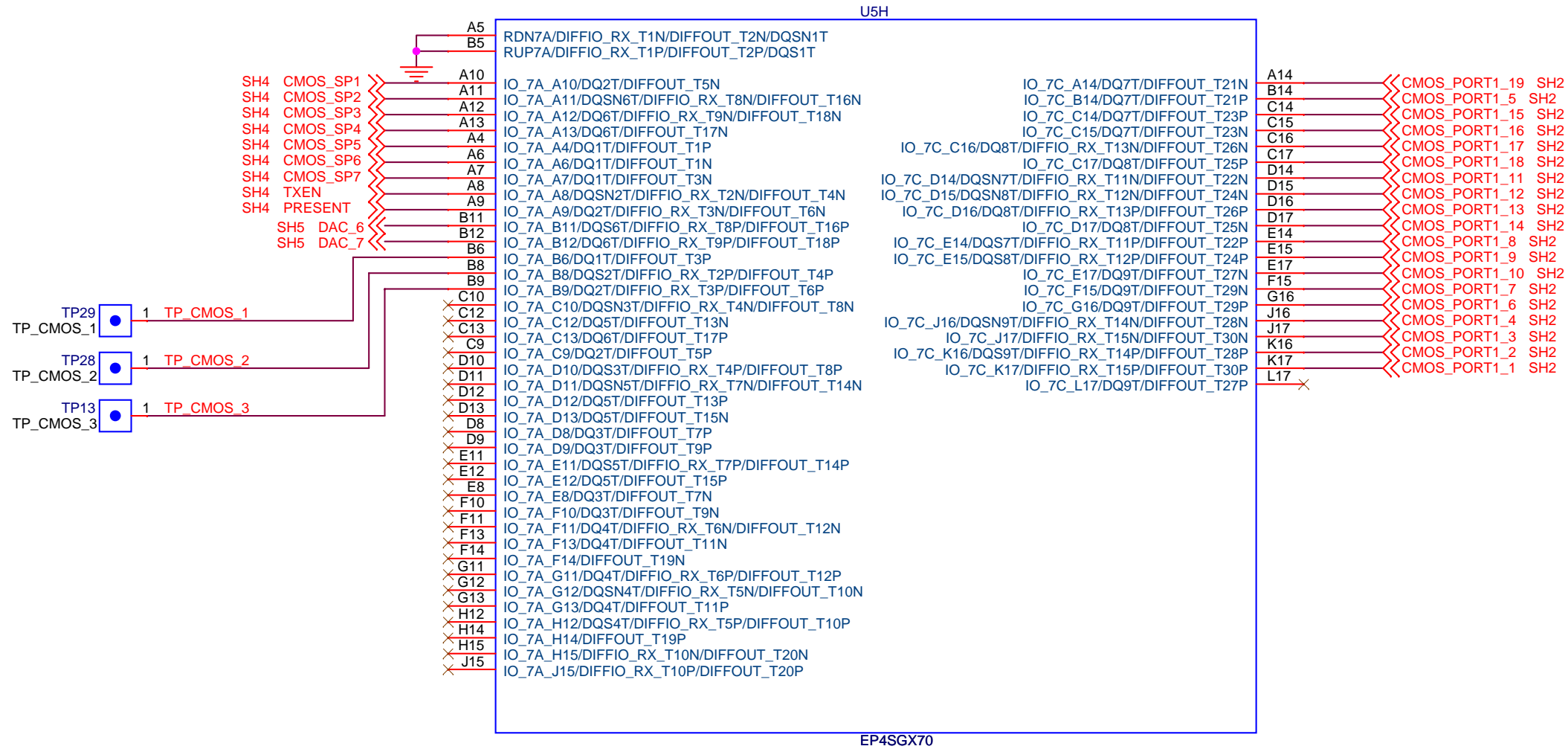


Title		
<b>Bank6</b>		
Size	Document Number	Rev
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# BANK7

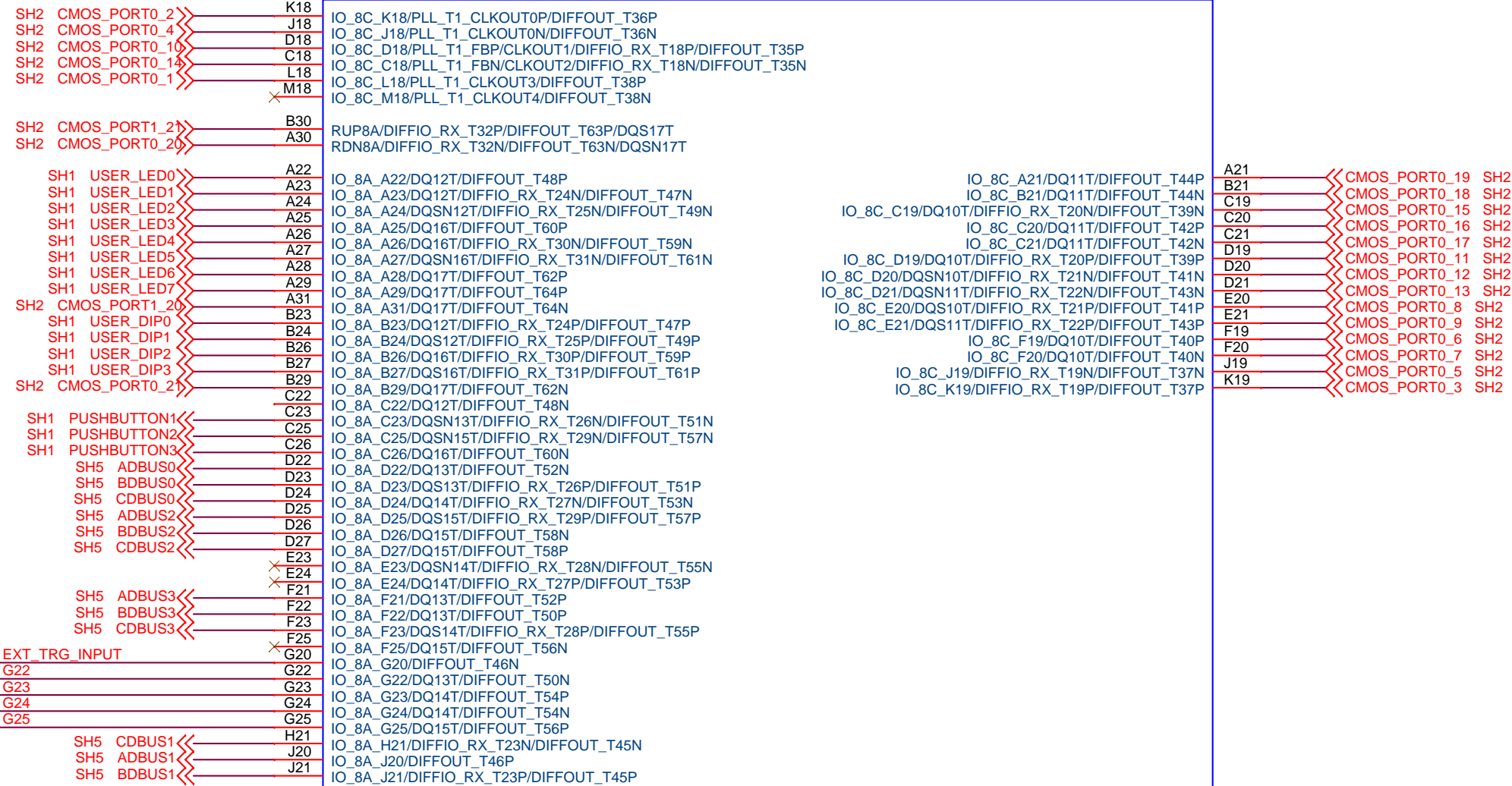
## 3.0V



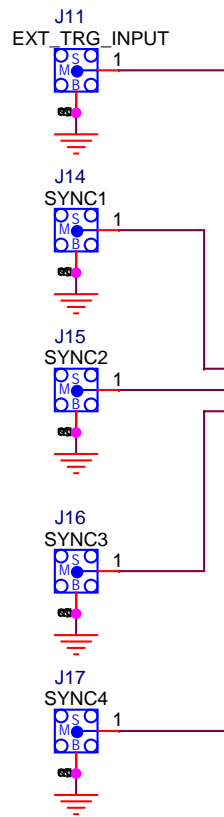
# BANK8

## 3.0V

U51



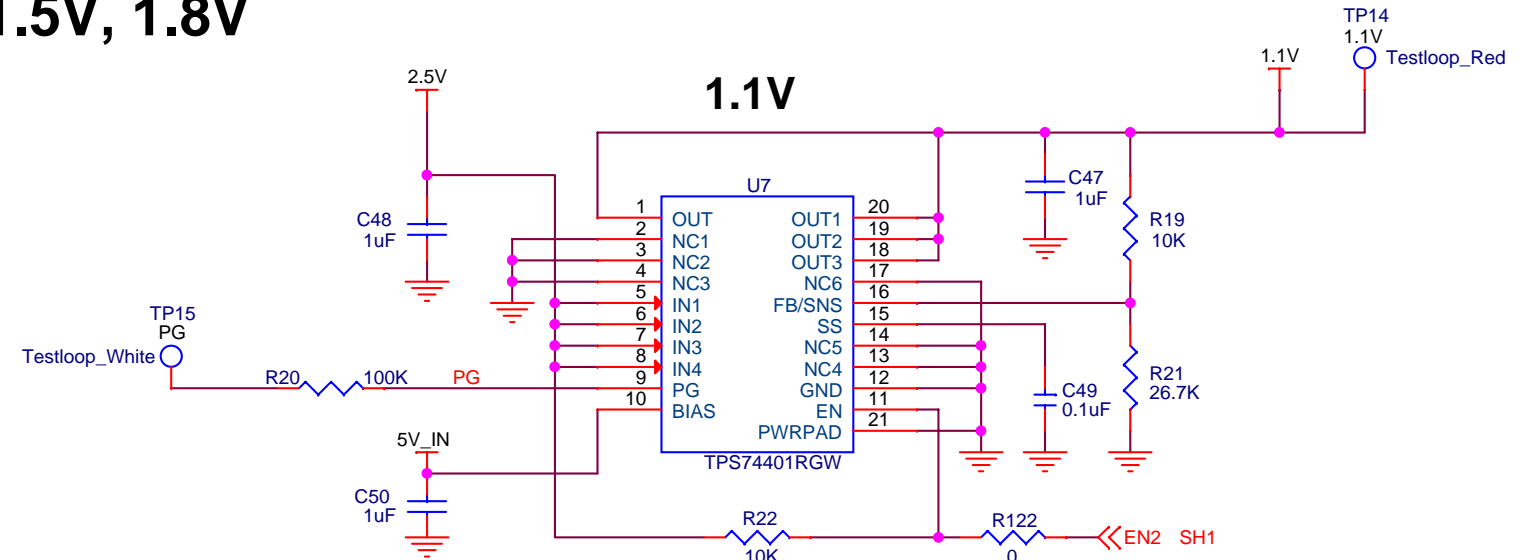
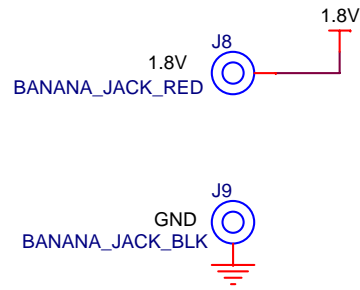
EP4SGX70



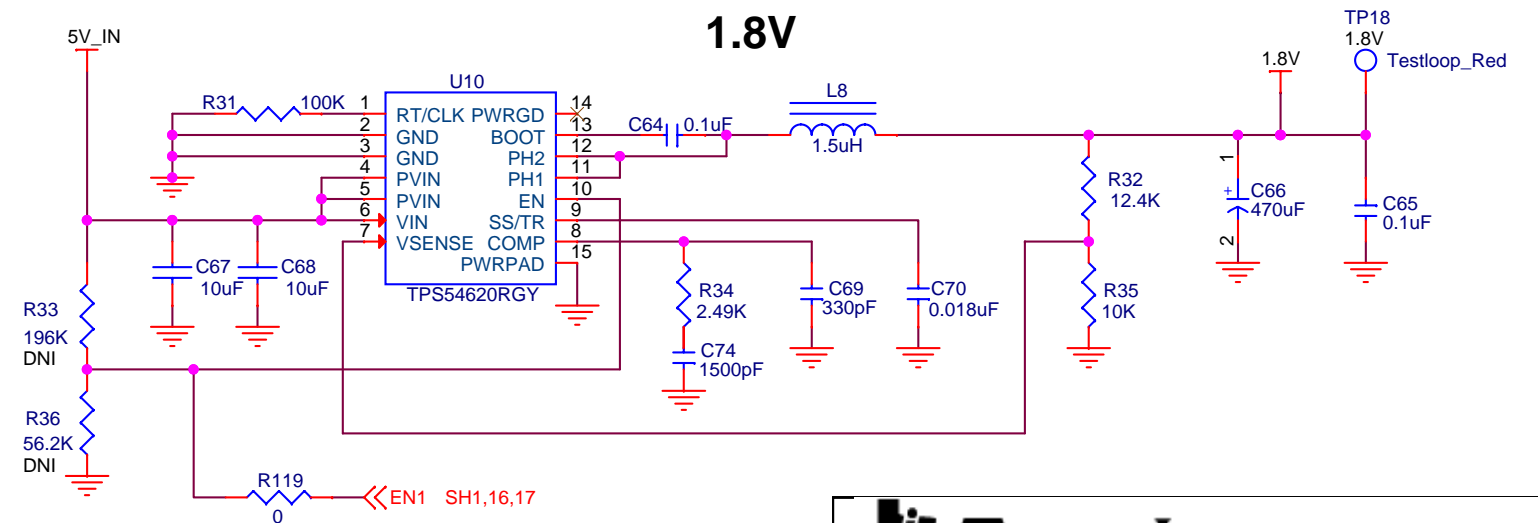
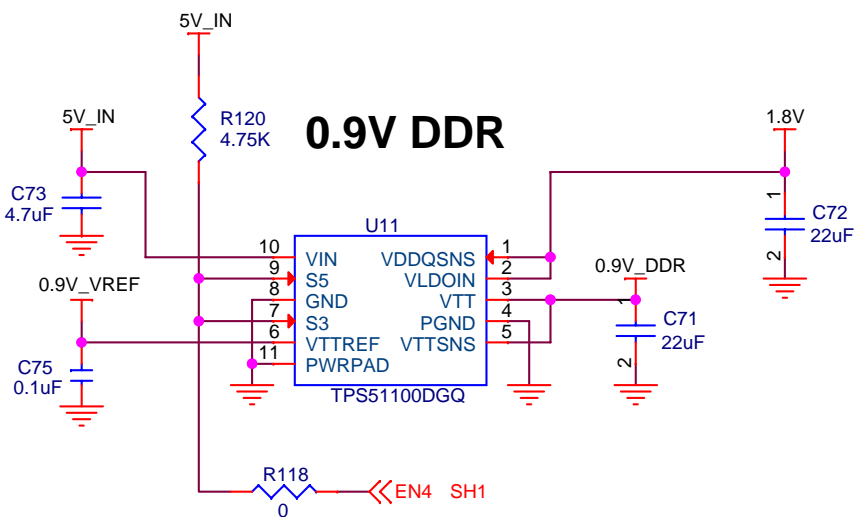
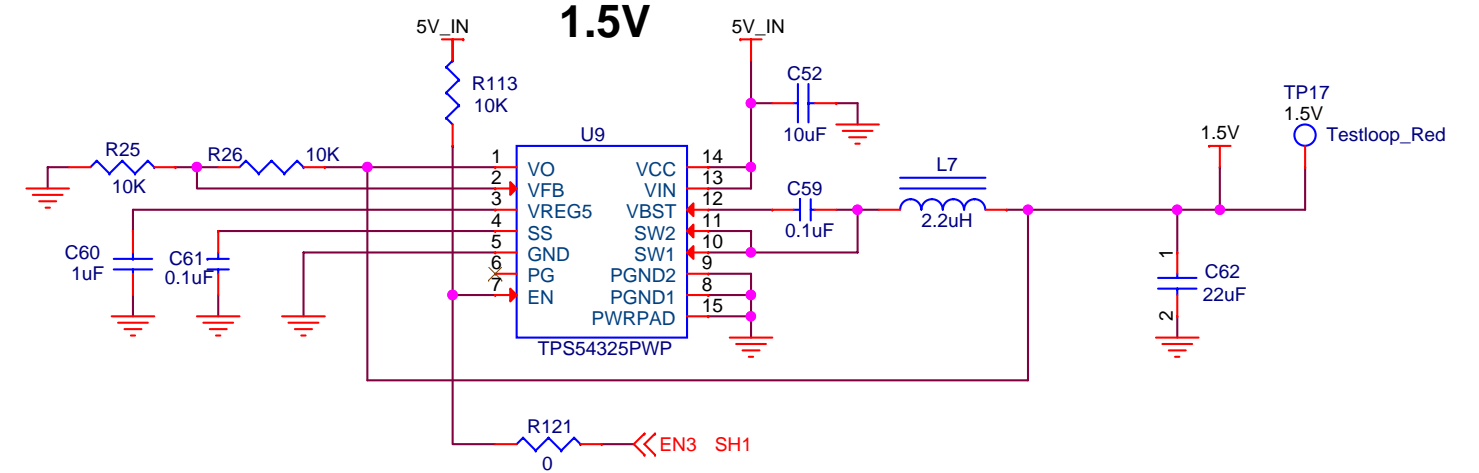
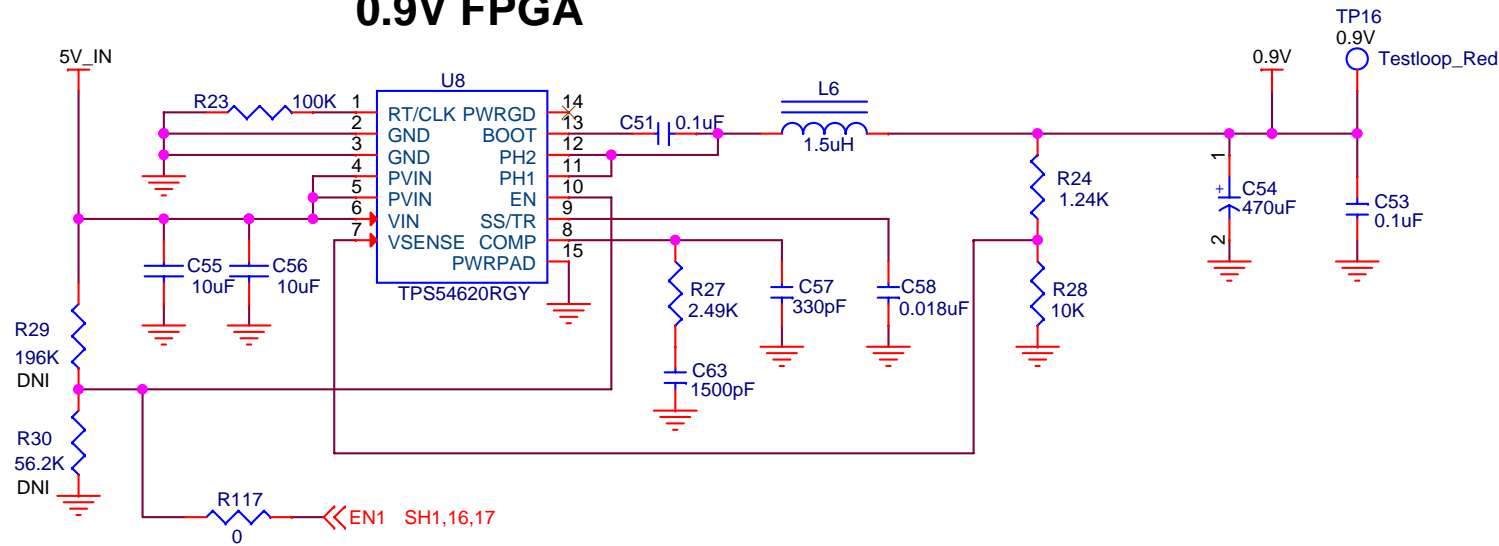
**TEXAS INSTRUMENTS**

Title		
Bank8		
Size	Document Number	Rev
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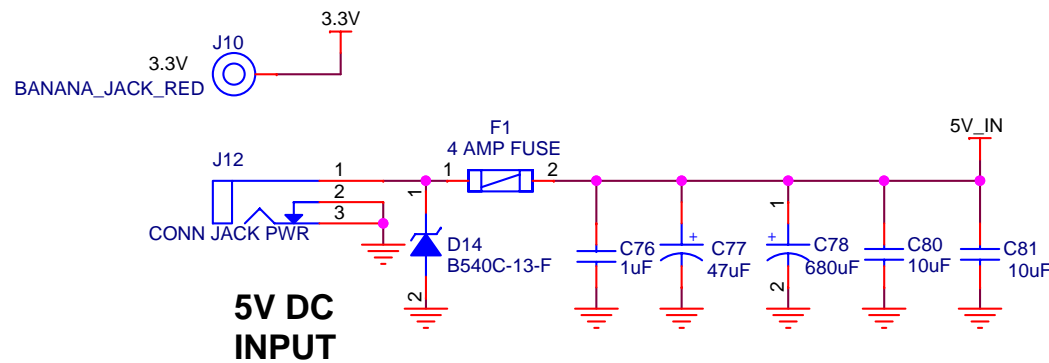
# 0.9V, 1.1V, 1.5V, 1.8V



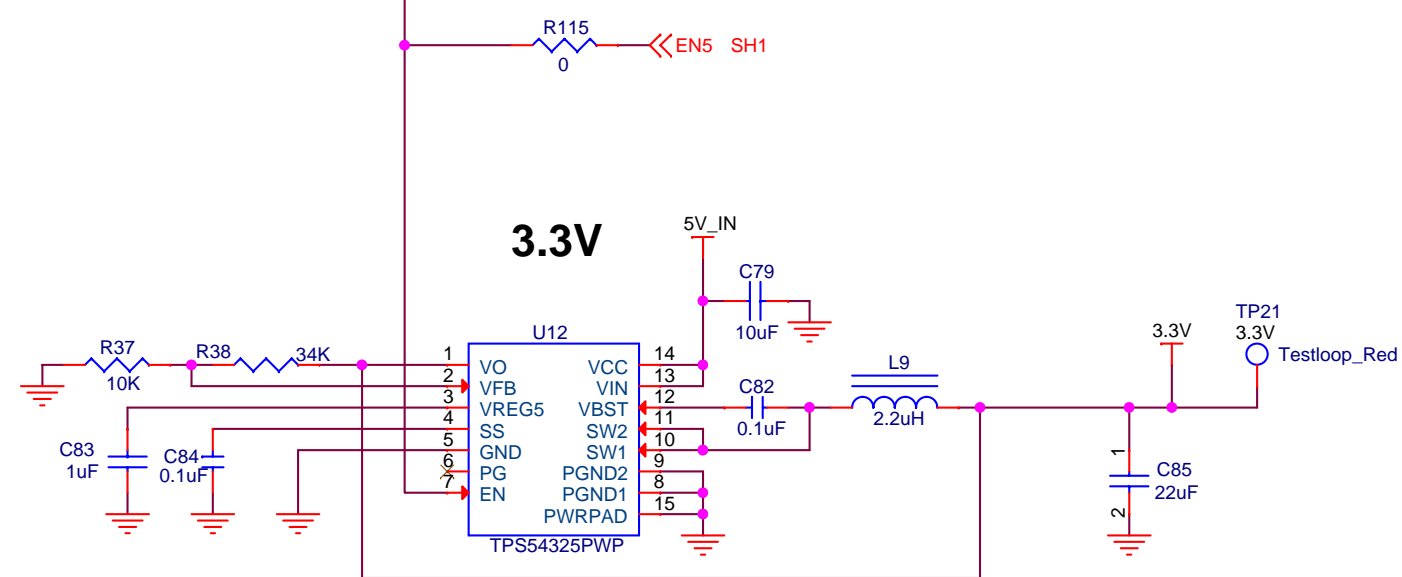
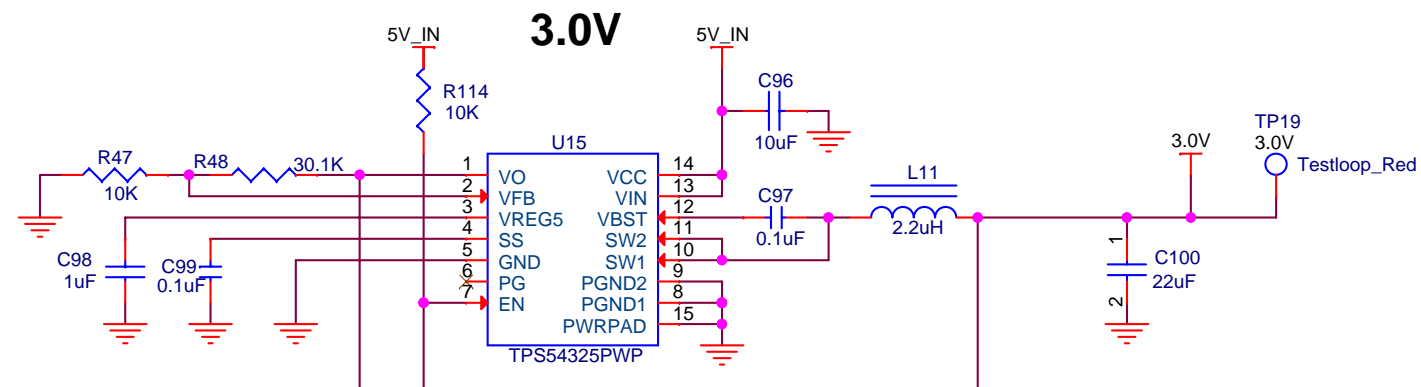
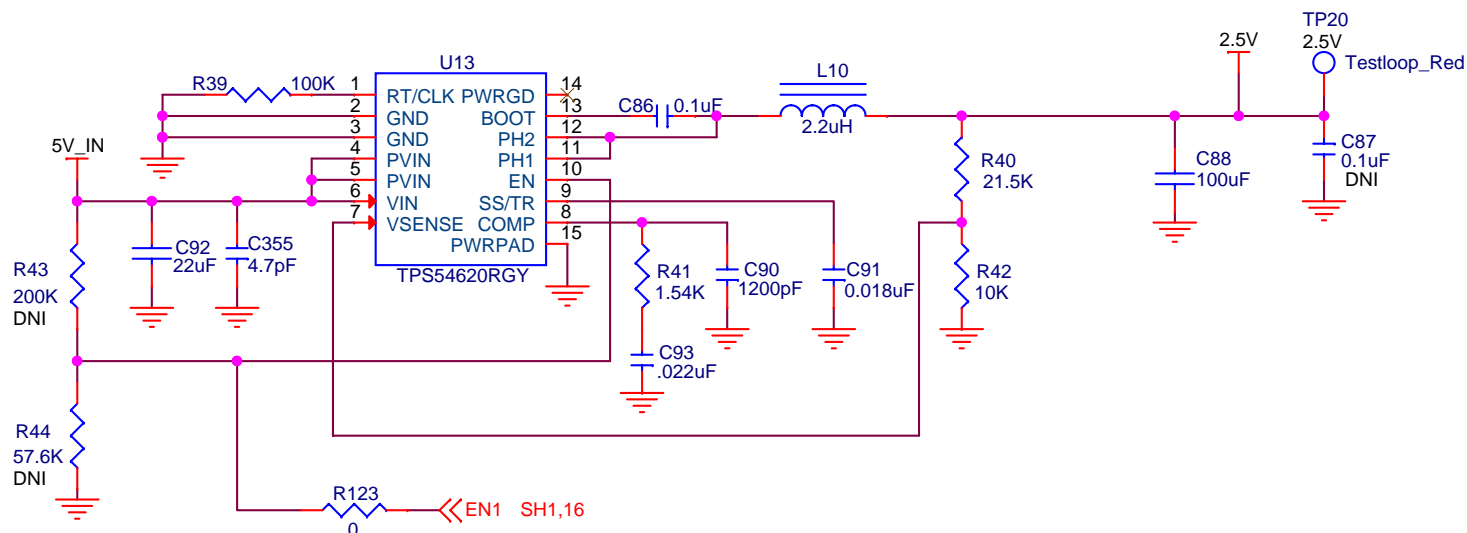
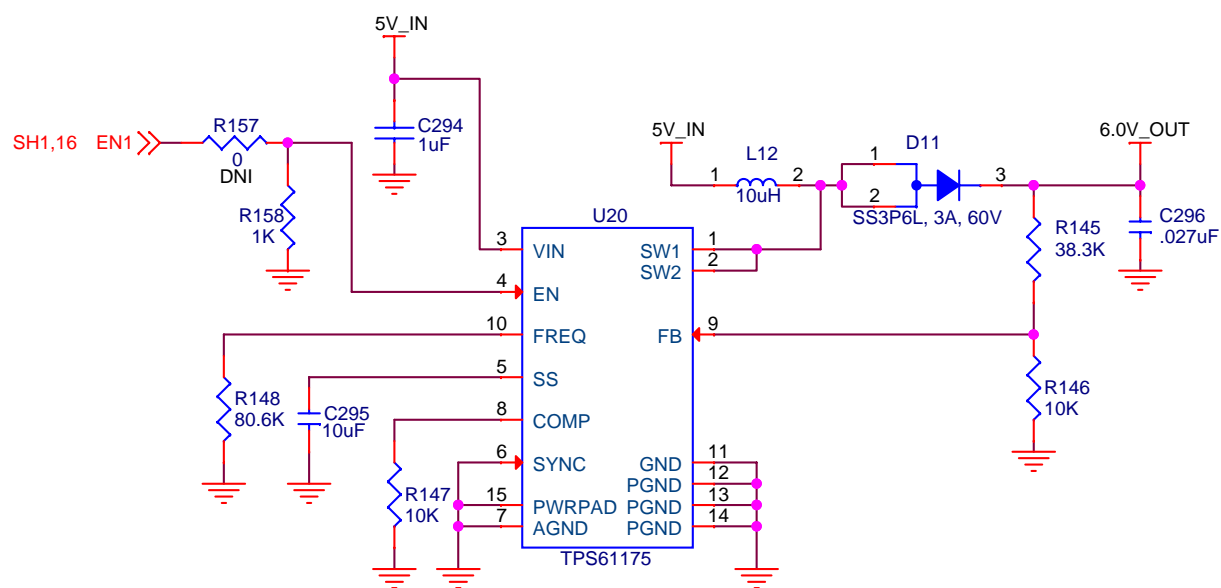
## 0.9V FPGA



Title		
POWERS 0.9V, 1.1V, 1.5V, 1.8V		
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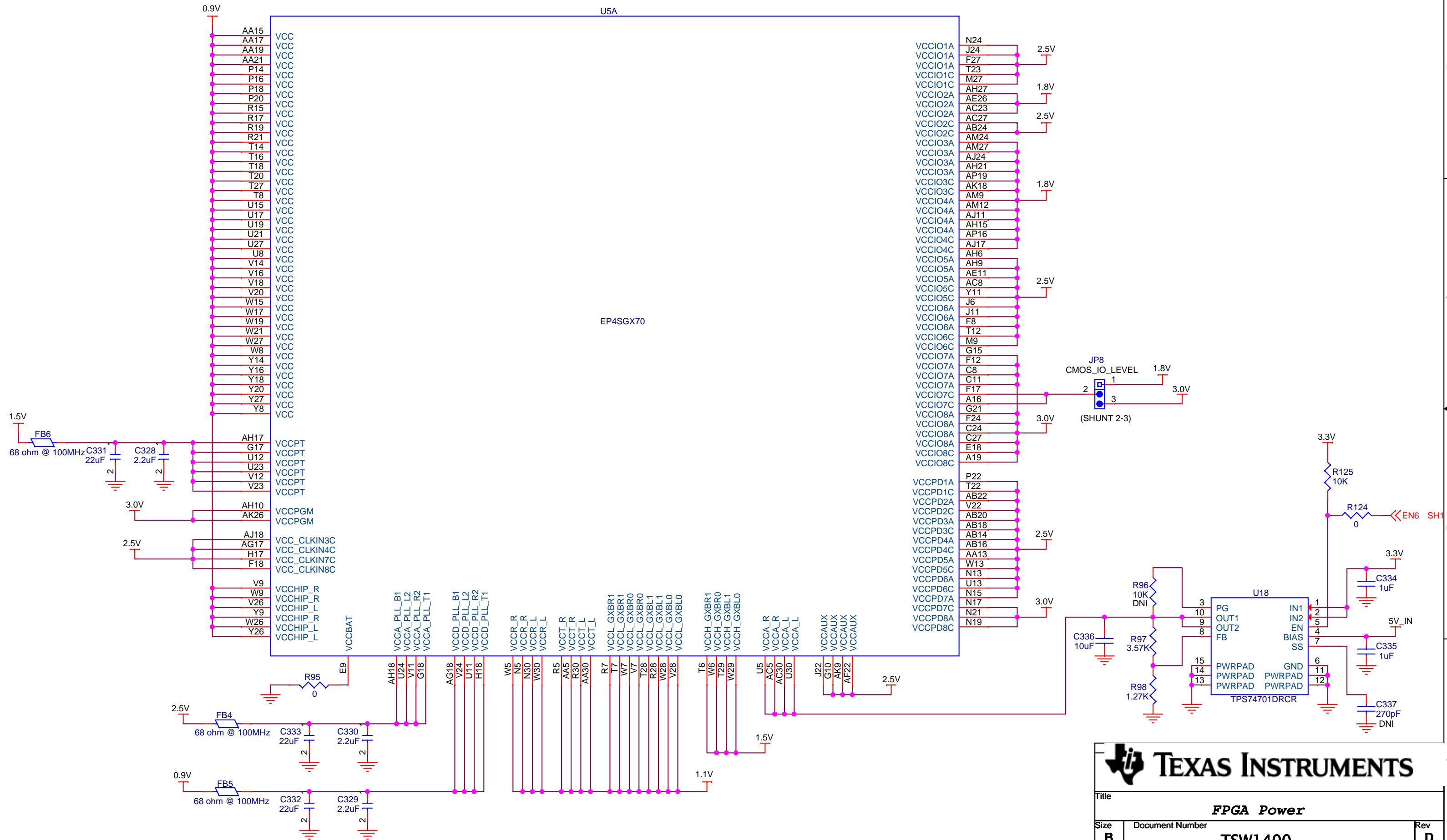


## 2.5V, 3.0V, 3.3V, 5V



Title		
POWERS 2.5V, 3.0V, 3.3V, 5V		
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# FPGA Power



**TEXAS INSTRUMENTS**

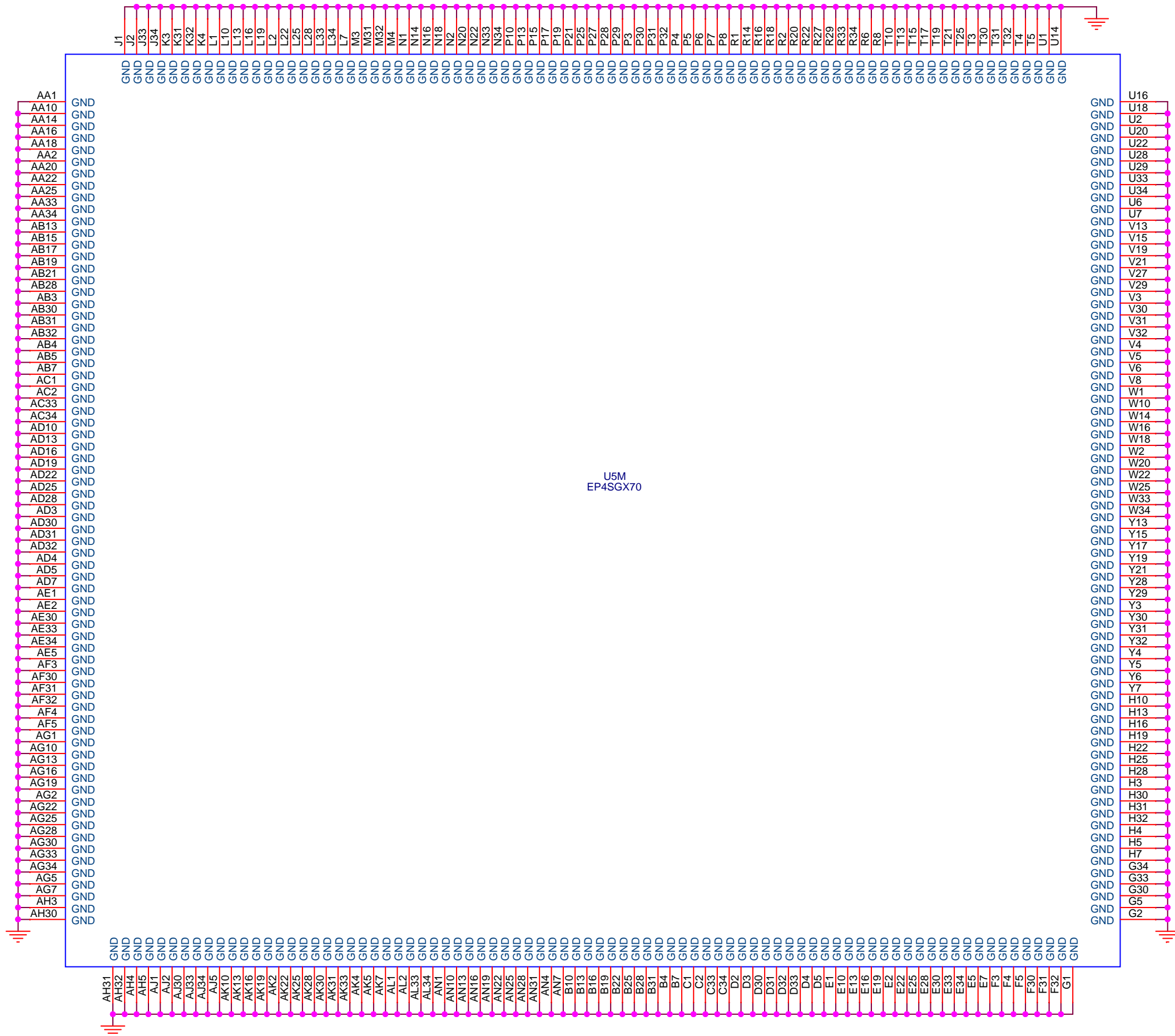
Title: **FPGA Power**

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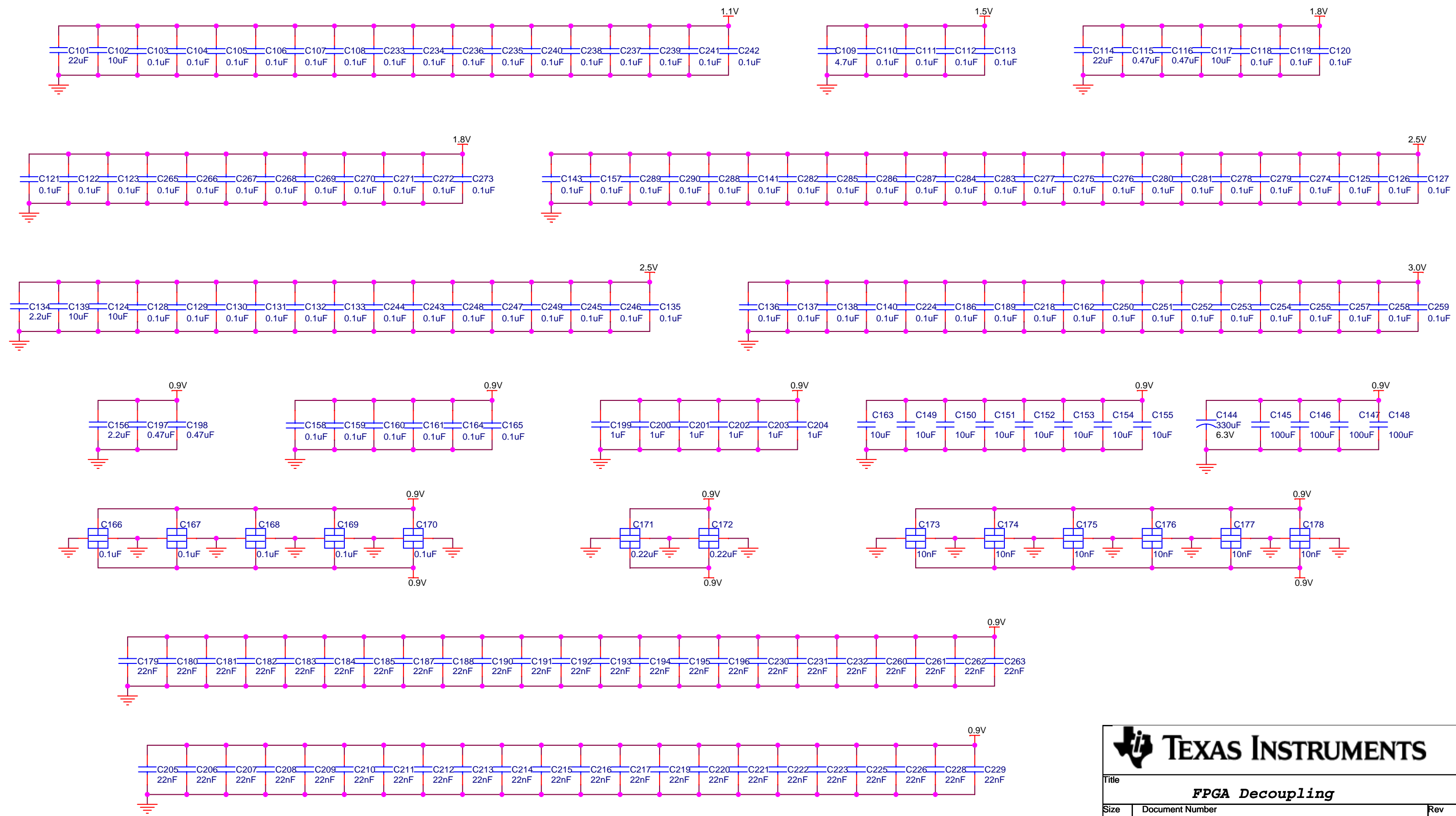


# FPGA Ground



Title		
<b>FPGA Ground</b>		
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<b>B</b>	<b>TSW1400</b>	<b>D</b>
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# FPGA Decoupling

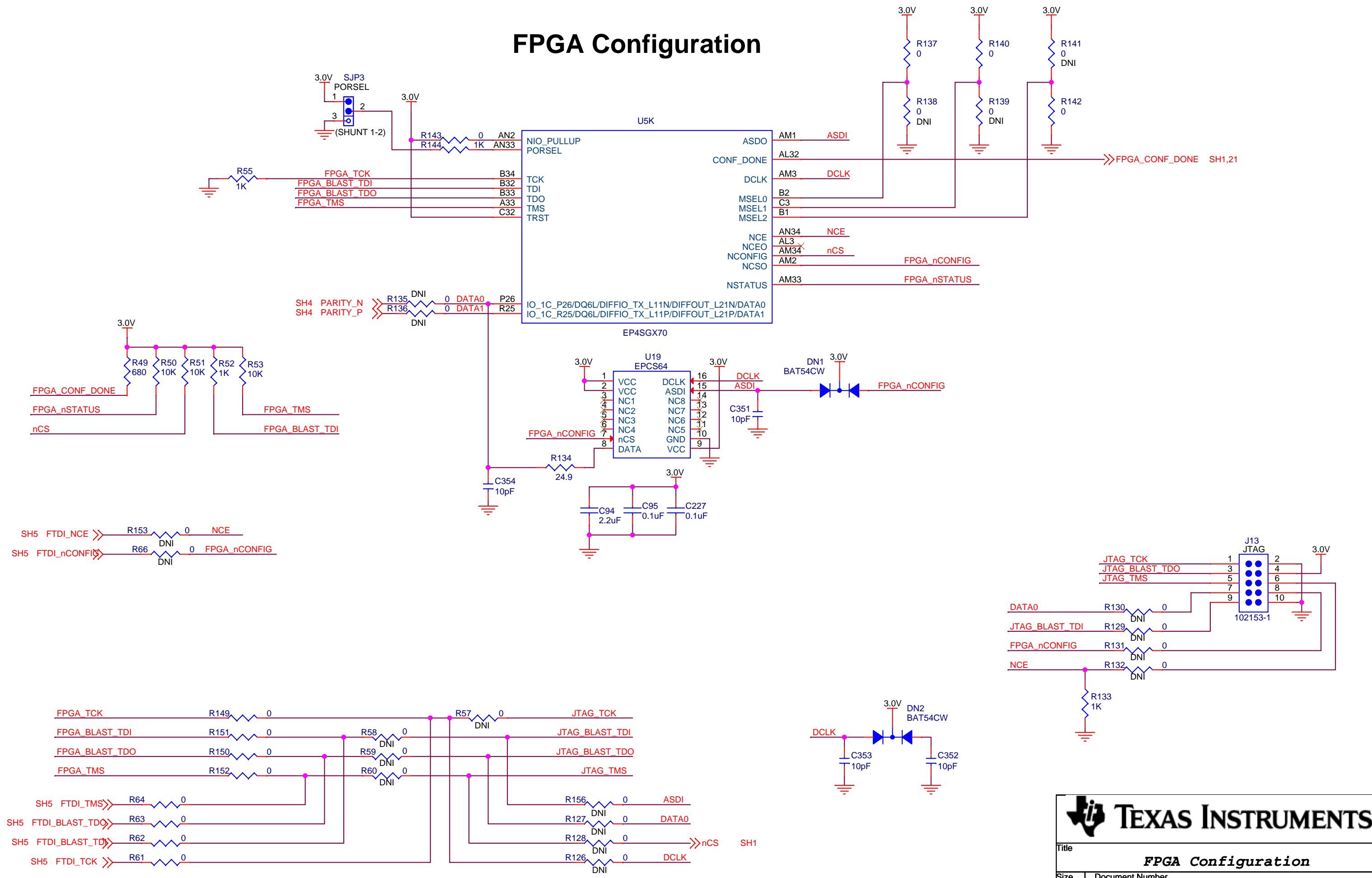


**TEXAS INSTRUMENTS**

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# FPGA Configuration



**TEXAS INSTRUMENTS**

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