Schematic Review

1. The DDC needs to have a voltage reference of +4.096V. Please use REF3040 as recommended in the datasheet with the appropriate buffering. The REF3025 used is a fix voltage reference of +2.5V and is not the correct voltage reference.
2. There should be placeholders in different locations for several AGND to DGND shorts connection in the design, either with zero ohms resistor or a ferrite bead, for fine tuning and noise optimization. Please refer to datasheet Figure 36 for reference and guide.
3. There is probably no need to have 10uF on every IC on the design.
4. The buffers (74LVC245AD) are probably not needed if the CPLD controller is placed close to the DDC. A place holder for the buffer can be added if there is a concern. The buffer can be bypassed if it proves that the buffer is not needed. This will save the BOM cost.
5. If there is a jumper option to connect the output of one DDC (DOUT1) as the input for a neighboring DDC (DIN0), then it may be useful to have the option to connect DIN0 to ground (in case it is not connected to DOUT1).
6. The PD diodes connection to the DDC channel inputs can be optimized in the schematic and layout to minimize cross trace and to reduce the number of PCB layers.
7. In the most sensitive gain settings, the parasitic capacitance of the input traces matters, so, if shielding is used (which may be needed on that environment to reduce interference) then a thicker board can be used and the ground layers can be placed further from the signal layers.
8. Typically, the photodiode (PD) cathodes must be connected to ground. So there is no need to place any capacitors to GND on the PD cathodes unless the plan is to apply a negative voltage to the PD cathodes. In such a configuration, check with TI for further support.

Layout Review

1. Option to have the chassis either connected to AGND or DGND with short jumper or have it totally isolated.
2. It is good to have no overlap of digital and analog at all layers.
3. Increase the number of short jumpers between AGND and DGND. Distribute them throughout the board to be able to optimize the design with the right short position later.
4. Make sure the electronics is shielded from direct and scatter x-rays.

5. In an ideal case, from the DDC perspective, it is possible to have the layout in 4 layers. As an example, the EVM PCB layout uses 4 layers with minimum 5 mil (0.127mm) copper width/spacing and smallest via size hole of 6 mil (0.1524mm). Nevertheless, in line scanner cards with two rows of photodiodes (64+64) stacked along the length of the card/x-ray beam, there may be the need to connect each array of 64 to one DDC264, to set different range/gain (for instance one PD array to 12.5pC FSR and the other to 50pC FSR). In that case, input traces would have to cross on the board which could increase the number of layers. Notice that if in any case, the signal would not exceed 12.5pC, then there is no need to cross the traces which may allow for 4 layers only, saving cost. Also, inside an industrial/security scanner, the environment may be noisy from an electrical perspective (EMC). To reduce interference coupling to the input traces, there may be the need to sandwich these input traces between ground planes (probably either AGND or QGND are fine), potentially requiring more than 4 layers too. This is not clear as based on EM shielding theory, one ground plane close enough/underneath the input traces may be almost as good as “boxing” the input traces between ground planes. Nevertheless, from our experience in the lab, we do use the DDC264 in a shielded box (although this may be more to shield the input connections to the AIB, Analog Input Board, for instance).

6. The combination of parasitic capacitance of the PD and the input traces will affect the device noise performance. Its effect can be easily computed from Table 1 or Figure 17. Notice that the effect of increased noise with input capacitance is accentuated at the higher gain settings (lower ranges). Continuing with the discussion on the number of layers required, placing a ground layer close to the input traces (underneath or boxing them) will increase the parasitic capacitance. To reduce this effect, a thicker board can be manufactured increasing the distance between layers (hence reducing the parasitic capacitance). For the same reason, designing the board to be able to apply two different gain settings, increases the length of the input traces, effectively increasing the capacitance, so, it better be avoided especially if signal levels across the whole array fit within one range setting. Regardless, all these are simply general statements to take into account on the design. A calculation of the input capacitance based on the layout of the board can be done and its effect on noise computed from Table 1 or Figure 17, as mentioned. Differences may be negligible from an input capacitance effect while having a good shielding and the possibility to set two different gains may be much more important.