

**Buttons, Switches,
LEDs**
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DDR III
SHEET 3

FMC CONN
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SHEETS 13

ARRIA High Speed Bank
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SHEETS 16

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SHEET 17

USB
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POWER SEQUENCER
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POWER SUPPLIES
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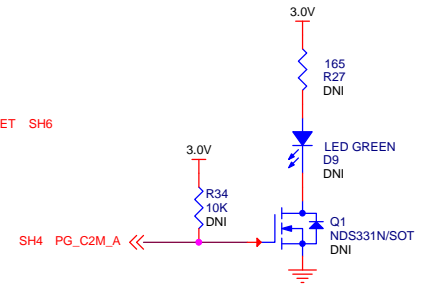
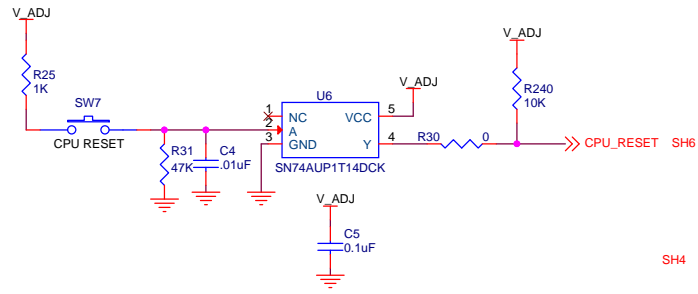
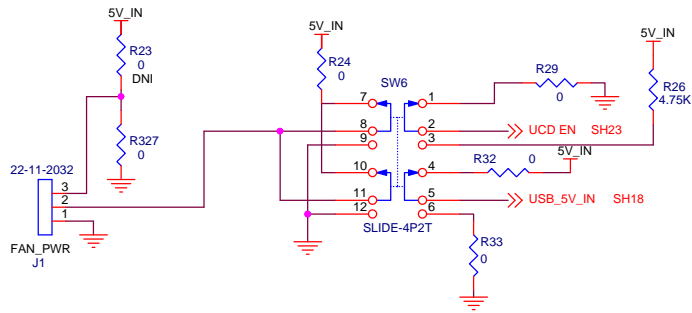
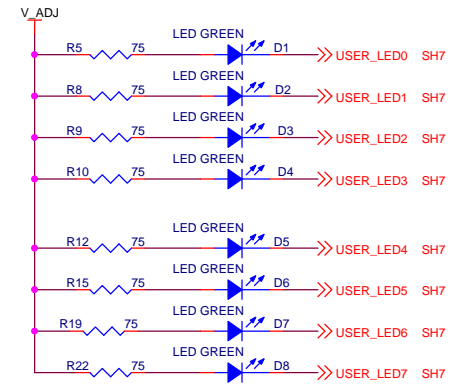
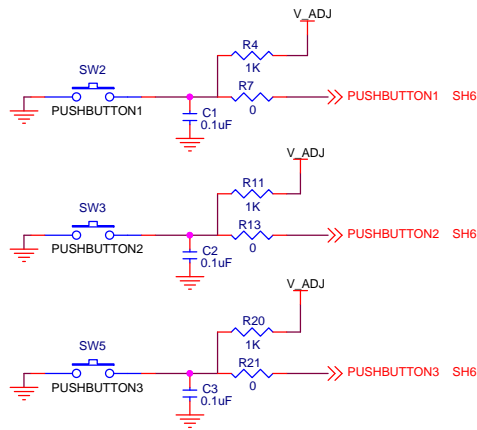
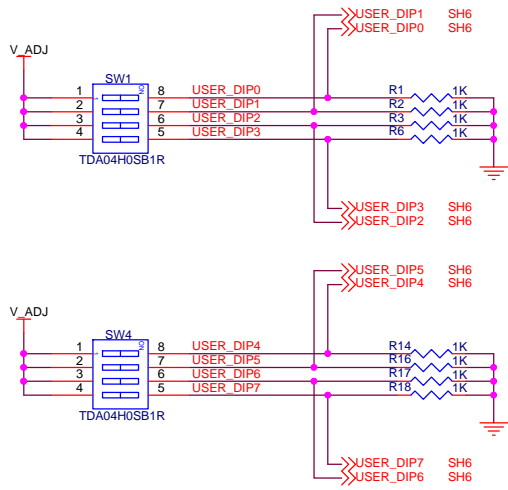
NOTE: DNI = DO NOT INSTALL COMPONENT.



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Drawn: L. NGUYEN	Size B	Document Number	Rev B
Engineer: J. SETON / E. DWOBENC	Date: Friday, August 16, 2013	Sheet 1 of 23	

Buttons, Switches, LEDs

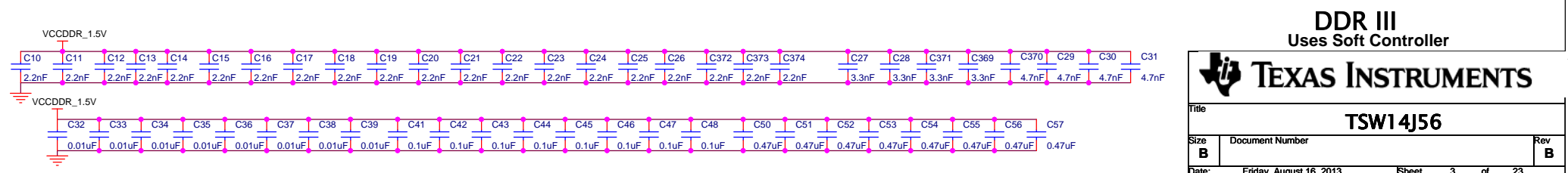
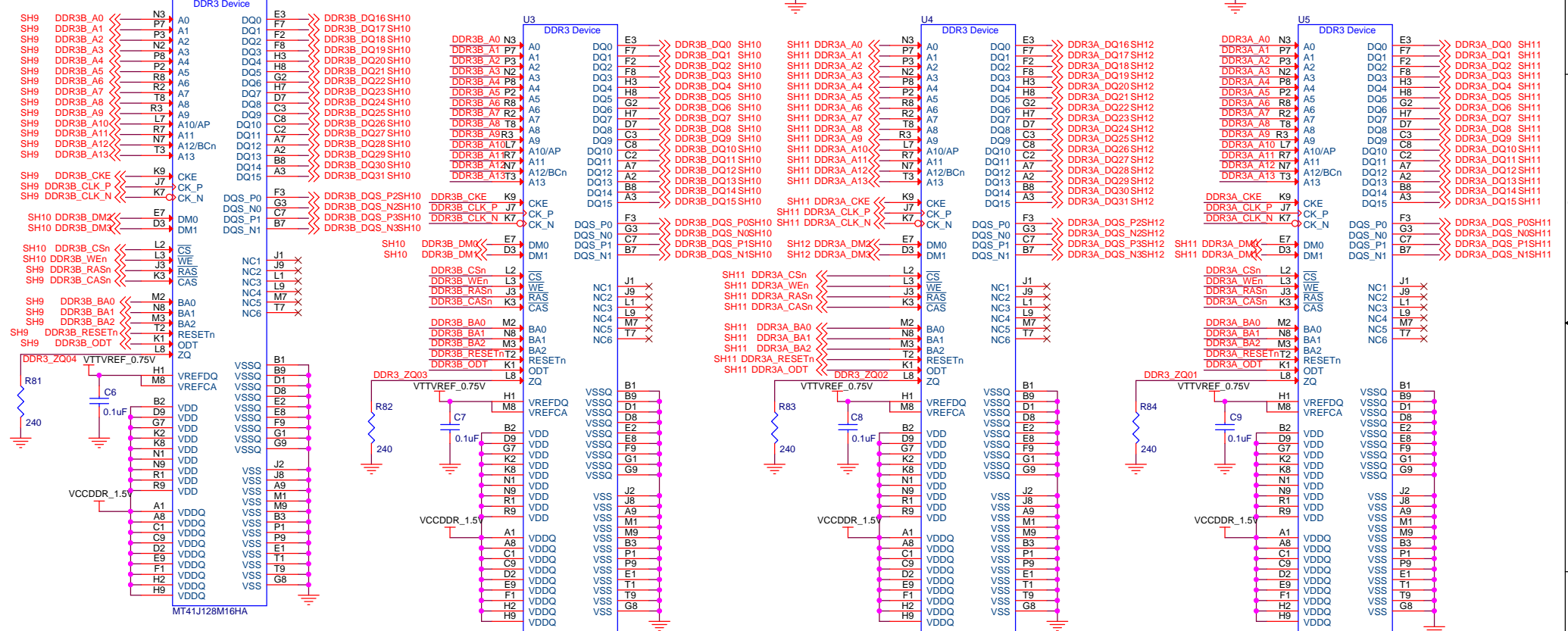
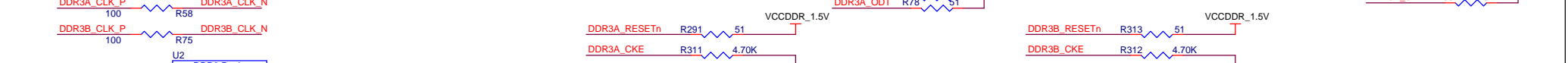
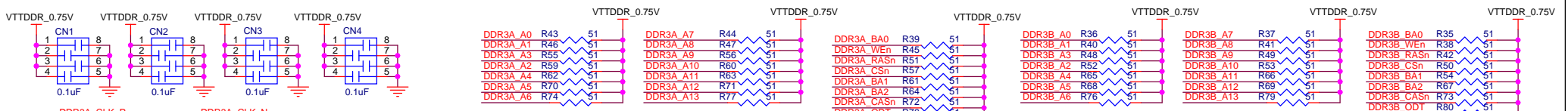


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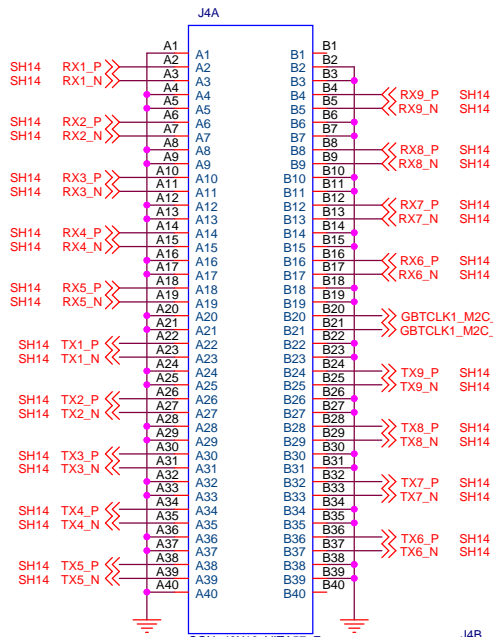
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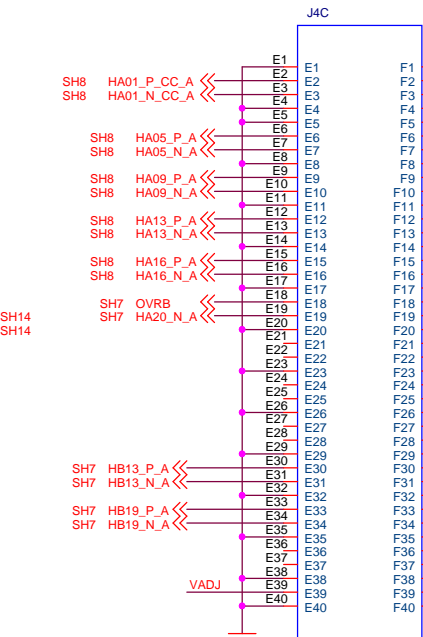
DDR III
Uses Soft Controller



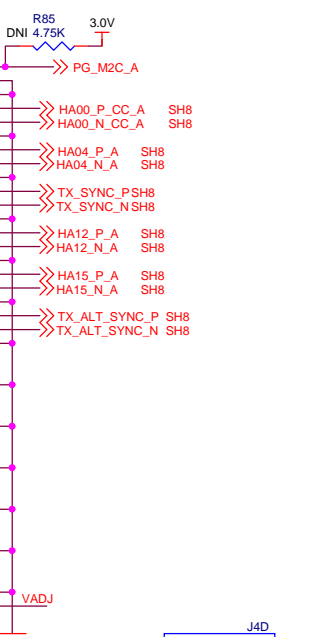
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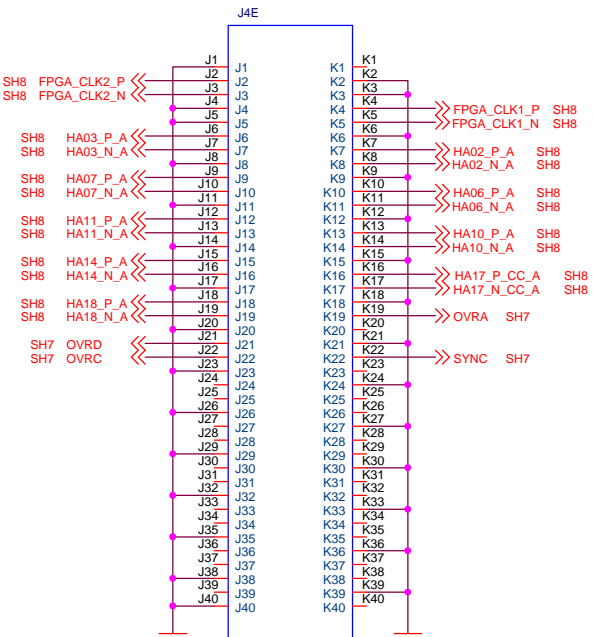
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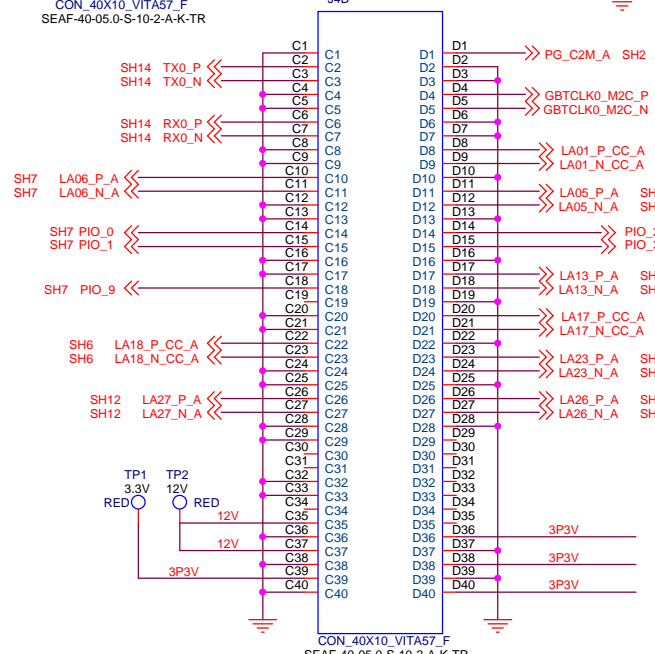
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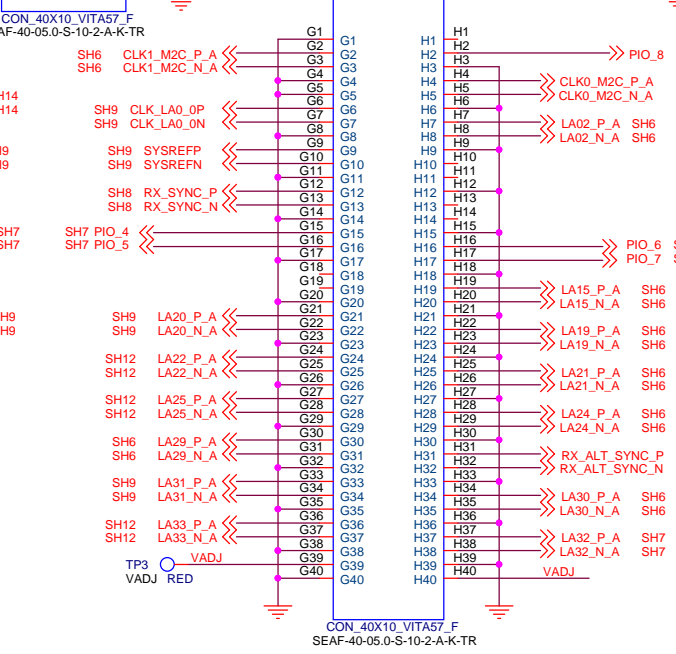
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CON_40X10_VITA57_F
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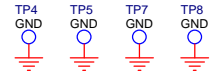
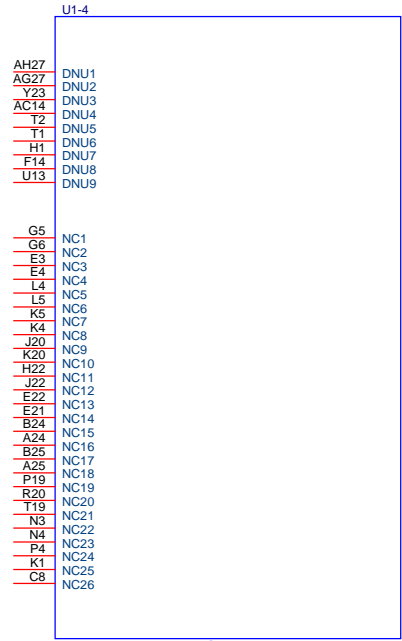
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FPGA=CARRIER
DUT=MEZ
M2C - ADC
C2M - DAC

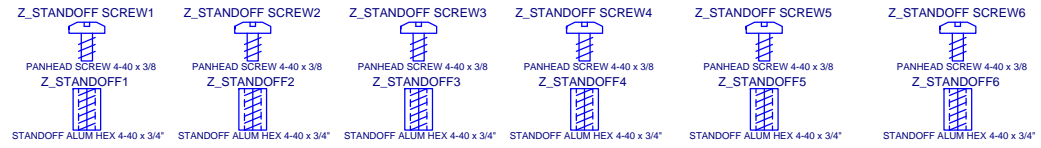
FMC HPC CONNECTOR



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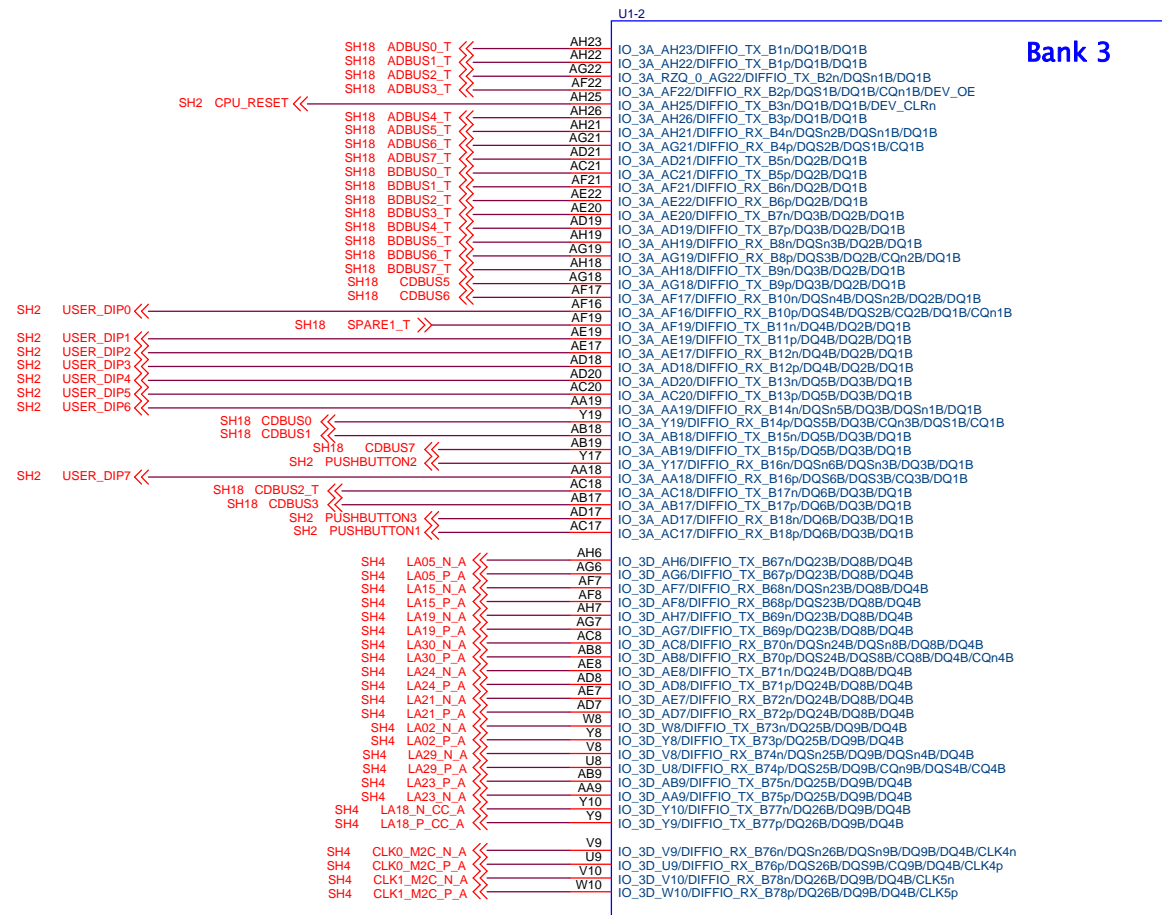
MECHANICAL PARTS



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BANK 3



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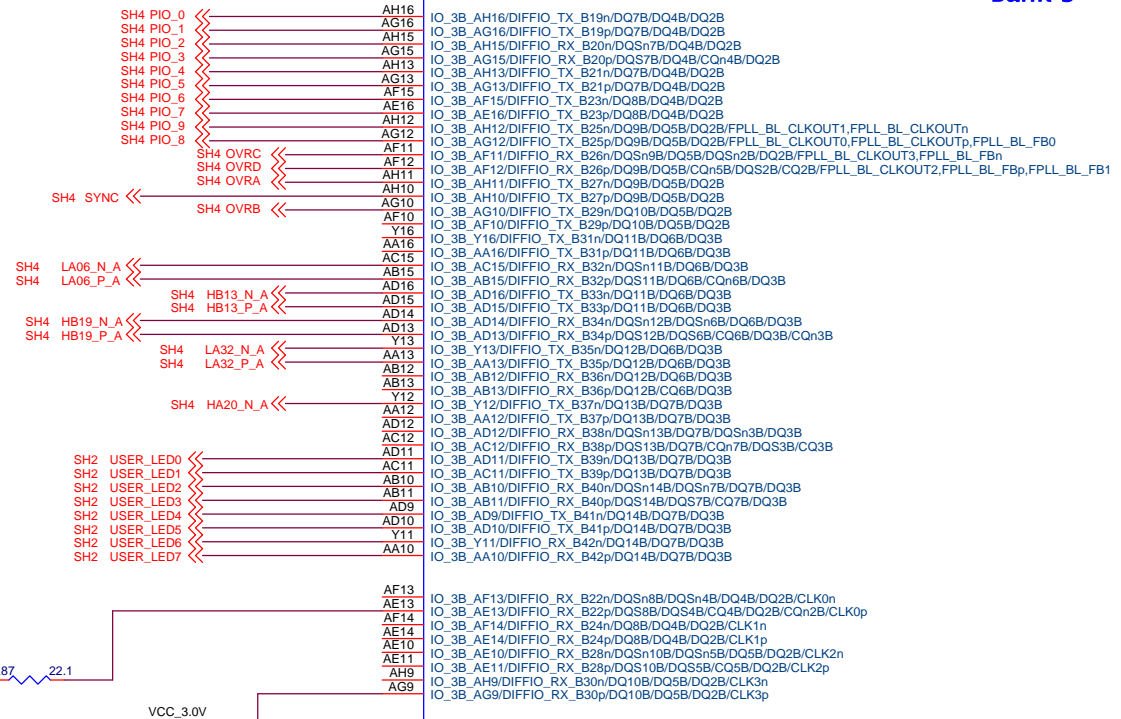
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Bank 3

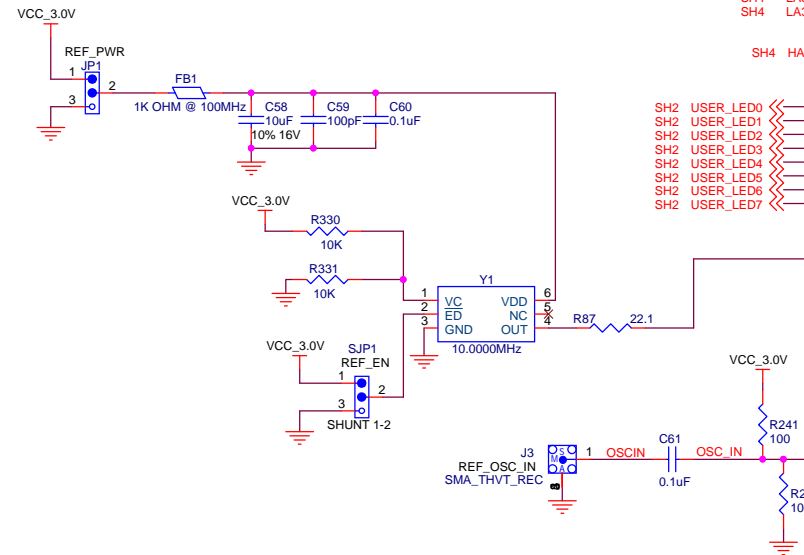


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BANK 3



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FPGA Bank 4

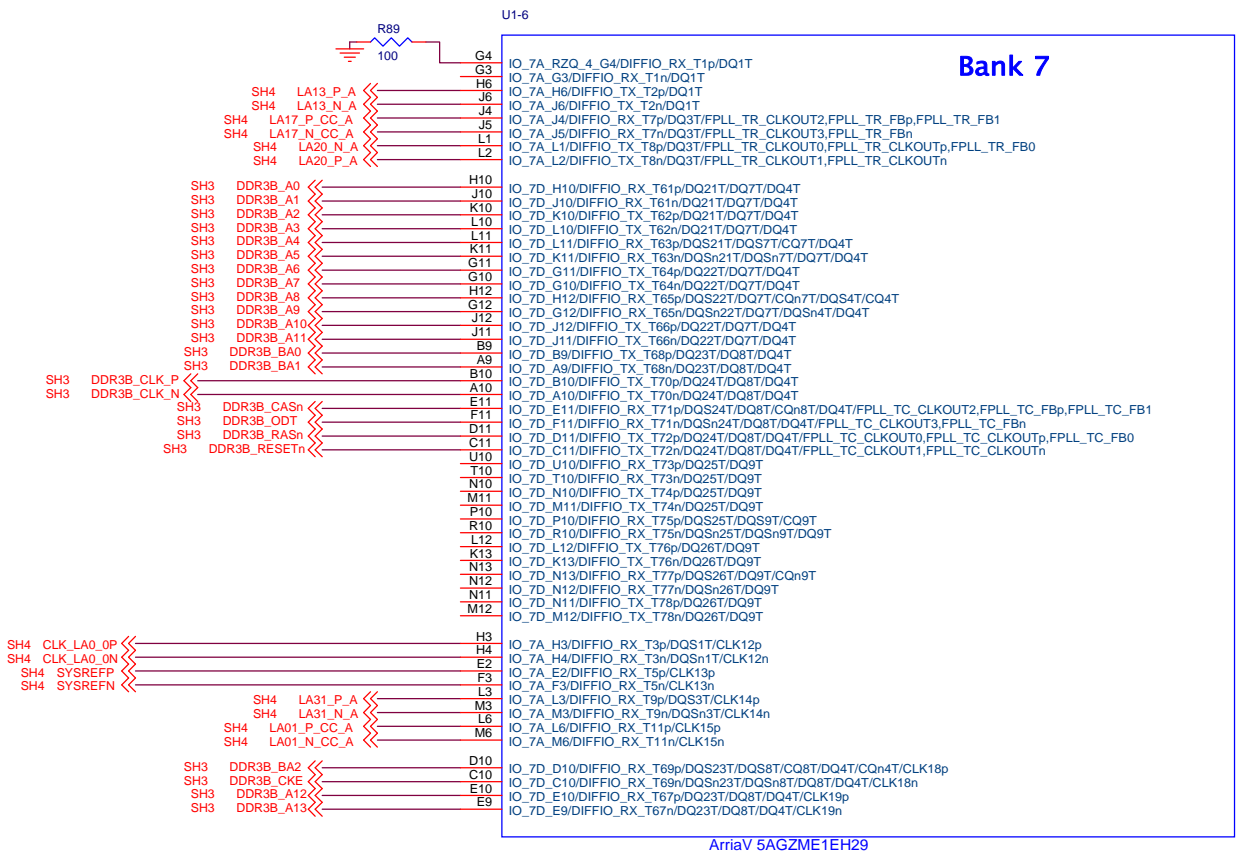
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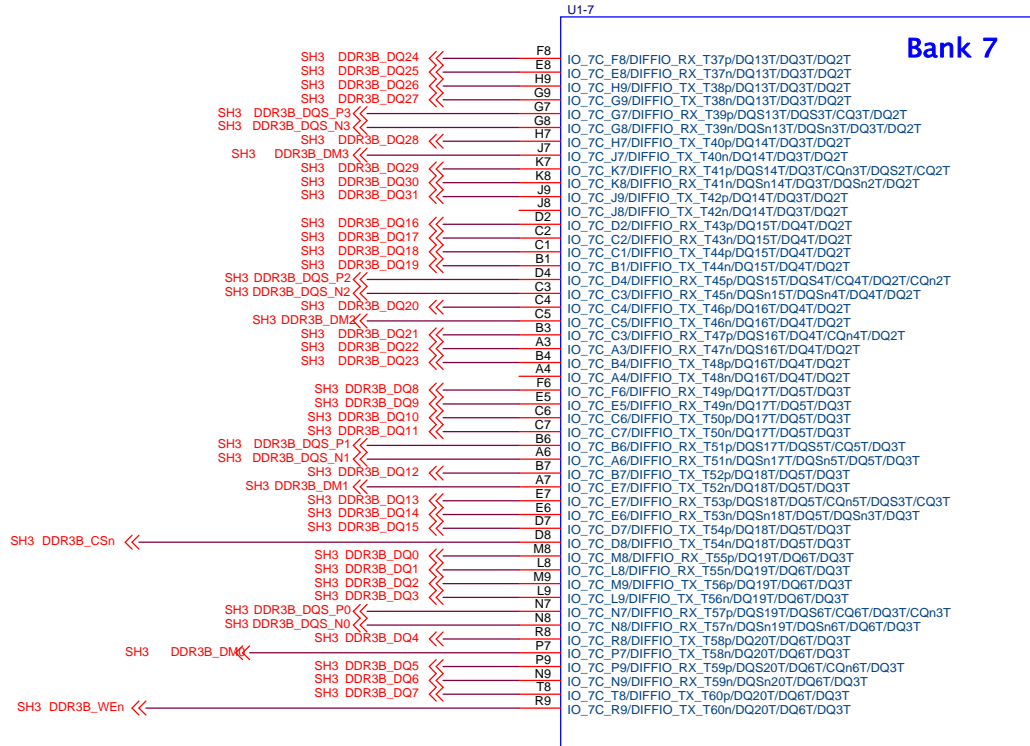
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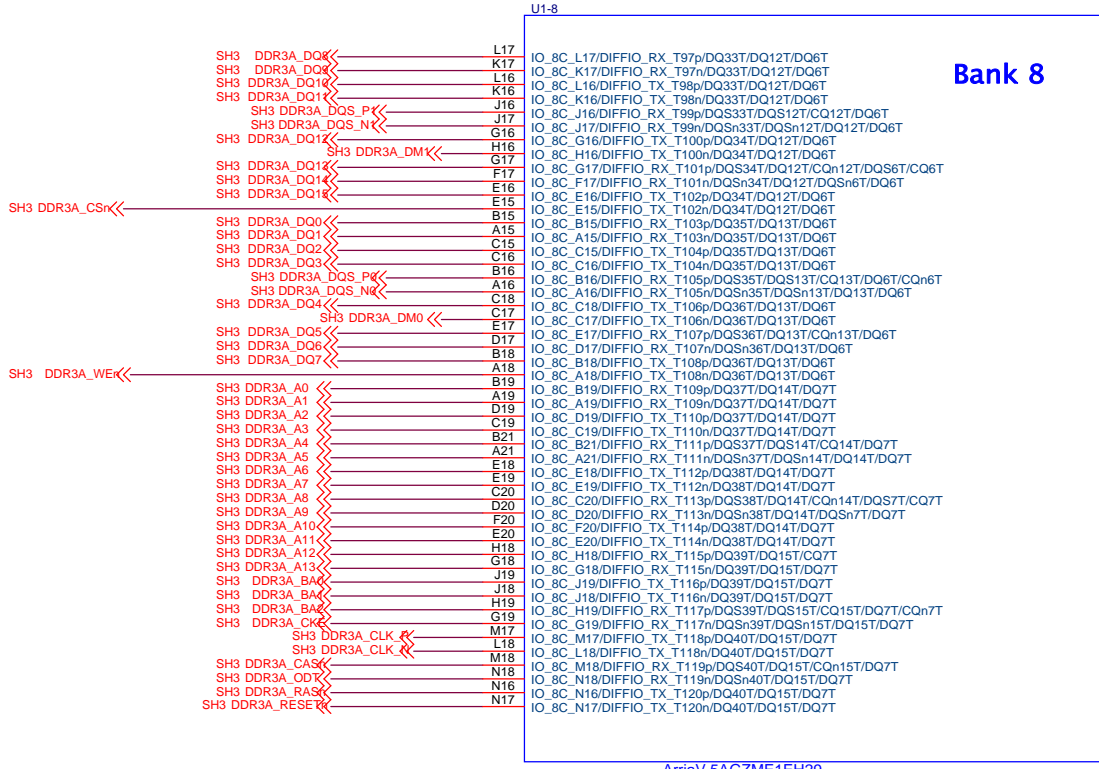
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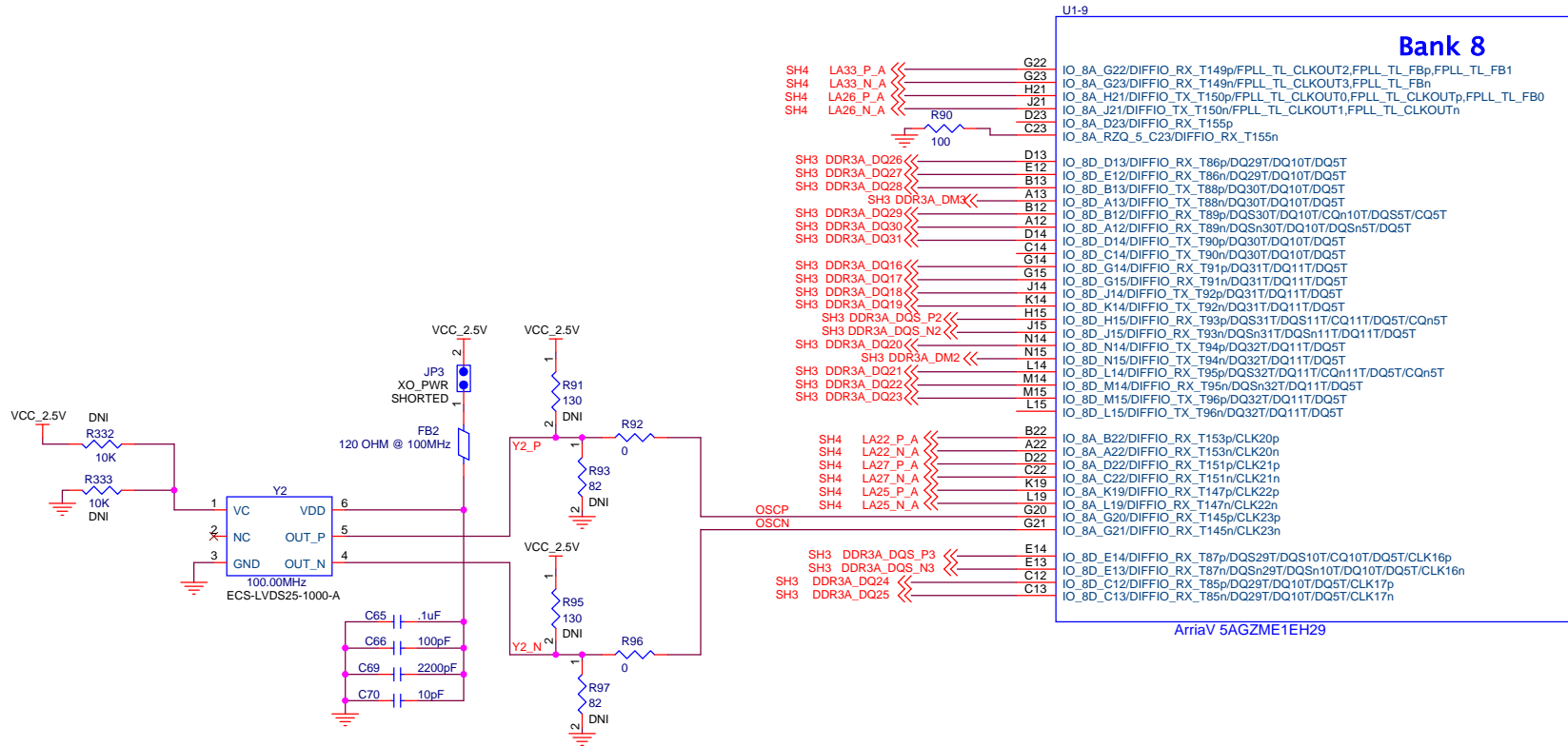
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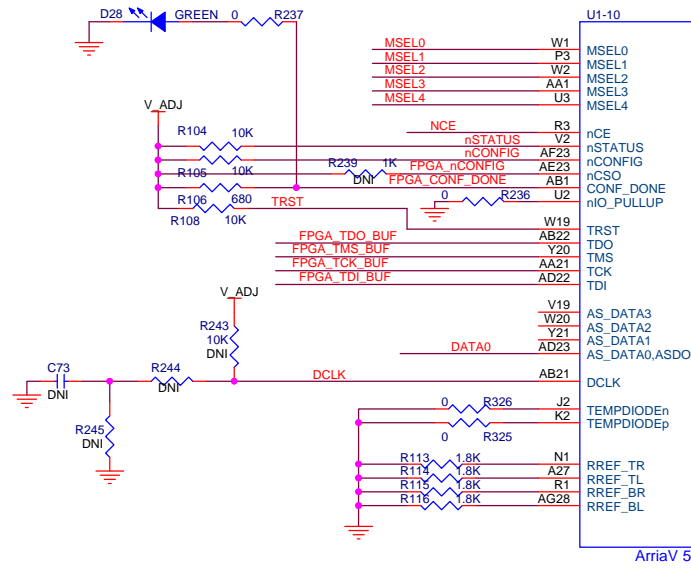
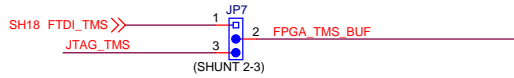
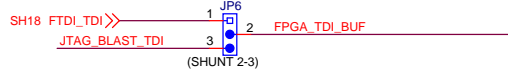
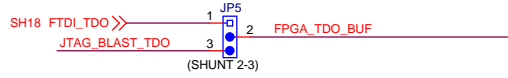
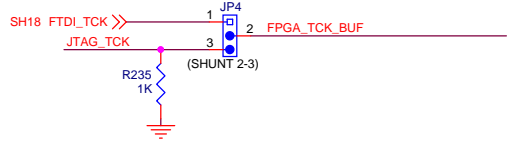
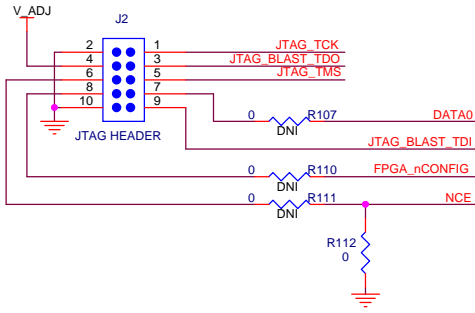
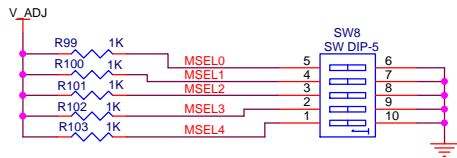
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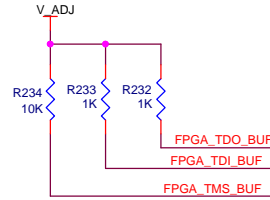
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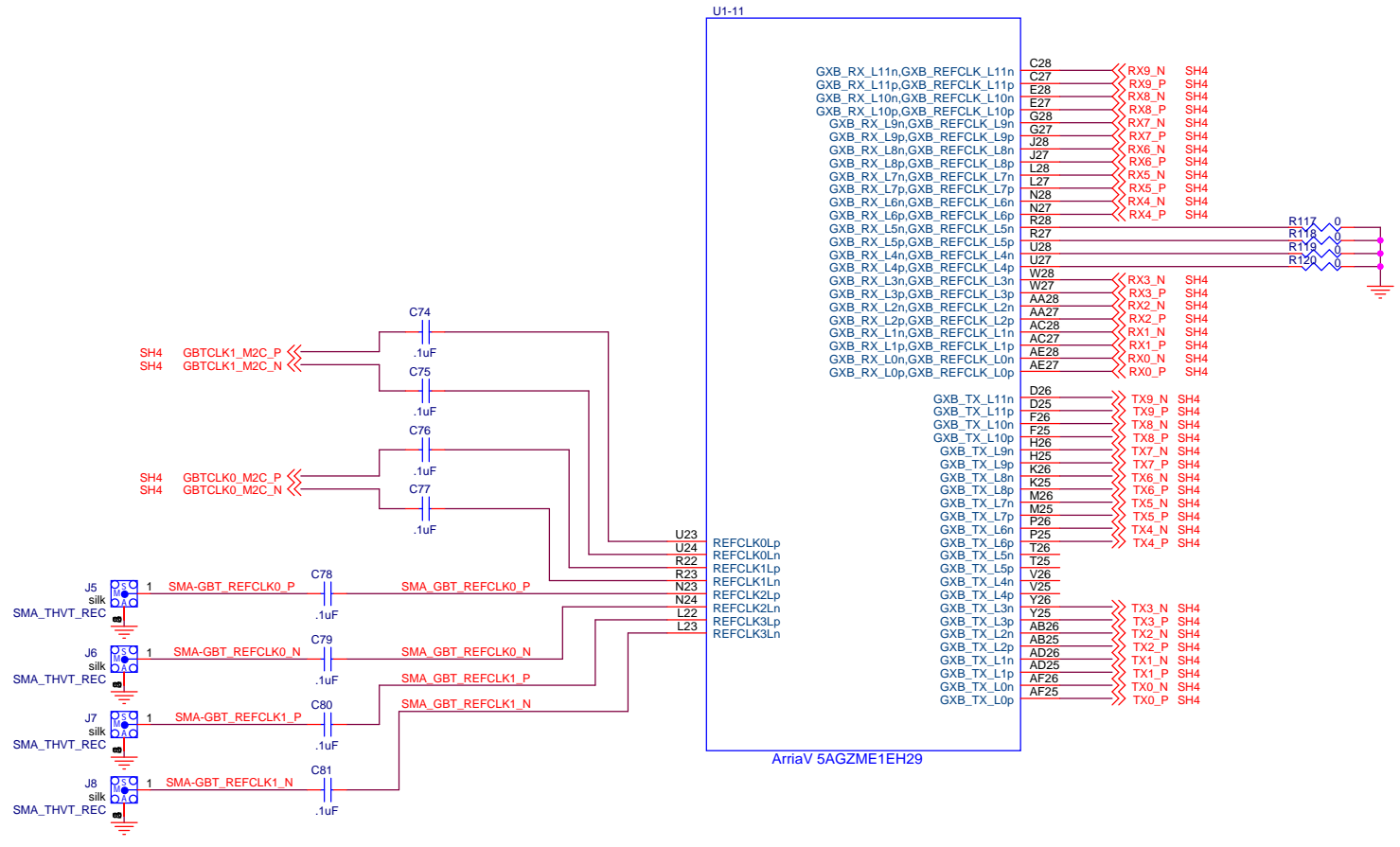
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FPGA CONFIGURATION



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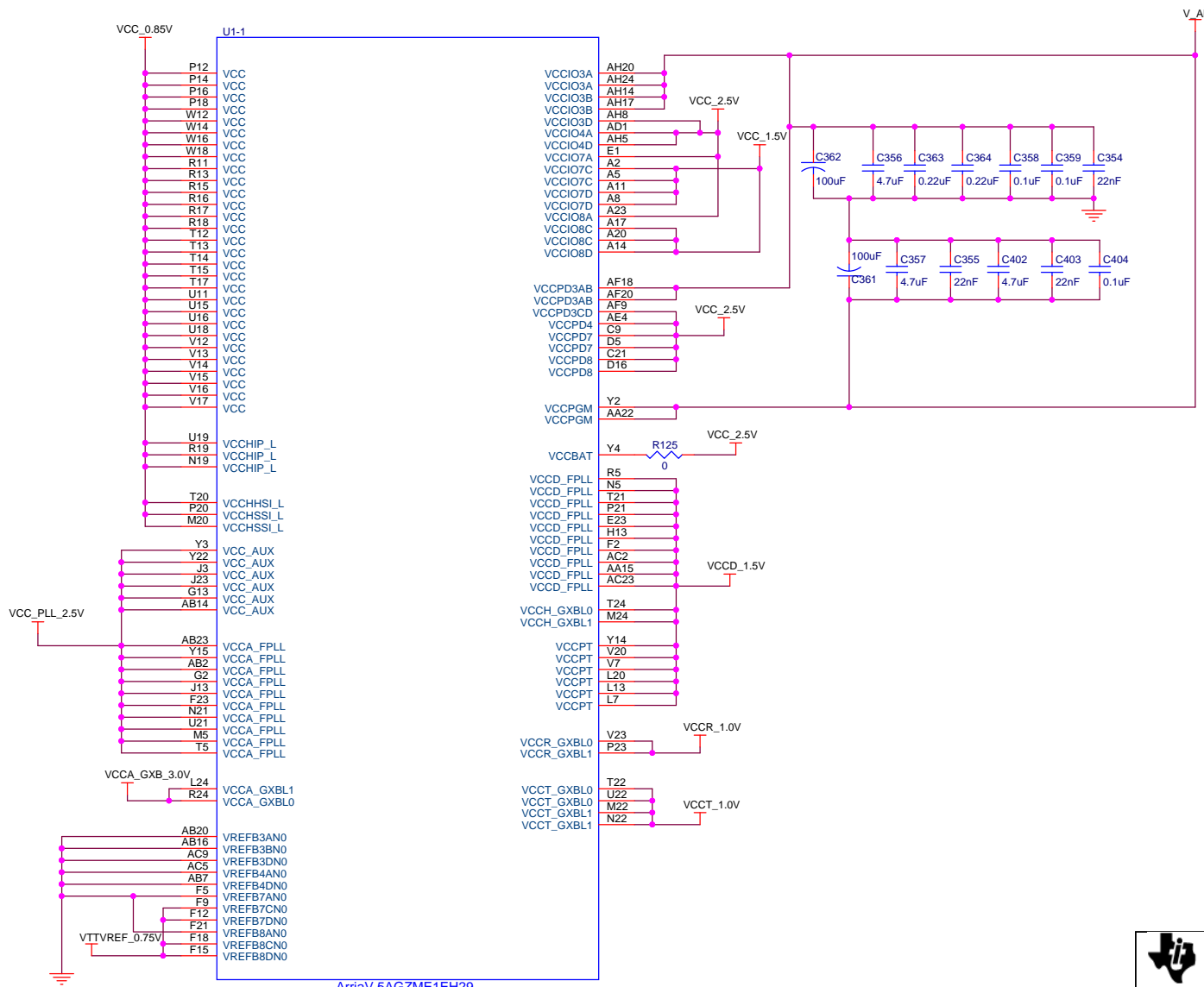
HIGH SPEED BANK

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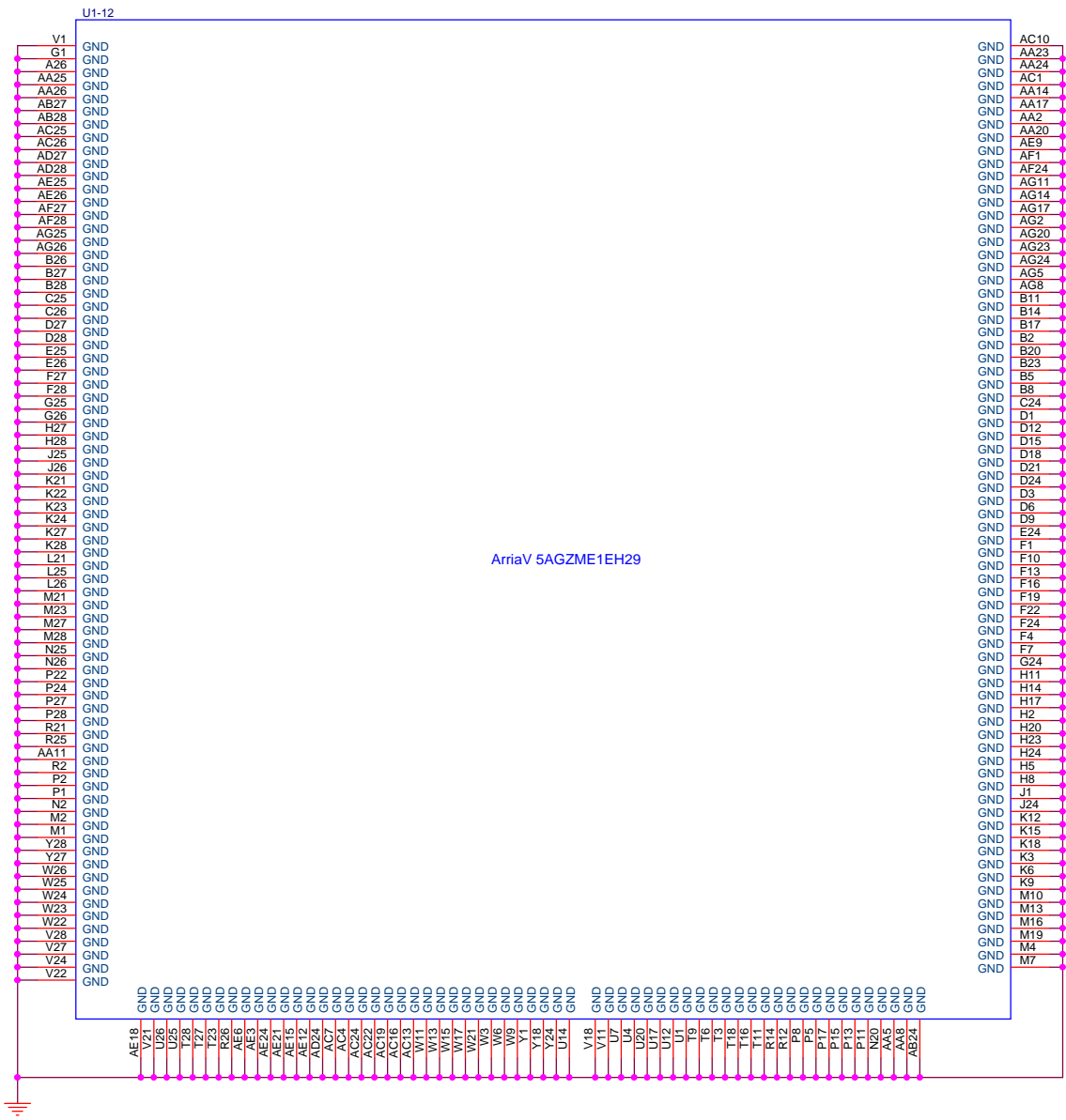


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FPGA POWER



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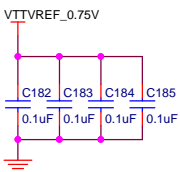
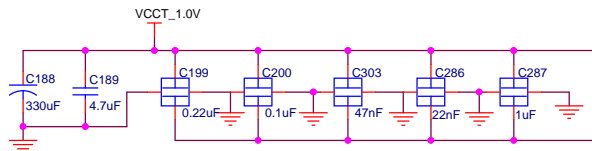
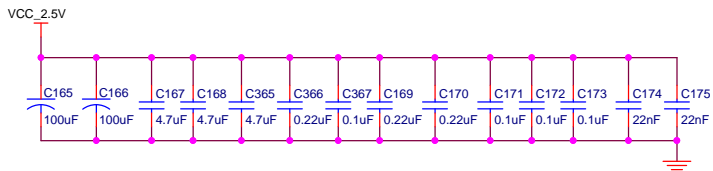
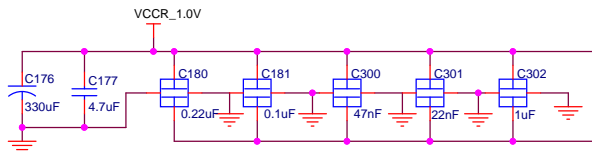
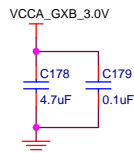
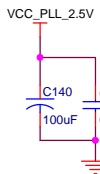
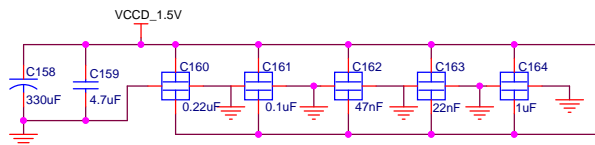
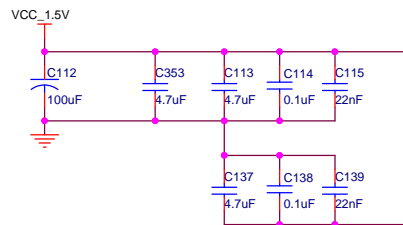
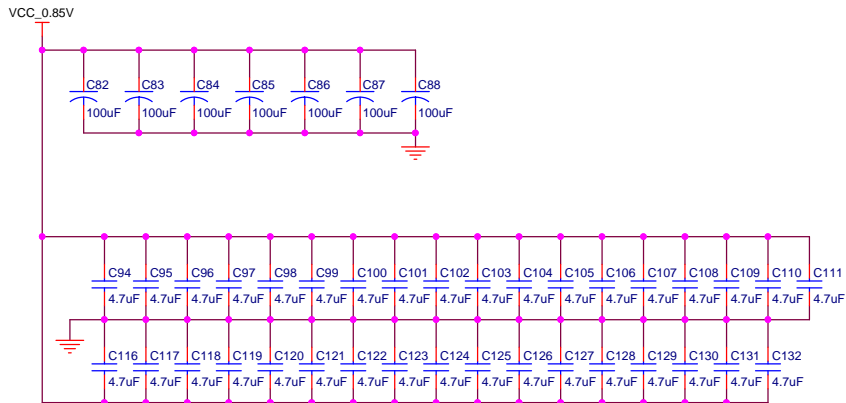
FPGA GROUND

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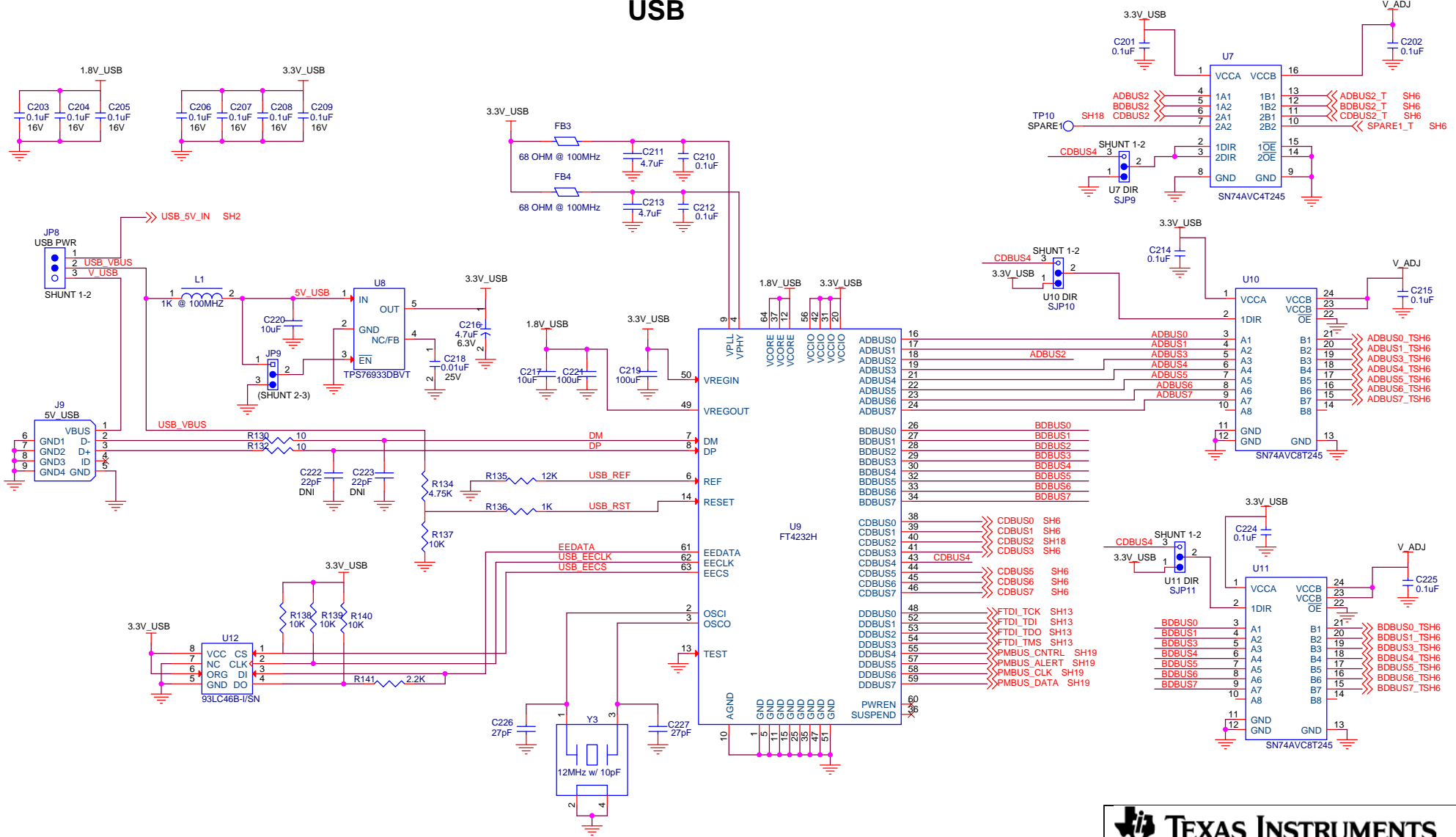


FPGA Decoupling



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USB



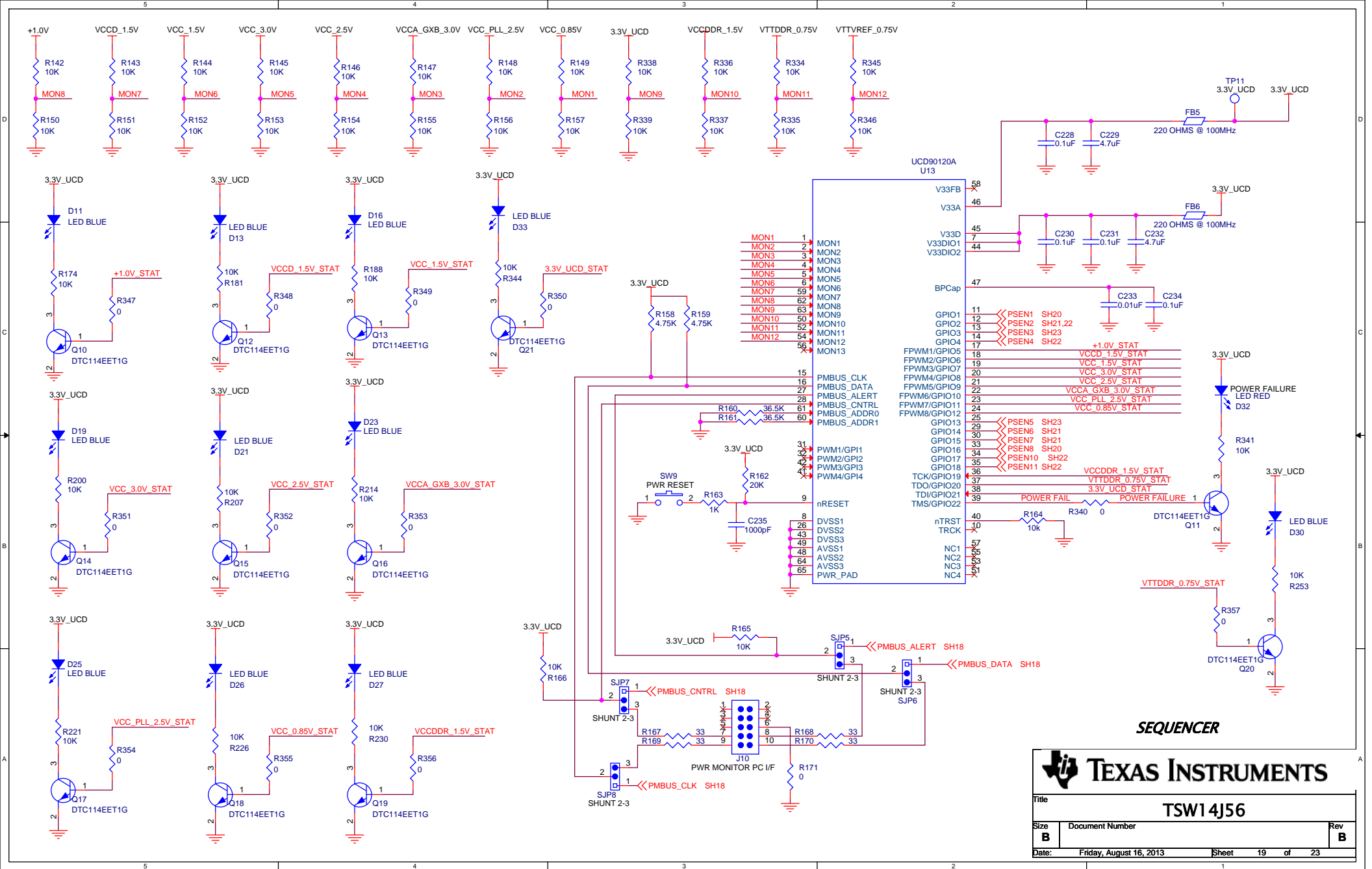
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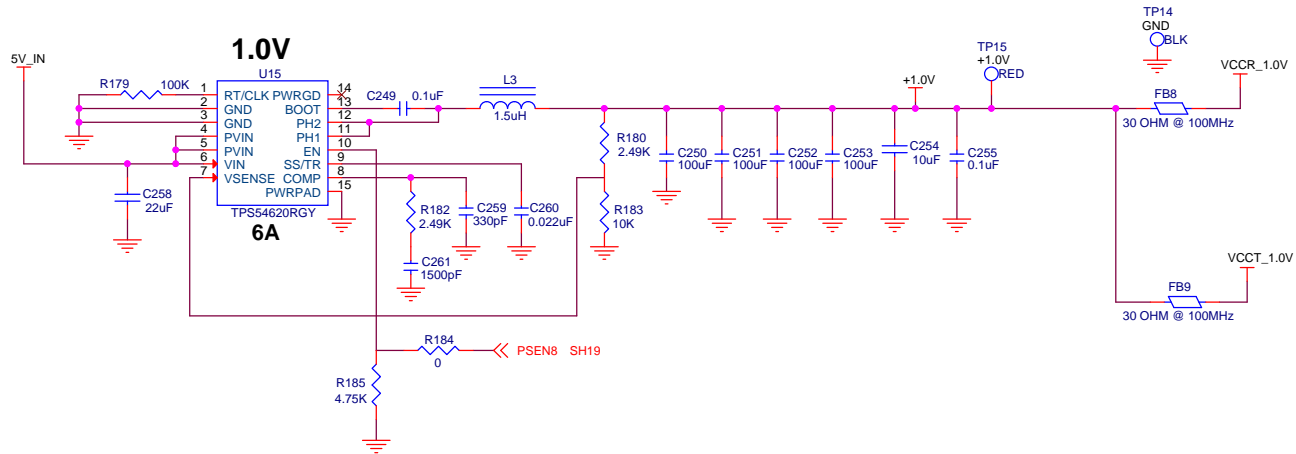
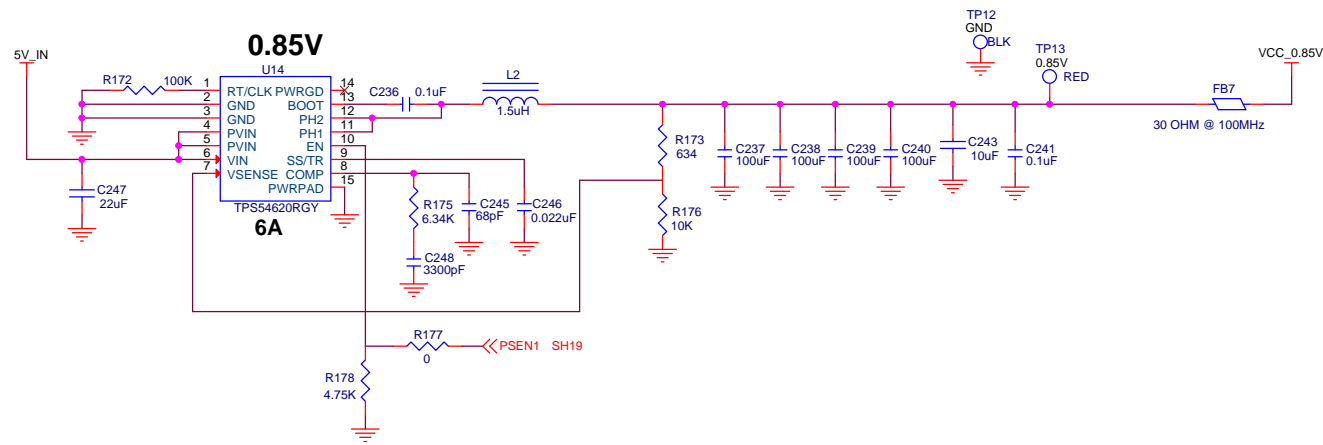
Rev B



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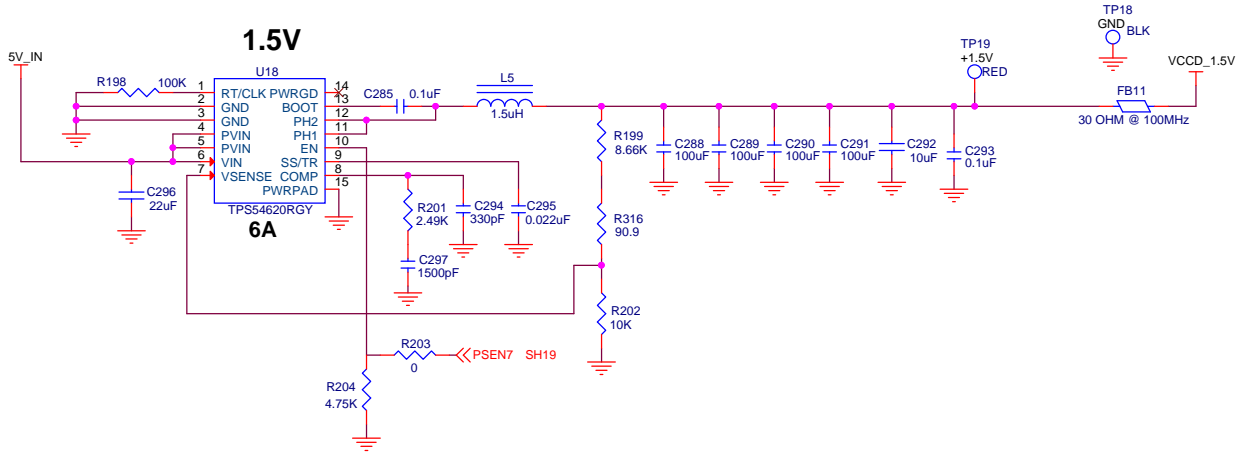
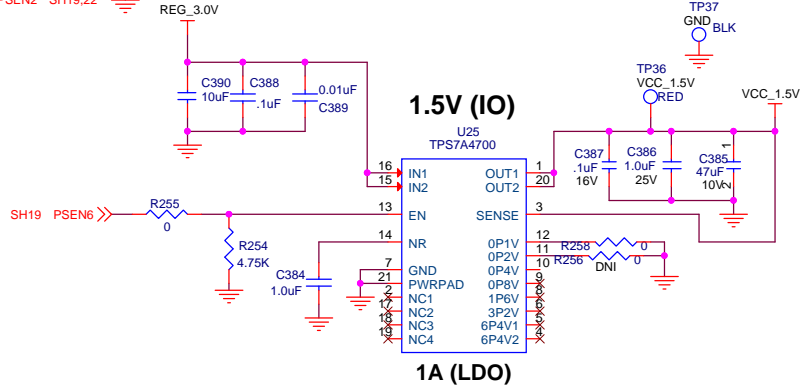
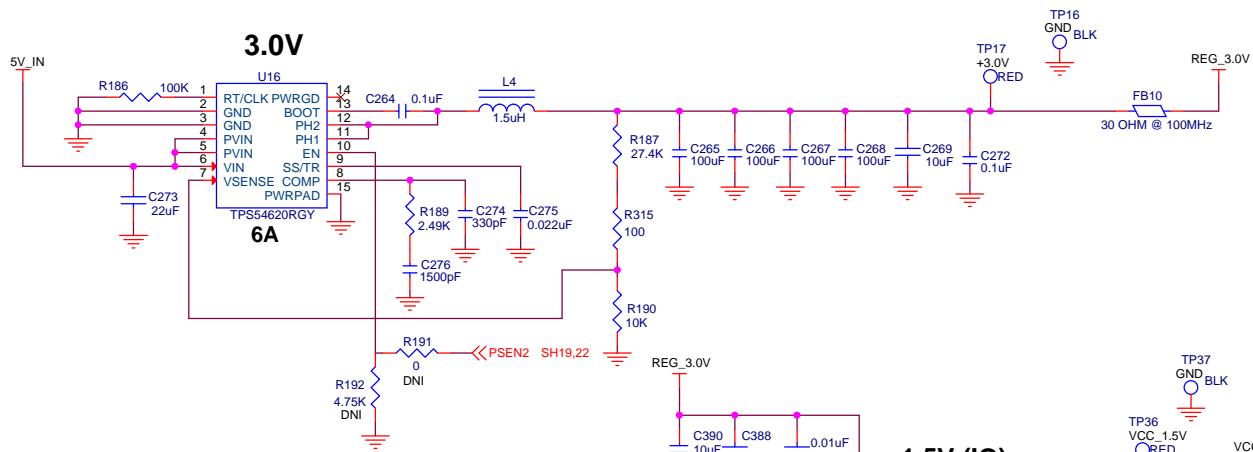
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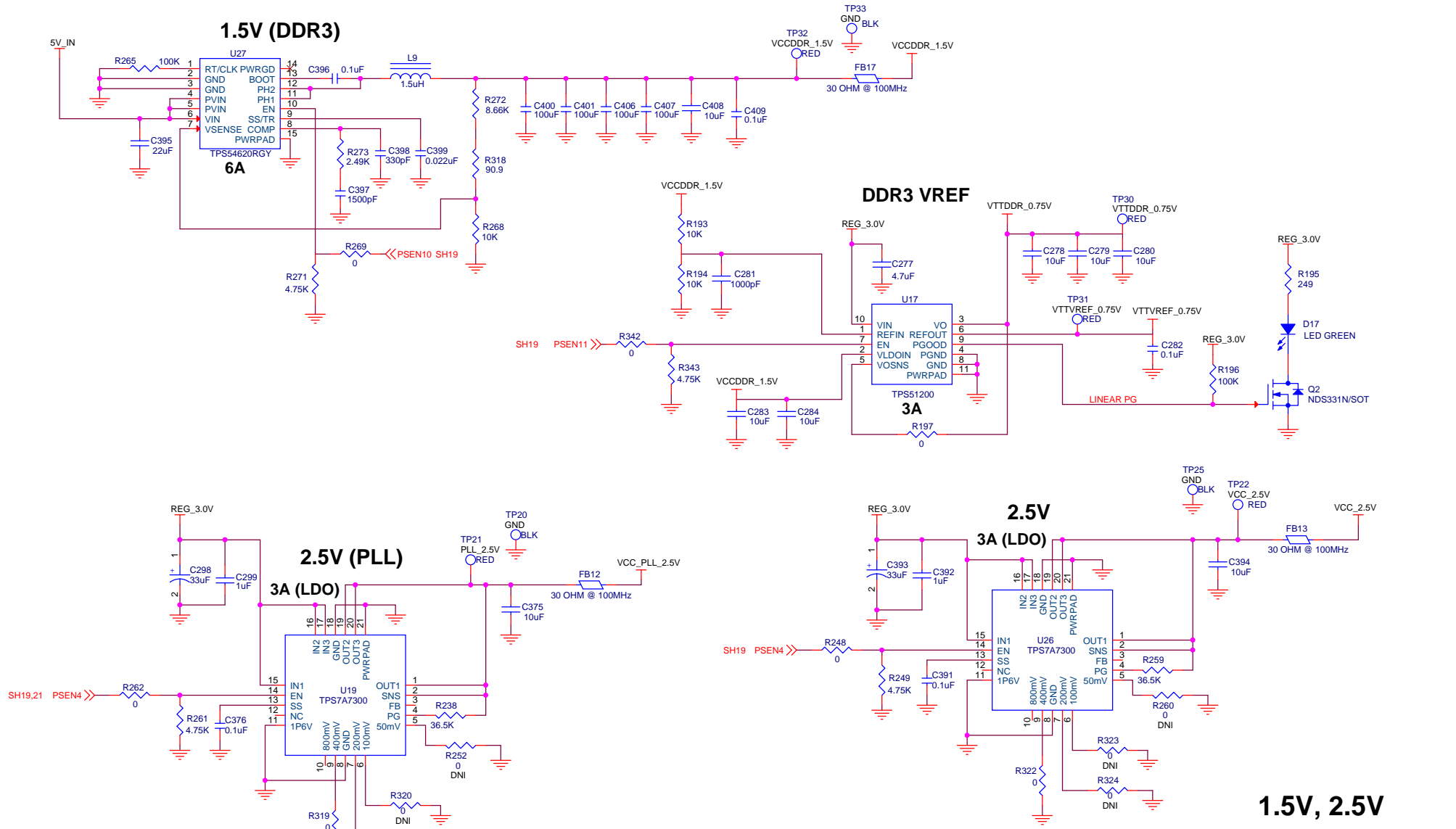
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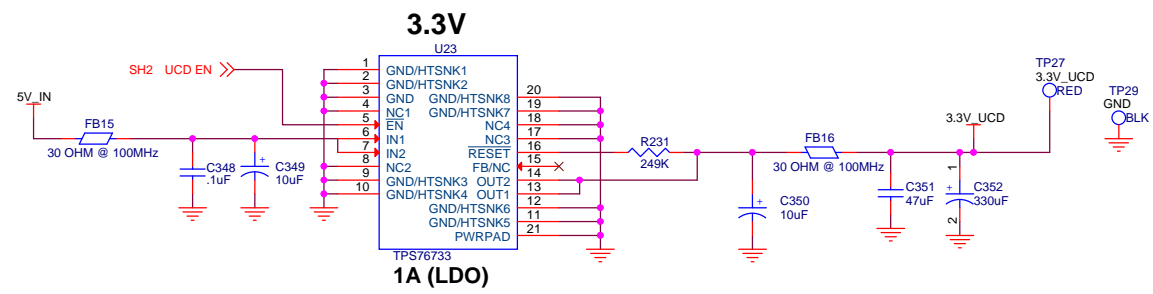
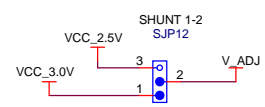
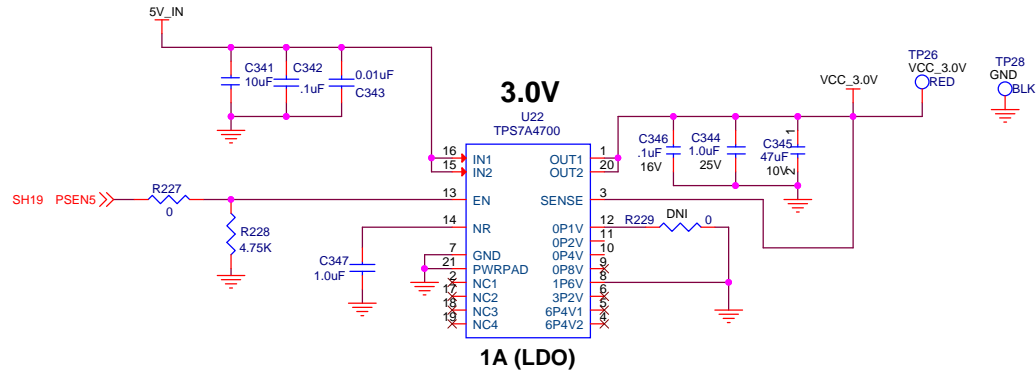
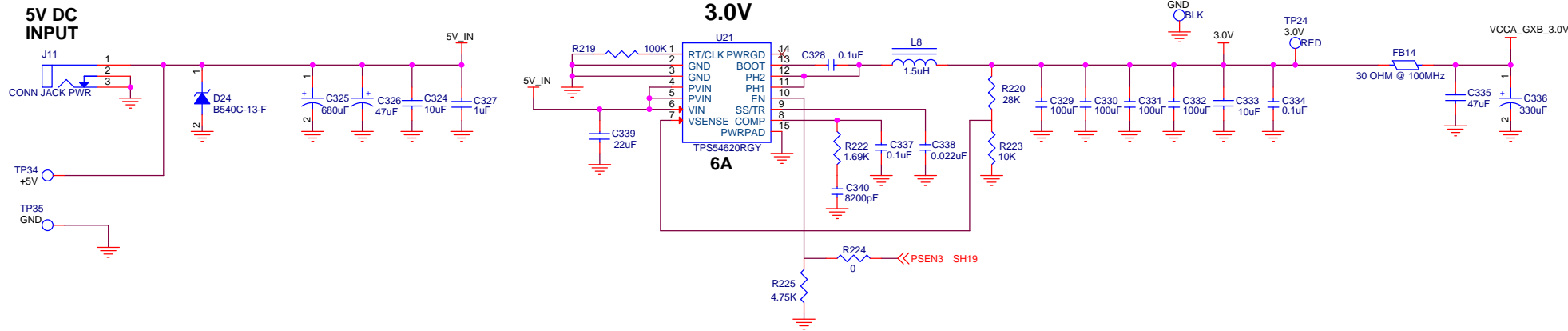
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3.0V, 3.3V

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