

# Setup ADC16DX370EVM with TSW14J10EVM and KC705

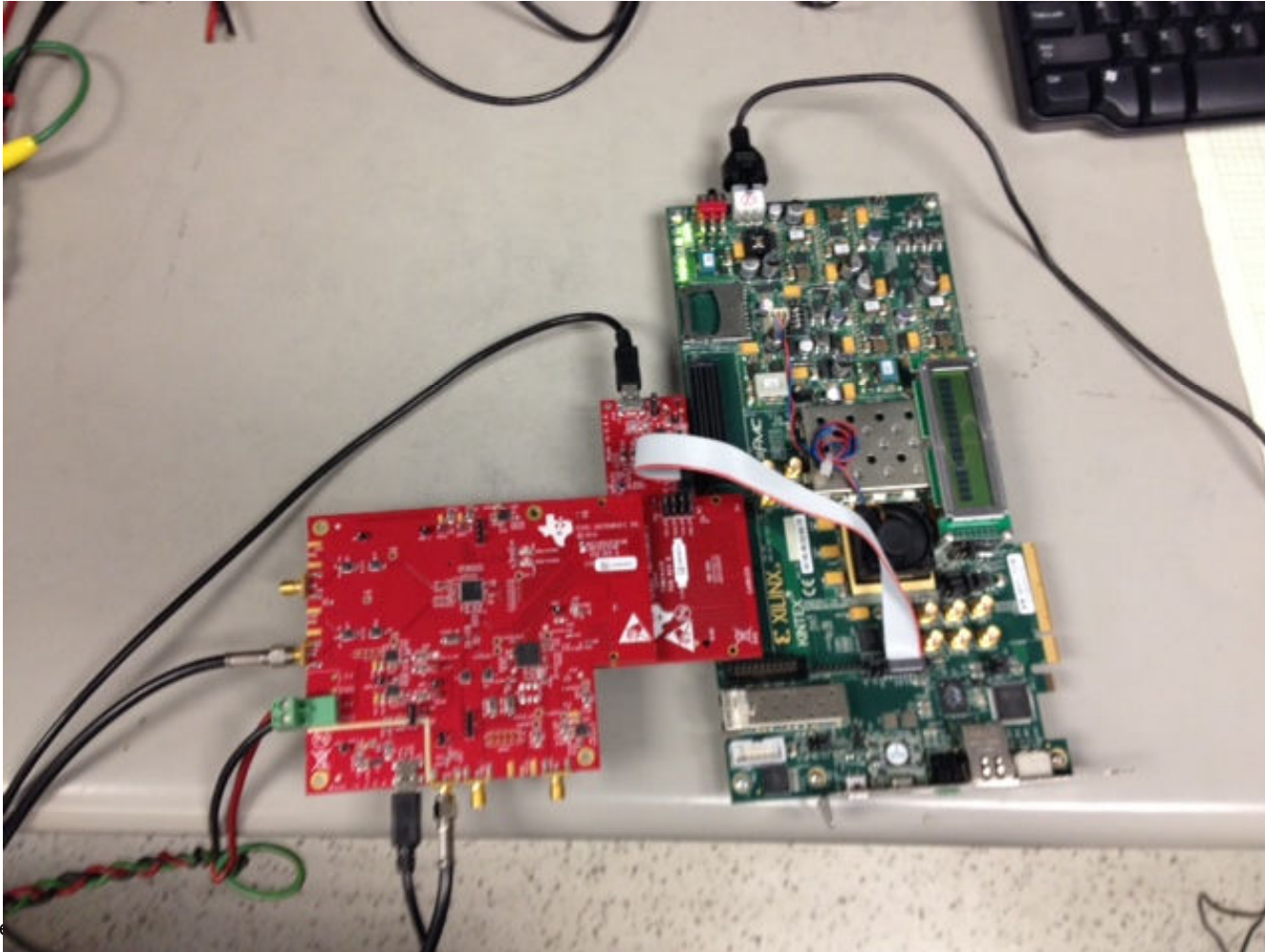
**11/2/2015**

# Notes

- This procedure outlines support for the ADC16DX370EVM TSW14J10EVM and KC705 (or VC707)
- This procedure has been verified with HSDC Pro v4.0

# Procedure

- Connect the hardware together, power up, and apply signals

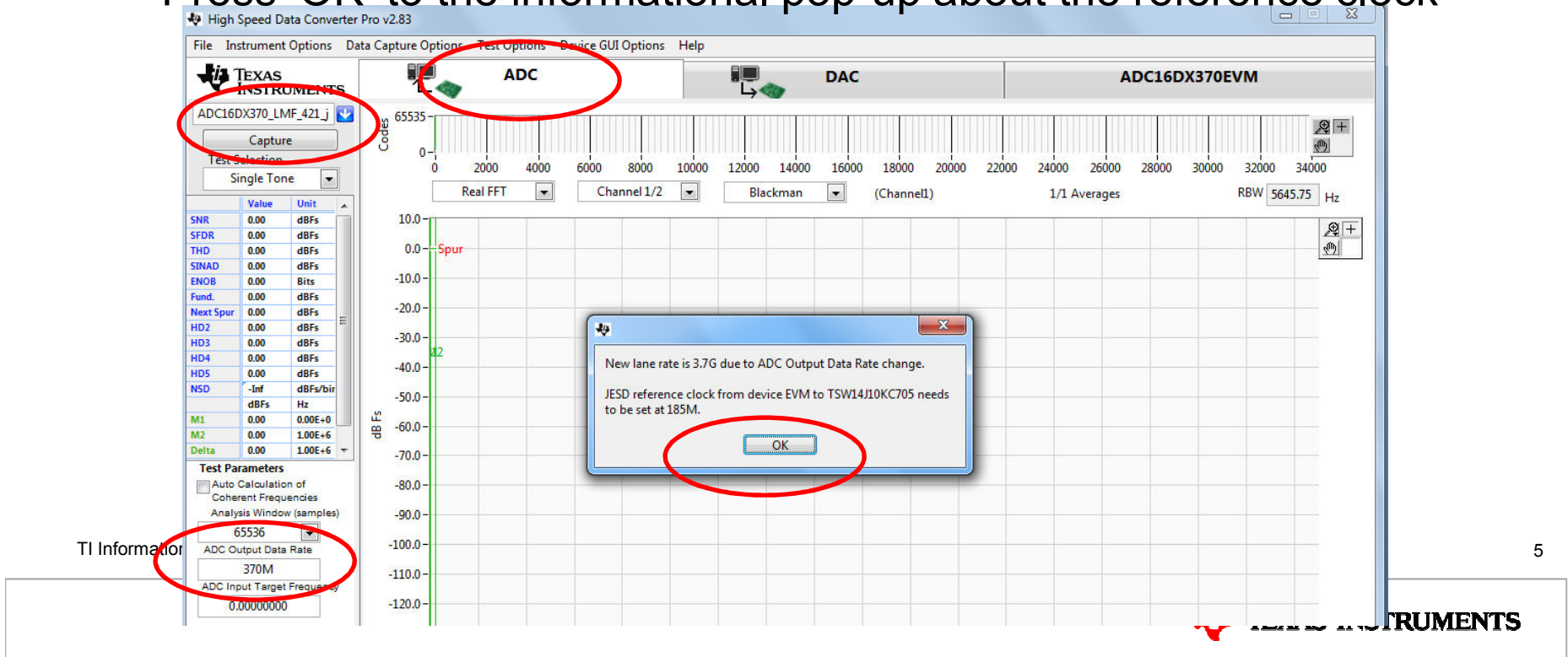


## Procedure (2)

- Install HSDC Pro v4.0
- If using the KC705:
  - Copy the 'ADC16DX370\_LMF\_421\_KC705.ini' and 'ADC16DX370\_LMF\_222\_KC705.ini' files to the following location
  - C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J10KC705 Details\ADC files\
- If using the VC707:
  - Copy the 'ADC16DX370\_LMF\_421\_VC705.ini' and 'ADC16DX370\_LMF\_222\_VC705.ini' files to the following location
  - C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J10VC707 Details\ADC files\

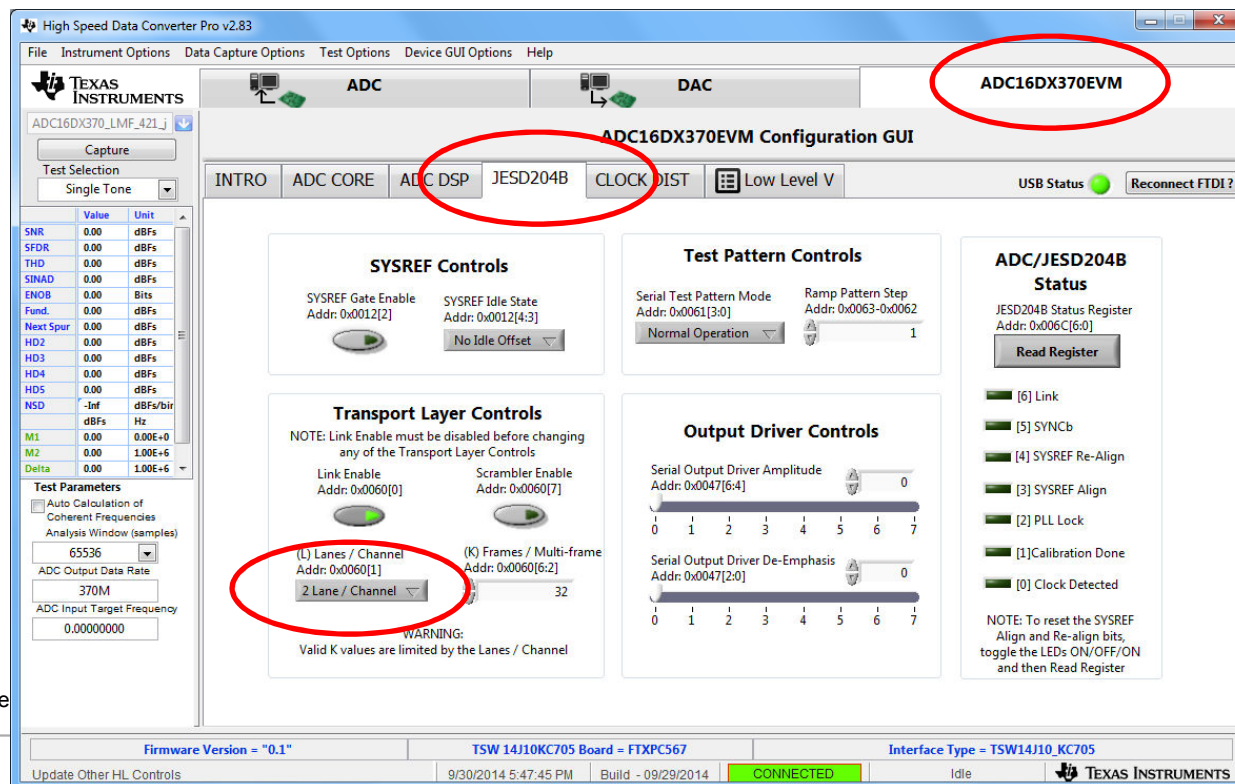
## Procedure (2)

- Open HSDC Pro, select the 'ADC' tab, select the ADC16DX370 device with the proper LMF and OK to update firmware
  - ADC16DX370\_LMF\_421\_KC705 for 2x JESD204 lanes / channel
  - ADC16DX370\_LMF\_222\_KC705 for 1x JESD204 lane / channel
- Enter '370M' (or appropriate value) as the ADC Output Data Rate
  - If this value is 320M or below for LMF=421, then this procedure is invalid
- Press 'OK' to the informational pop-up about the reference clock



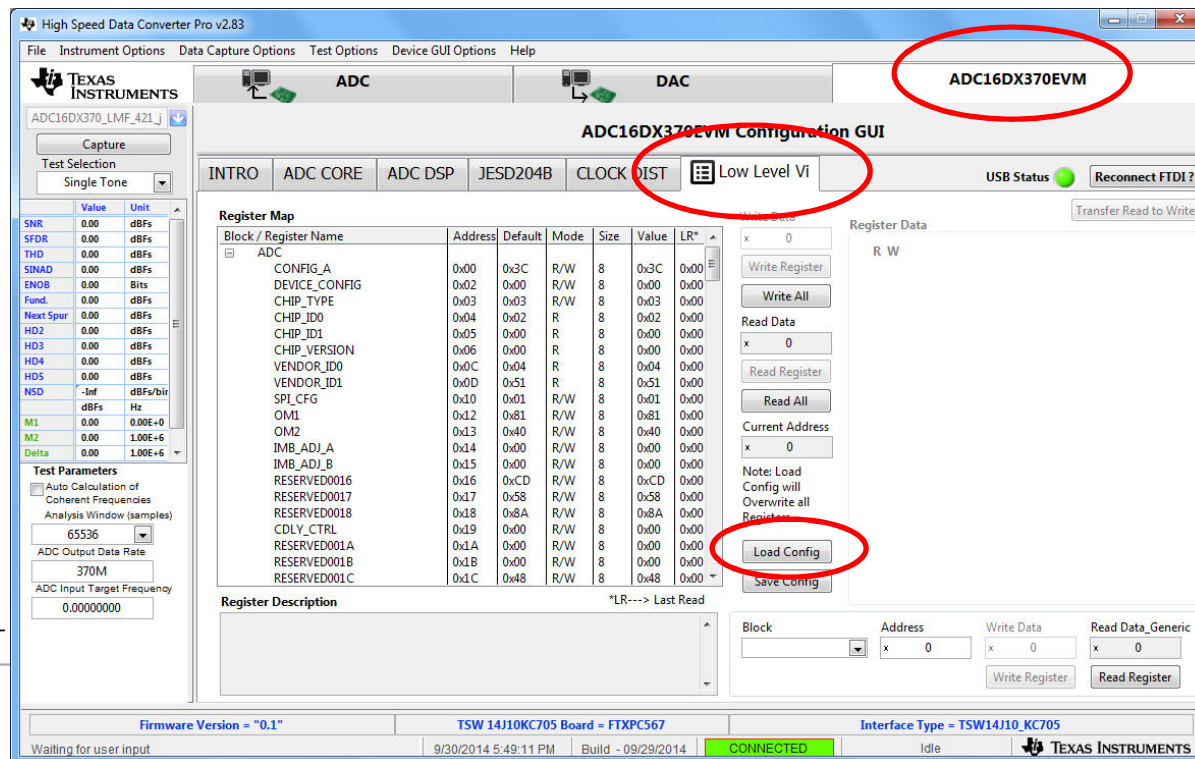
# Procedure (3)

- Click over to the ADC16DX370EVM tab
- Click over to the JESD204B sub-tab
- Correctly set the number of Lanes per Channel
  - For LMF=421, set the Lanes/Channel = 2
  - For LMF=222, set the Lanes/Channel = 1



# Procedure (4)

- Click over to the ADC16DX370EVM tab
- Click over to the Low Level V sub-tab
- Press the 'Load Config' button
- Select the proper LMK04828 config file and press OK
  - LMK04828\_config\_TSW14J10\_KC705\_ADC16DX370\_LMF\_421.cfg for LMF=421
  - LMK04828\_config\_TSW14J10\_KC705\_ADC16DX370\_LMF\_222.cfg for LMF=222

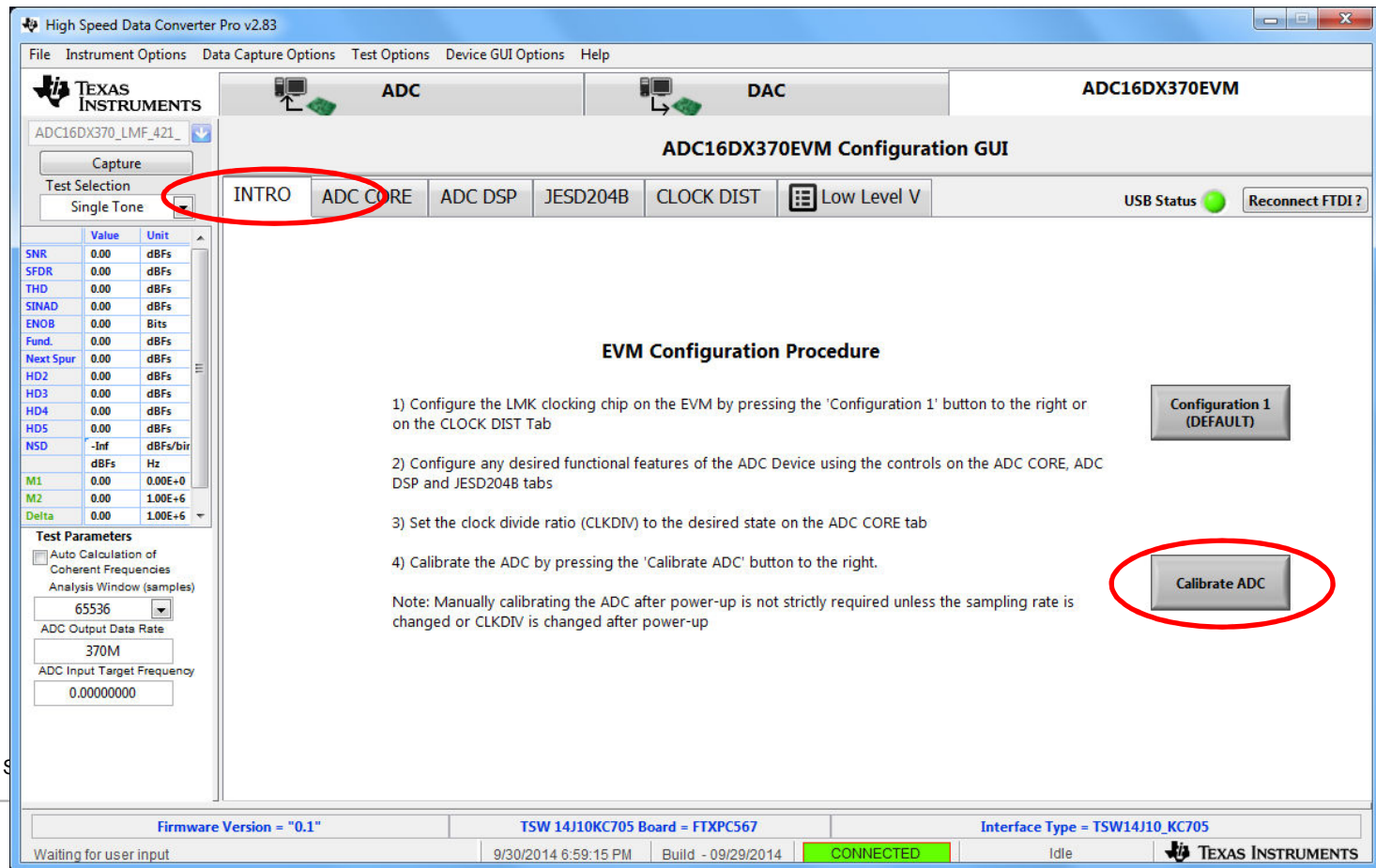


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# Procedure (4)

- Click over to the INTRO sub-tab
- Press the 'Calibrate ADC' button



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## Procedure (5)

- Click back to the 'ADC' tab
- Capture data
- After capturing data for the first time, the LED status on the KC705:
  - LED7: Blinking
  - LED6: Blinking
  - LED5: Blinking
  - LED4: Off
  - LED3: ON
  - LED2: Off
  - LED1: ON
  - LED0: Off

# Notes

- Using the TSW14J10EVM + Xilinx Reference board requires an extra clock from the EVM's LMK device that is not required when capturing data with the TSW14J56EVM
  - If this clock is not active, or is the incorrect frequency, bad data captures will result with shifted/incorrect bits
  - DEVCLK10 on the LMK04828 must be LVDS active with a frequency of  $F_s/4$  to supply an FPGA core clock via the FPGA\_DEVCLKB signal (see schematic)
  - This extra clock is enabled by running the appropriate custom LMK04828 script done earlier in this procedure (i.e. LMK04828\_config\_TSW14J10\_KC705\_LMF\_xxx.cfg)