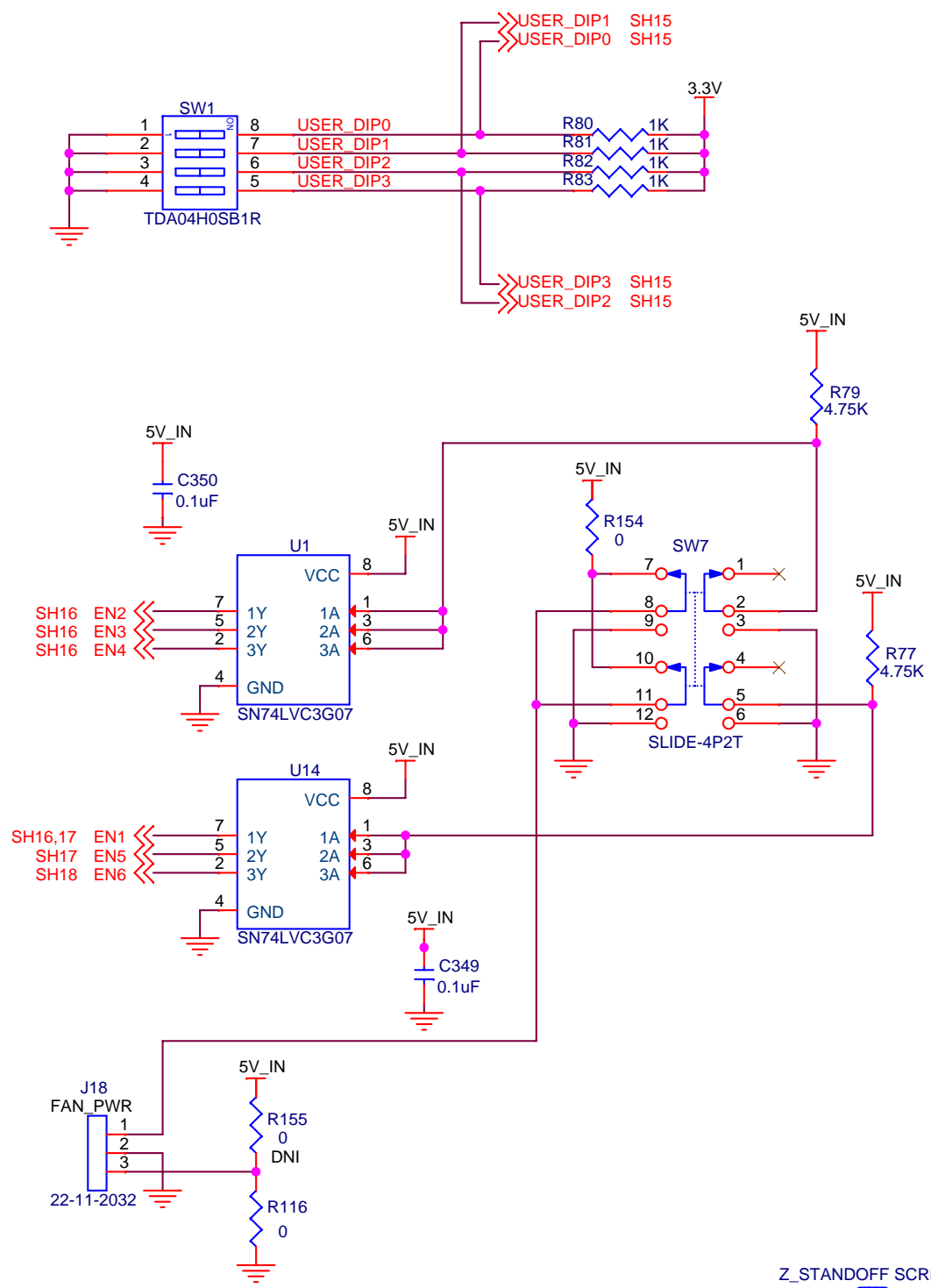
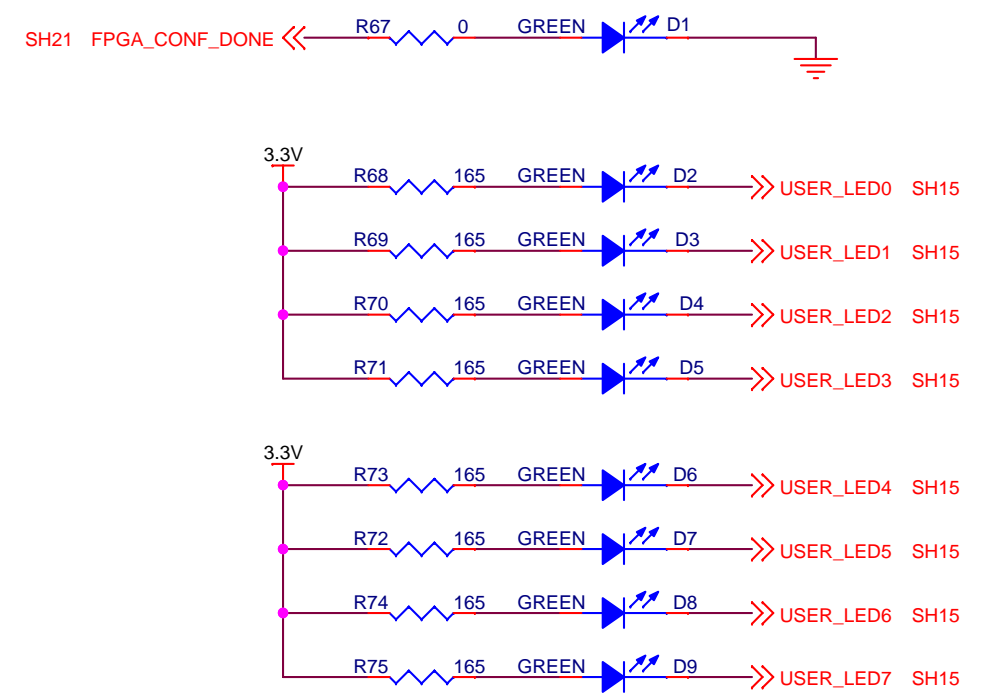


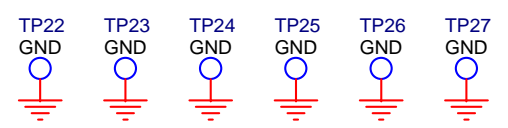
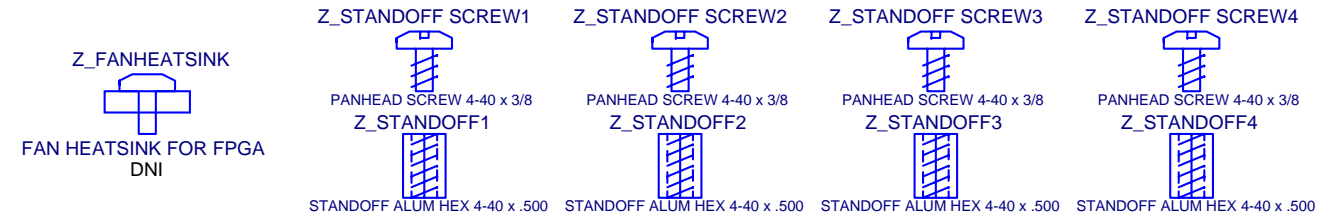
Buttons & Switches



LEDs



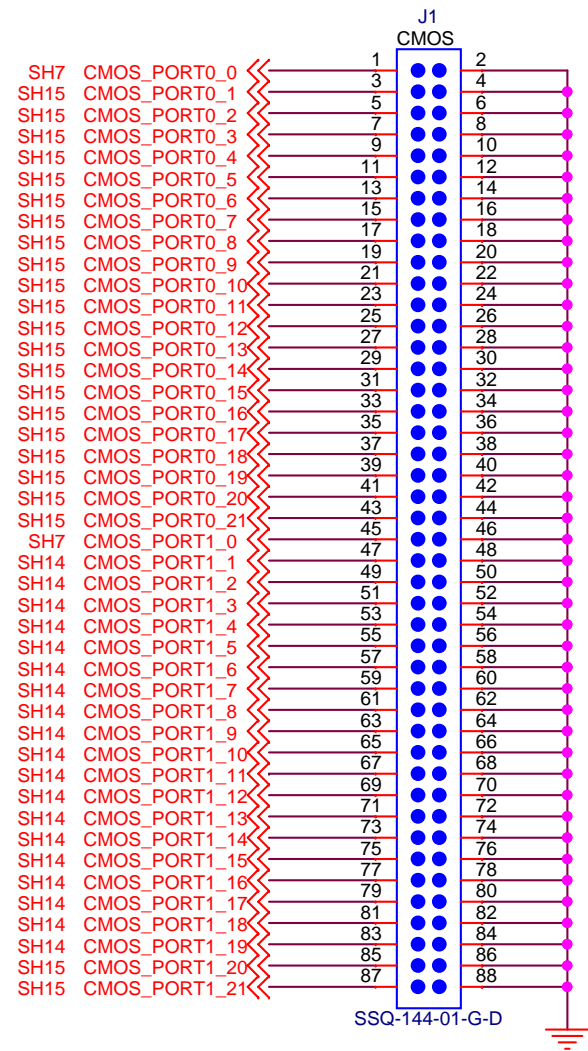
MECHANICAL PARTS



Title BUTTONS, SWITCHES, LEDS		
Size B	Document Number TSW1400	Rev D
Date: Friday, October 07, 2011	Sheet 1	of 21

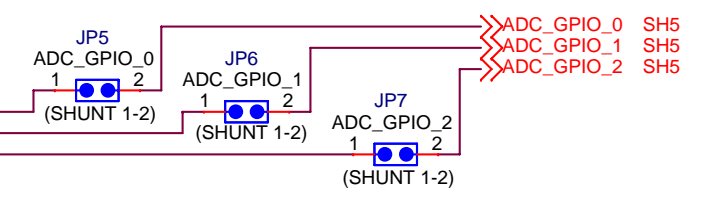
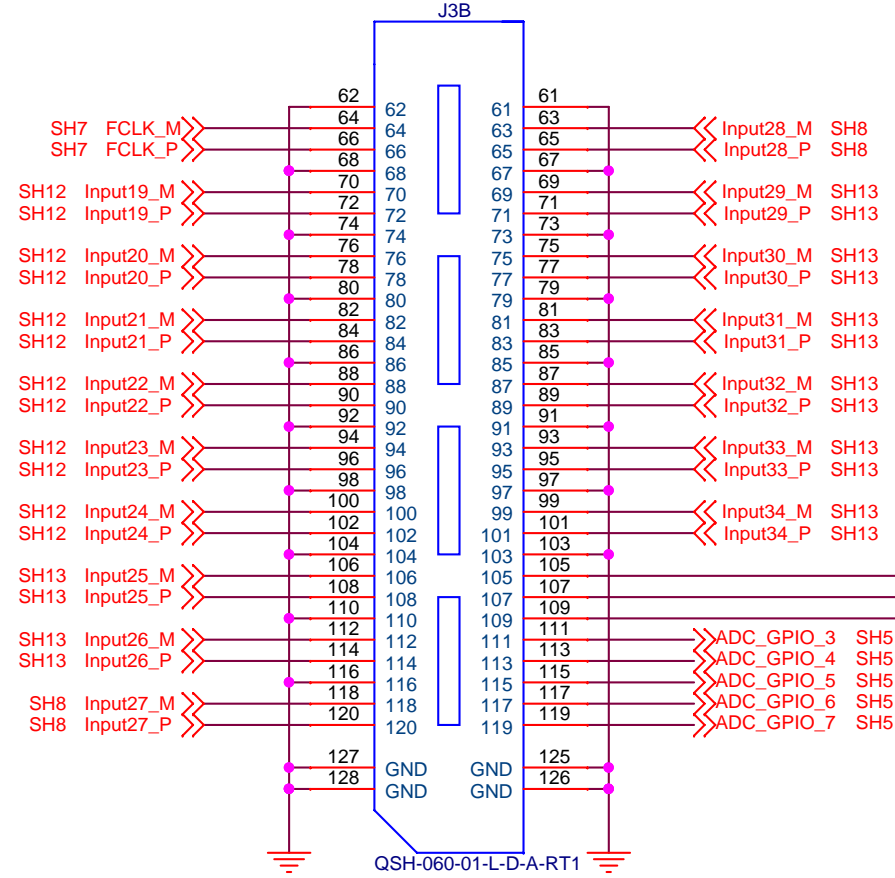
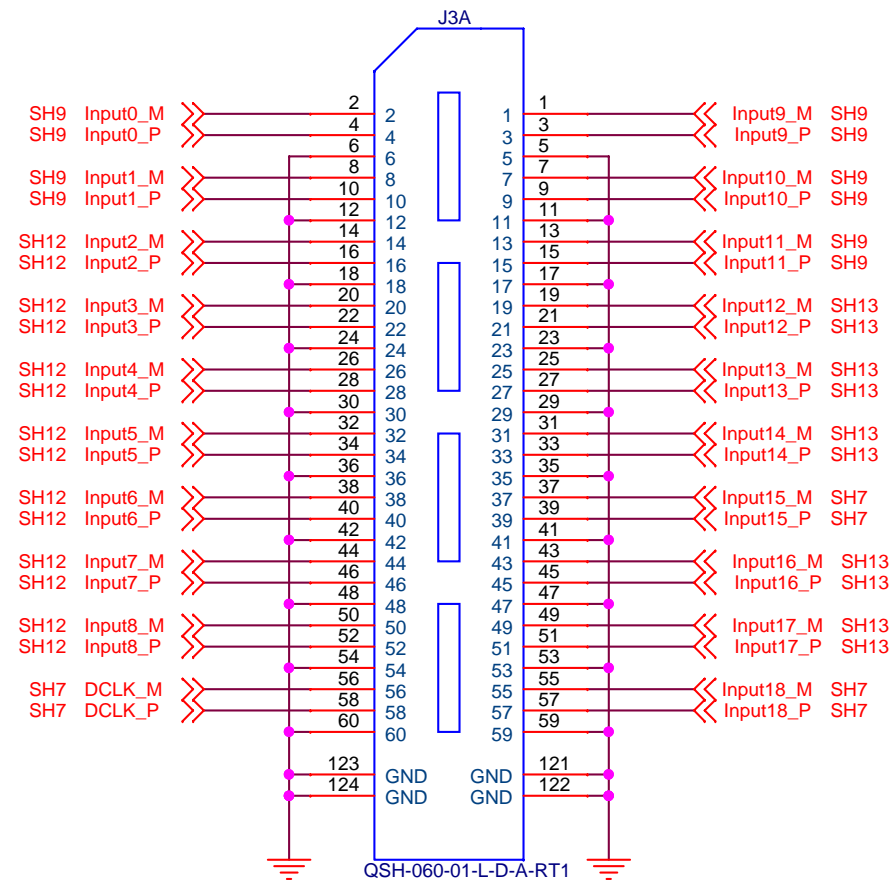
Drawn: P. LARSON
Engineer: J. SETON

CMOS Header

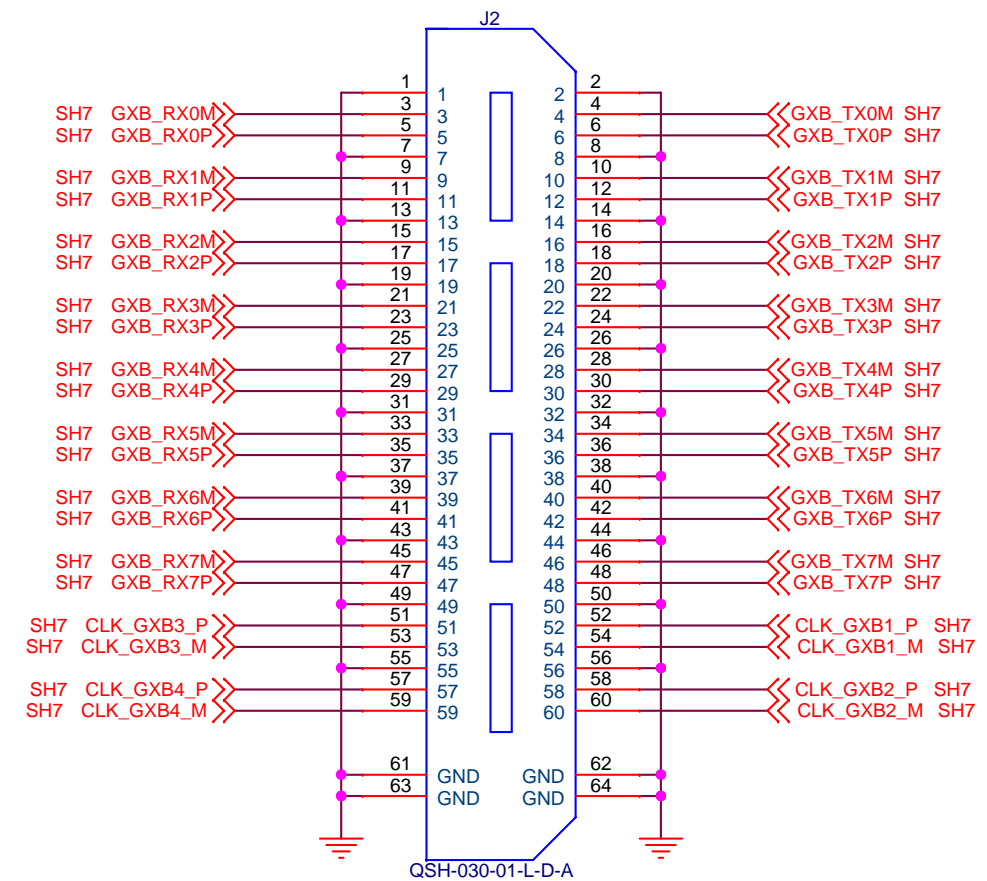


Title		
CMOS Header		
Size	Document Number	Rev
B	TSW1400	D
Date:	Friday, October 07, 2011	Sheet 2 of 21

ADC Interface



JESD

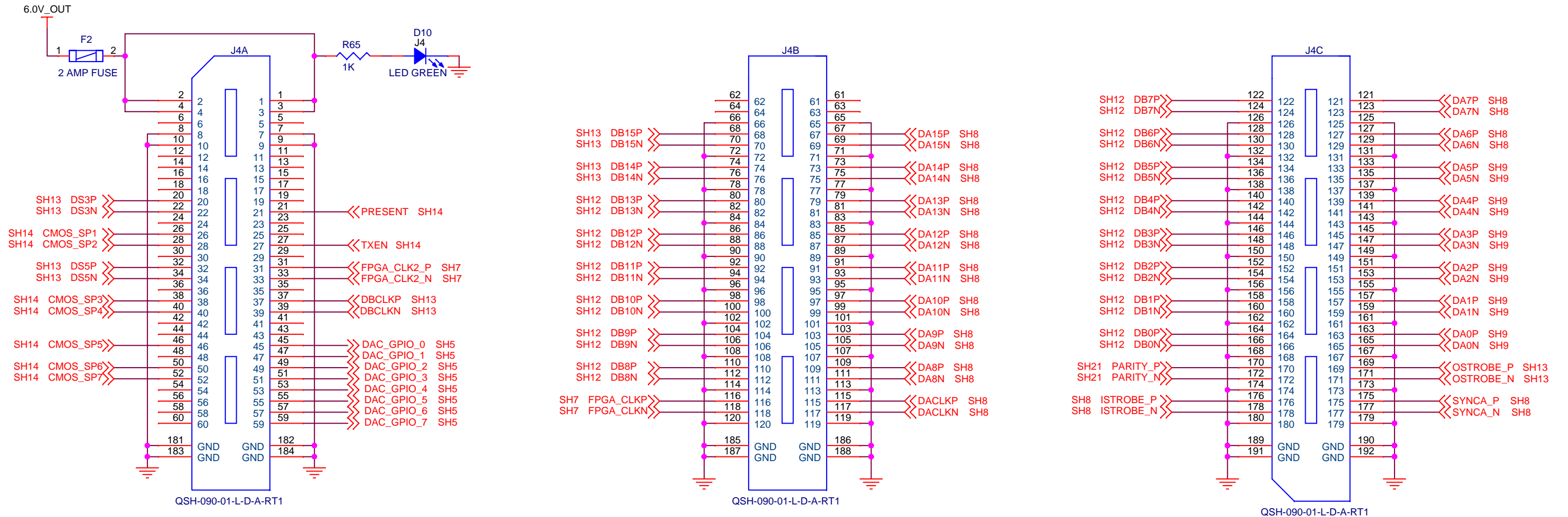


TEXAS INSTRUMENTS

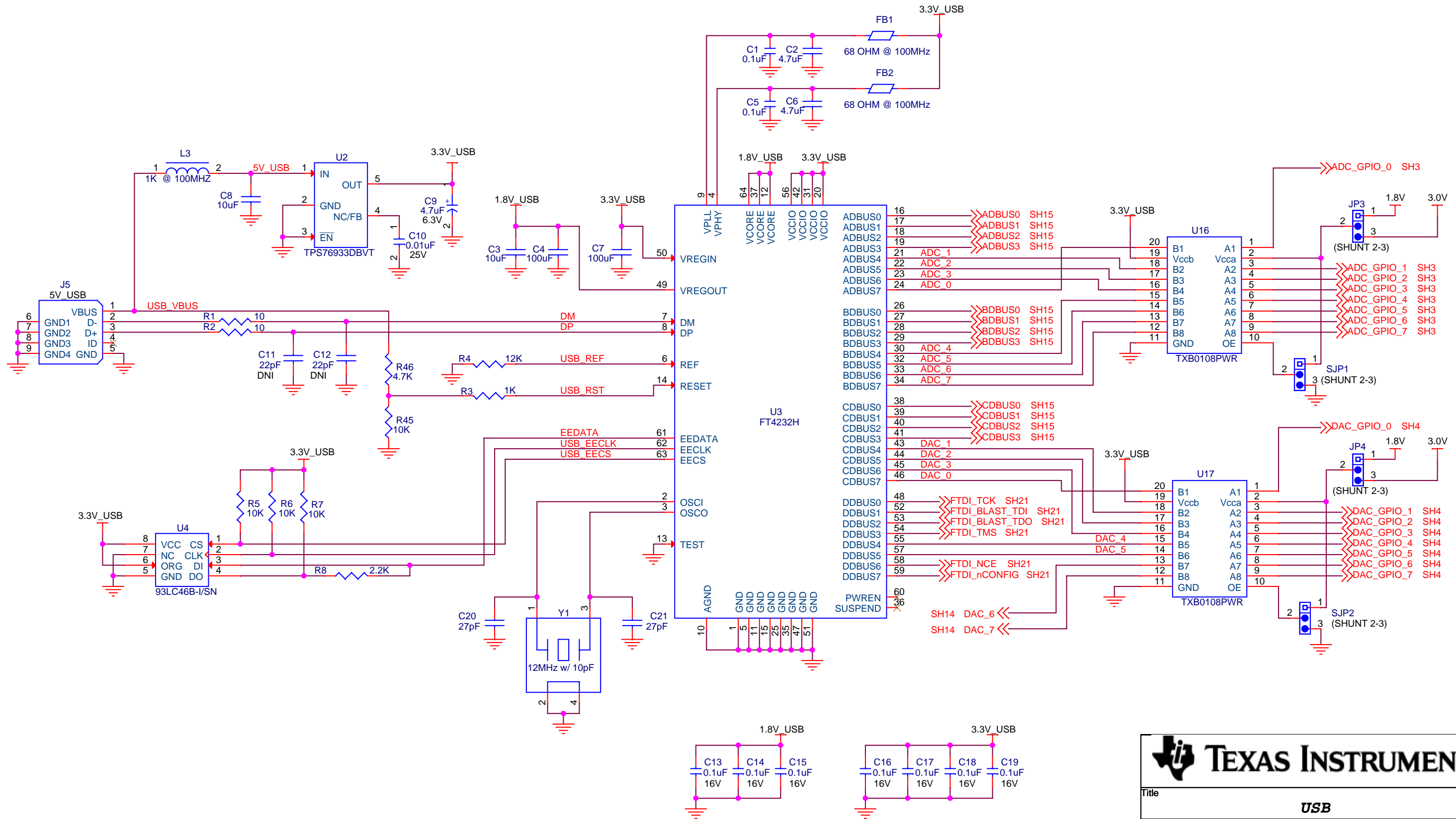
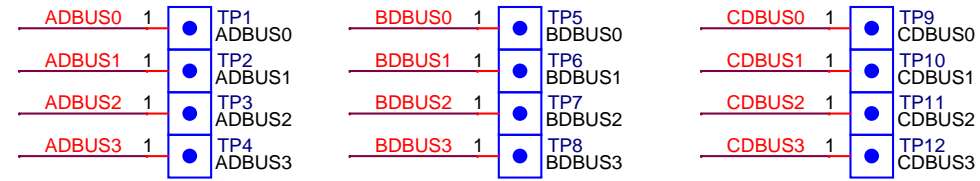
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Size: B	Document Number: TSW1400	Rev: D
Date: Friday, October 07, 2011	Sheet: 3 of 21	

DAC Interface



USB



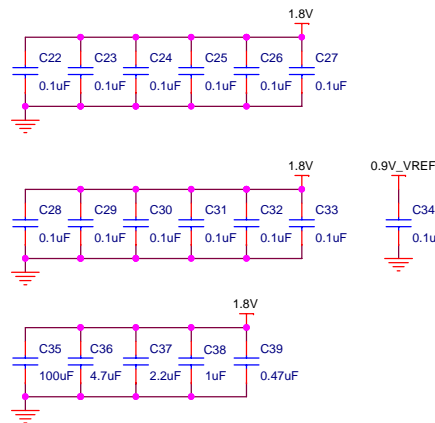
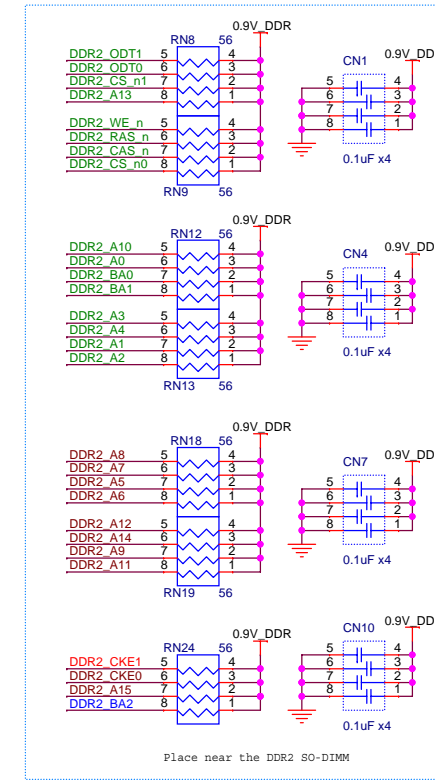
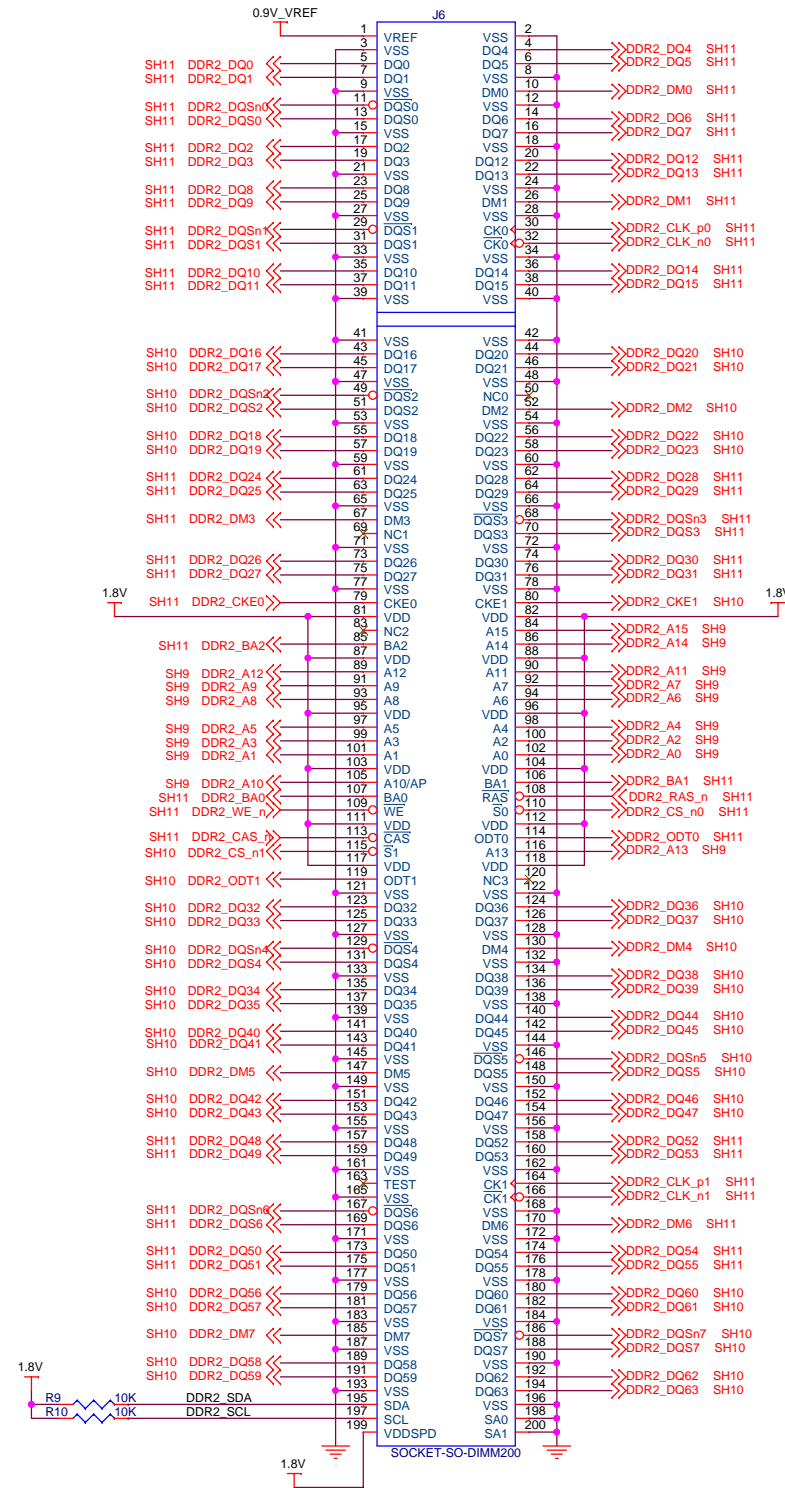
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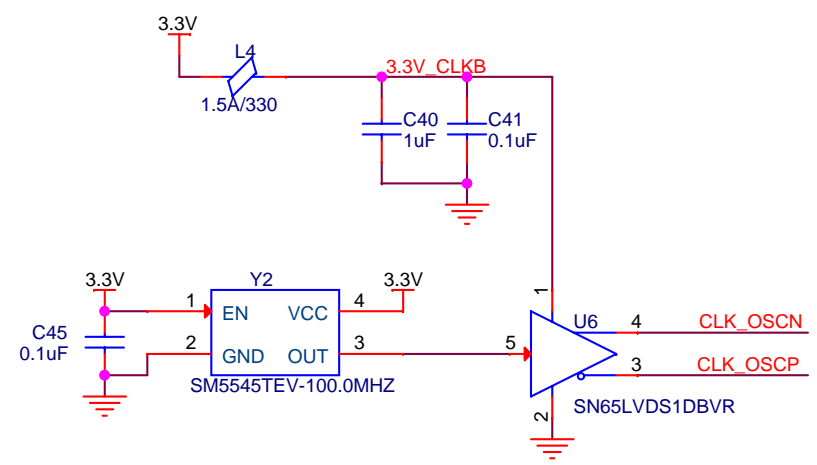
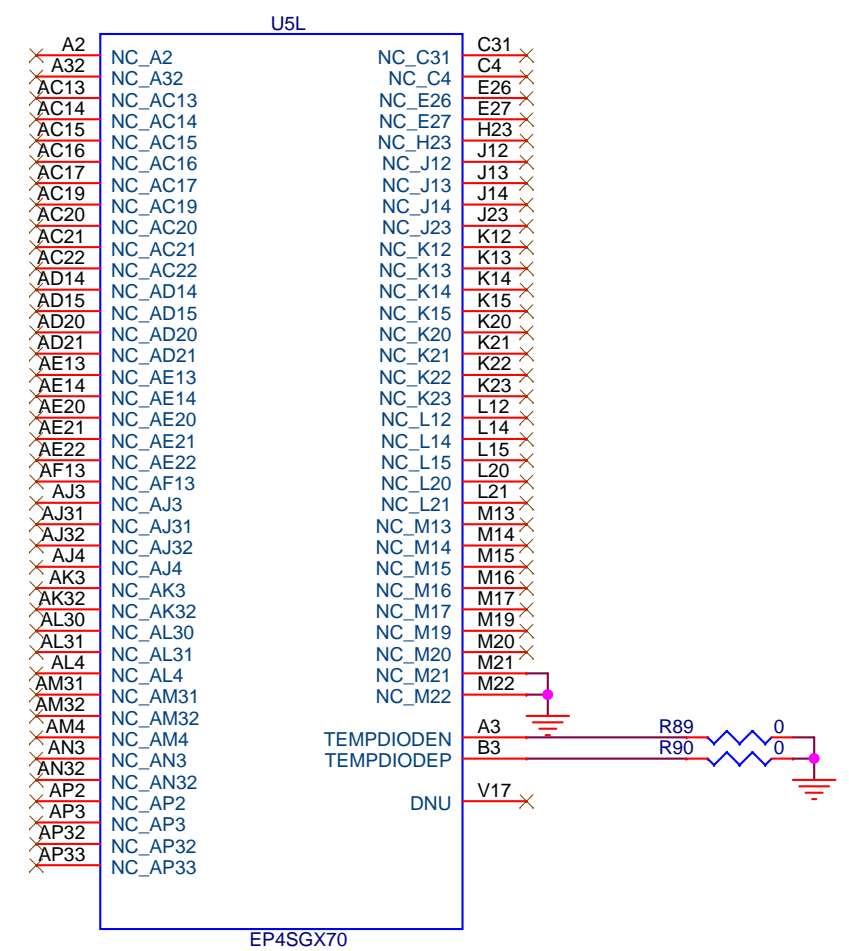
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Size: **B** | Document Number: **TSW1400** | Rev: **D**

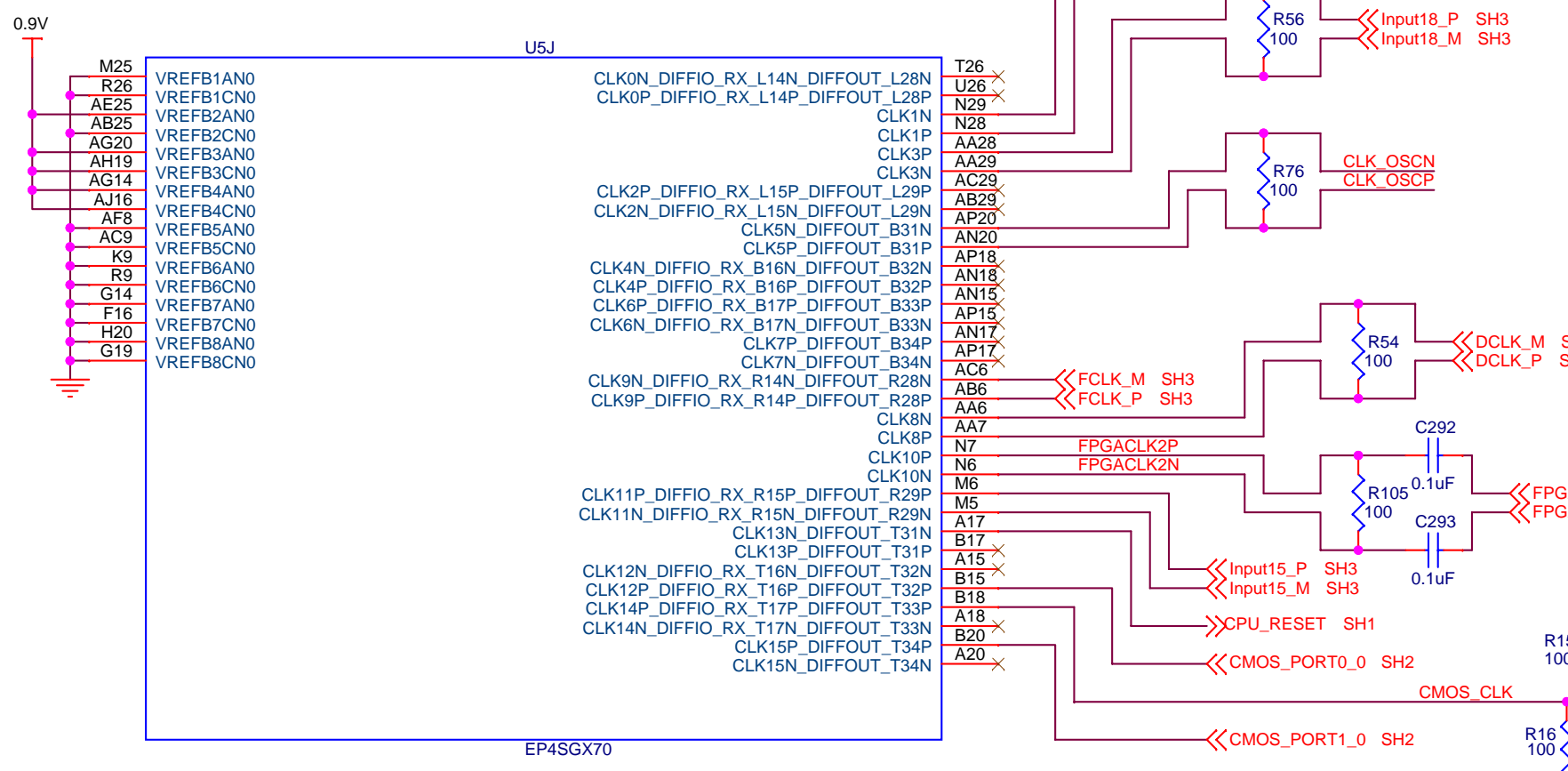
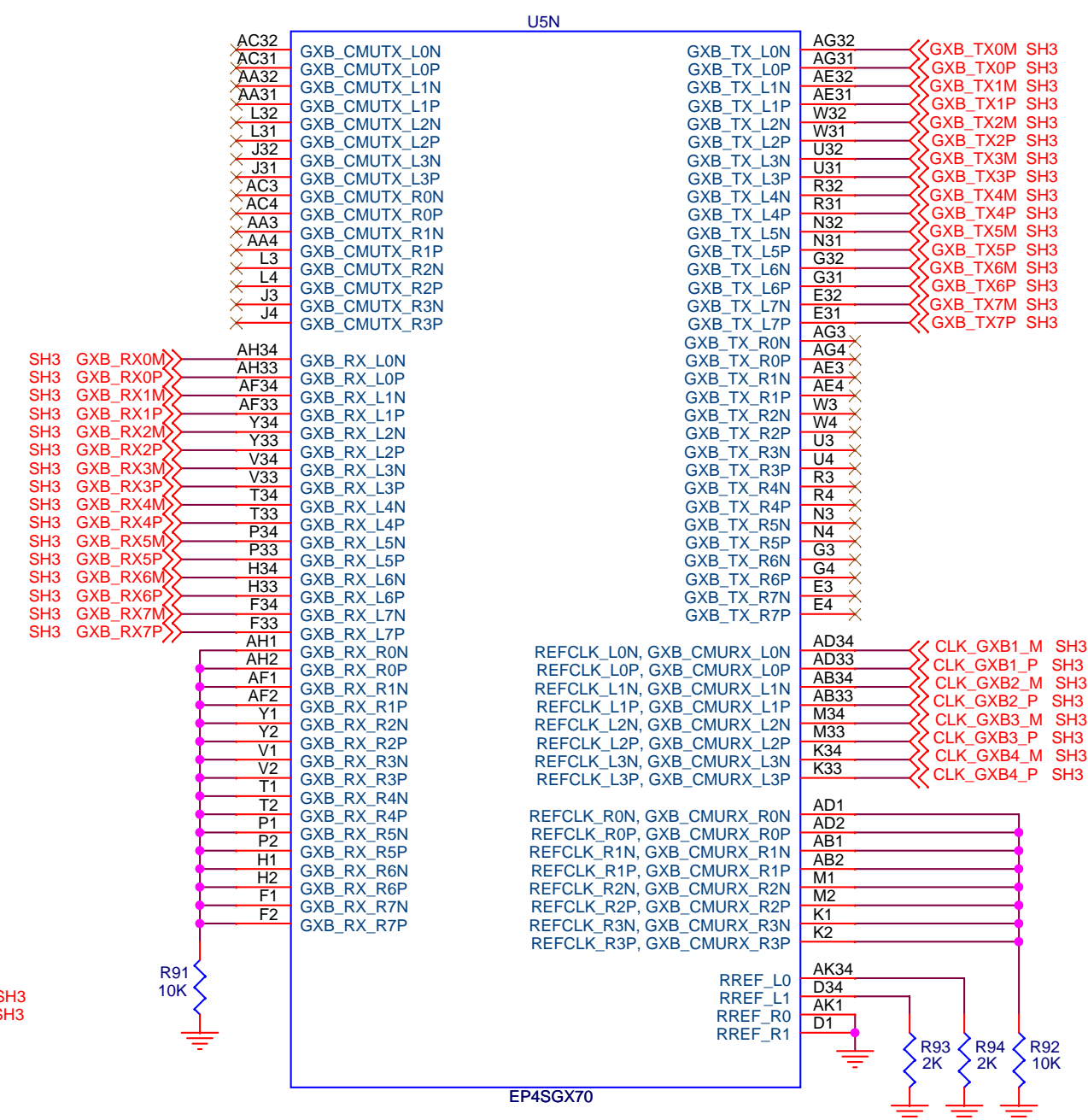
Date: Friday, October 07, 2011 | Sheet: 5 of 21

DDR2 SO-DIMM





BANK QL



TEXAS INSTRUMENTS

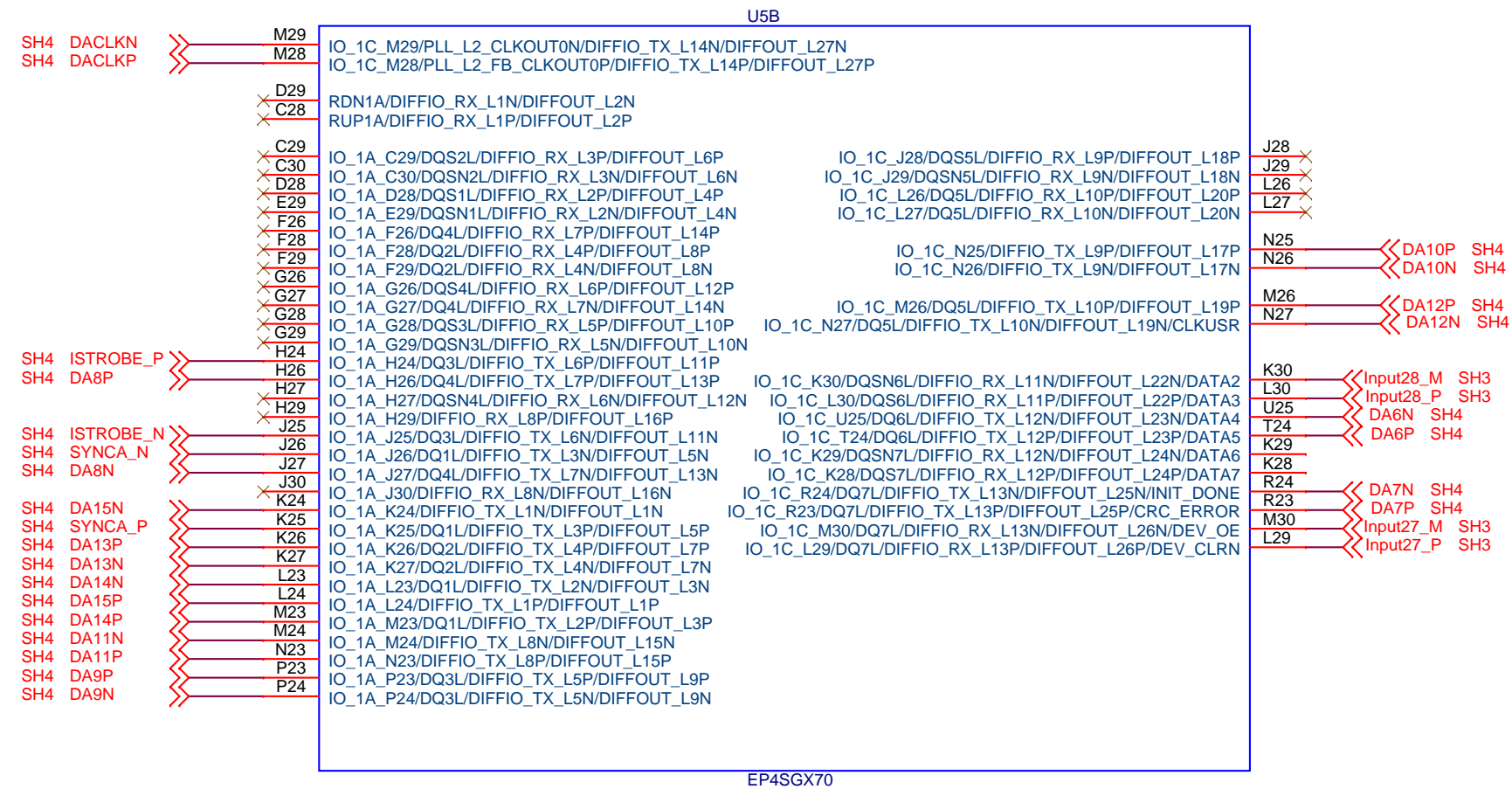
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Size: **B** | Document Number: **TSW1400** | Rev: **D**

Date: Friday, October 07, 2011 | Sheet: 7 of 21

BANK1

2.5V



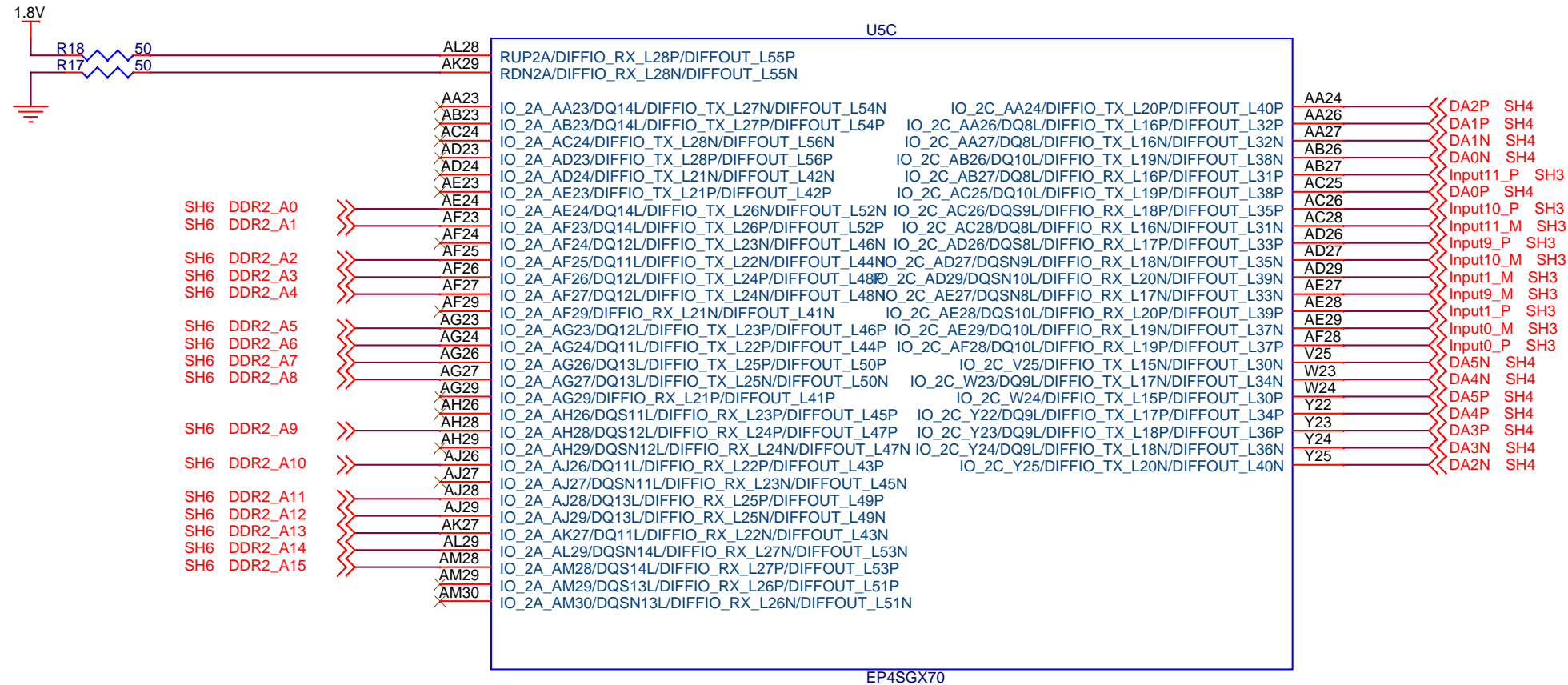
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Title		
Bank1		
Size	Document Number	Rev
B	TSW1400	D
Date:	Friday, October 07, 2011	Sheet 8 of 21

BANK2

1.8V

2.5V



TEXAS INSTRUMENTS

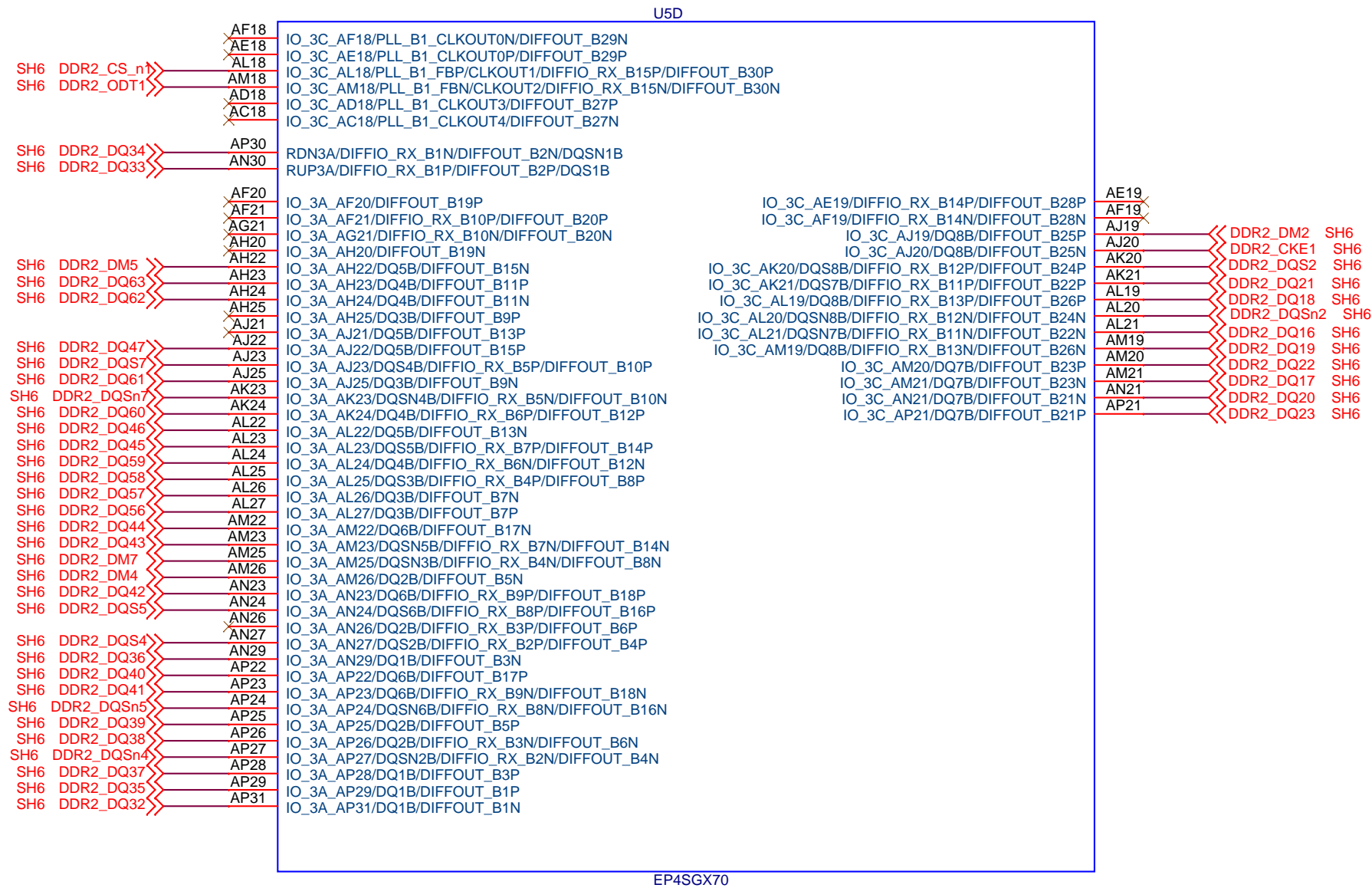
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Size: **B** Document Number: **TSW1400** Rev: **D**

Date: Friday, October 07, 2011 Sheet 9 of 21

BANK3

1.8V

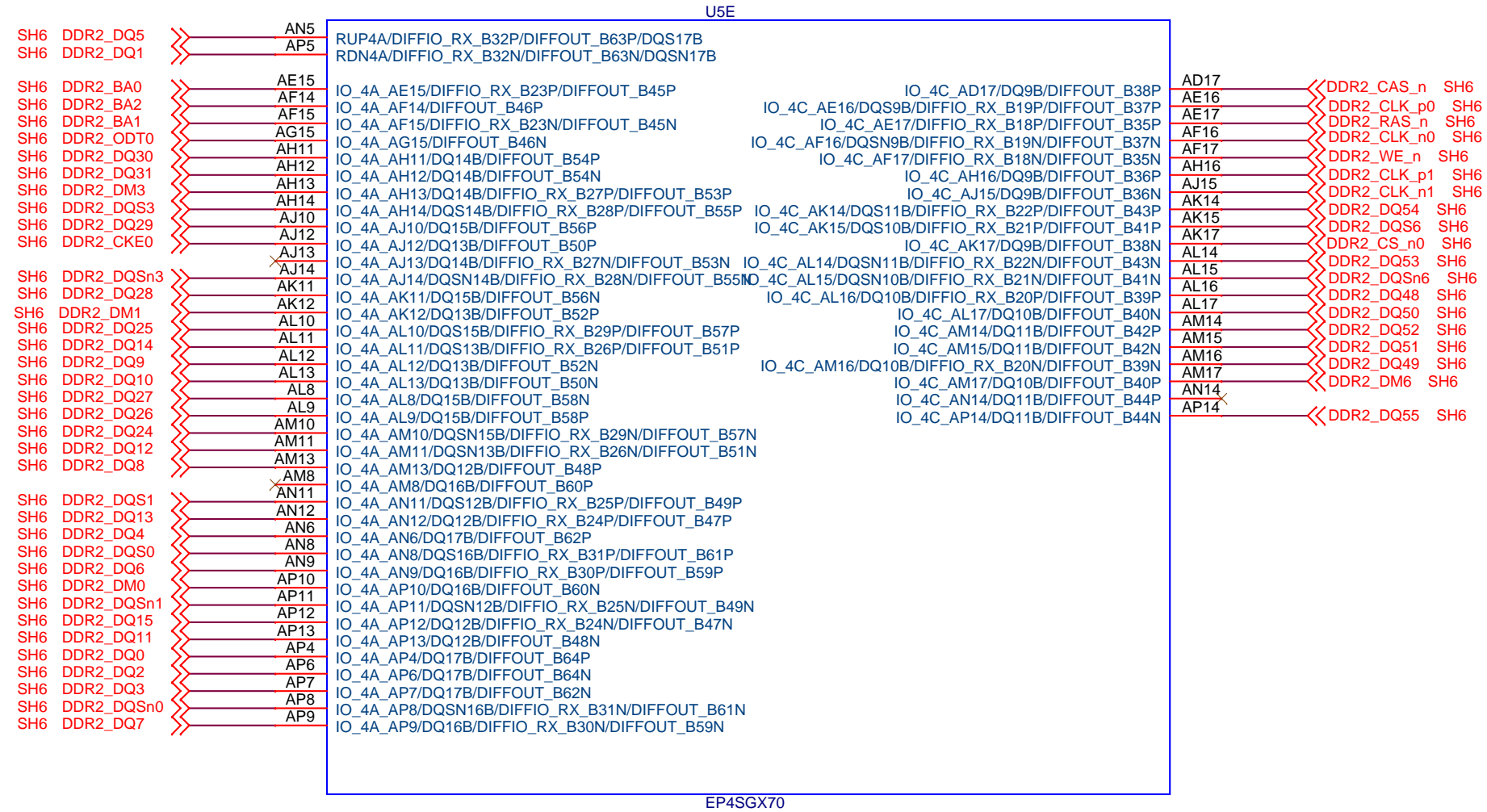


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Size	Document Number	Rev
B	TSW1400	D
Date:	Friday, October 07, 2011	Sheet 10 of 21

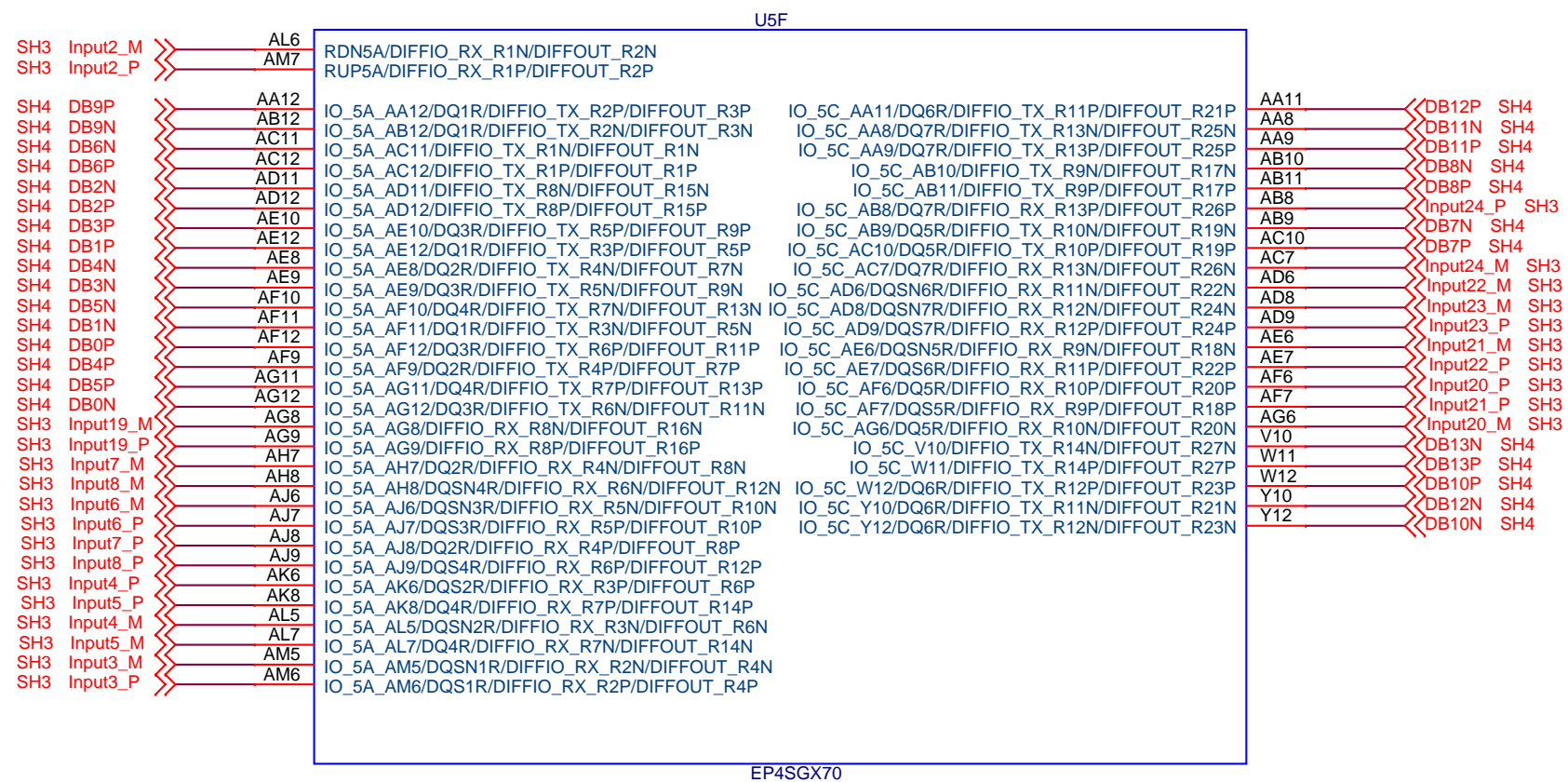
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1.8V



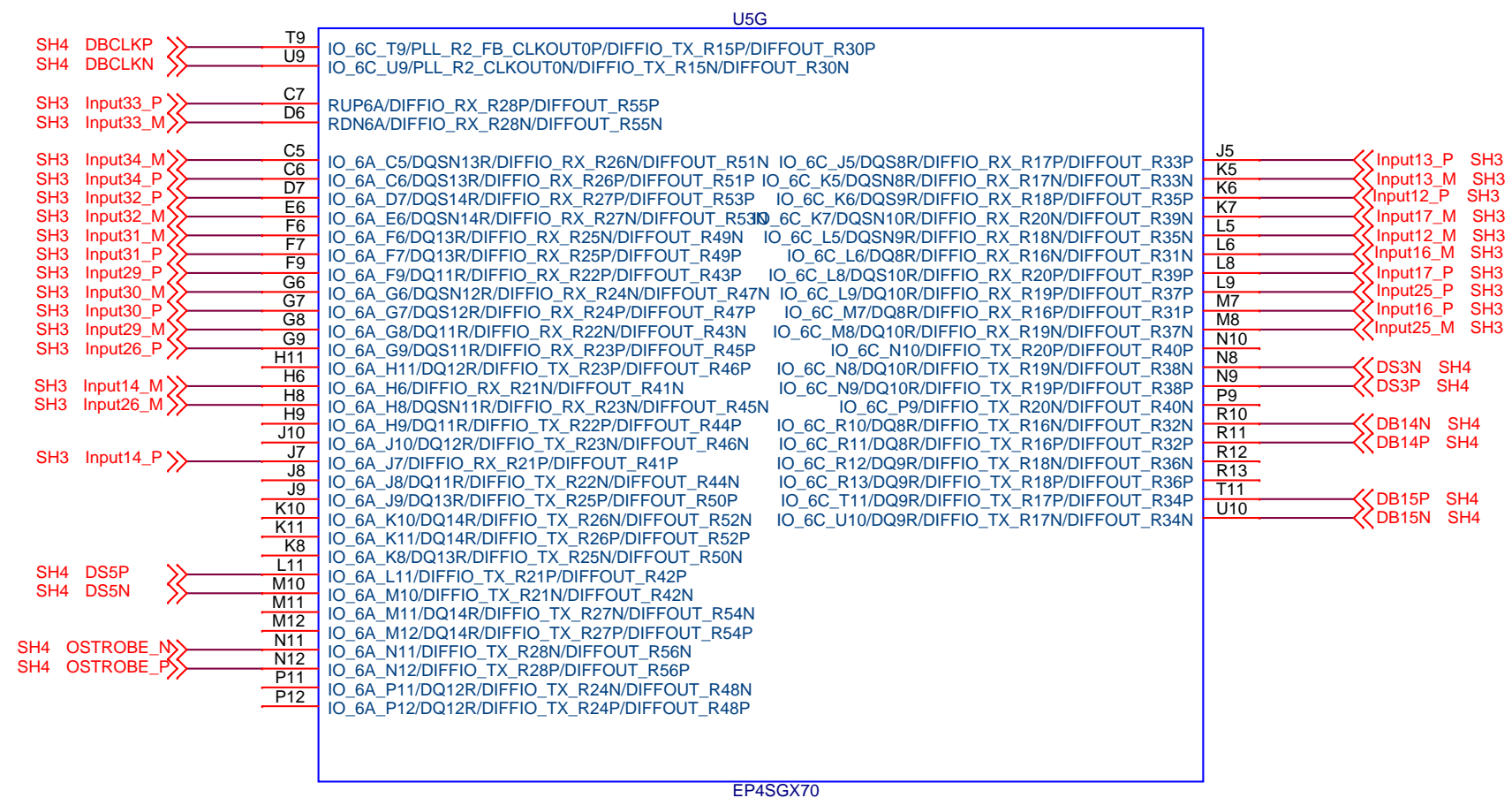
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Size	Document Number	Rev
B	TSW1400	D
Date:	Friday, October 07, 2011	Sheet 11 of 21

BANK5 2.5V



Title		
Bank5		
Size	Document Number	Rev
B	TSW1400	D
Date:	Friday, October 07, 2011	Sheet 12 of 21

BANK6 2.5V

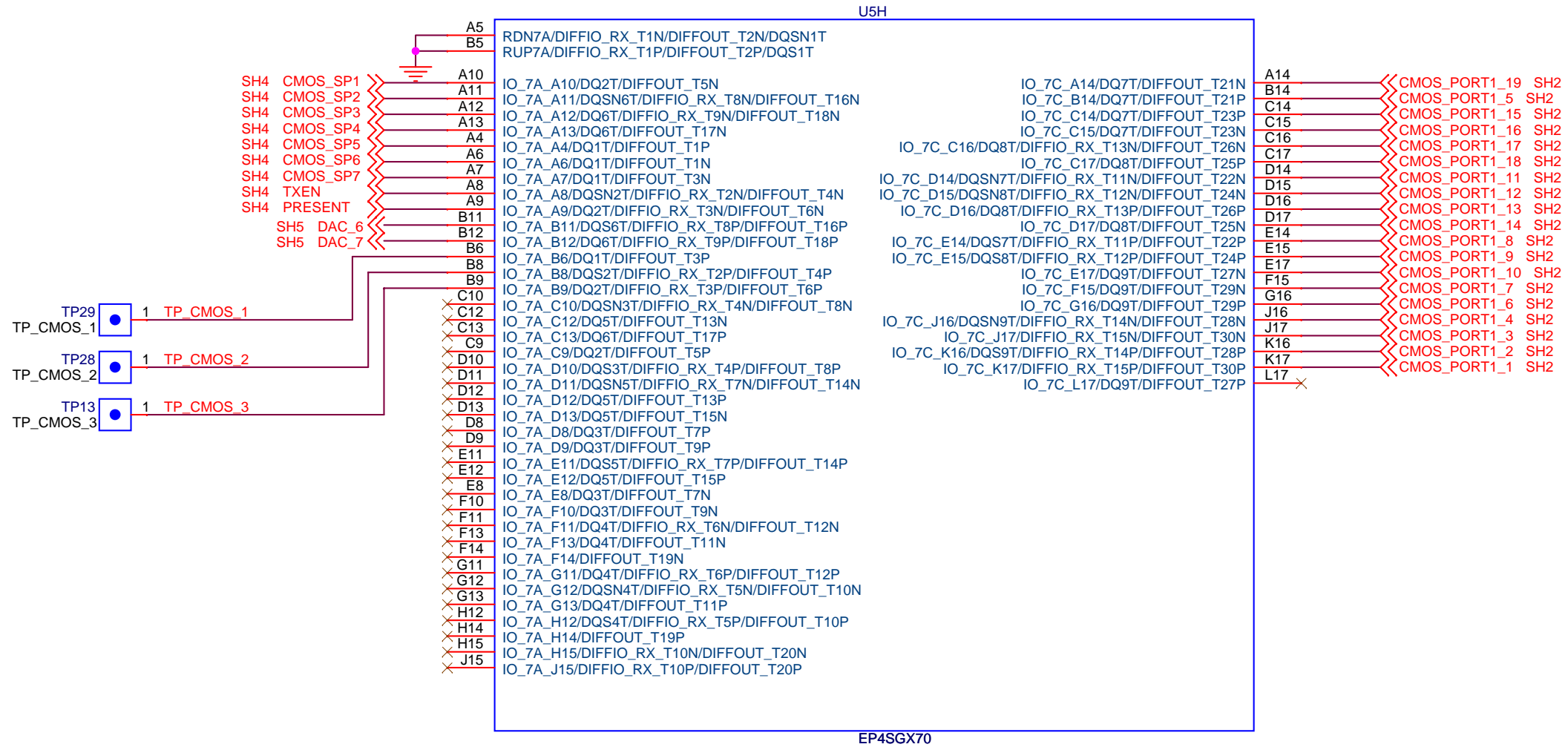


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Size	Document Number	Rev
	TSW1400	D
Date:	Friday, October 07, 2011	Sheet 13 of 21

BANK7

3.0V



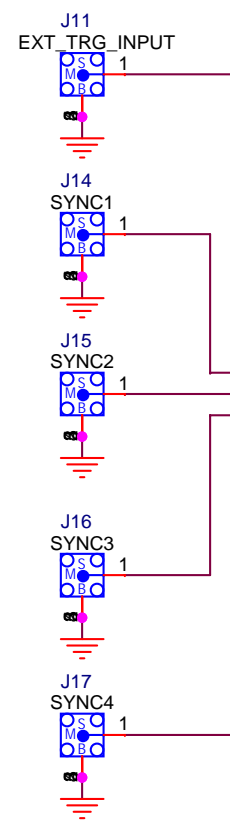
BANK8

3.0V

U51



EP4SGX70



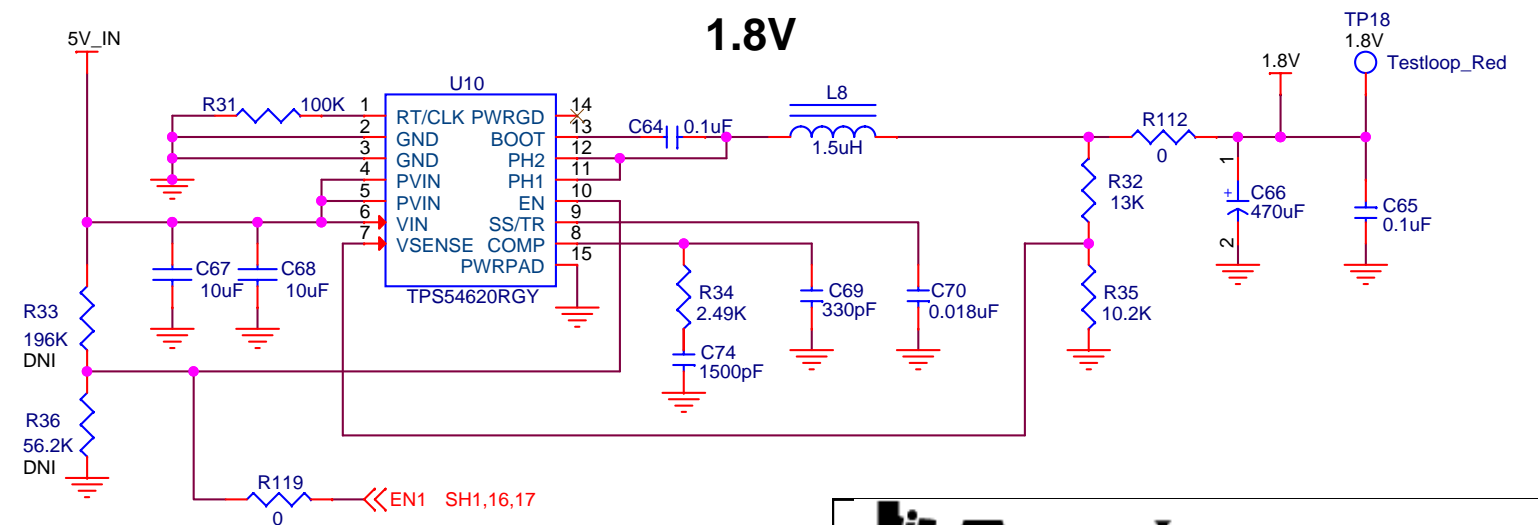
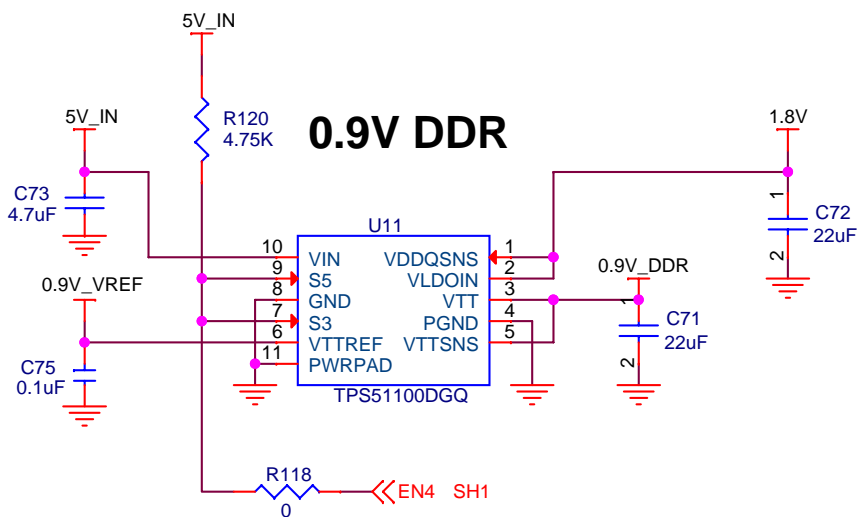
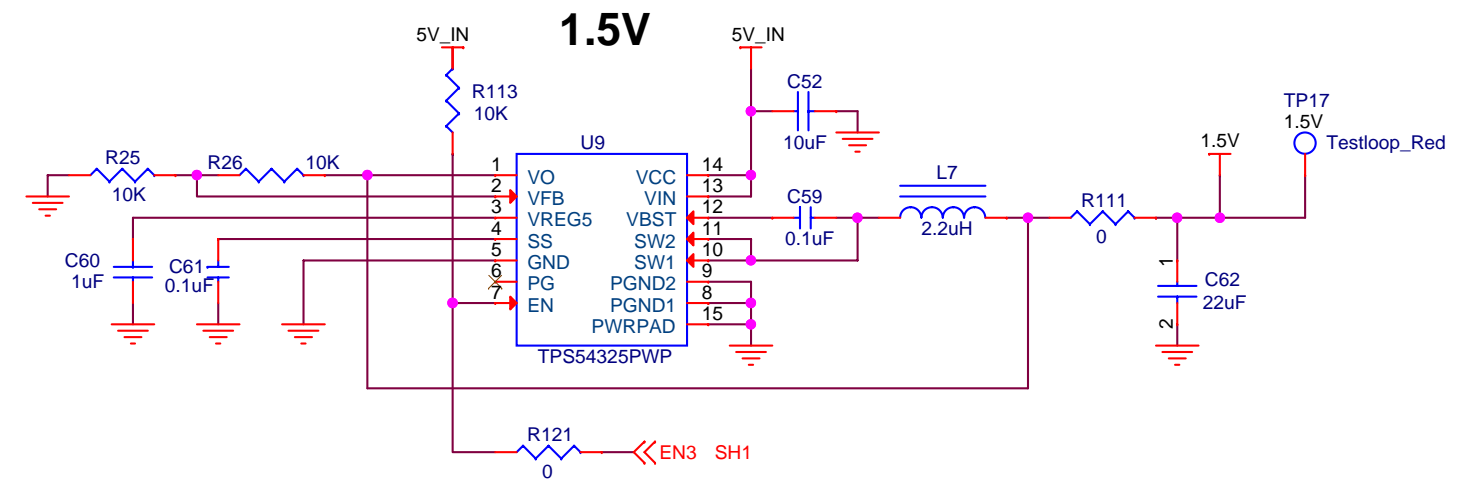
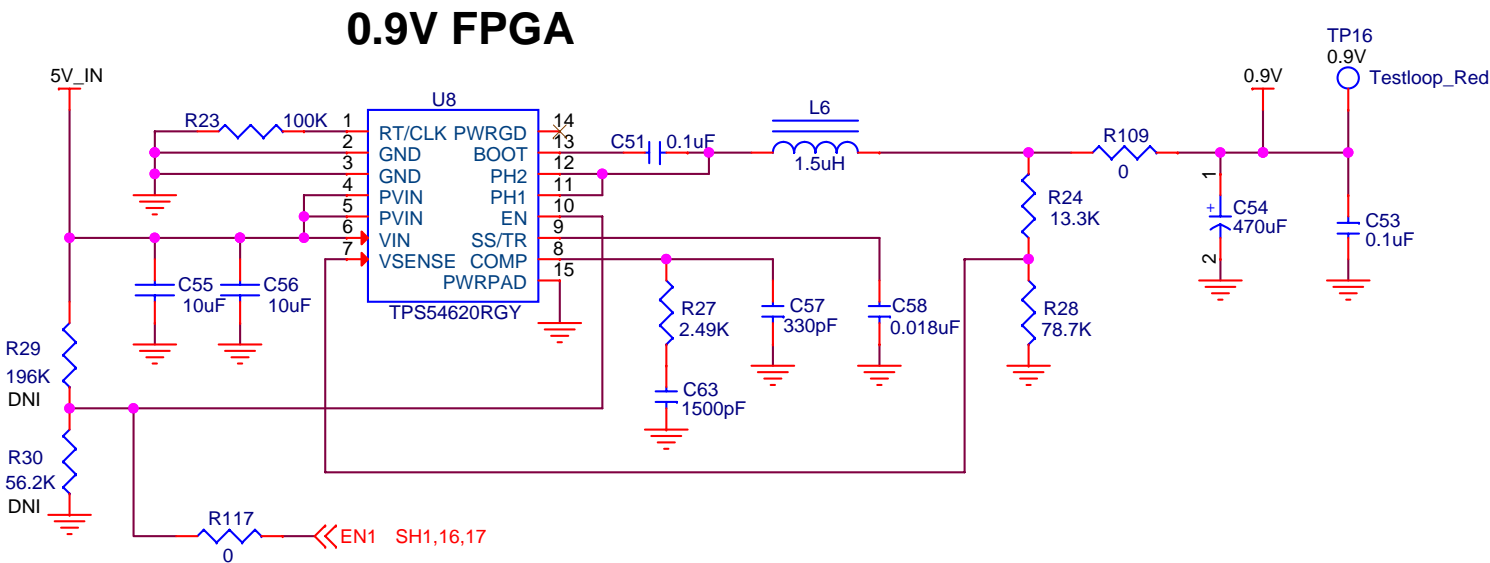
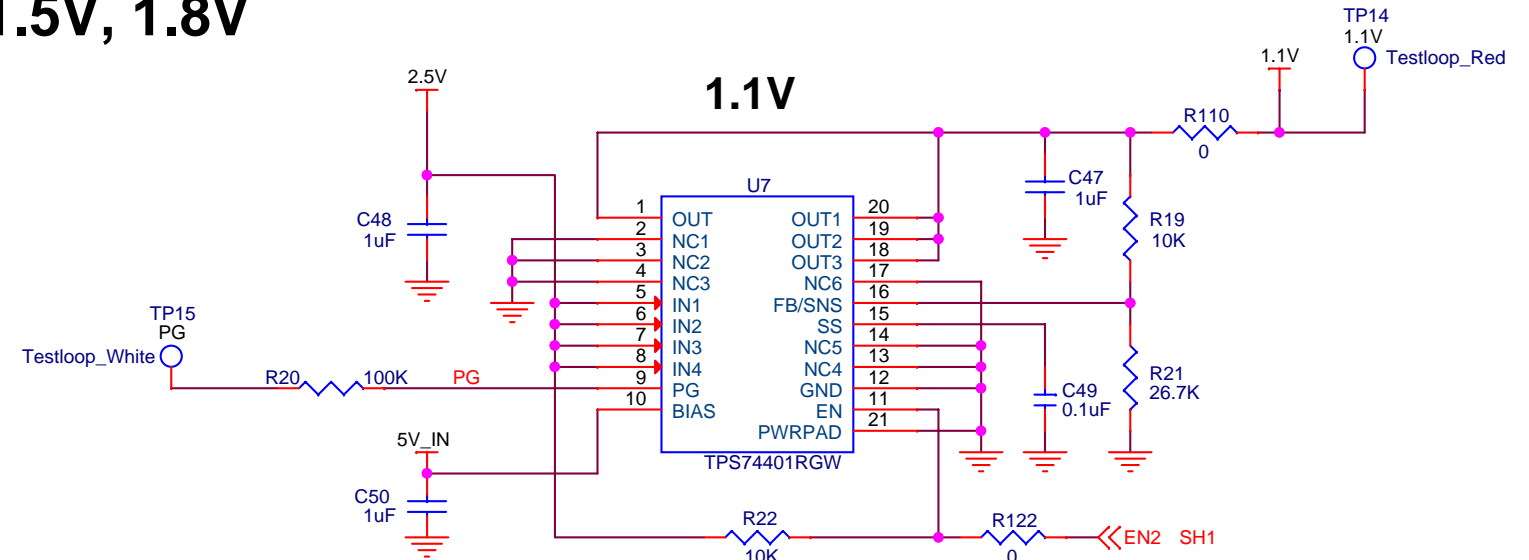
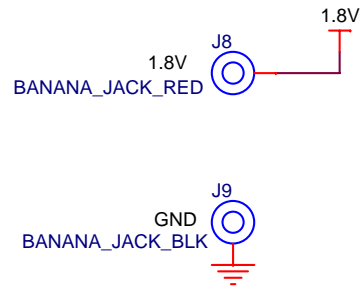
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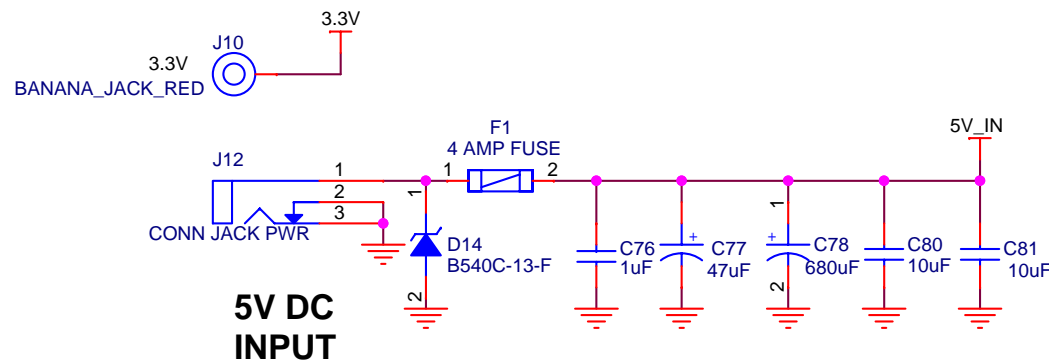
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Date: Friday, October 07, 2011 Sheet 15 of 21

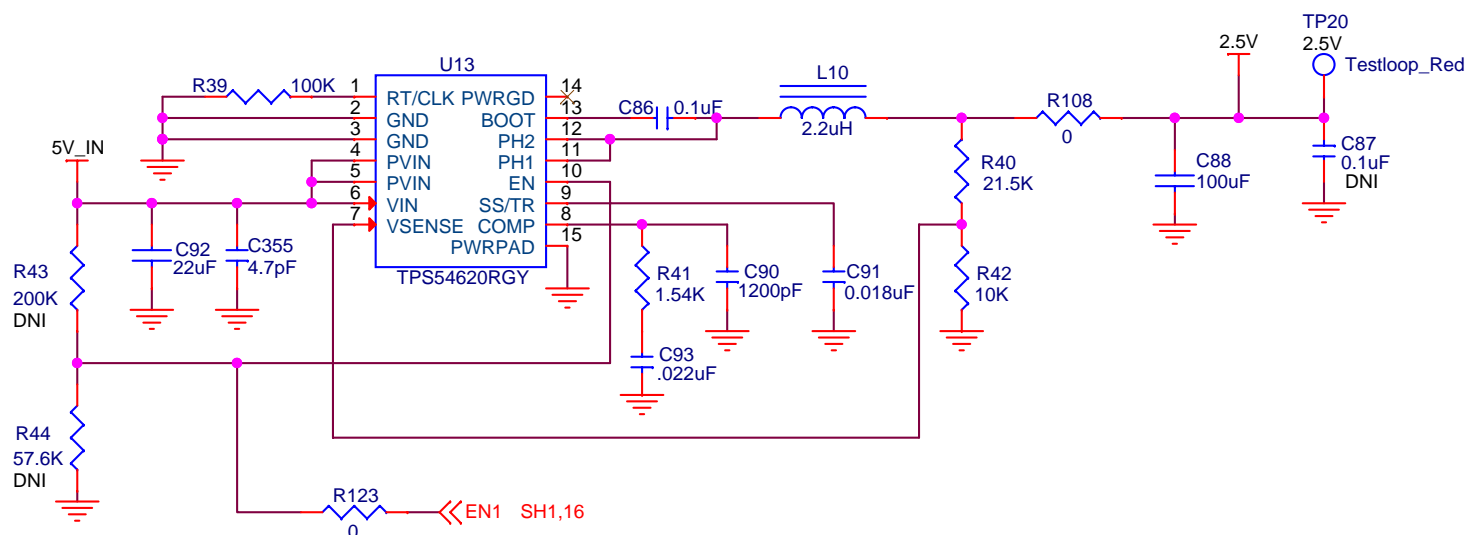
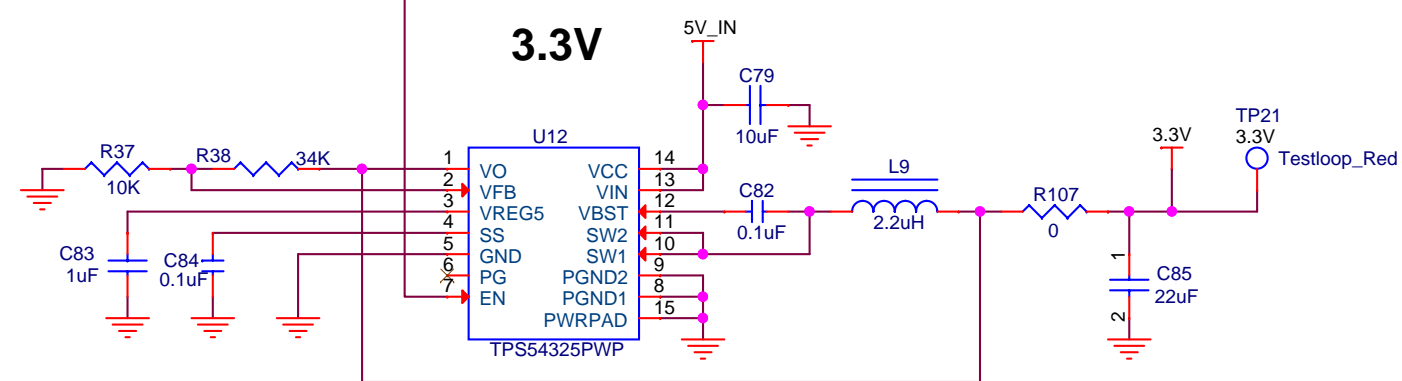
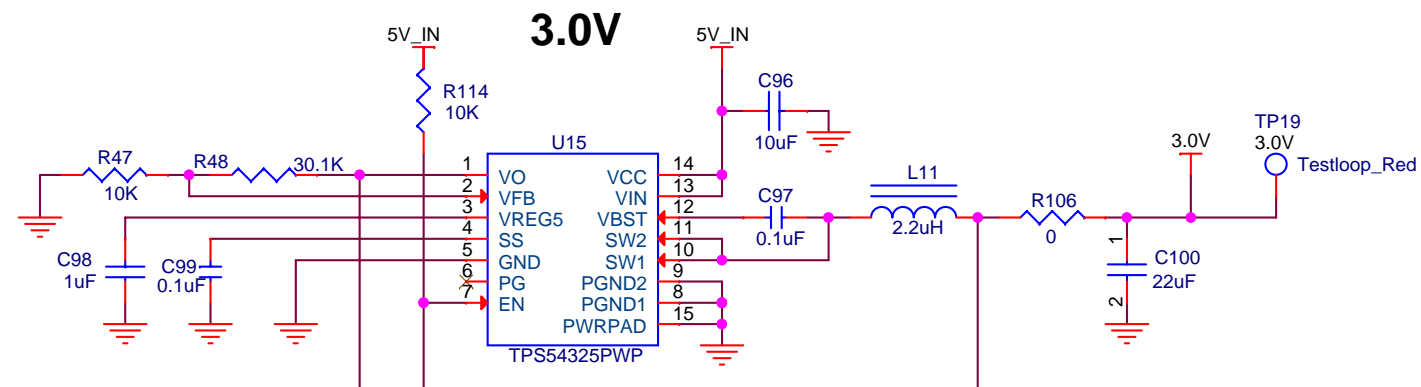
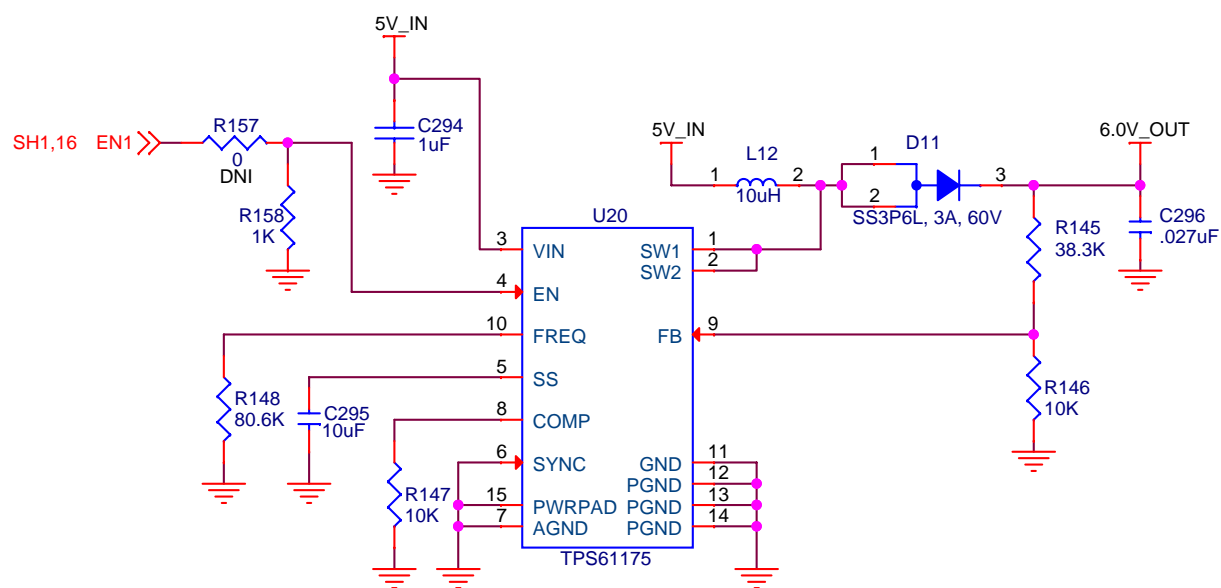
0.9V, 1.1V, 1.5V, 1.8V



Title		
POWERS 0.9V, 1.1V, 1.5V, 1.8V		
Size	Document Number	Rev
B	TSW1400	D
Date:	Friday, October 07, 2011	Sheet 16 of 21

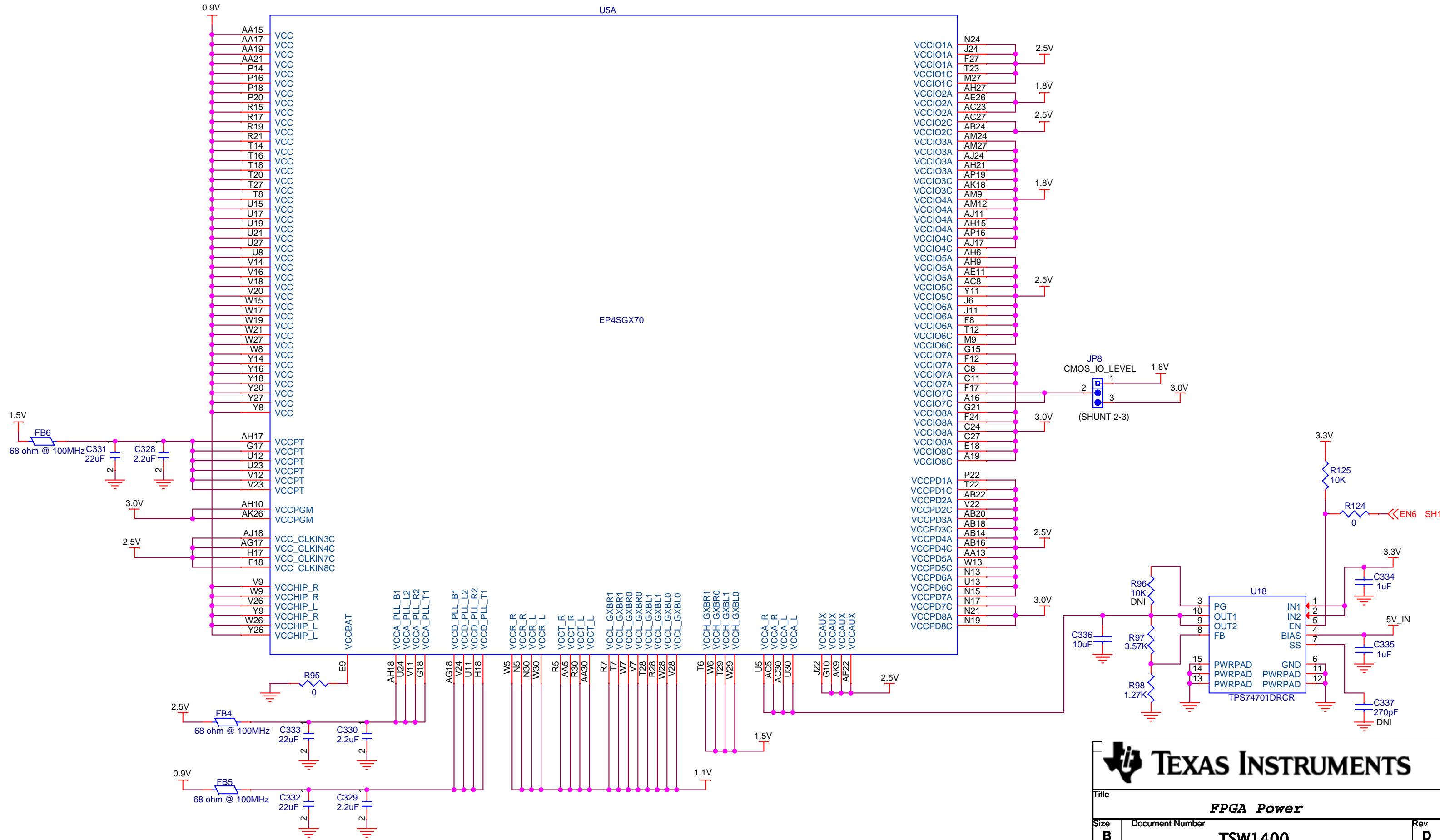


2.5V, 3.0V, 3.3V, 5V



Title		
POWERS 2.5V, 3.0V, 3.3V, 5V		
Size	Document Number	Rev
B	TSW1400	D
Date:	Friday, October 07, 2011	Sheet 17 of 21

FPGA Power



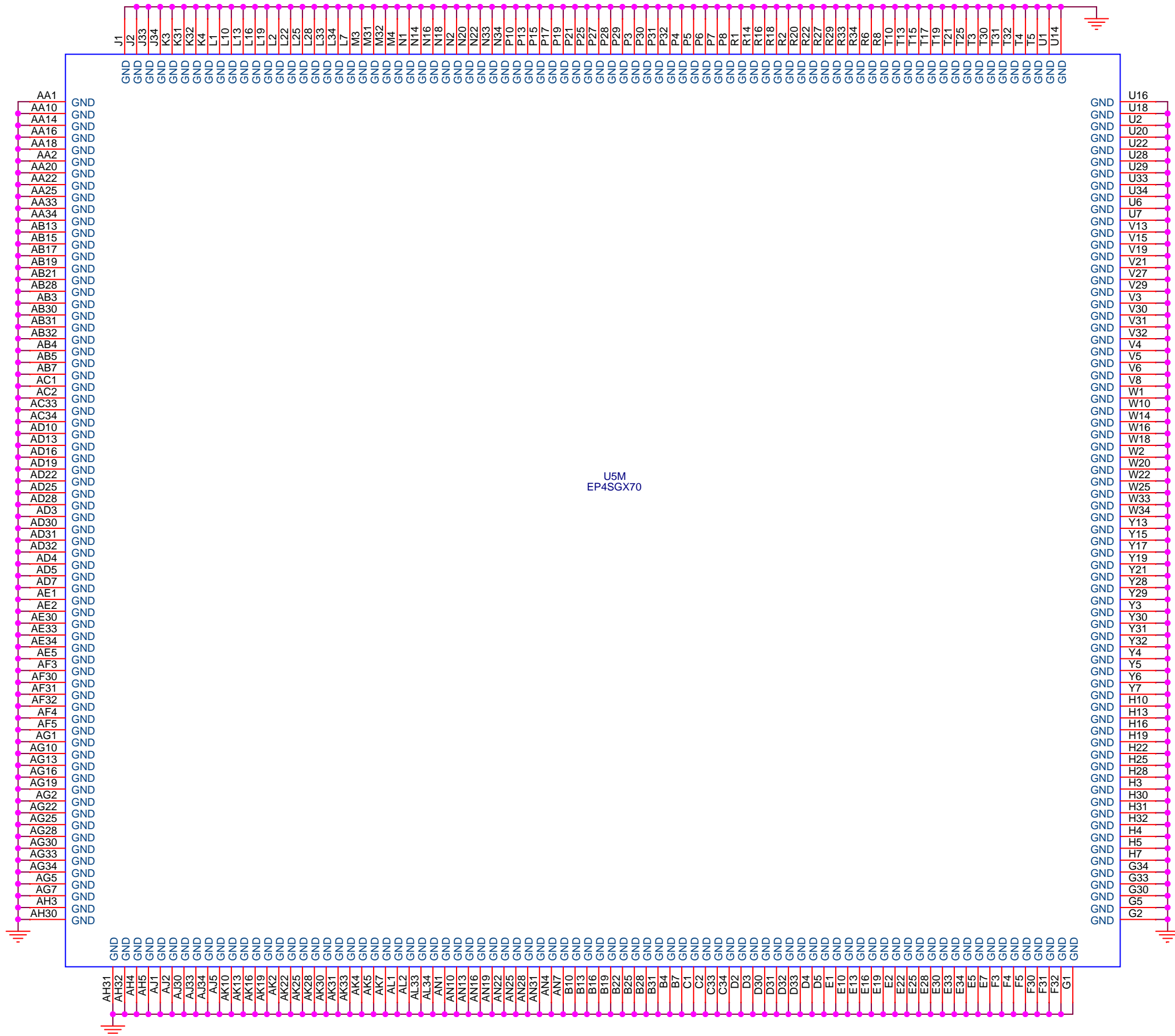
TEXAS INSTRUMENTS

Title: **FPGA Power**

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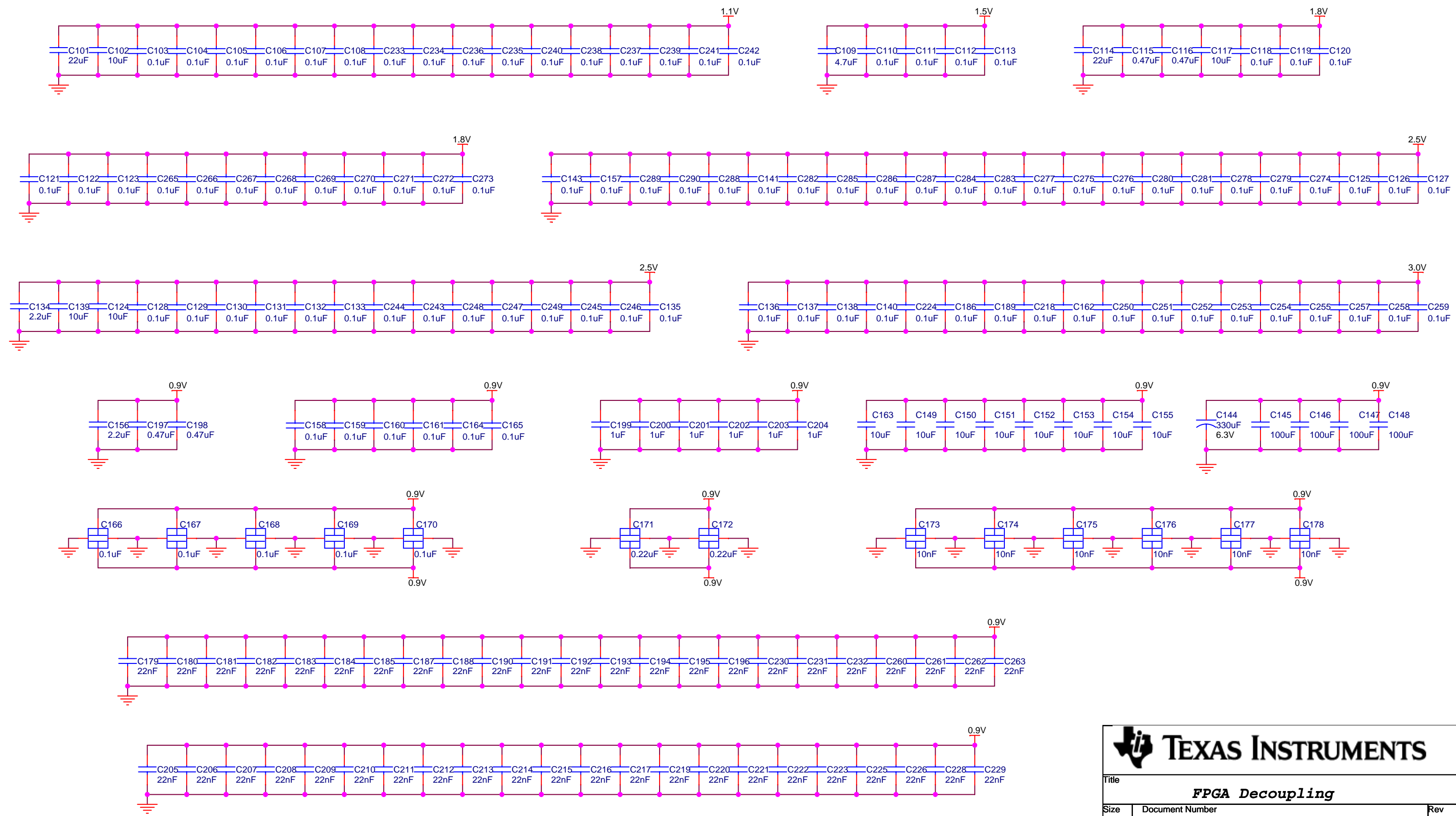
Date: Friday, October 07, 2011 | Sheet: 18 of 21

FPGA Ground



Title		
FPGA Ground		
Size	Document Number	Rev
B	TSW1400	D
Date:	Friday, October 07, 2011	Sheet 19 of 21

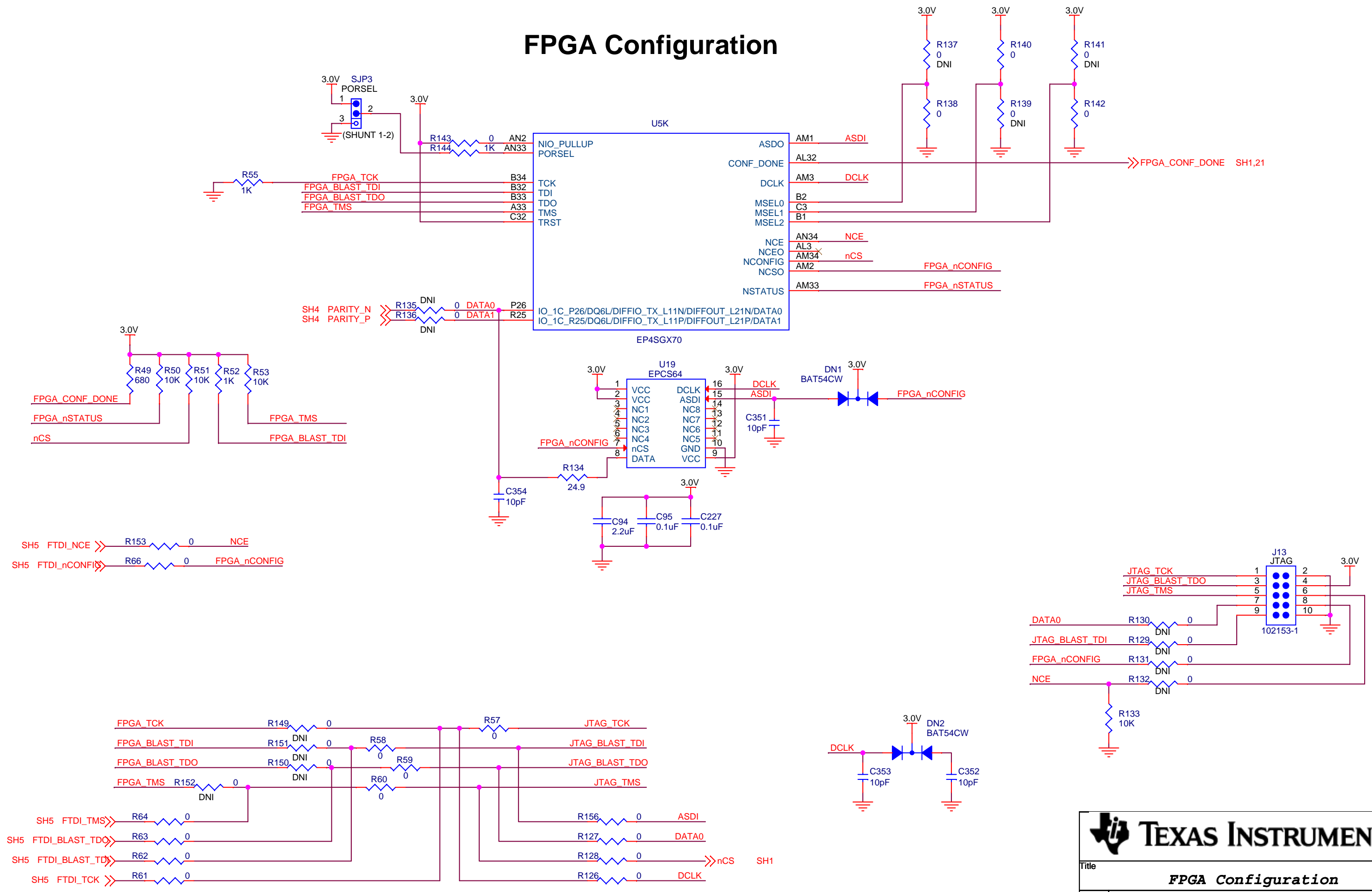
FPGA Decoupling



TEXAS INSTRUMENTS

Title FPGA Decoupling		
Size B	Document Number TSW1400	Rev D
Date: Friday, October 07, 2011	Sheet 20	of 21

FPGA Configuration



TEXAS INSTRUMENTS

Title: **FPGA Configuration**

Size: B	Document Number: TSW1400	Rev: D
Date: Friday, October 07, 2011	Sheet: 21 of 21	