7.3.1.2.3 Link Initialization

The DAC3xJ8x has an internal JESD204B receiver logic block, which handles the initial JESD204B link establishment for up to two independent links (i.e. link0 and link1). By default, the JESD204B block is in initialization mode and reset state (i.e. config74 (0x4A), init\_state = 2b’1111 and JESD\_reset\_n = 2b’0). In this stage, the JESD204B receiver block will not start the link establishment.

In order to start the JESD204B link establishment, the system must have the following conditions:

1. The JESD204B transmitter logic device (i.e. FPGA or ASIC) must be initialized and ready for link establishment.
2. The DAC3xJ8x receiver logic block must be out of initialization state and reset state.
	1. Set the JESD204B block to exit out of the reset state: JESD\_reset\_n = 2b’1 in config74 (0x4A).
	2. Set the JESD204B block to exit out of the initialization state: init\_state = 2b’0000 in config74 (0x4A).

Note: TI recommends programming step 2a and 2b separately.

1. The correct SYSREF signal is applied to the DAC3xJ8x SYSREF receiver block. The SYSREF signal is based on the programming of sysref\_mode\_link0 and/or sysref\_mode\_link1 in config92 (0x5c) register.

Once the system environment satisfied the conditions listed above, the DAC3xJ8x will pull the associated ~sync signal to logic LOW. The physical reflection of ~sync signal will be based on the programming of syncncd\_sel, syncnab\_sel, and syncn\_sel of config97 (0x61) register. The syncncd\_sel reflects the output of SYNCCD CMOS signal, the syncnab\_sel refelects the output of SYNCAB CMOS signal, while the syncn\_sel reflects the output of SYNCB LVDS signal. Each physical output signal can reflect link 0 and/or link1. For instance, syncncd\_sel can be programmed to reflect link1 ~sync status by programming syncncd\_sel as 2b’0010, and syncnab\_sel can be programmed to reflect link0 ~sync status by programming syncnab\_sel as 2b’0001. To have a master gating signal to reflect the status of both link0 and link1 ~sync signals accordingly, program the syncn\_sel to be 2b’0011. In this fashion, the LVDS SYNCB signal will reflect the status of both links with the ~sync of link0 and ~sync of link1 in an logic AND function.

If the ~sync signal is in logic LOW, the JESD204B transmitter logic device will accept the ~sync signal and start transmitting K28.5 common characters onto the RX lanes. The DAC3xJ8x JESD204B receiver block will interpret these characters and start the code group synchronization (CGS). Once CGS completes, the ~sync signal will be pulled to logic HIGH. This will be reflected physically onto the programmed SYNCCD, SYNCAB, or SYNCB outputs. If both link0 and link1 are implemented in the system with a single physical output reflecting the link status of the two links, then the physical output will not be pulled to logic HIGH until both ~sync status of link0 and link1 are logic HIGH after successful CGS stage. I.e. if syncn\_sel is programmed to be 2b’0011, the LVDS SYNCB will only be pulled to logic HIGH once both link0 and link1 achieves successful CGS stage.