Application Report
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Correcting the Low-Frequency Response of the ADS42LBxx, ADS42JBxx for Time-Domain Applications

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ABSTRACT

In this application report, simple schemes are described to correct the low-frequency response of ADS42LBxx, ADS42JBxx family of analog-to-digital converters (ADCs). The described schemes are useful for time-domain applications where the ADC samples a low-frequency pulse signal. These schemes are simple to implement in either analog or digital domains with minimal changes to the bill of materials (BOM).

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1 Introduction

TI's ADS42LBxx, ADS42JBxx (that is, ADS42LB49, ADS42LB69, ADS42JB46, ADS42JB49, and ADS42JB69) series of devices are a family of high-linearity, dual-channel, 14- and 16-bit, 250-MSPS ADCs with double data rate (DDR), quad data rate (QDR) low-voltage differential signaling (LVDS) or JESD204B interface options. The analog input buffer in these devices is designed to provide excellent spurious-free dynamic range (SFDR) over a large input frequency range (up to 300 MHz) with low-power consumption and maintain uniform input impedance.

1.1 Analog Input Buffer at Very Low Input Frequencies

Although the buffer response (transfer function) remains flat in nearly the entire Nyquist band, when the input frequency is very low (in the kHz range) a high-pass filter (HPF) type of response is exhibited, as shown in Figure 1.

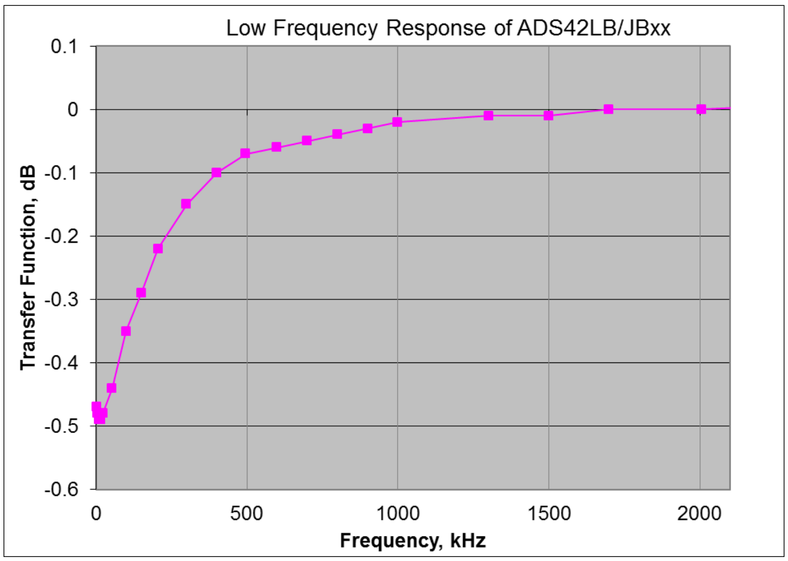

Figure 1. Input Buffer Transfer Function for Very Low Inputs Frequencies in the ADS42LBxx, ADS42JBxx

1.2 Explanation

For enhancing device linearity, the input buffer is implemented differently than usual. Figure 2 shows the implementation of the analog input buffer. This implementation has two paths: high gain (G = 0.95) and low gain (G = 0.05), as shown in Figure 2. The high gain path is straight and the low gain path has a first-order RC high-pass filter with a typical 3-dB cut off frequency of f_0 = 190 kHz, where w_0 is the corresponding frequency in radians per second. Although this implementation improves linearity at high frequencies, artifacts may result in the low-frequency signals in time-domain applications that deal with pulse signals, as shown in Figure 3.

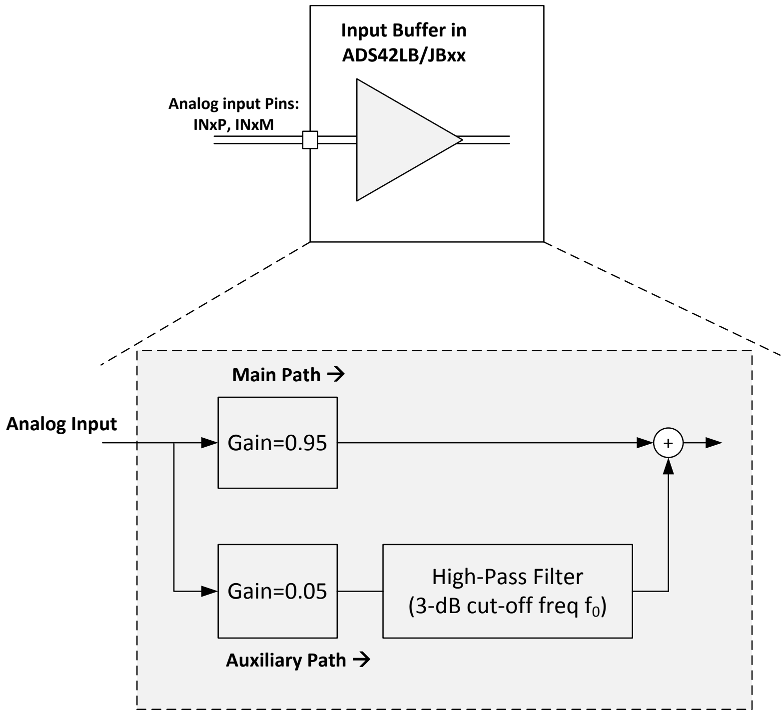

Figure 2. Input Buffer Implementation

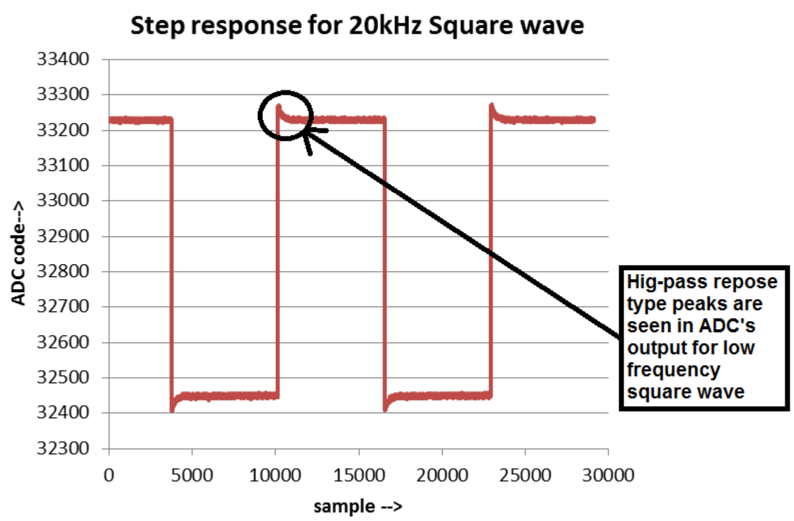

Figure 3. Time-Domain Response (16-Bit Device)

2 Solution

The problem for time-domain pulse applications can be corrected by either using an analog or digital compensation network.

1. Analog approach: designing a compensating network before the analog inputs corrects for the input buffer HPF-like behavior.
2. Digital approach: design a digital filter that has an inverse response of the analog input buffer of the device.

   Using simple math, the transfer function of the input buffer illustrated in Figure 2 is derived as Equation 1:

$$H_{(S)} = (G \times w_0 + s) / (w_0 + s) \quad (1)$$

where

- $w_0 = 2 \times \pi \times f_0$,
- f_0 is the cut-off frequency of the HPF in the input buffer (typical value = 190 kHz)
- G is the gain of the main signal path in the buffer (typical value = 0.95)

The analog or digital networks must be designed with a transfer function that is an inverse of the transfer function of the input buffer shown in Equation 1 so that the overall response to low input frequencies becomes flat.

In an analog approach, such a network can be implemented using resistors and capacitors and kept before the analog input pins of the device; whereas in a digital approach, the network essentially can be realized by an infinite-impulse-response (IIR) filter implemented in the receiving field-programmable gate array (FPGA) or application-specific integrated circuit (ASIC).

Note that at very-low input frequencies, the high-pass structure inside the analog buffer results in a degradation of linearity (for example, degraded harmonic or SFDR performance) as well. The compensating network only corrects the low-frequency response of the buffer and cannot correct the linearity degradation.

2.1 Using an Analog Compensation Network

An external network that can compensate for an auxiliary HPF present inside device can be designed in a simulation deck of the advanced design system (ADS) tool shown in Figure 4. In this network, the compensating resistors and capacitors can be chosen by using Equation 2 and Equation 3:

$$R_{COMP} = R_S \times 2 \times (1 - G) / (2 \times G - 1) \quad (2)$$

$$C_{COMP} = 1 / w_0 \times R_{COMP} \times (2 \times G - 1) \quad (3)$$

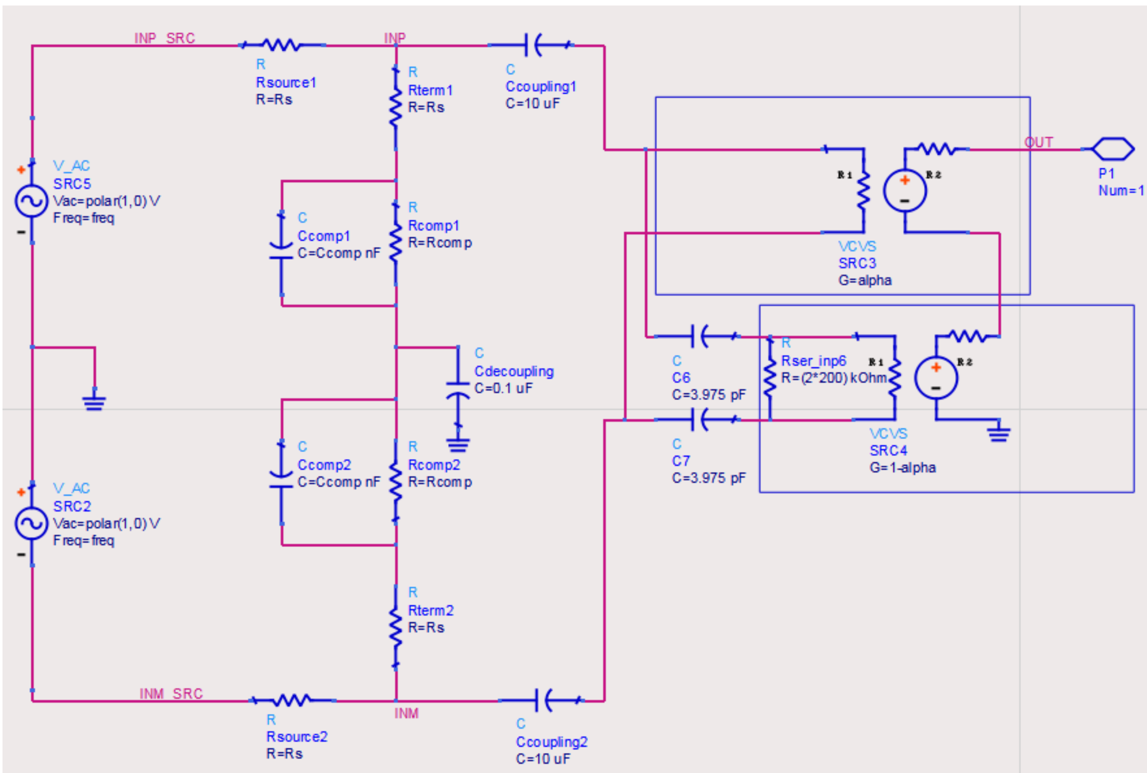

Figure 4. Adding an Analog Network Before the Input Pins of the Device

2.1.1 Experimental Results

In lab experiments, the following values were chosen for R_{COMP} and C_{COMP} to measure the effect of the compensating network:

- Source impedance R_S = 50 Ω
- R_{COMP}= 12.5 Ω
- C_{COMP} = 60 nF

Measurement data showed significant improvement in the frequency response of the device after the compensation network was placed before the device, as shown in Figure 5.

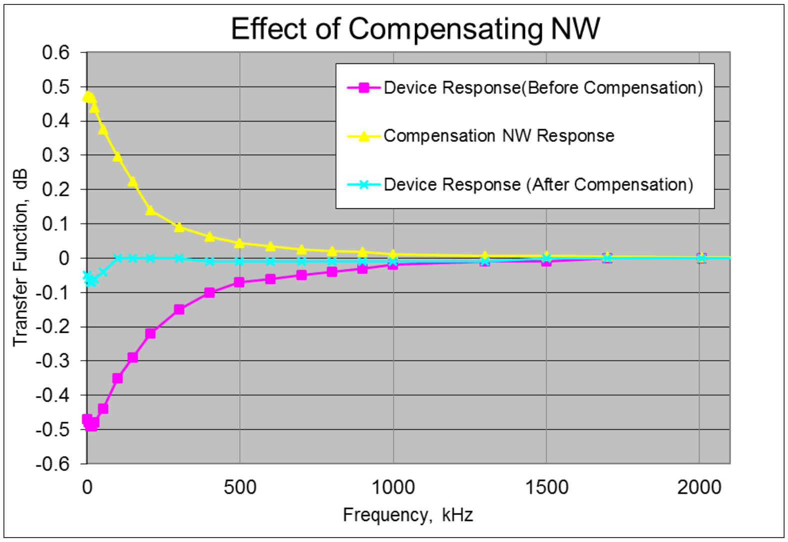

Figure 5. Effect of an RC Compensating Network on the Low-Frequency Response of the Device

To evaluate the affect of the network on the step-response of the device, a circuit was tested with a 50-kHz square-wave pulse and the device output was analyzed in time-domain. As shown in Figure 6, significant correction was achieved in the device output when the compensation network was added before the analog inputs.

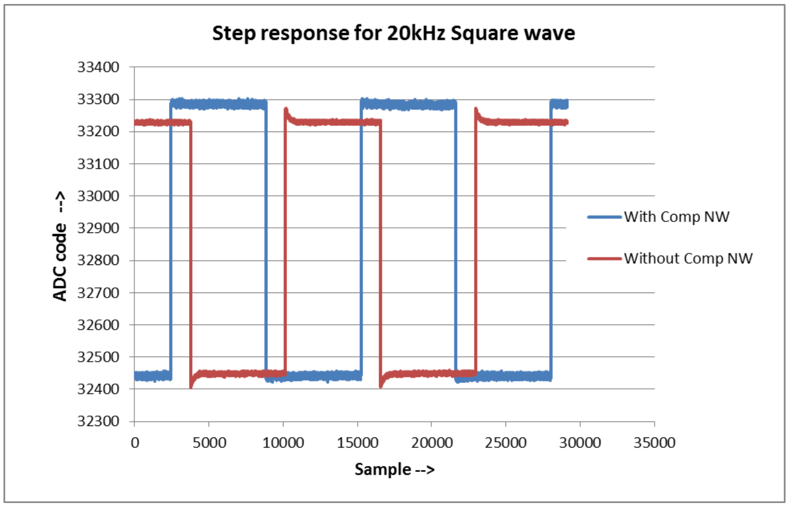

Figure 6. Effect of an RC Network on the Step-Response of the Device

2.1.2 Using a Digital Compensation Network

A digital compensating circuit can also be worked through to compensate for the device response. Given that the sampling rate is 250 MSPS and the corner frequency is approximately 190 kHz, the digital compensating network can be reasonably effective.

Reproducing Equation 1 here where $w_0 = 2 \times \eta \times f_0$ and f_0 is the cut-off frequency of the HPF in the input buffer (typical value = 190 kHz) yields Equation 4:

$$H(s) = (G \times w_0 + s) / (w_0 + s)$$

where

- $w_0 = 2 \times \pi \times f_0$ (4)

The inverse of this response must be implemented using an IIR structure as the compensating circuit, as calculated by Equation 5:

$$H_{COMP}(s) = (w_0 + s) / (G \times w_0 + s)$$

where

- $w_0 = 2 \times \pi \times f_0$ (5)

Now, using a bilinear first-order approximation for $s = \log_e(z) \approx (1 - z^{-1}) / (1 + z^{-1})$, the equivalent transfer function is given by Equation 6:

$$H_{COMP}(z) = (w_0 + 1 + (w_0 - 1)\, z^{-1}) / (\, G \times w_0 + 1 + (G \times w_0 - 1)\, z^{-1}\,)$$

where

- $w_0 = 2 \times \pi \times f_0 / f_S$ (6)

The circuit implementation of this structure is shown in Figure 7.

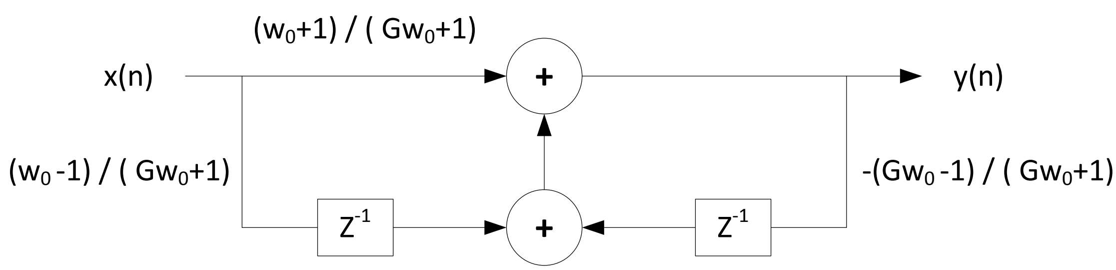

Figure 7. Digital Compensating Network Using an IIR Filter

2.1.2.1 Experimental Results

A test 10-kHz square-wave was applied to the device without a compensation network onboard and the time domain output of the device was stored. An IIR filter, as shown in Figure 8, was implemented in MATLAB® by using G = 0.95 and f_0 = 195 kHz. Then, the time-domain output of the device was passed through the IIR compensating filter. Results are shown in Figure 9 and Figure 10. The IIR filter corrects the data significantly.

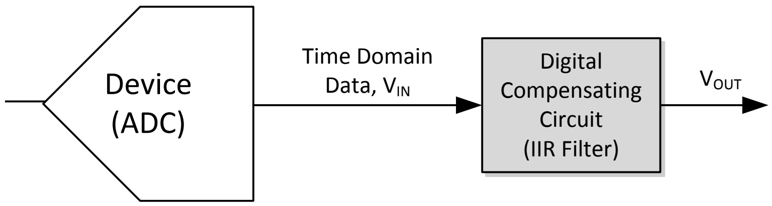

Figure 8. IIR Filter for Correcting the Low-Frequency Response of the Device

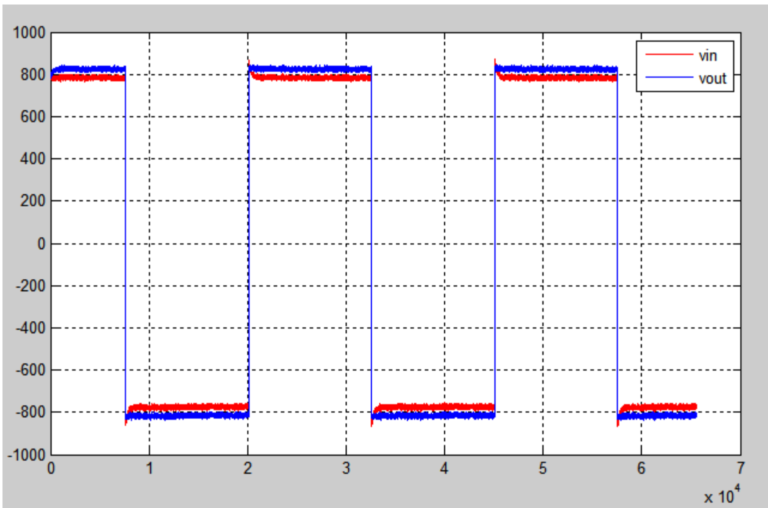

Figure 9. Effect of the Digital Compensating Network (IIR Filter) on the Step-Response of the Device

The IIR filter also corrected the low-frequency response of the device significantly as shown in Figure 10.

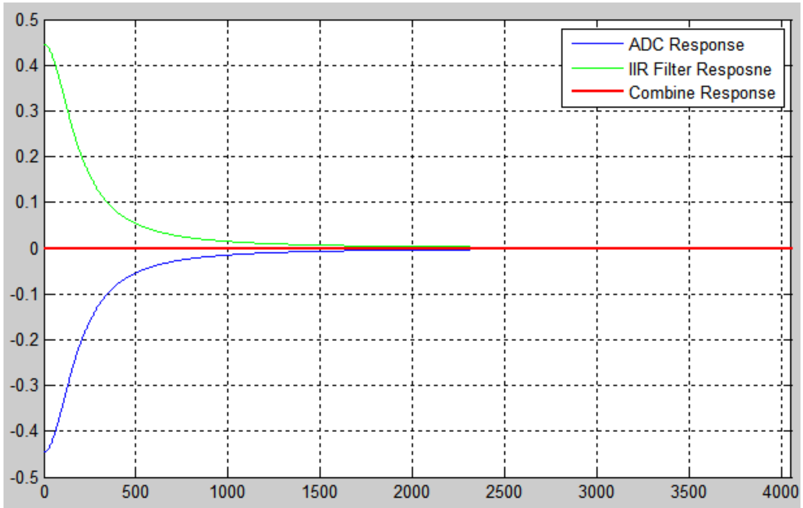

Figure 10. Effect of the Digital Compensating Network (IIR Filter) on the Low-Frequency Response of the Device

3 Effect of PVT

When designing the compensating network, note that the accuracy of the gain and corner-frequency values (0.95 and 190 kHz) of the auxiliary network in the device can vary over temperature and devices. Over the process-voltage-temperature (PVT) variation, gain G can change from 0.93 to 0.97 whereas the 3-dB frequency of the HPF can change from 150 kHz to 300 kHz. Changes in process corners for example, a different lot of devices) is the main contributor in the variation of G and f_0 as shown in Figure 11. These parameters remain almost impervious to change in voltage and temperature.

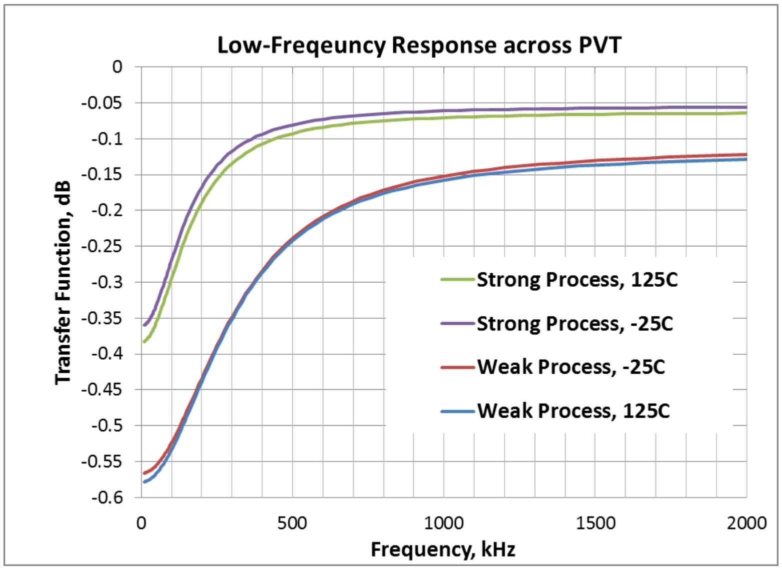

Figure 11. Effect of PVT Variation on the Frequency Response of the Device

4 Conclusion

This application report highlighted the high-pass type behavior of the frequency response of the ADS42LBxx, ADS42JBxx series of ADCs for very low input frequencies. This report also presented two easy schemes of correcting the low-frequency response. Depending upon resources, either an analog or digital compensation scheme can be used.

5 Reference

1. ADS42LB69 Data Sheet, SLAS904
2. ADS42JB69 Data Sheet, SLAS900