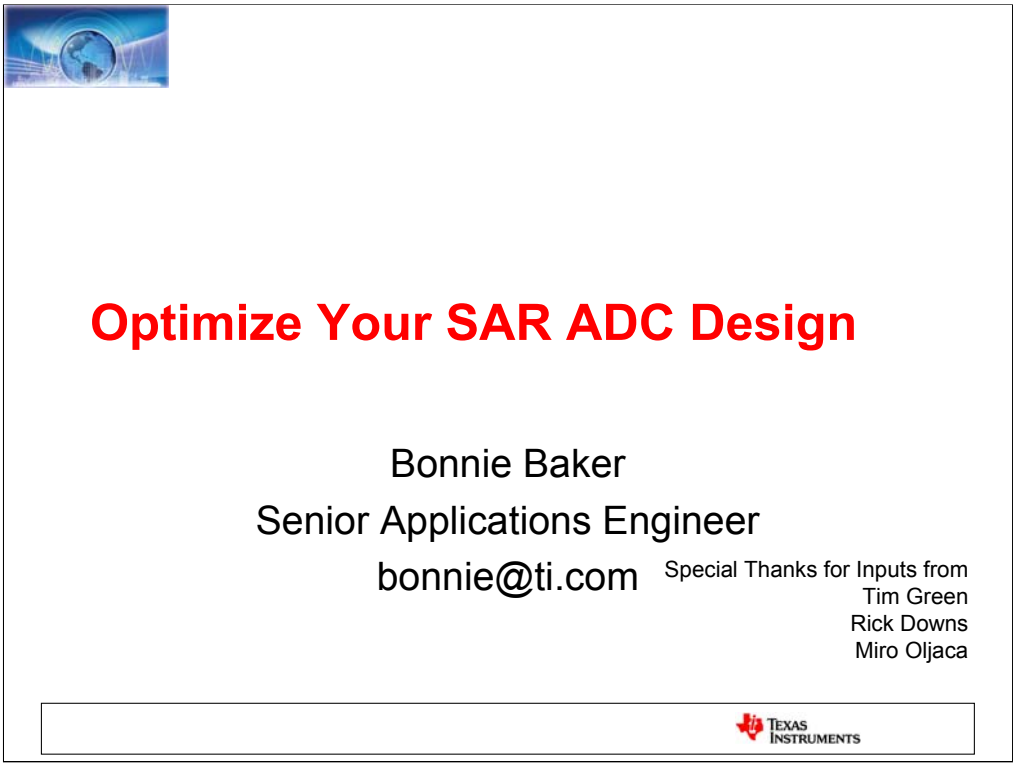
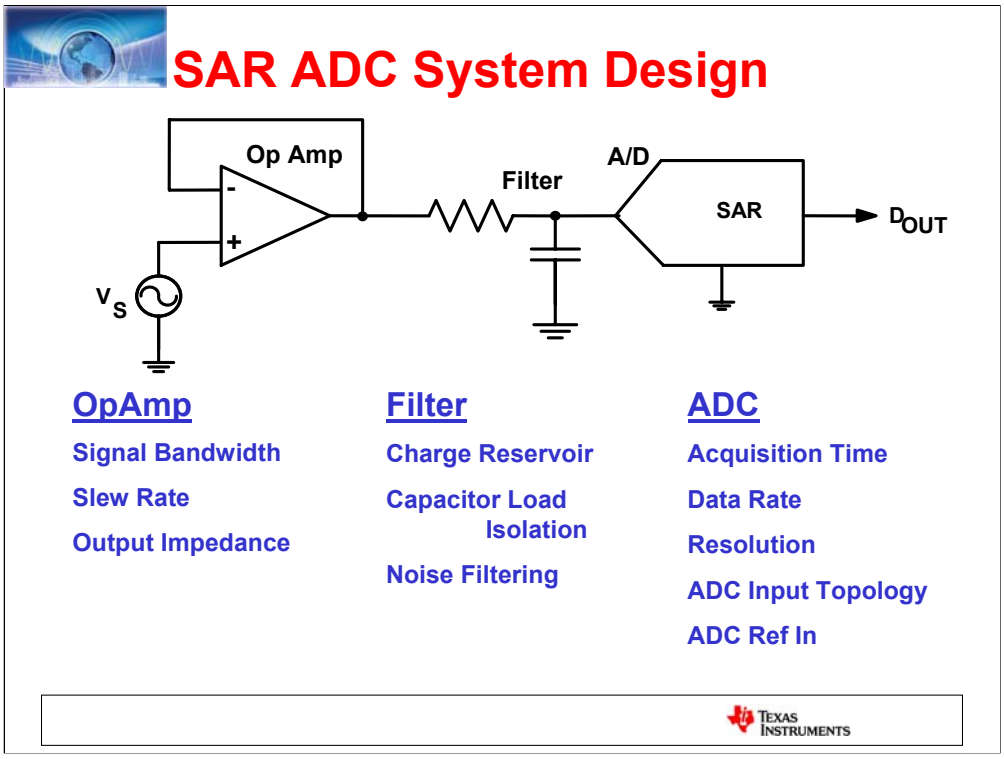
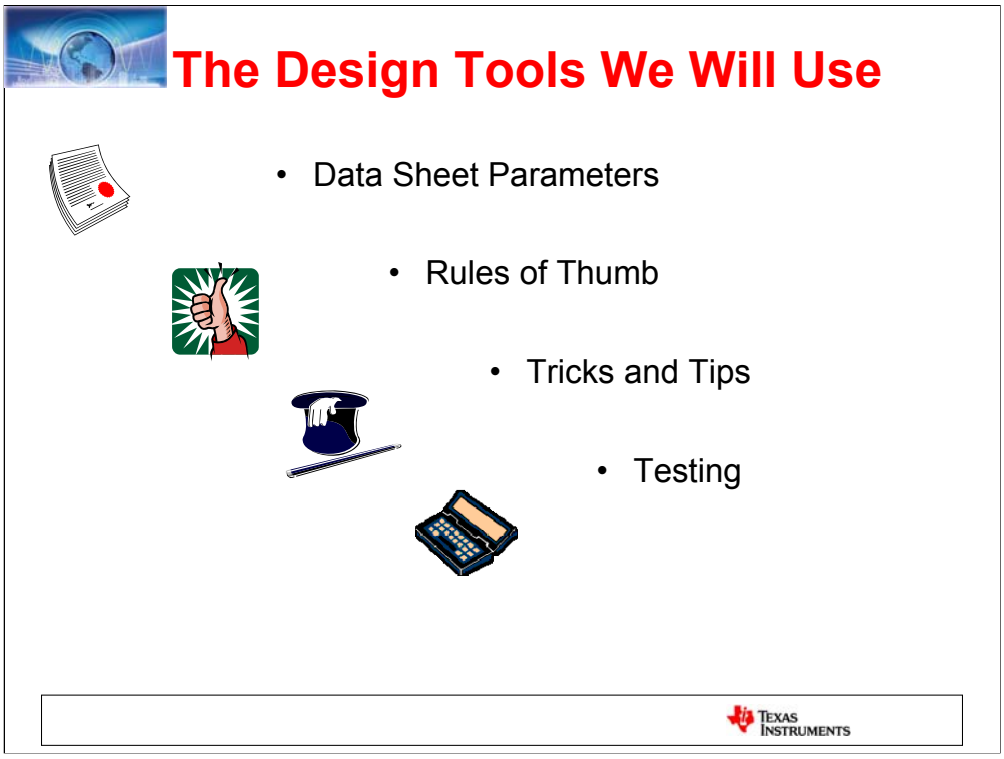


The most popular and versatile Analog-to-Digital Converter (ADC) has a Successive Approximation Register (SAR) topology. These converters work by comparing an analog voltage signal to known fractions of the full-scale input voltage and then setting or clearing bits in the ADC's data register. Modern SAR converters use a Capacitive Data Acquisition Converter (C-DAC) to successively compare bit combinations. Usually these devices have an integrated sample/hold input function. It is common to use an operational amplifier (Op Amp) to directly drive the input of a SAR Analog-to-digital converter (SAR-ADC). Although this configuration is an acceptable practice in manufacturer's data sheets, it has the potential to create circuit performance limitations. For optimum performance, C-DAC SAR-ADCs require the correct front-end buffer and filter. The additional input filter or RC-network will relax the driving Op Amp requirements. This presentation details the reasons for an input filter and buffer amplifier to the C-DAC SAR-ADC along with an analytical approach to selecting the filter components and op amp characteristics.



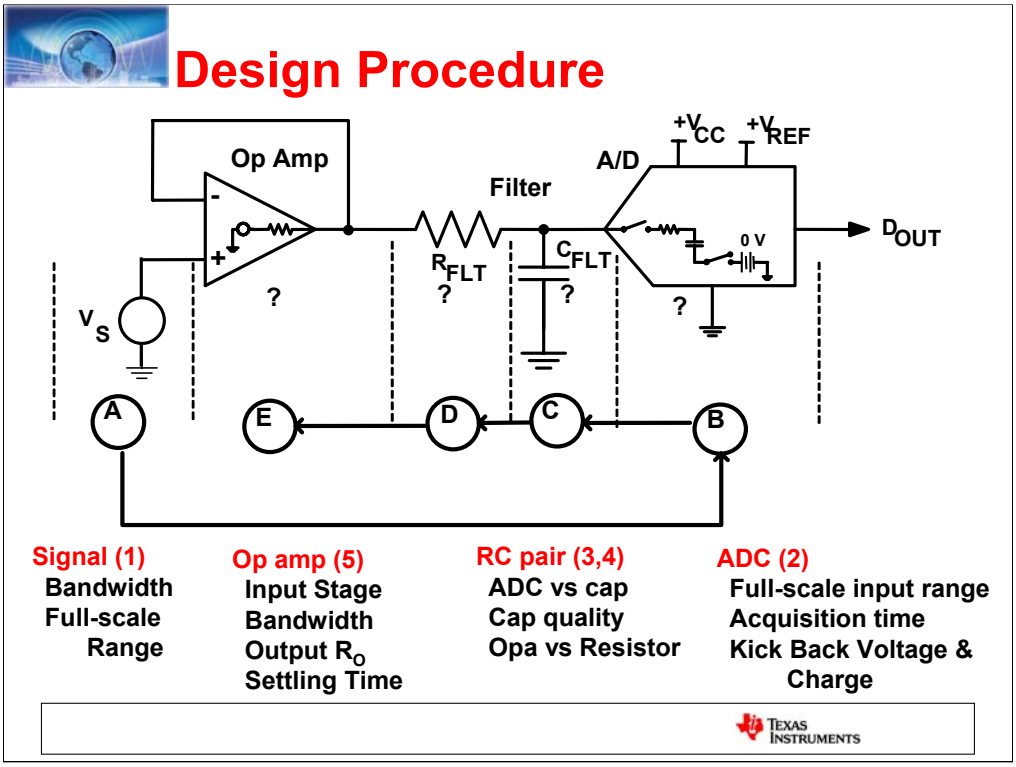
A typical input stage for a SAR ADC system is shown above. A buffer amplifier is used, driving a small RC-filter prior to the input to the ADC. We'll examine just what these elements do for us in this seminar. Each of these elements have a relationship to the preceding or the following element which will make the combination more powerful than the individuals.

As we can see, for each part of this circuit, there are many considerations, all of which potentially affect the accuracy and resolution of the system. When choosing components for this system, we must be mindful of all of these considerations.



Many articles have been written about choosing op amps for use in driving ADCs (see last page of this presentation). All of the articles point out things that we should watch out for. From these articles and this seminar, we will observe some guidelines and make it easier and faster to get to a good design.

The design procedure we will present contains some rigorous analysis, but also observes rules of thumb, some “tricks”, and of course refers to the datasheets of the products in our circuit. As always with analog circuitry and proof of function will be required with some testing and prototyping.

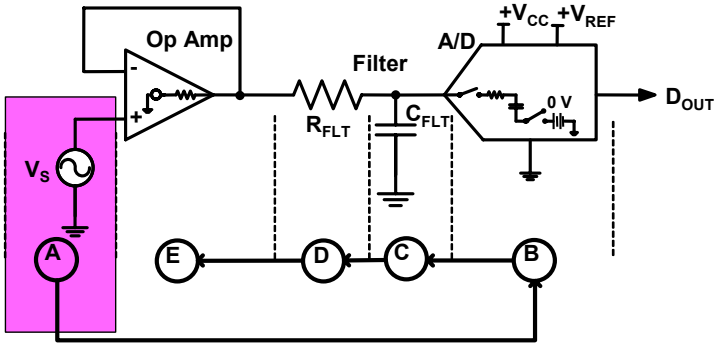


So this is how we design our SAR-ADC circuit from beginning to end. We will first determine what our input signal looks like in terms of the bandwidth and a full-scale range. Once we understand the characteristics of our input signal, we will take a look at the ADC. The ADC that we select should match the bandwidth of our input signal per nyquist. This device should also have an appropriate resolution for our signal. With the ADC selected, we will determine the acquisition time and the ADC sampling capacitance.

Once we've selected our ADC, we determine the values of the external input capacitance (C_{FLT}) and input resistance (R_{FLT}). We will find that the quality of our capacitor is critical if we are concerned about the distortion that will be generated by our circuit. The value of our capacitor insurers that our ADC will have ample charge for each conversion. The value of the resistor insurers that our operational amplifier will be stable.

We will finally select our operational amplifier. At this point, we will determine what style of the input stage we need. we will also select an amplifier that has ample bandwidth for the input signal.

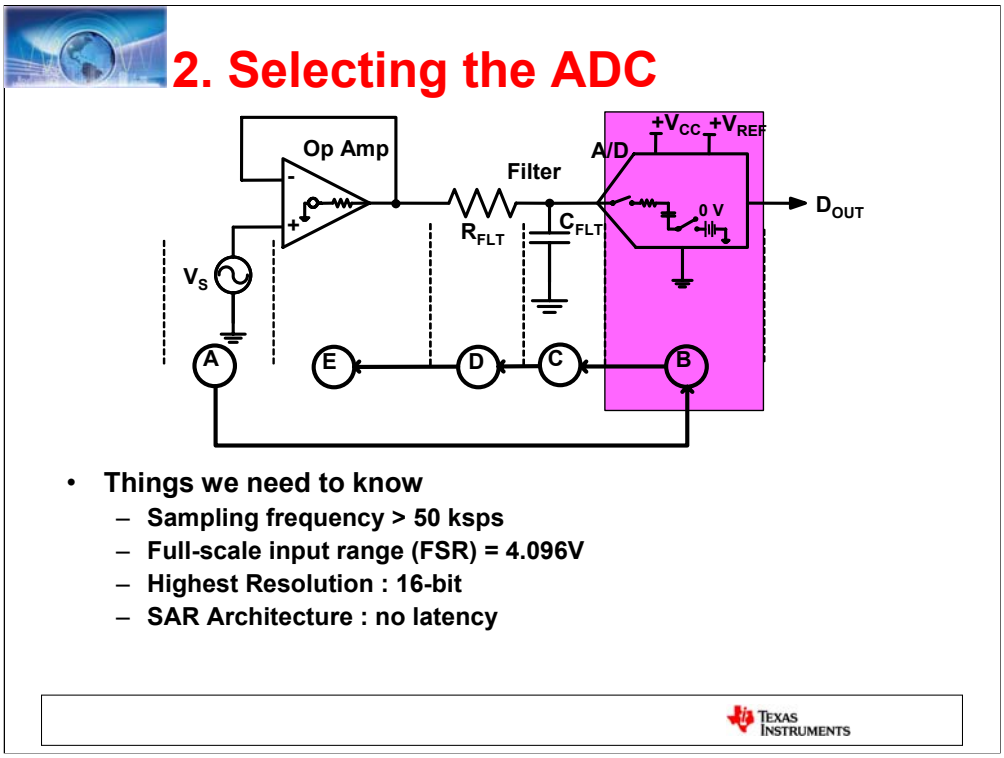
1. Define Input Signal



- **Highest Frequency**
  - **1 kHz (single channel)**
- **Largest Voltage Swing**
  - **0 to 4.096 V**
- **High Accuracy**
  - **62.5 μV LSB size or 16-bit with range of 4.096**

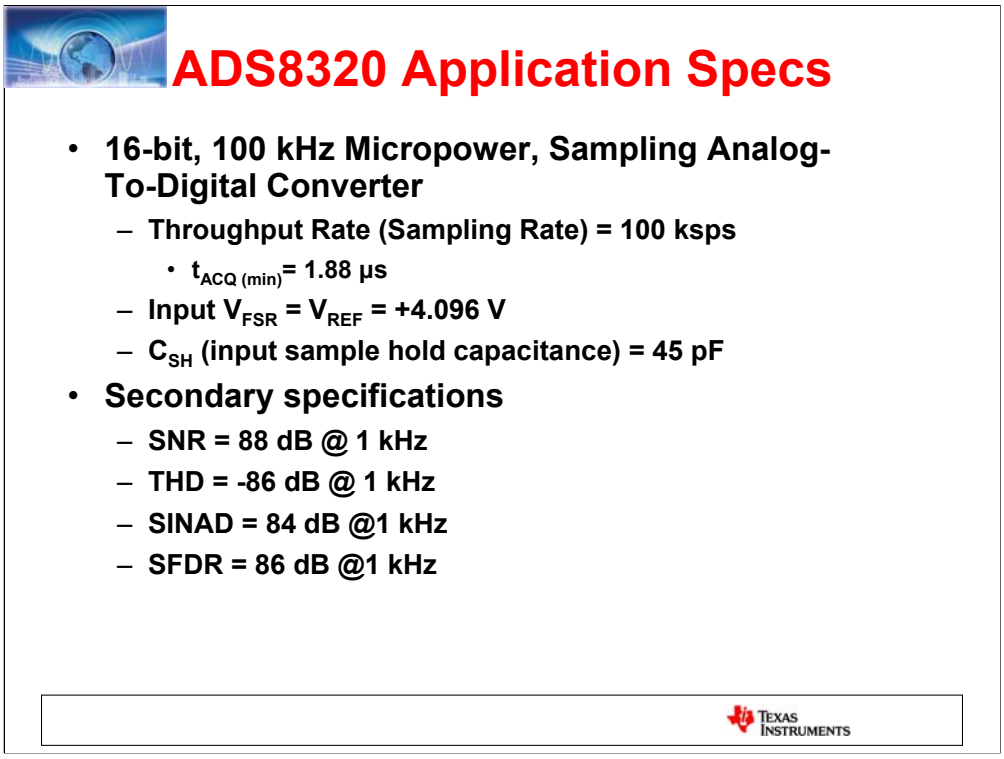
Texas Instruments

These are characteristics of the input signal that we will use in our discussion of our circuit. The highest input frequency in our SAR-ADC system is 1 kHz. The largest voltage swing of our ADC should be able to handle on its input from 0 to 4.096V. We want to have 16-bit resolution or a 62.5 μV LSB size to our analog signal. We will design the entire system around these specifications.



Once we know the pertinent characteristics of the input signal we can select the ADC for this circuit. In particular, we want an ADC that has a minimum sampling frequency that is two times higher than the maximum signal frequency plus an additional 10 to 20 x multiplier so that we capture a better picture of the input signal. With this logic we will need an ADC that has a maximum sampling frequency of at least 20 ksps.

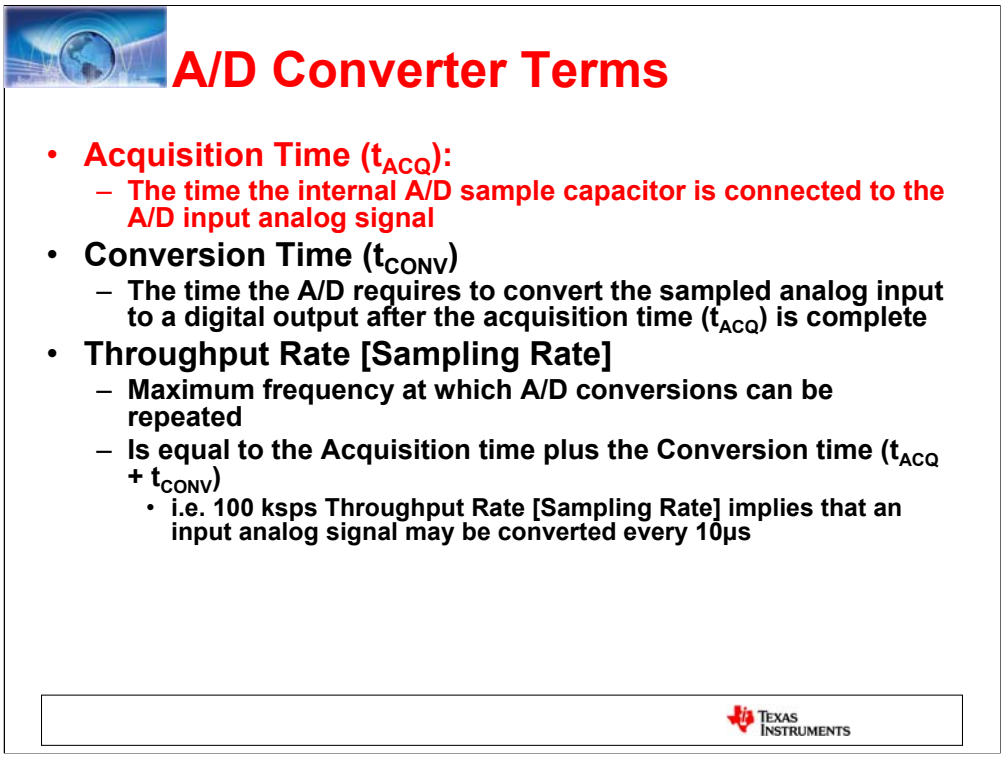
Given the sampling rate of > 20 ksps, the appropriate architecture for this application circuit is a SAR converter. We will use a SAR architecture for its low latency, and chose this particular converter architecture because it offers the highest speed and resolution combination of converters that operate at this sampling speed.



For the TI product line, the ADS8320 best matches our input requirements. This slide shows some of the important ADS8320 specifications we'll need to know. Fortunately, all of these parameters are specified in the datasheet.

The maximum throughput rate of the ADS8320 at 100 ksps exceeds the >20 ksps requirement. The input range of the ADS8320 is equal to the reference voltage supplied to the converter. A 4.096 reference voltage is recommended. Specifications that we are going to need through out the remainder of this discussion is the signal acquisition time (t_{ACQ} = 1.88 µs) and the value of the input capacitance of the SAR converter. In the case of the ADS8320, the input capacitance (C_{SH}) is equal to 45 pF.

Secondary specifications, such as Signal-to-Noise Ratio (SNR), Total harmonic Distortion (THD), Signal-to-Noise Ratio plus Noise (SINAD), and Spurious Free Dynamic Range are specifications that we will keep our eye on as we proceed through the design.

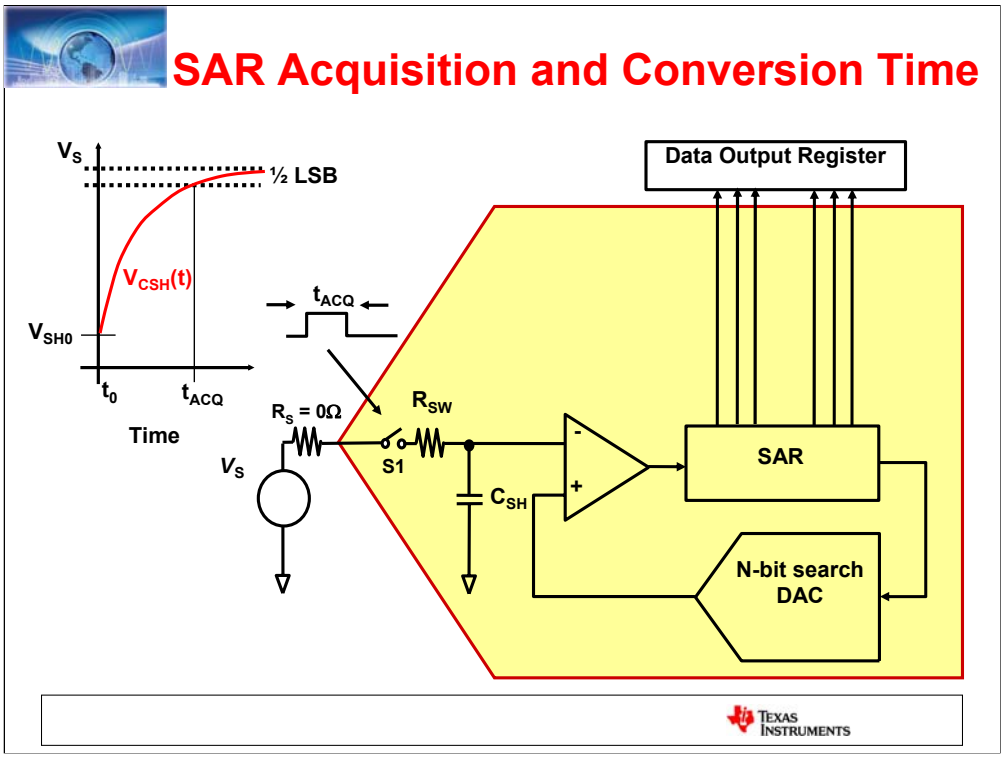


Before going further, it's important to understand some of the timing characteristics of the ADC that we'll be using.

A SAR ADC takes a sample of a signal at a moment in time, and converts that one sample to a digital value. It takes a certain amount of time for the input signal to be connected to the internal capacitor of the ADC and store its voltage on the internal sampling capacitor. The amount of time allowed to get the input voltage stored on the ADC input capacitor to the accuracy required by the ADC is the **acquisition time** of the converter.

Once the sample voltage is stored on the sampling capacitor, the actual conversion process takes place, where the sample is successively compared to known fractions of charge. The time it takes to make all of the comparisons and generate the digital value is the **conversion time**.

To accomplish a complete conversion, both the acquisition and conversion times must pass. The fastest a system can sample and convert a signal would be the rate at which it can successively sample. The **throughput rate** of a converter describes the fastest speed that the ADC can successively sample. This rate must also include the settling time of the converter's input stage, as well as settling times for the other amplifiers and elements in the signal chain.



A typical SAR conversion cycle has two phases; a sampling phase and a conversion phase.

During the sampling phase, the analog input signal charges the ADC's Sample-and-Hold (S/H) capacitor (C_{SH}) through the switch resistance (R_{SW}) to a level proportional to the analog input. The combination of the switch resistance (R_{SW}), the source resistance (R_S), and the sampling capacitor (C_{SH}) determine the rate of change of the charge on the sampling capacitor (C_{SH}).

The diagram in the upper left portion of this slides illustrates the rise time characteristics of the voltage on C_{SH} during the acquisition phase. As expected, this rise time has a single pole response.

Conversion begins immediately following the sampling phase with the opening of the input switch (S1). Conversion successively compares the unknown value of the charge stored on the S/H capacitor to known fractions of charge. After each comparison, logic on the ADC determines if the unknown charge is greater or smaller than the known fractional charge.

At the end of the process the data register will contain a binary value proportional to the value initially placed on the S/H capacitor. The user reads this value out as converted data.

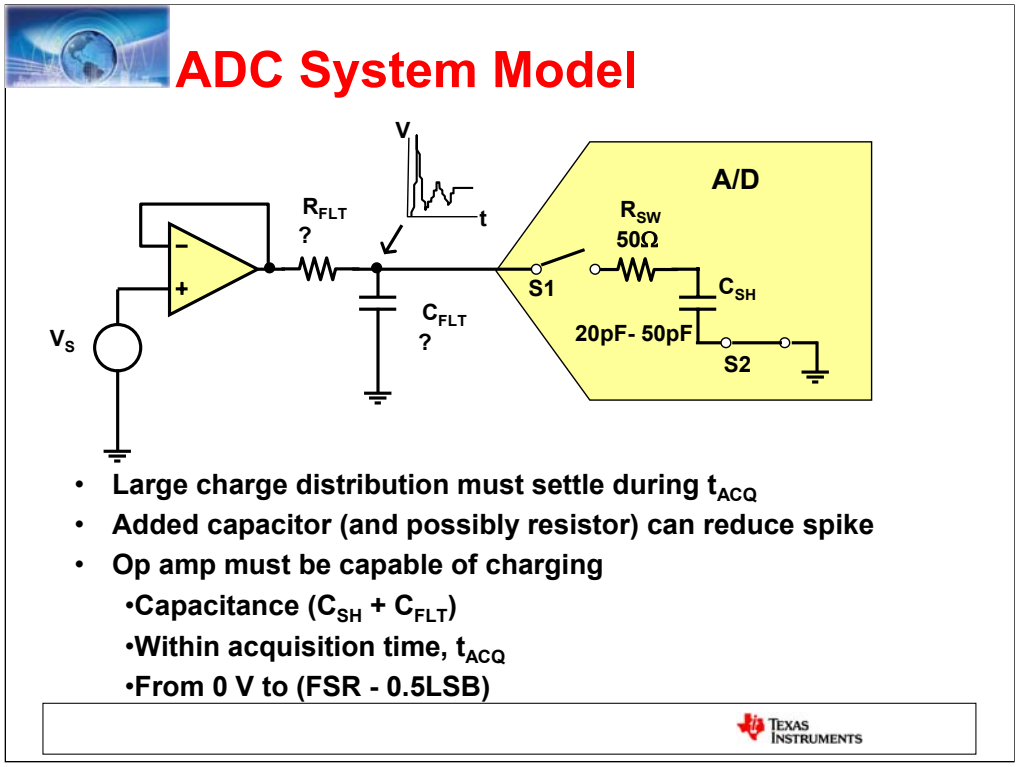
As shown in the diagram above, the converter we are evaluating does not have an internal input buffer amplifier. This may not be the case with the particular SAR converter you may use. The product data sheet provides details on the input structure for a particular product.

Single-pole, Time Constant Multiplier

Number of bits	0.5LSB	Time Constant (k) Multiplier
10	0.0488281%	8
12	0.0122070%	9
14	0.0030518%	11
16	0.0007629%	12
18	0.0001907%	13
20	0.0000477%	15
22	0.0000119%	17
24	0.0000030%	18

Texas Instruments

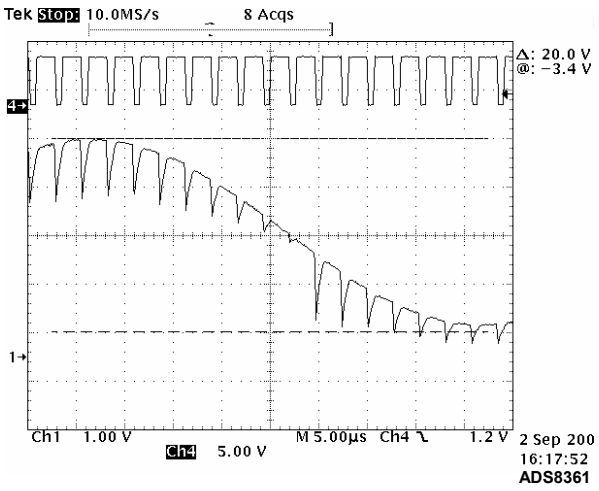
The amount of time needed to settle the input structure of the SAR-ADC depends on the number of bits of the converter. This table lists the number (k) of time constants (τ) required to settle to within a half LSB to a given number of bits. For our 16-bit example, we will allow the twelve time constants for the ADC input stage to settle or k =12. The time constant of the ADS8320 alone is equal to R_{SW} (~100 Ω) times C_{SH} (= 45 pF, typ) or $\tau_{ADC} = C_{SH} \times R_{SW}$ = 4.5 ns. The input structure of the ADC requires a total of k x τ_{ADC} time or 540 ps to charge. When we add the external RC network before the ADC, the time constant of the system will change to become τ_{FLT} which equals C_{FLT} times R_{FLT}.



The input of a modern SAR ADC can be modeled as shown above. At any time, the sampling capacitor can have an initial voltage ranging from 0V to the supply voltage, from sample to sample. This presents a very dynamic load to the driving op amp. Because the sample capacitor may have residual charge on it from a previous conversion, it is not uncommon for this charge to discharge back out of the ADC input terminal. This “kickback” charge injection can sometimes be seen with an oscilloscope.

To help reduce this effect, and to provide a charge reservoir for charging the sampling capacitor (C_{SH}), an $R_{FLT}|C_{FLT}$ circuit is added between the op amp and the ADC. The op amp must be capable of driving this capacitive load, and settle from zero volts to within full-scale range (FSR) minus 0.5LSB of V_S, within the acquisition time of the ADC. Generally, this means that the op amp must have a low wideband open-loop output resistance (R_O). We’ll look at the op amp requirements in more detail later.

SAR ADC Input Charge Distribution



- **Op amp requirements**
  - **Must charge the ADC cap quickly & accurately**

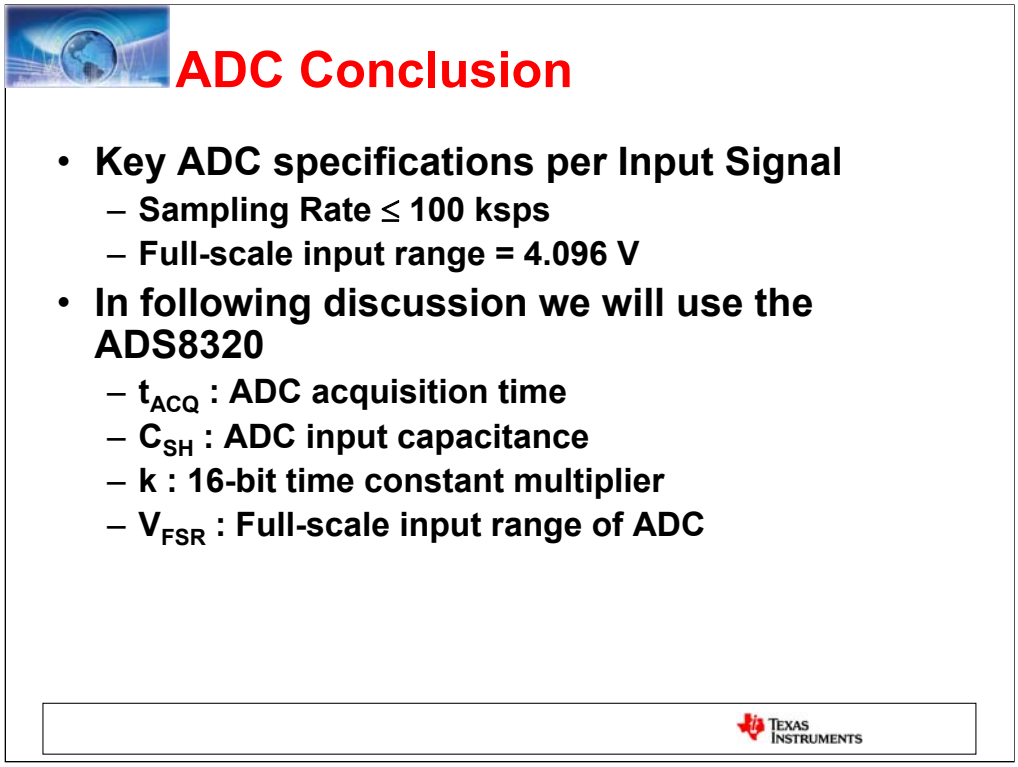
TEXAS INSTRUMENTS

This is a scope capture of the input of a SAR ADC, which clearly shows the charge distribution at the input of the 16-bit ADS8361. This particular converter (ADS8361) shows about a 20mV spike, which is equivalent to a little more than 16LSBs.

The scope photo in this slide shows the ADS8361 charge injection transients. This data was generated by placing a 10 kΩ resistor between the buffer op amp and the SAR ADC input, so we could clearly see the spikes. In general, the input impedance presented to a SAR converter should never be as high as 10 kΩ. If we can see spikes like this on the input to our SAR, it means that the impedance of our source is too high.

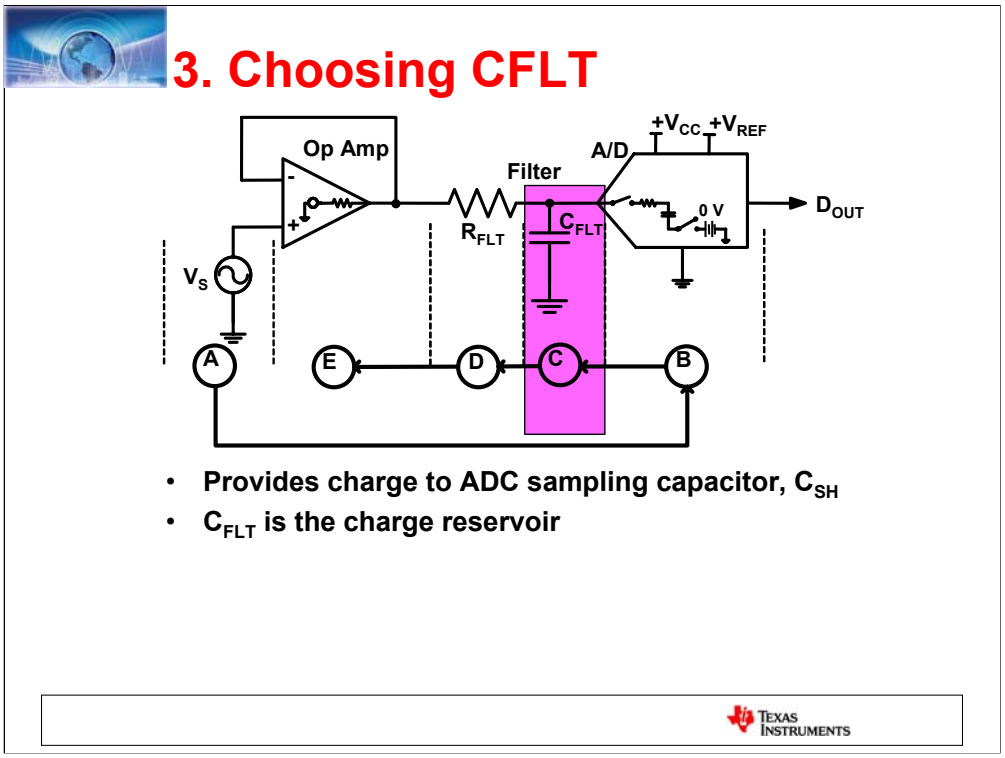
Even with lower impedances, we may see spikes at the input of our SAR ADC. The spikes are caused by the internal switching while the converter is acquiring the input signal value. If these spikes do not settle back to match the input value within the acquisition time of the converter, there may be a measurement error. These spikes also present a very demanding load to the driving op amp.

The functions of the $R_{FLT}|C_{FLT}$ filter in front of the SAR is to provide a path for this charge injection to come and go from, and to do some minimal isolation of the op amp output to these transients.



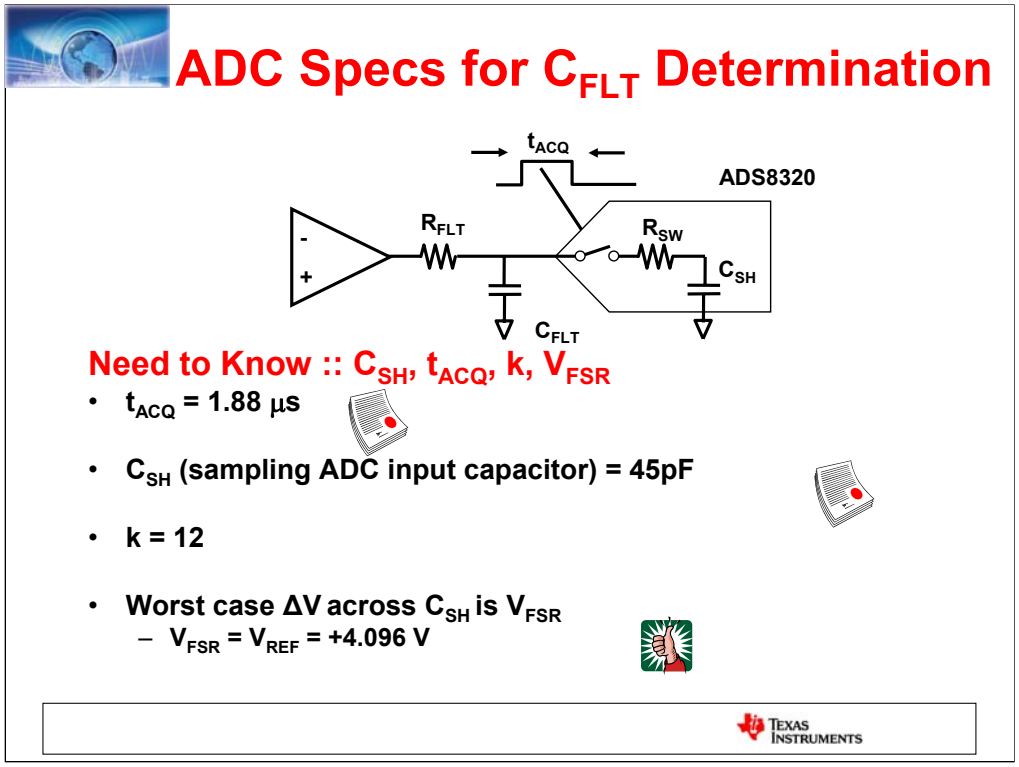
The converter that we have chosen for our example circuit is the ADS8320. This converter is capable of converting at a 100 ksps rate. The ADS8320 can also operate with a full-scale voltage input range of 4.096V if the reference to the converter, V_{REF}, is equal to 4.096V.

As we define the value of the external capacitor, C_{FLT}, we need to know the acquisition time of the converter (t_{ACQ}), the ADC input capacitance (C_{SH}), the time constant multiplier for an 16-bit converter (k), and the converter full-scale input voltage range (V_{FSR}).



C_{FLT} serves several purposes. The first purpose that this capacitor serves is to store energy to charge the ADC internal sampling capacitor (C_{SH}). Secondly, C_{FLT} provides a place for the internal capacitor's charge to go.

Due to the storage capabilities of C_{FLT}, we will sometimes refer to this capacitor as the "flywheel" capacitor. C_{FLT} has this alternative name because, like a flywheel, it stores energy for when we need it; during the acquisition time of the ADC. Another name we will use to describe C_{FLT} is charge reservoir.



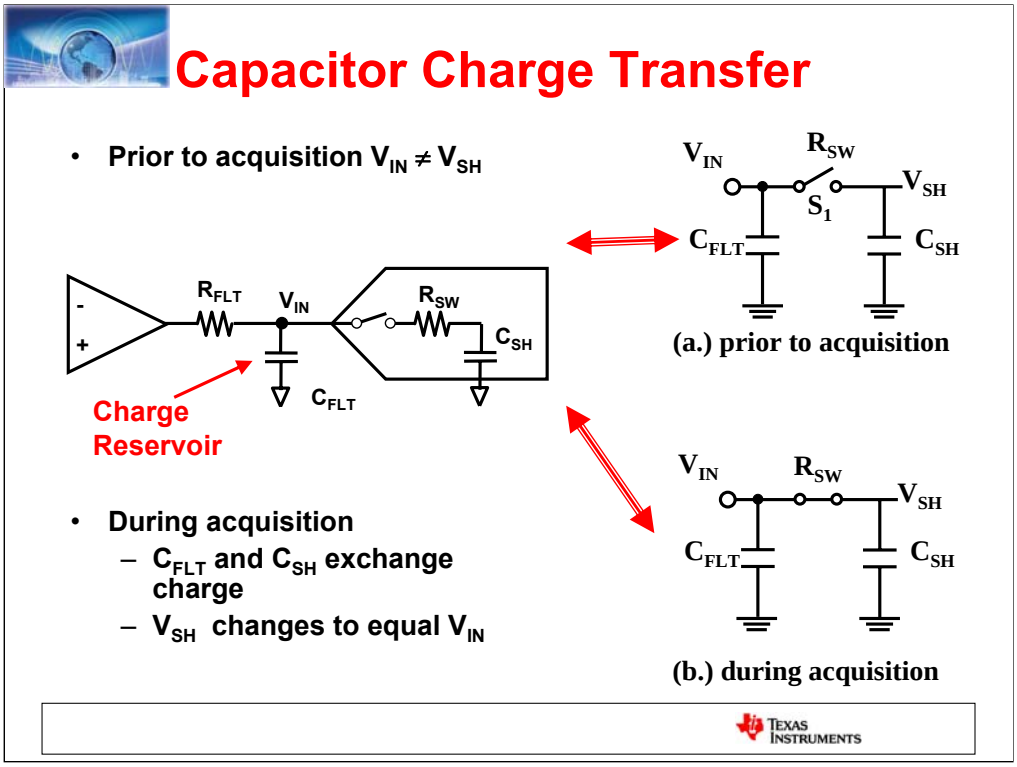
Continuing on, the ADC values that we are going to use in our calculations are t_{ACQ}, C_{SH}, k, and V_{FSR}.

As we select the value for C_{FLT}, it is critical that we meet the acquisition time (t_{ACQ}) requirements of the converter. This will be specified in the manufacturer's data sheet. The size of the external capacitor must facilitate this effort by minimizing the impact of the charge injection on the output of the driving op amp. This charge is generated by the ADC input structure at the beginning of the acquisition period.

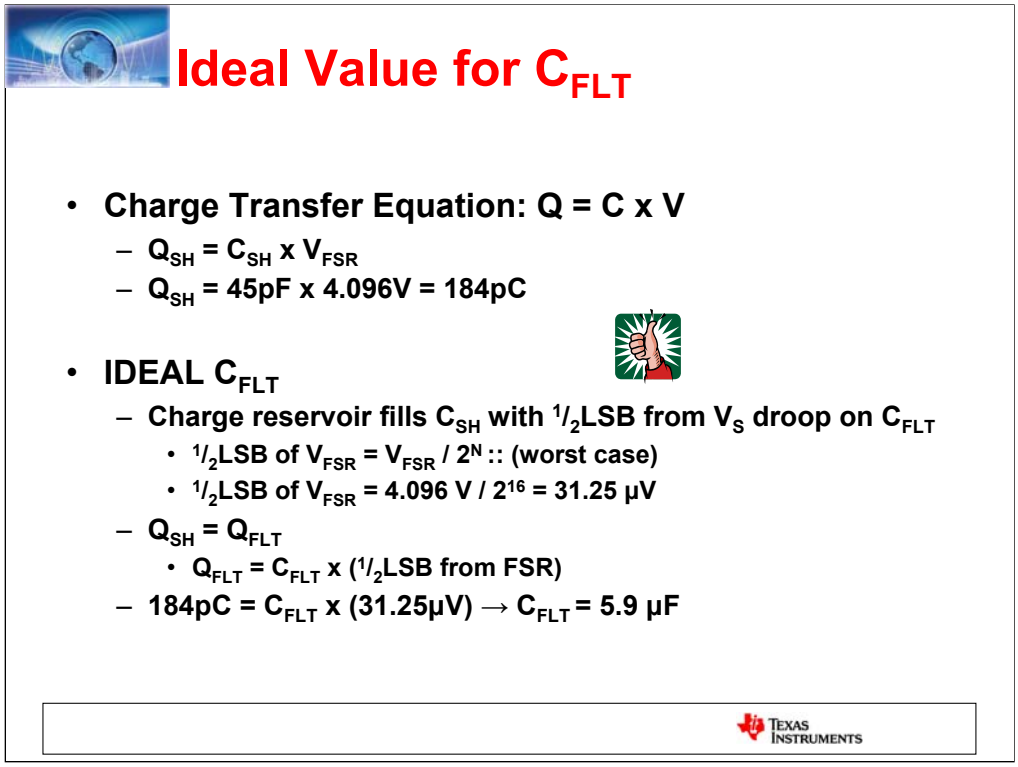
We will need to know the value of the ADC input capacitance (C_{SH}) to insure that the external capacitor reduces the impact of the charge injection from the converter on the operational amplifier. Again, the ADC input capacitance value can be found in the manufacturer's data sheet.

We have identified a time constant multiplier (k, slide 10) equal to twelve for a 16-bit ADC. This number will be used when we size the external capacitor.

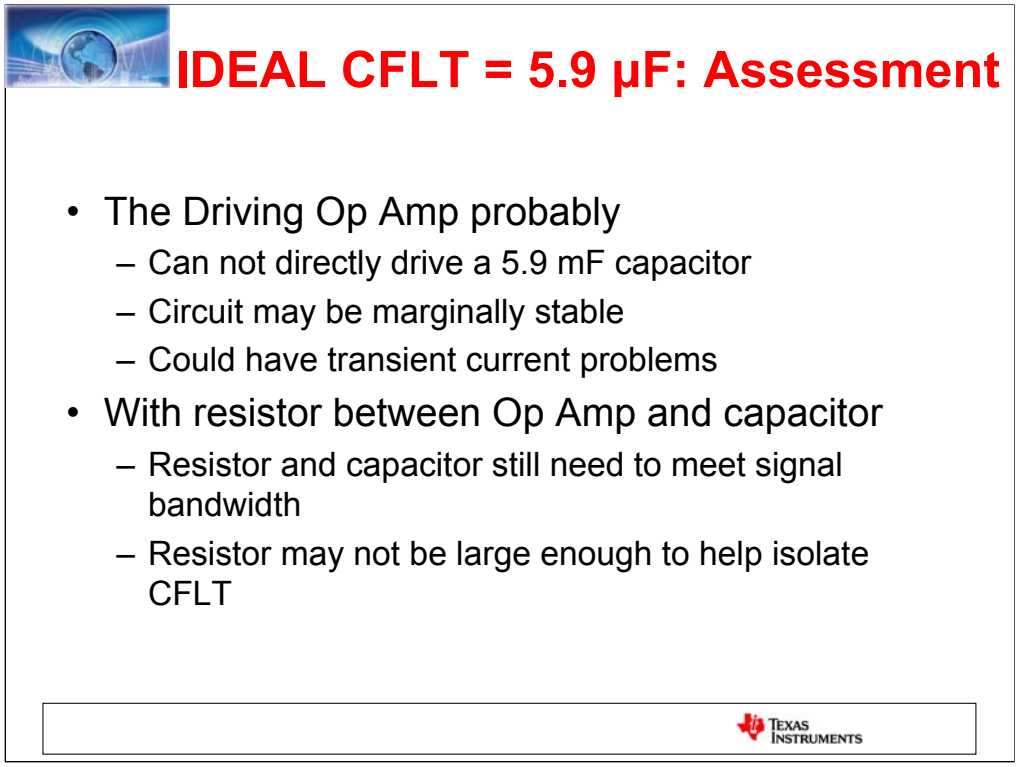
Finally, we will perform a worst case calculation using the full-scale range of the converter as a maximum input and the initial voltage on C_{SH} equal to zero volts. Although it is possible to characterize the charge injection characteristics of the ADS8320, a worst case assumption will make our work applicable to all SAR converters.



This slide shows a simplified circuit for the capacitive input stage of the circuit in the previous slide. Prior to the input signal acquisition, S1 is open (diagram a). The input capacitor, C_{FLT}, has an initial voltage of V_{IN} and the voltage across the sample capacitor, C_{SH}, is V_{SH0}. S1 closes at the start of signal acquisition (diagram b). After the sampling switch (S1) closes, the capacitor voltages, V_{IN} and V_{CSH}, start to settle to the final value of V_{IN} as the charge quickly redistributes between C_{FLT} and C_{SH}.



We can calculate the charge (Q_{SH}) needed to charge the internal sampling capacitor to the input voltage. Ideally, the charge reservoir provides enough charge to the internal sampling capacitor so that the voltage on the filter capacitor droops by less than 0.5LSB of V_S. If we assume the worst case condition, V_S equals V_{FSR} and 0.5LSB of V_{FSR} equals 31.25 µV. This would require a filter capacitor (C_{FLT}) of 5.9 µF be placed in front of the ADC.



With a capacitance value of 5.9 µF, the op amp may not be able to drive such a large capacitive load. If an external resistor (R_{FLT}) is added, the $R_{FLT}|C_{FLT}$ time constant may not be small enough to allow the input signal to settle in a reasonable amount time. Moreover, the capacitor using your calculations and ADC may be too large and perhaps expensive.

CFLT Suggested Modification

- **Starting Point :: Partition the charge reservoir**
  - **95% from C_{FLT}**
  - **5% from Op Amp**

- **C_{FLT} value provides Q_{SH} with <5% droop on C_{FLT}**
  - **$Q_{FLT} = Q_{SH}$**
  - **$Q_{FLT} = C_{FLT}$ x (0.05 V_{FSR})**
  - **184pC = C_{FLT} x (0.05 x 4.096V) → C_{FLT} = 898 pF**
  - **We'll use 1000pF or 1 nF**

- **Ensure $C_{FLT} \geq 20$ x C_{SH}**
  - **During t_{ACQ} the Op Amp must be able to replace 5% V_{FSR} on C_{FLT}**

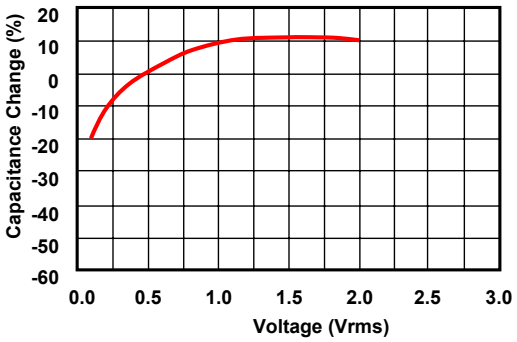
Texas Instruments

If we partition the charge reservoir and the op amp, the amplifier provides some of the current to charge the sampling capacitor. Now, as a starting point, the filter cap provides a less than 5% droop when supplying the charge. This suggests a more reasonable value for C_{FLT} of about 898 pF – we'll use 1 nF as a close approximation. Remember, all the values we find are starting points, and then we'll optimize, so there's no need to be too rigid about the results.

As a check, we make sure that the filter capacitor value chosen is at least 20 times the internal capacitor value. In our case, it's more than 20 times the size, so we're meeting that rule of thumb.

Capacitor Voltage Coefficient

- Voltage coefficient causes distortion
  - C = C0 x (1+bVCAP)
  - Also has non-linear error proportional to frequency
- Voltage and frequency coefficients impact ADC distortion



Source: Murata

Texas Instruments

One thing to watch out for in choosing the filter capacitor is distortion. The distortion occurs due to the normal capacitor voltage dependant characteristic, meaning that the capacitance changes with the voltage applied.

An equation that describes this change in one region of the voltage curve is:

$C = C_0 \ (1 + bV_{CAP})$,

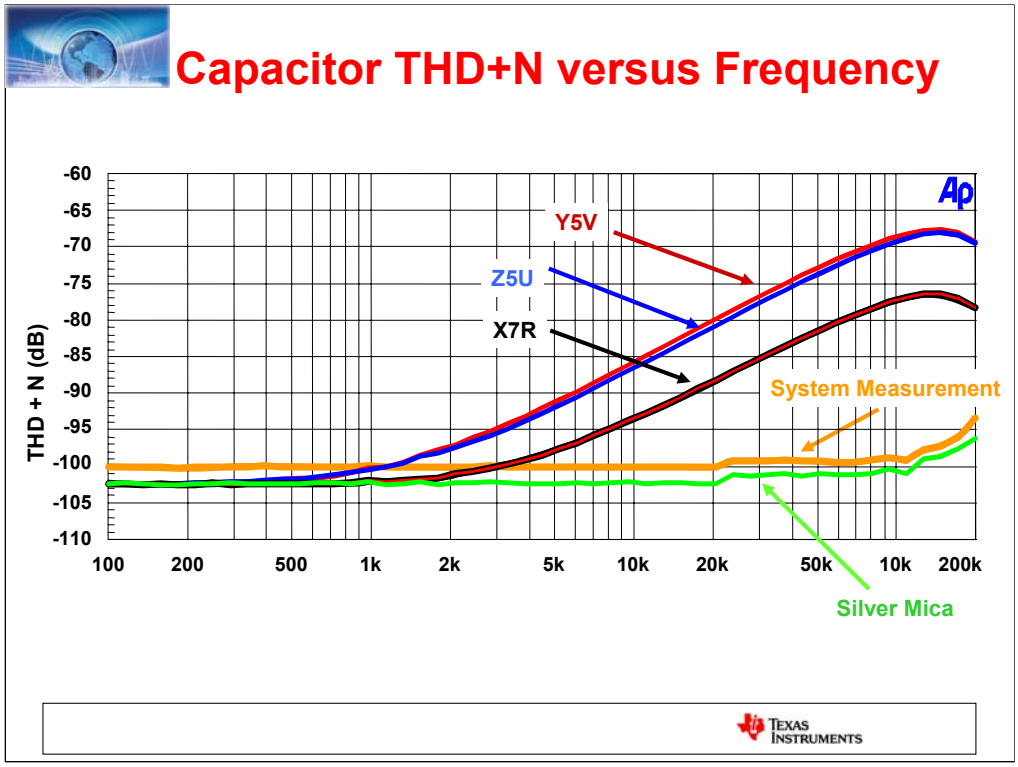
where

C_0 is the nominal capacitance,
V_{CAP} is the voltage across the capacitance,
b is the voltage coefficient of the capacitor.

A plot of a typical curve of this capacitance is shown in this slide.

The current or input charge travels through the ADC driving impedance, which creates a voltage drop error, which again varies with voltage. Since the charging current from C_{FLT} is voltage dependant, it creates a non-linear error. For a sine wave, this error contains harmonics.

The capacitor voltage coefficient characteristic can be more pronounced in semiconductor process technologies. Since the ADC input has an internal input RC, this distortion-producing phenomena also occurs at the input of the converter.

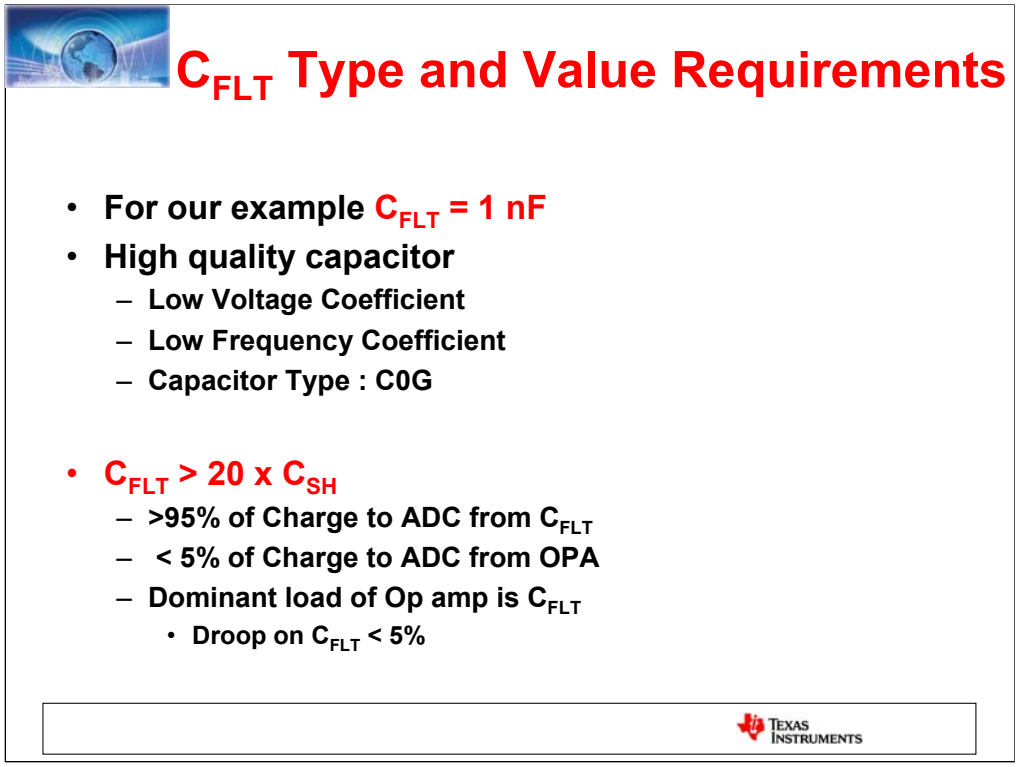


The input signal frequency across C_{FLT} can also impact the accuracy of your conversion. Capacitors have a voltage coefficient, which means the capacitance changes with applied voltage. The capacitance value also tends to be nonlinear, and introduces distortion which also changes with frequency.

This graph shows the characteristics of several capacitor technologies and their Total Harmonic Distortion plus Noise (SINAD) versus frequency performance. The lowest line on this chart is taken using a Silver Mica capacitor. The line above the Silver Mica Capacitor data shows the system measurement. The other lines on this chart are from ceramic caps with different dielectrics - Z5U, Y5V, and X7R. Note that these types of capacitors introduce significant non-linearity and signal distortion over frequency.

Not shown on this chart is the ceramic C0G type capacitor. The C0G type capacitor closely matches the silver mica performance

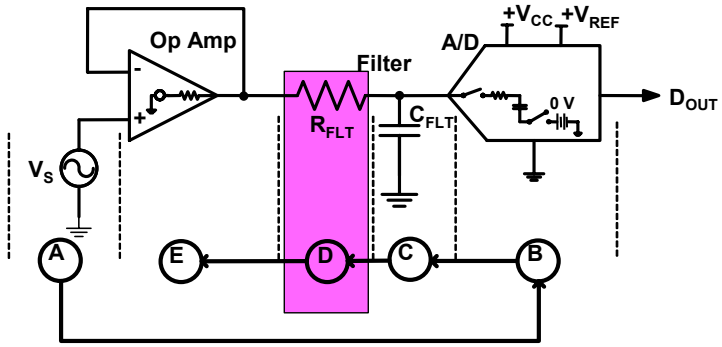
It is critical that you select the right capacitor type for C_{FLT}. We will find that a higher quality external capacitor (C_{FLT}) will not degrade the AC specifications of the ADC. The larger voltage coefficient of the smaller internal ADC capacitor (C_{SH}) will be dwarfed by the lower voltage coefficient of the larger external capacitor.



The capacitance value that we have chosen for our design example is 1 nF. This capacitor should be a high quality capacitor with low voltage and frequency coefficients. Recommended capacitor types is silver Mica or C0G.

If we design the external capacitor value to be at least twenty times larger than the size of the internal sampling capacitor, 95% of the charge required during the acquisition time comes from the external capacitor, C_{FLT}. This minimizes the effects of the charge redistribution on the driving amplifier. Additionally, this configuration reduces the voltage droop at the input to the SAR ADC, insuring that the instantaneous voltage droop at the amplifier is less than 5% of the original voltage droop without C_{FLT}.

4. Choosing RFLT



- Things we need to know
  - t_{ACQ} = ADC acquisition time (1.88 μs)
  - k = Single-pole time constant multiplier for 16-bit ADC (12)
  - C_{FLT} = External input capacitor to ADC (1 nF)

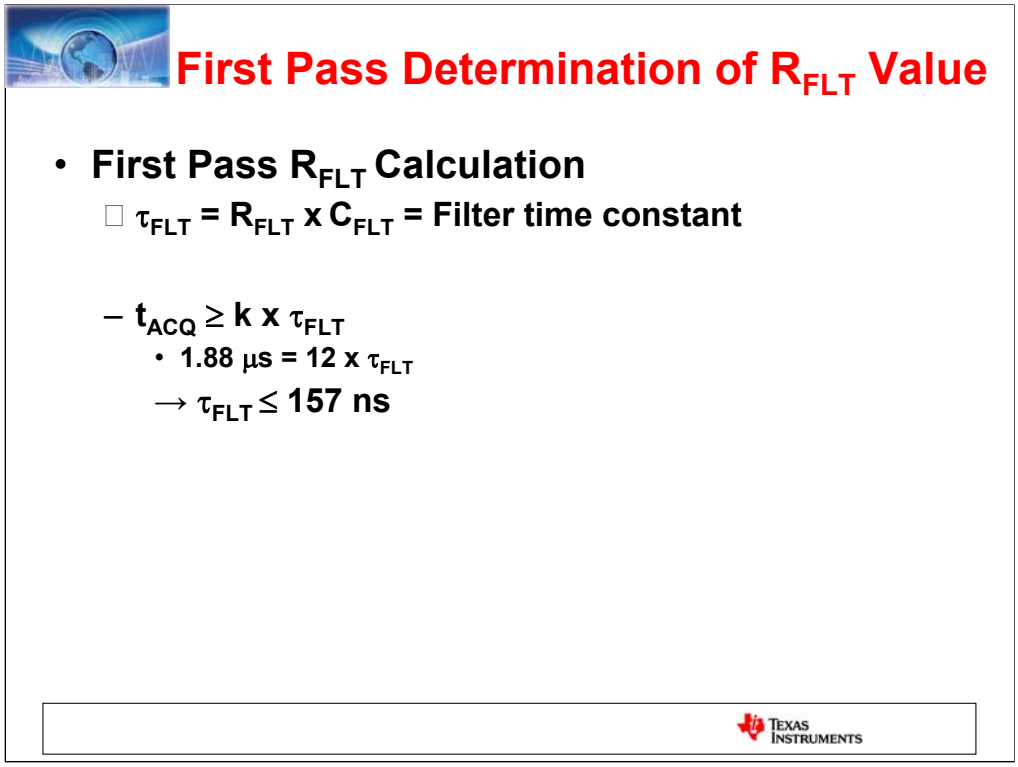
Texas Instruments

With the capacitor chosen, we move on to the resistor, R_{FLT}.

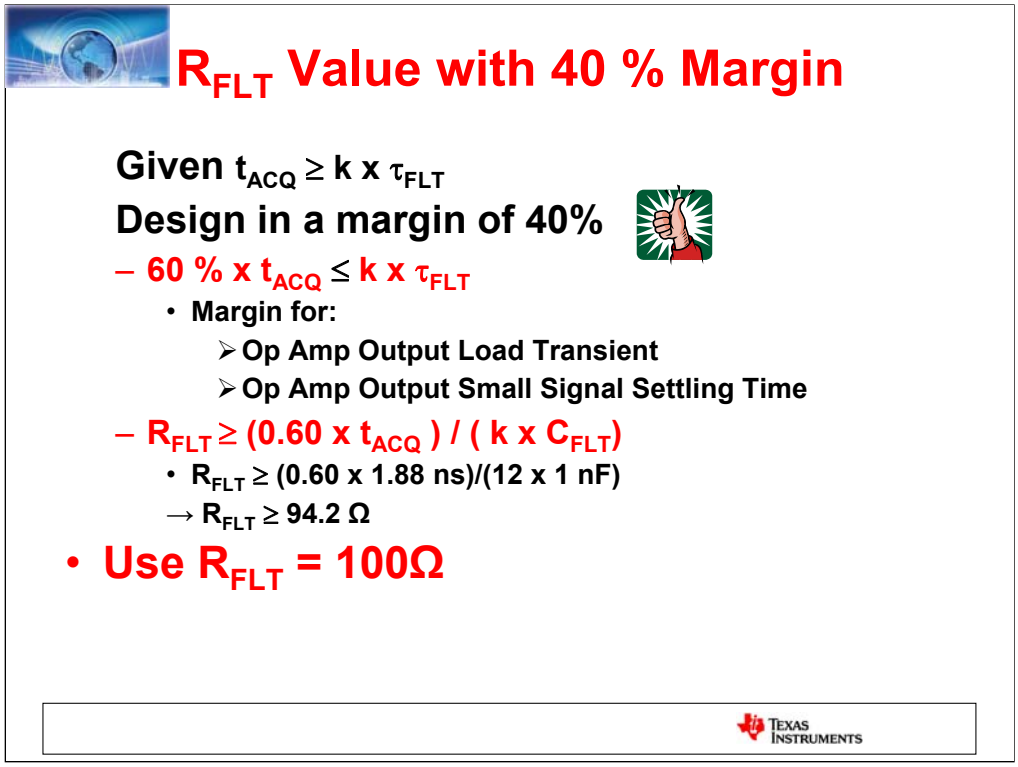
As we work thru the resistor selection we will again need to know the acquisition time of the converter (t_{ACQ}), the time constant multiplier (k), and the value of the filter capacitor (C_{FLT}).

The acquisition time of the converter will assist in choosing a resistor that balances with C_{FLT}. The value of “k” will also be used in this part of the resistor value identification.

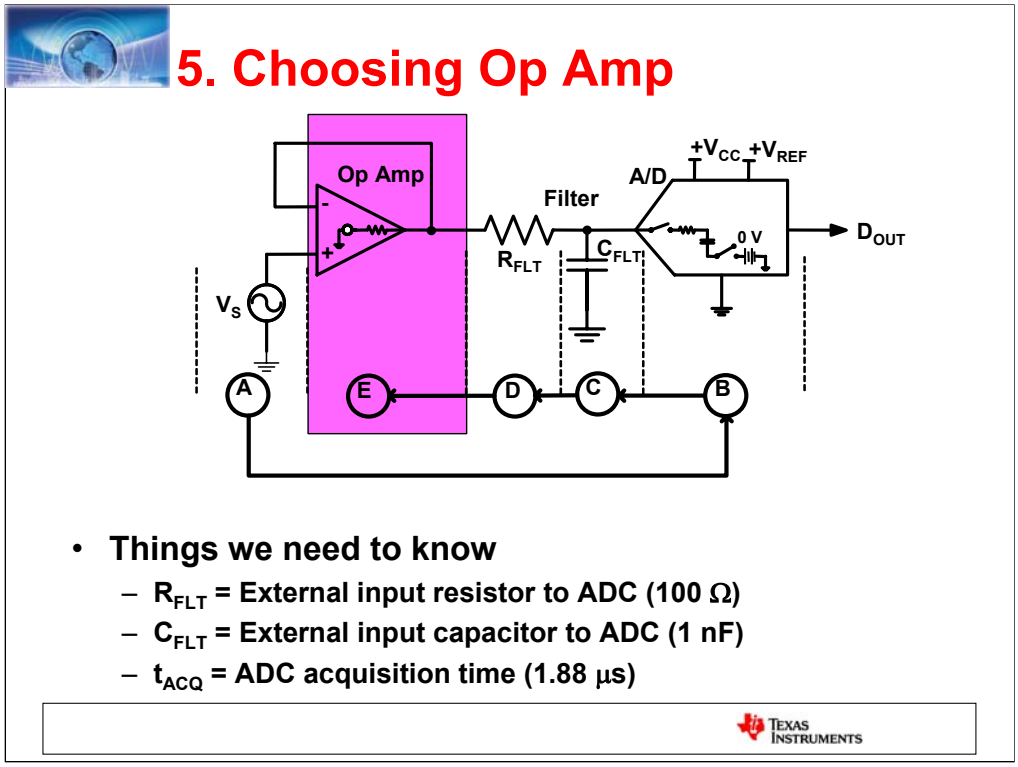
We will use the combination of values of R_{FLT} and C_{FLT} to verify the stability of our circuit.



The external $R_{FLT}|C_{FLT}$ network must settle within the ADC acquisition time. Using the converter's acquisition time (t_{ACQ}), the maximum filter time constant (τ_{FLT} for $R_{FLT}|C_{FLT}$) for this circuit is 157 ns.



As a rule of thumb, we will set the external $R_{FLT}|C_{FLT}$ settling time constant a bit faster than ideal – 60% say, to allow a margin for error of the op amp load transient and the small signal settling time. Using this guideline, we can calculate a resistance value that is more forgiving.

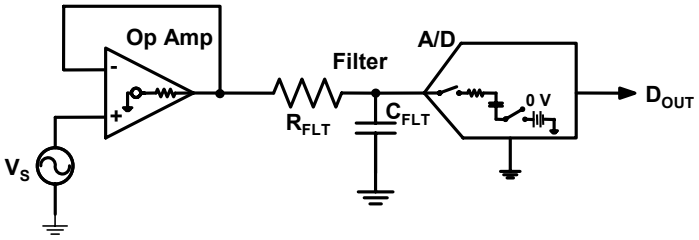


With our $R_{FLT}|C_{FLT}$ filter values chosen, we can now search for a suitable op amp to drive this system. The combination of R_{FLT} and C_{FLT} will be used to determine the stability of the operational amplifier. During this evaluation process, the open-loop output resistance of the amplifier will help to verify amplifier stability and the value of R_{FLT}.

The acquisition time of the converter will be compared to the amplifier large signal and small signal settling time. In our evaluation we will insure that the amplifier we have selected will settle in enough time for the ADC to complete the signal acquisition.

Primary Op Amp Buffer Specs

Specification	Symbol
Gain Bandwidth Product	GBWP
Closed Loop Gain Bandwidth	f_{CL}
Slew Rate to Track 100kHz Input	SR_{OPA}

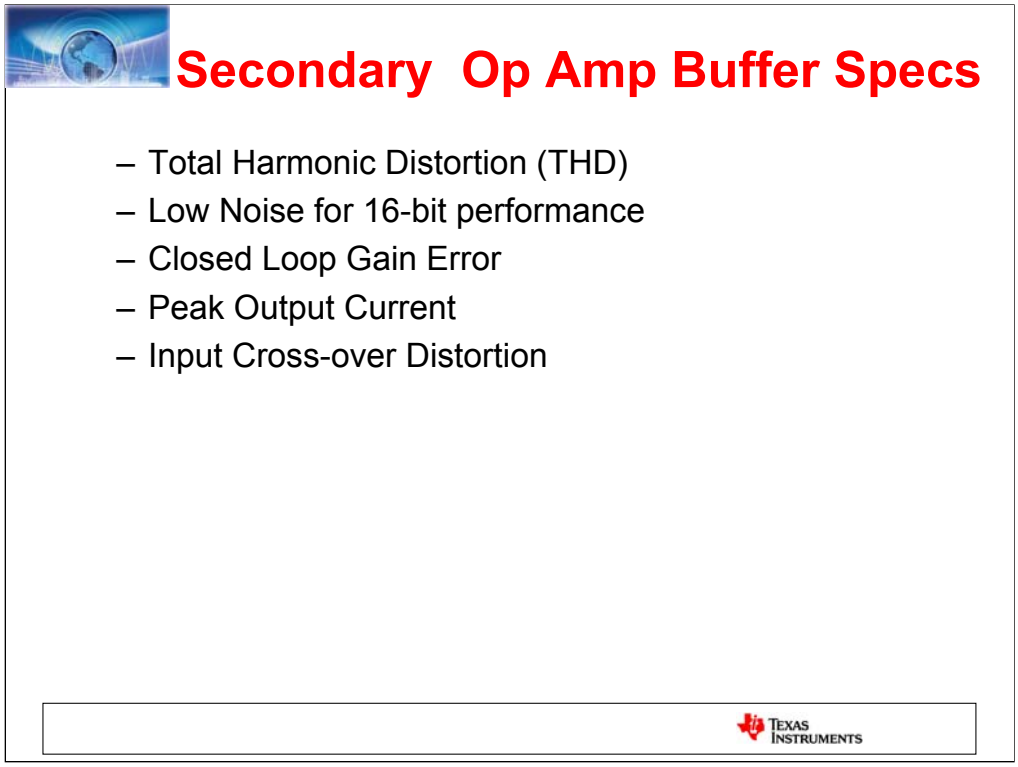


As mentioned earlier, knowing what power supplies we plan to use to power the op amp is important. It helps to narrow down the available operational amplifier choices. In our case, we'll opt to use a single, 5V supply.

The buffer amplifier may be configured as either a follower (noninverting gain of +1 V/V) or an inverting gain of –1 V/V amplifier. We've chosen a non-inverting configuration.

We will pick the GBWP of the amplifier to make sure that the input signal bandwidth is accounted for, and the amplifier is stable with the $R_{FLT}|C_{FLT}$ load.

The amplifier must have sufficient slew rate to charge the $R_{FLT}|C_{FLT}$ changes. A wideband amplifier will generally have a fast transient response and will be able to handle the load transients better.



The THD, noise, closed loop gain error, and peak output current capabilities are secondary op amp specifications.

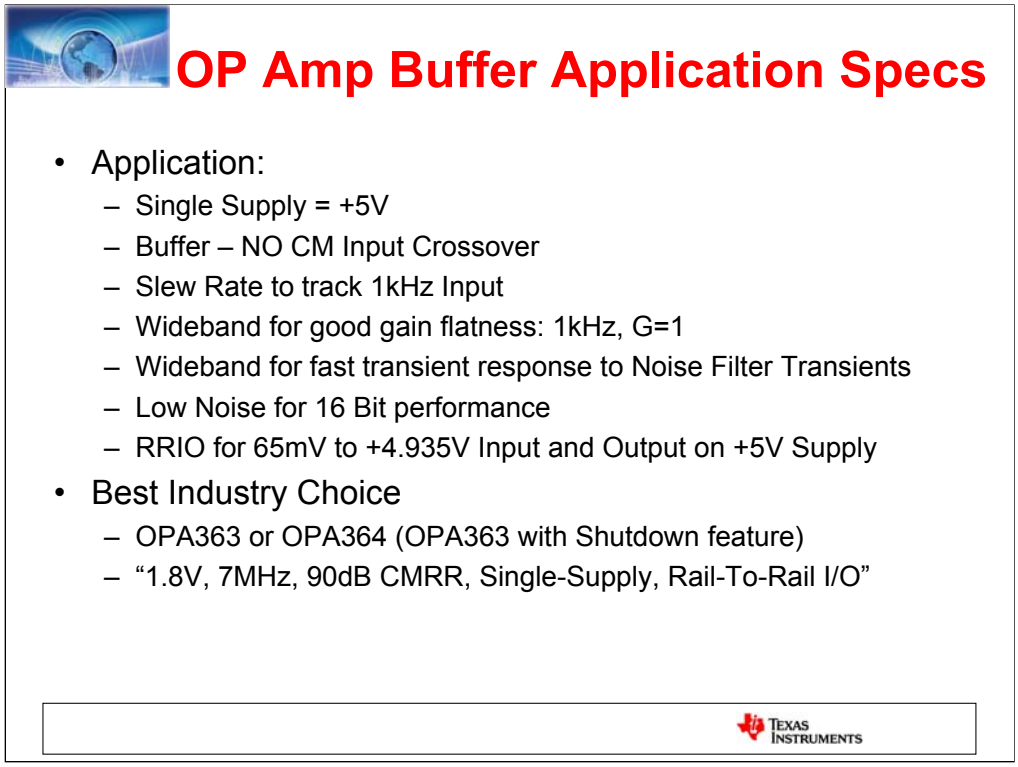
At our 16-bit level, we'd like an amplifier that has extremely low distortion in our signal range of interest. This requires digging into the op amp product data sheets, because this parameter is rarely shown in selection tables. Usually a curve is included in the datasheet showing THD even if it is not specified in the specification table.

Because of our 16-bit system, a low noise amplifier is a must. The op amp data sheet has the noise specification in the Electrical Characteristics table.

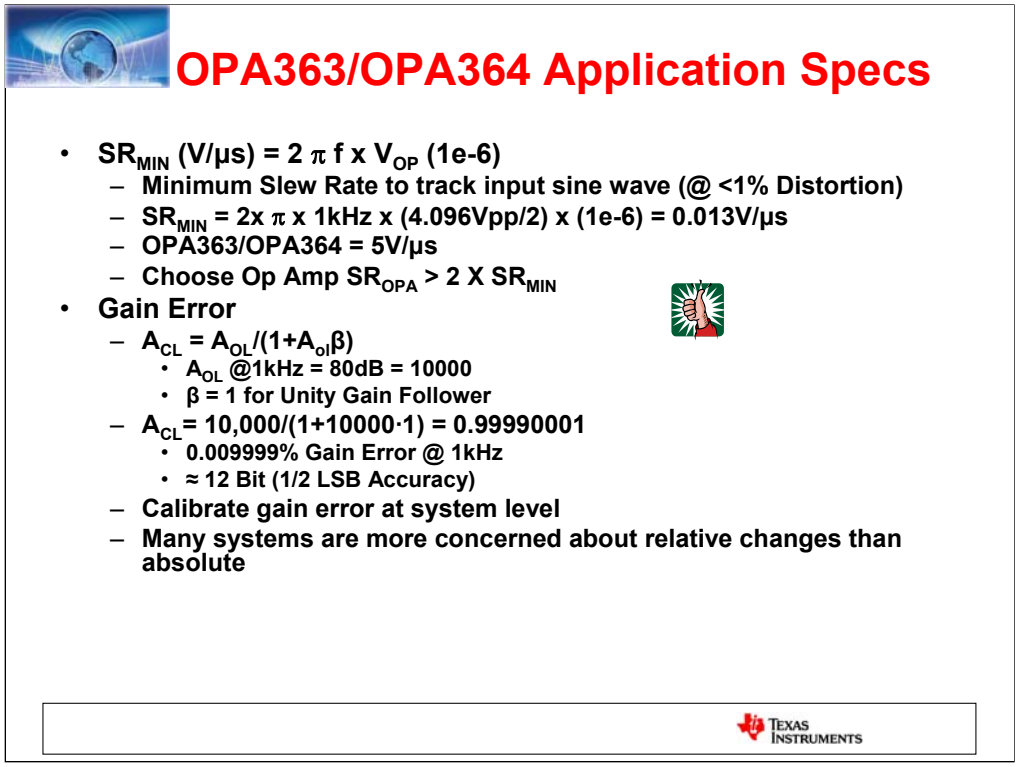
Another thing to consider is the open loop gain of the op amp, and how that might contribute to gain error. For example, an op amp with 97dB of open loop gain would give us a gain accuracy to approximately a 13-bit level. Is this a problem? Probably not – the other gain error sources in the system, from our front end to the reference, are generally much larger. Calibration at the system level can remove this error, and is generally required of any measurement system.

The limit of the peak output current is calculated by using the value of the filter resistor (R_{FLT}) we will find, and remembering that the op amp is asked to supply 5% of V_{FSR} to recharge the flywheel capacitor.

We have elected to use the operational amplifier in a buffer configuration where the gain is equal to +1 V/V. Consequently, we will use an amplifier that does not display input cross-over distortion.



The absence of common-mode crossover makes the OPA363 and OPA364 excellent buffer amplifiers. In addition, they have fast settling time and output drive current to provide a good filter transient response. Excellent rail-to-rail performance allows us to take full advantage of the ADS8320 dynamic signal range.



The relationship between frequency and slew rate is given by SR (Volts per second) equals 2* π *V_{OP} per cycle.

There are T seconds per cycle. T equals 1/f , so SR= 2* π * V_{OP} *f . V_{OP} =V(full scale)/2 and V(full scale) is 4.096V from a prior slide. So now SR = 2* π *f*(4.096/2) = 15.3 * f = 15.3 * 1000

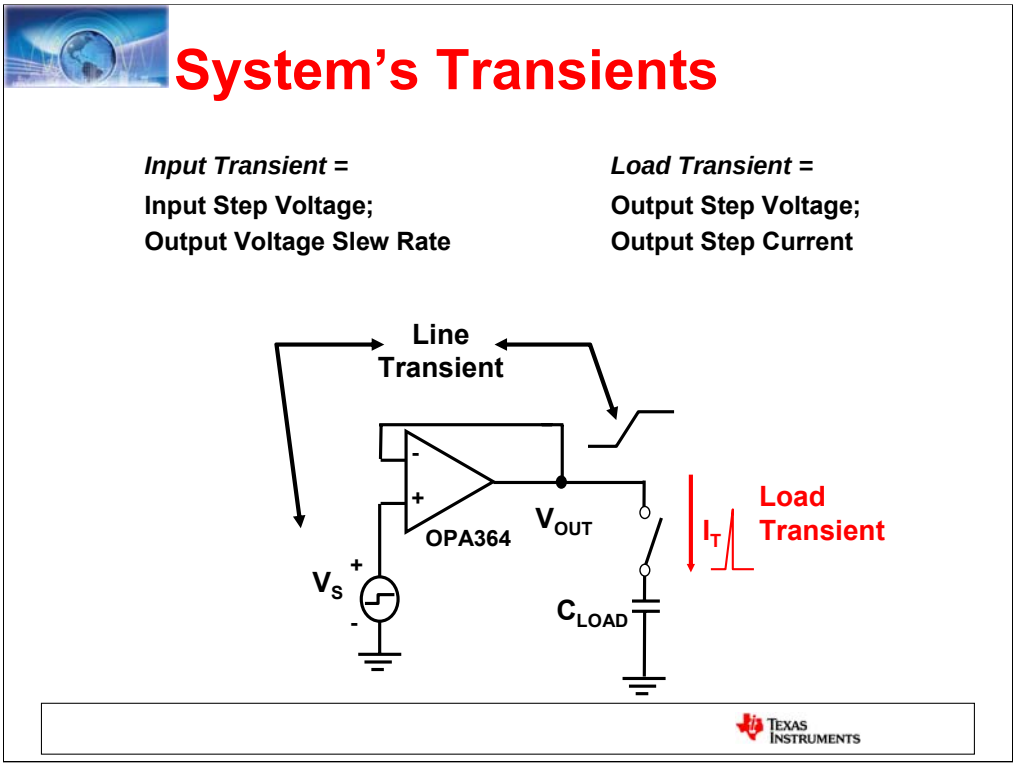
To express SR in V/µs we will divide by 1,000,000.

This then leaves us SR_{MIN} = 0.013 V/µs.

A good rule of thumb is to select an op amp with 2*SR_{MIN}

The OPA363 with a SR_{OPA} of 5V/µs more than meets this criterion.

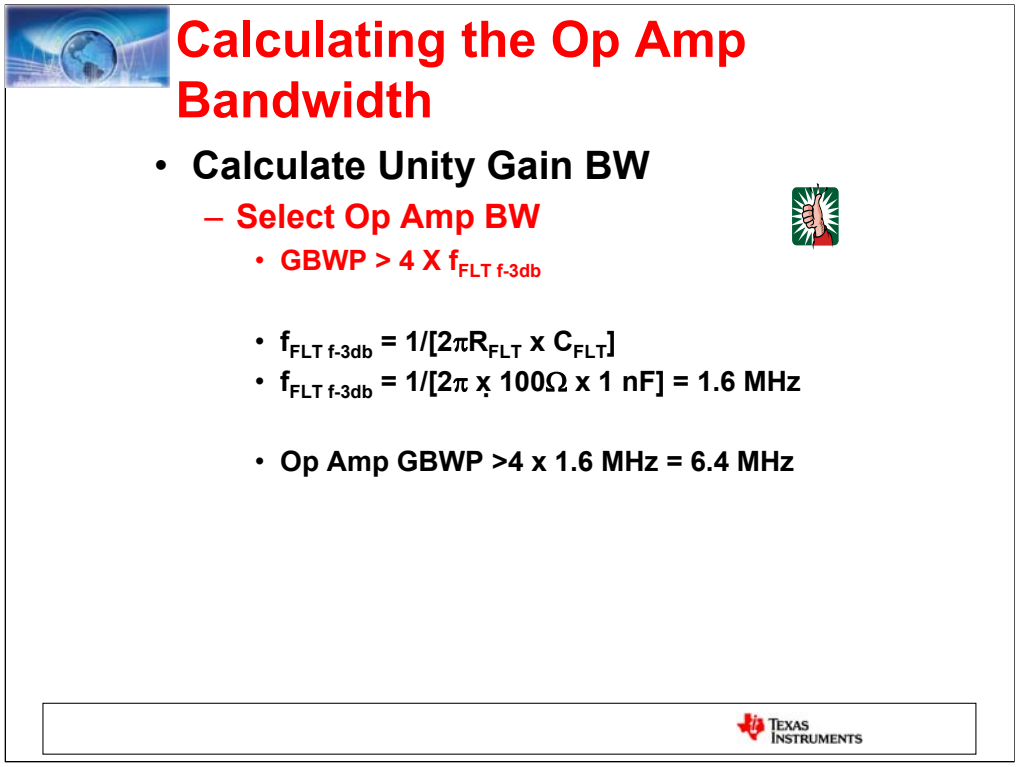
Gain error at 1kHz is on the order of 12 bits but can be calibrated out at the system level.



Another issue to be aware of is the dynamic requirements that are placed on the op amp by the ADC. The input signal can change across the full voltage range and the amplifier must slew and settle to final value. Op amp data sheets may specify a settling time, but if they do, it is usually only to 0.01%, which is only about 12 bits of accuracy. Our 16-bit system needs 0.0001907% settling – and we're not likely to find that specified in an op amp data sheet.

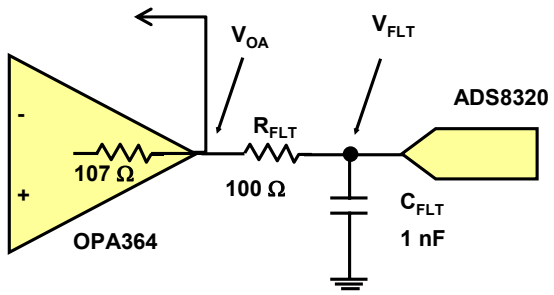
The load transient poses the biggest problem for us in choosing an op amp, because while we know the load is the input capacitor of the ADC, we don't know what voltage might be on it at any given time. No op amp data sheet even discusses the effect of load transients of this nature.

As we go forward in this discussion we will use the OPA364 amplifier at the input of at our SAR system. The OPA364 amplifier has a GBWP of 7 MHz. The slew rate of this amplifier is typically 5 V/μs. It typically produces a low noise at 17nV/√ Hz at frequencies greater than 10 kHz.



Now we need to find what bandwidth we need for the op amp. The rule of thumb is to select an op amp with a unity gain bandwidth at least four times the bandwidth of our $R_{FLT}|C_{FLT}$ filter. The amplifier in our example needs to have a GBWP larger than 6.4MHz. The OPA364's GBWP is 7 MHz.

OpAmp + Filter: Small Signal



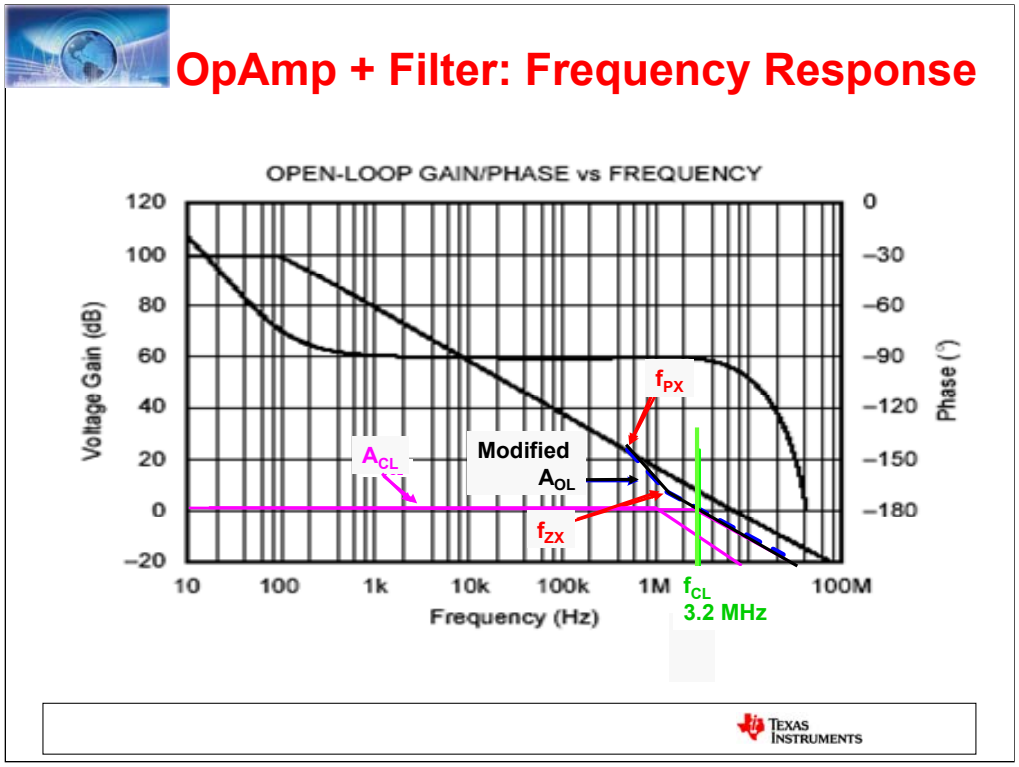
- **Modify AoI due to R_{FLT} & C_{FLT}**
  - **$f_{PX} = 1/[2\pi(R_O + R_{FLT})C_{FLT}]$**
    - **$f_{PX} = 1/[2\pi(107\Omega + 100\Omega)1\ nF] = 768kHz$**
  - **$f_{ZX} = 1/[2\pi R_{FLT}C_{FLT}]$**
    - **$f_{ZX} = 1/[2\pi\ x100\Omega\ x1\ nF] = 1.6MHz$**

Texas Instruments

The reason we need to know the open loop output resistance (R_O) is that we now must check the small signal performance of the chosen op amp, and check for stability of this op amp driving the $R_{FLT}|C_{FLT}$ circuit.

The open-loop gain (A_{OL}) of the op amp will be modified by a pole present from the open loop resistance plus $R_{FLT}|C_{FLT}$, and then cancled by a zero from the $R_{FLT}|C_{FLT}$.

OpAmp + Filter: Frequency Response



Drawing the pole and zero in on the open-loop gain chart shows us the modified open-loop gain response. The closed loop gain can then be plotted, so that we can find the closed-loop corner frequency of the op amp response.

In the diagram in this slide, the left y-axis plots the open-loop and closed-loop gain of our amplifier. The units of this axis are decibels (dB). The right y-axis plots the open-loop phase response of the amplifier. The units of this axis are degrees (°). The x-axis plots the frequency response of the gains (left y-axis) and phase (right y-axis). The units of the x-axis is hertz (Hz).

The open-loop gain curve for this amplifier (OPA364) has a gain of 100 dB at 10 Hz. As frequency increases, this gain curve changes (~100 Hz) to a -20 dB/decade slope. This slope continues until the curve continues past 0 dB. The frequency at the intersection point between the open loop gain curve and 0 dB is 7 M Hz.

When the external filter ($R_{FLT}|C_{FLT}$) loads the amplifier, the open-loop gain curve is modified. In this slide the blue curve represents the modified open loop curve. The pole at f_{PX} increases the roll-off towards 40dB/decade but the zero at f_{ZX} straightens the curve back out to a safe 20dB/decade well before crossing the closed loop curve A_{VCL} at f_{CL} thus assuring stability.

As shown in this diagram the pole from this filter network occurs at 769 kHz and the zero occurs at 1.6 MHz. The slope of this modified open-loop gain curve changes from -20dB/decade to -40 dB/decade slope with f_{PX} and the reverts back to a slope of -20 dB/decade with the zero, f_{PZ} at 1.6 MHz.

Circuit stability is defined at the intersection point of the open-loop gain curve and the closed-loop gain curve. At this intersection point, if the difference between the slopes of these two curves is 20 dB/decade, the amplifier will be stable. If the difference between these slopes is greater than 20 dB/decade (ex 40 dB/decade) the amplifier circuit will be marginally stable.

OpAmp + Filter: Stability

- **Buffer Closed Loop Gain Bandwidth as modified by $R_{FLT}|C_{FLT}$**
  - **f_{CL} = 3.2 MHz**
- **Stability Check**
  - **At f_{CL} = 3.2 MHz "Rate-of-closure" is 20dB/decade → f_{ZX} cancels f_{PX} before f_{CL}**
    - **$f_{CL} > 2 \times f_{FLT\text{-}3dB}$**
  - **f_{PX} and f_{ZX} are $\leq$ decade apart**
    - **Phase of pole will be cancelled by phase of zero**
    - **$R_O \leq 9 \times R_{FLT}$**
  - **$f_{FLT\text{-}3db} = 1/[2\pi R_{FLT} \times C_{FLT}] = 1.6MHz$**

Texas Instruments

Now that we know the closed loop bandwidth of the operational amplifier, we can do a stability check. The rule of thumb is to make sure that the rate of closure at the corner frequency is 20dB/decade. Generally this is assured if the zero of the $R_{FLT}|C_{FLT}$ cancels the pole before reaching the closed loop bandwidth frequency, and the zero frequency is less than a decade from the pole frequency. In our case, this checks out.

There are two key issues that have occurred with the addition of $R_{FLT}|C_{FLT}$ to the circuit. The closed loop bandwidth has been reduced and there is a danger that the open-loop gain curve and closed-loop gain curve can intercept with a difference in slopes of 40 dB/decade, creating a possible instability. We must assure that the op amp gain bandwidth is more than four times the filter bandwidth, which in our case is true.

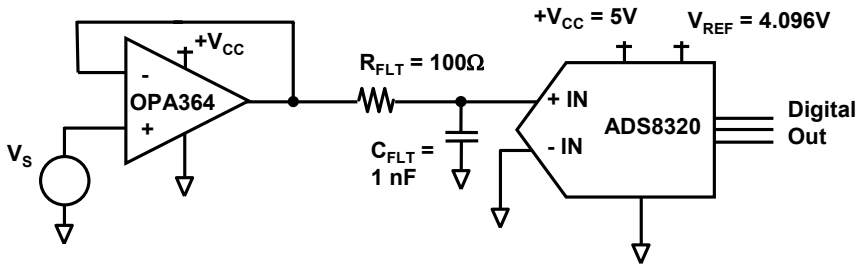
Amplifier Selection Guidelines

- **Stability insured and Bandwidth exceeds input signal**
  - **GBWP > 4 x $f_{S(MAX)}$**
  - **GBWP ≥ 2 / (π C_{FLT} x R_{FLT})**
    - **$R_O \leq 9 \times R_{FLT}$**
  - **$f_{CL} > 2 \times f_{FLT\text{-}3dB}$**
- **Slews fast enough for the input signal**
  - **$SR_{OPA} > 4\pi \times f_{S(MAX)} \times V_{OP} \times (1e\text{-}6)$**

Texas Instruments

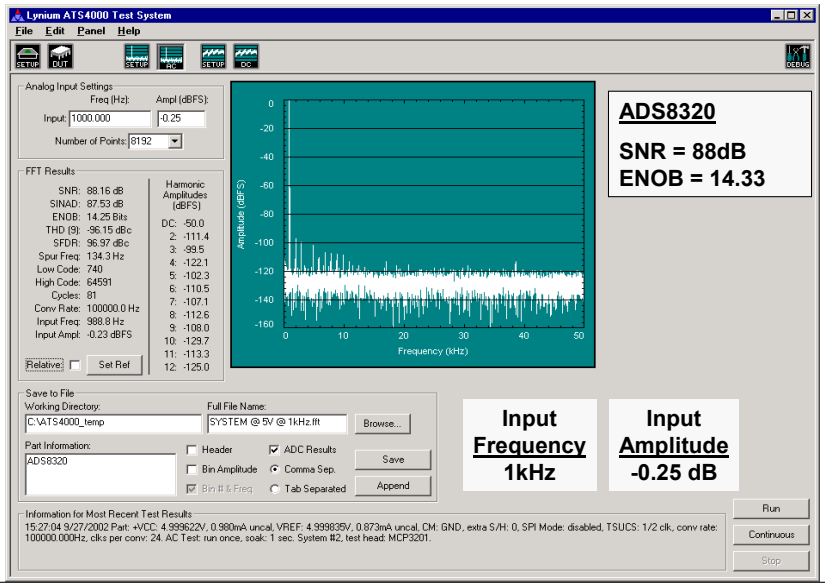
You should apply the guidelines in this slide when you select our amplifier for this SAR system.

Final OPA-SAR Circuit Design



Our finished design is shown in this slide.

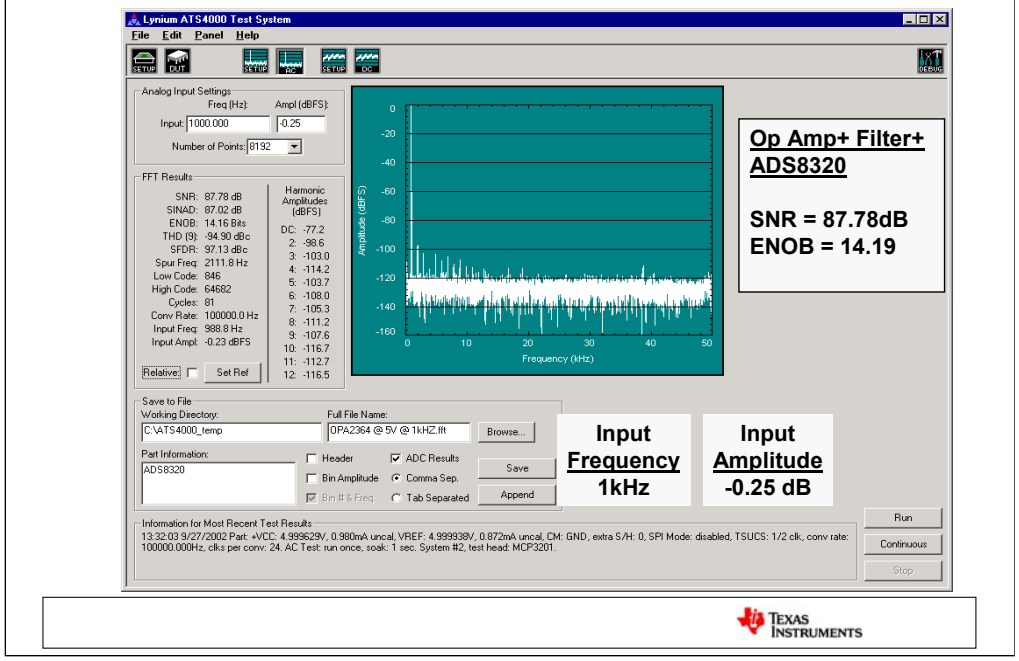
ADS8320 On Test System



The next three slides are displays from a Lynium ATS4000 tester. This slide shows the performance of a stand alone ADS8320. The tested SNR value for the ADS8320 without $R_{FLT}|C_{FLT}$ is 88.16dB.

The frequency of the input signal is 1 kHz with a magnitude of -025 dB (11 mV less than the FSR of the converter).

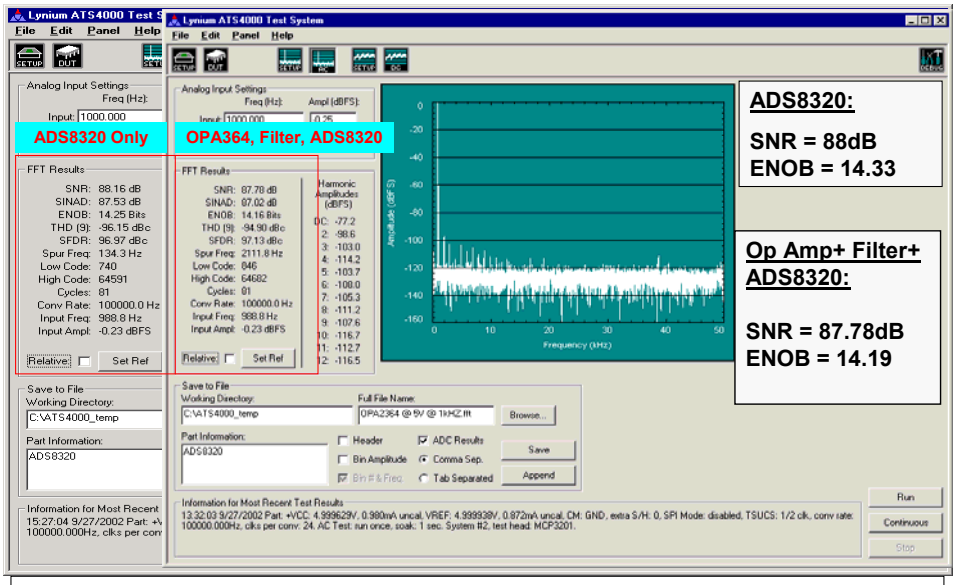
OPA364 + Filter + ADS8320



This slide shows the SNR performance of the entire system: the op amp, the filter, and the ADS8320. Note the tested SNR is equal to 87.78 dB.

The frequency of the input signal is 1 kHz with a magnitude of -025 dB (11 mV less than the FSR of the converter).

Comparison of Tests



This slide shows a side-by-side comparison. The difference in SNR is only 0.22dB or 0.14 effective number of bits. Fortunately the addition of the buffer and filter does not significantly degrade the overall performance of the A/D.

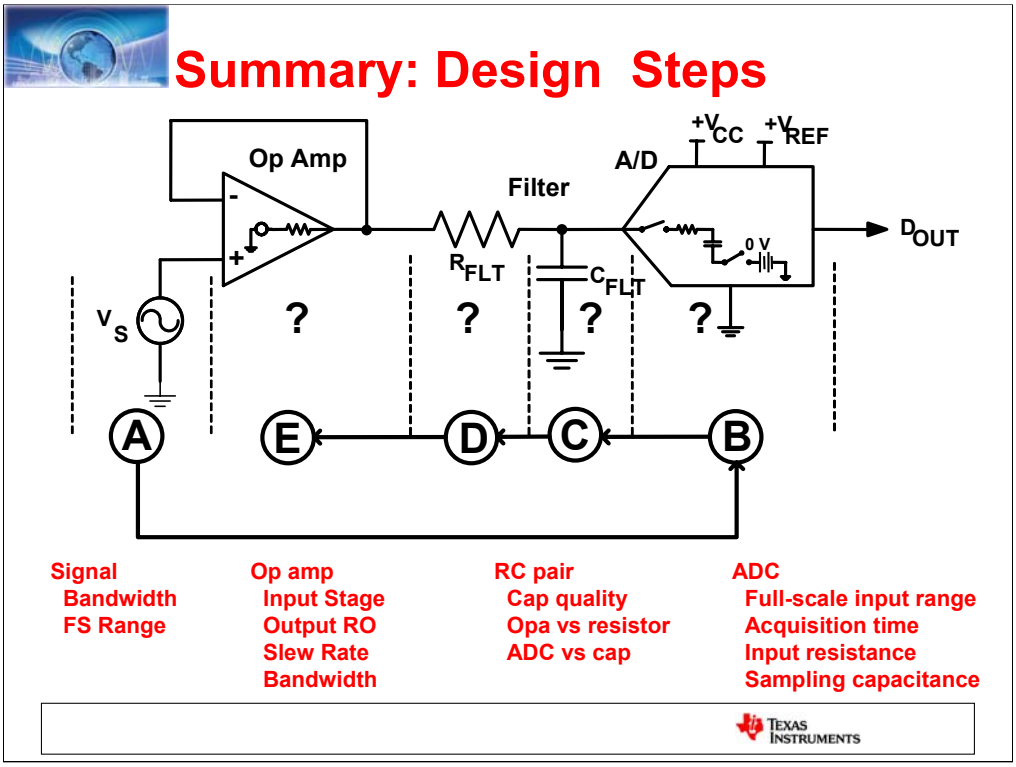
Design Equations: SAR-ADC System

- **Filter Capacitor and Resistor Values**
  - $C_{FLT} > 20 \times C_{SH}$
  - $R_{FLT} \geq (0.60 \times t_{ACQ}) / (k \times C_{FLT})$
- **Select Amplifier**
  - $GBWP > 4 \times f_{S(MAX)}$
  - $GBWP \geq 2 / (\pi C_{FLT} \times R_{FLT})$
  - $R_O \leq 9 \times R_{FLT}$
  - $f_{CL} > 2 \times f_{FLT\text{-}3dB}$
  - $SR_{OPA} > 4\pi \times f_{S(MAX)} \times V_{OP} \times (1e\text{-}6)$

Texas Instruments

Following the selection of the ADC, you will calculate the filter capacitor and resistor ($R_{FLT}|C_{FLT}$) values . It is important that the filter capacitor technology is high quality , such as capacitors constructed with Silver Mica or CO8 with low voltage and frequency coefficients.

With the identification of the values of $R_{FLT}|C_{FLT}$, you will select your amplifier. Using the Gain Bandwidth Product (GBWP), output open-loop resistance (R_O), and the amplifier slew rate (SR_{OPA}) you can determine the appropriateness of the amplifier that you finally intend to select with the formulas in this slide.



So this is how you design your SAR ADC system from beginning to end. You will first determine what your input signal looks like in terms of the bandwidth and a full-scale range. Once that is determined take a look at the ADC. The ADC that you select should match the bandwidth of your input signal. This device should also have an appropriate resolution for your signal. When you select your ADC, you need to determined the acquisition time, input resistance, and the sampling capacitance.

Once you've settled on your ADC, the values of the external input resistance and external input capacitance are determined. The quality of your capacitor is critical if you are concerned about the distortion that will be generated by your circuit. The value of your capacitor insures that your ADC will have ample charge for each conversion. The value of the resistor insures that your operational amplifier will not oscillate.

You will finally select your operational amplifier. At this point, you will determine what style of the input stage you need. You will also select an amplifier that has ample bandwidth for the input signal.

References:

Reference 1: *Baker, B., Oljaca, M., "Use External components to Improve the Accuracy of a SAR ADC", EDN 2007*

Reference 2: *Green, Tim, "Operational Amplifier Stability – Part 3 of 15: R_O and R_{OUT}", AnalogZone Acquisition Zone*

Reference 3: *Oljaca, M. and McEldowney, J. (2002.) Using a SAR Analog-to-Digital Converter for Current Measurement in Motor Control Applications. Burr-Brown Application Report SBAA081.*

Reference 4: *Downs, R. and Oljaca, M. (2005) Designing SAR ADC Drive Circuitry Part II. AnalogZONE: Acquisition Zone.*

Reference 5: *Downs, R., Oljaca, M., "Designing SAR ADC Circuitry – Part 1: A Detailed Look at SAR ADC Operation", AnalogZone: Acquisition Zone*

Reference 6: *Downs, R., Oljaca, M., "Designing SAR ADC Drive Circuitry – Part 3: Designing the Optimal Input Drive Circuit for SAR ADCs", AnalogZone Acquisition Zone*

Reference 7: *Green, T. (2005) "Operational Amplifier Stability - Part 6 of 15: Capacitance-Load Stability: RISO, High Gain & CF, Noise Gain" AnalogZONE: Acquisition Zone.*

Reference 8: *Baker, Bonnie, "A Glossary of Analog-to-Digital Specifications and Performance Characteristics", Texas Instruments, SBAA147*

Symbols:

A_{CL} = Operational Amplifier closed loop gain

A_{OL} = Operational Amplifier open loop gain

b = the voltage coefficient of the capacitor

C_0 = nominal capacitance of a capacitor

C_{FLT} = External filter capacitor between Op Amp and SAR ADC

C_{SH} = Input sampling capacitance of SAR ADC

f_{CL} = Op Amp Closed Loop Gain Bandwidth

$f_{FLT-3dB}$ =

f_{PX} = Pole that effects open-loop gain response of an amplifier. Generated by $R_O + R_{FLT}$ and C_{FLT}

f_S = Input Signal frequency for the SAR-ADC system

$f_{S(MAX)}$ = Maximum Input Signal frequency for the SAR-ADC system

FSR = Full-scale signal range

f_{ZX} = Zero that effects open-loop gain response of an amplifier. Generated by R_{FLT} and C_{FLT}

GBWP = Gain Bandwidth Product

k = Single pole time constant multiplier to calculate converter settling time

Q_{FLT} = Charge on the external filter capacitor (C_{FLT}) in SAR ADC system

Q_{SH} = Charge on the internal sampling capacitor (C_{SH}) of SAR ADC

R_{FLT} = External filter resistor between Op Amp and SAR ADC

R_O = Open-loop output resistance of an operational amplifier

R_{SW} = Parasitic switch resistance at input of SAR ADC

S1 = Sampling switch at the input of the SAR ADC

S2 = Switch to charge C_{SH} to V_{SH0} prior to signal acquisition

SR_{MIN} = minimum Slew Rate required to track a 1 kHz signal with < 1% distortion

SR_{OPA} = Op Amp Slew Rate

t_{ACQ} = ADC acquisition time

t_{CONV} = ADC conversion time

V_{CAP} = the voltage across a capacitor

V_{CC} = Positive power supply voltage

V_{FSR} = Full-scale voltage input range of ADC

V_S = Input signal for the SAR ADC system

V_{OP} = Output voltage of Op Amp

V_{REF} = Voltage reference for the ADC. For the ADS8320 $V_{REF} = V_{FSR}$

τ_{ADC} = Time constant of input structure of ADC equalling $R_{SW} \times C_{SH}$

τ_{FLT} = Time constant of R_{FLT} and C_{FLT}

τ_{FLT}^* = Time constant of R_{FLT} and C_{FLT} with a 40% margin

Optimize Your SAR ADC Design