TI Healthtech
JESD204B Training

JESD Parameters

- **N** is the converter resolution
- **N'** is the serialization factor, e.g. 16x
- **M** is the # of ADC in our device, which is 16.
- **L** is # of JESD lanes. # of ADC/Lane is M/L, or 16/L.

- **F** is #of octets, where *F = (***N'** ** (16/L)) / 8 =* ***2*N'/L.*** N' Factor is always 16x or 8x when Sing_Conv_per_Octet = 1.
  - e.g. for 2L mode and 12x N', F=2*N'/L =12 octets.

- **K** is the # of Frames/Multi-Frame. 17 < F*K and F*K must be a multiple of 4.

- **JESD Lane Rate(speed of 1 lane)**= *Fs*F*8*(5/4) =* ***10*Fs*F,*** where Fs is sampling freq, 8 is 8 bits/octet and (5/4) is due to a property of JESD204B transmission.
  - e.g. LR = 40M*8*8*5/4=3.2Gbps.

Clock Configuration

- Using our device with the Altera JESD IP requires 2 clocks and 2 sysref signals from the clock chip.
- The sysref signals to the ADC and FPGA will be pulses or can be a continuous clock at Fs/(K*n) where n is an integer. Pulses are recommended to avoid an unwanted spur in the signal spectrum from the sysref continuous clock.

- The two clocks are the device clock to the ADC, and the GTX clock going directly to the FPGA. The device clock frequency is Fs, which affects the lane rate, and the GTX is always 10x,20x or 40x slower than the lane rate (depending on the chosen MIF configuration).

- Lane Rate = *10*Fs*2*N'/L =20 *Fs *N'/L*
- GTX = LR/MIF= (*20/MIF) *Fs *N'/L, or Fs*N'/L when MIF is 20x*
- Clock Ratio is always **GTX/Fs = (20/MIF) *N'/L**