

TI Designs

Continuous-Wave Phase-Aligned Multitone Generator: DC-to-6-GHz RF-Sampling DAC Reference Design



TI Designs

The TIDA-01084 reference design demonstrates the use of an RF sampling DAC to generate continuous-wave (CW), phase-aligned multitone waveforms. With four 48-bit independent numerically-controlled oscillators (NCOs), the 14-bit, 9-GSPS DAC38RF83 can generate four CW tones placed anywhere within the first Nyquist zone or up to 6 GHz in the second. This reference design covers the theory of operations, explanation of the GUI, and directions for programming NCOs to generate the tones without the requirement of an external pattern generator. This design demonstrates an easy-to-use method which greatly simplifies and reduces the bill of materials (BOM) for CW multitone generation.

Design Resources

TIDA-01084	Design Folder
DAC38RF83 EVM	Product Folder
LMK04828	Product Folder
LMX2582	Product Folder
DAC38RF83	Product Folder

Design Features

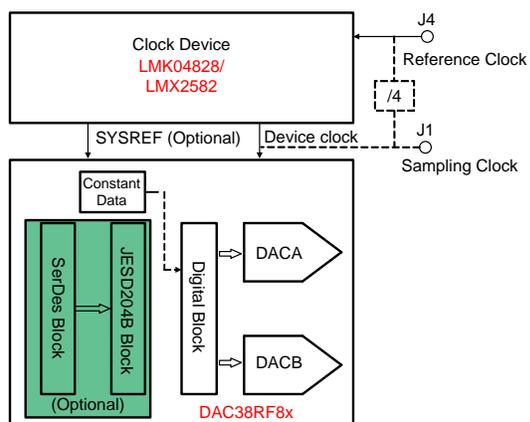
- Generates Multiple CW tones in First Nyquist; up to 6 GHz Supported in Second Nyquist
- Digital Single-Side Band (SSB) Upconversion
- Phase-Aligned Multitone Generation

Featured Applications

- Radar System
- Frequency Synthesizer
- Test and Measurement



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1 System Description

Traditionally, a CW tone can be generated by using phase-locked loop (PLL) to synthesize a relative high-frequency tone referenced from an accurate lower-frequency reference source. In this design, an RF sampling digital-to-analog converter (DAC) is used to generate a CW tone with input digital data.

A CW can be very useful in radar systems where the CW tone is transmitted and then received. The CW tone generator is used as a key technology in various applications such as radio communication and on-off keying.

In this design, the RF sampling DAC38RF83 is used to generate CW tones, which are implemented in a way similar to direct digital synthesis (DDS). The input digital data can be routed from the JESD204B link or internal constant data block. This design focuses on using the internal constant block to serve as input data without the external JESD204B link establishment.

Four independent NCOs can be used to place four tones at arbitrary frequencies. If 1st Nyquist zone is of interest, the NCOs can only place up to a 4.5 GHz tone at a maximum sampling rate of 9 GSPS. A 48-bit NCO resolution generates a tone frequency that is very accurate with a frequency resolution of [Equation 1](#).

$$f_{\text{resolution}} = f_{\text{sample}} / 2^{48} \quad (1)$$

$f_{\text{resolution}}$ is the minimum frequency resolution the output tone can achieve. f_{sample} is the DAC sampling rate and also the NCOs clock rate. When $f_{\text{sample}} = 9$ GSPS, $f_{\text{resolution}}$ can be as low as 3.1974×10^{-5} Hz.

Due to the operation in digital domain, the DAC38RF83 provides the user with faster frequency switching time compared to analog PLL in generating CW tone. The analog PLL locking time is related to comparing the frequency of the phase frequency detector (PFD) and loop bandwidth. The DAC38RF83 also offers the user external trigger signals to synchronize all four NCOs inside the device, which can be used to achieve aligned phase among output CW tones.

Moreover, by providing the same external trigger signal to multiple DAC38RF83s, all the CW tone outputs of the DAC38RF83 devices can be synchronized. This capability is often referred to as multiple device synchronization. Besides frequency placement and time delay programmability, the DAC38RF83 also provides a flexible way to control output power. The output power can be controlled by tuning the following three settings:

- Users can set the value of the constant data block in digital domain to tune output power.
- The mixer inside the DAC offers an additional 6 dB gain boost feature.
- Output full-range current of the analog output stage can be adjusted using register settings.

1.1 DAC38RF83 JESD204B 9-GSPS High-Speed DAC

The DAC38RF83 is a family of high-performance 14-bit DACs, which can run a sampling rate as high as 9.0 GSPS with programmable interpolating filters. The DAC38RF83 has four independent NCOs with 48-bit resolution, which can be used to generate four CW tones at a very accurate frequency.

The DAC38RF83 has two DAC output channels. For each DAC channel, two digital upconverters (DDCs) are implemented. Additionally, each DDC can use the constant input tone to generate a single tone. The internal summation block at the DDC outputs can sum up any number of DDC outputs, which means that the maximum number of generated tones is four tones per DAC output. The main difference between the DAC38RF83 and DAC38RF80 is that the DAC38RF80 has internal balun at the output, which leads to single-ended output, while the DAC38RF83 has differential output without internal balun. The DAC38RF83 offers the user the flexibility to select the output interface network.

1.2 LMK0482x JESD204B Compliant Jitter Cleaner

The LMK0482x family is the highest-performance clock conditioner with JESD204B support in the industry. With up to 14 clock outputs from the low-jitter synthesizer, the output can be configured to support JESD204B, including up to 7 JESD204B converters and logic devices with both a device clock and SYSREF signal. Figure 1 shows the typical applications of the LMK0482xB device.

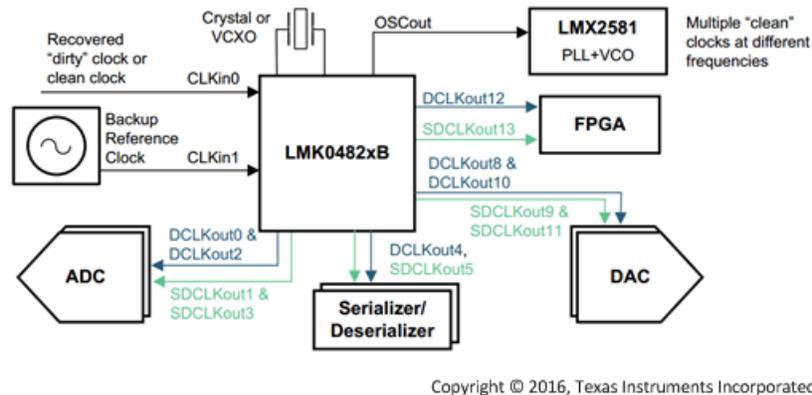


Figure 1. LMK0482xB Simplified Schematic

In this design, the LMK04828 is used to provide the SYSREF and reference clock to the DAC internal PLL input when internal PLL is used to drive the DAC clock. The LMK04828 is featured by its JESD204B-compliant performance, which is used to provide the common sourced SYSREF and device clock to the DAC. If the sampling clock of the DAC38RF83 is driven by an external clock, the LMK04828 is also used in clock distribution mode to provide the SYSREF to the DAC.

2 Block Diagram

Figure 2 shows the Simple CW multitone generator block diagram. The LMK04828 is used to provide the device clock and SYSREF to the DAC38RF83. The input data of the DAC is routed from the internal constant data block in this simple CW multitone generator design. If the DAC38RF83 on-chip PLL is used to generate the sampling clock, then the reference clock should be provided into J4 SMA. The LMK04828 is used to divide down reference, to provide the SYSREF to the DAC. If an external sampling clock is used to drive the DAC, then J1 is the SMA input. Because the LMK04828 cannot support input frequency higher than 3100 MHz, when clock distribution mode is used, a divide-by-four buffer is used to divide the sampling frequency down and then feed it to the LMK04828.

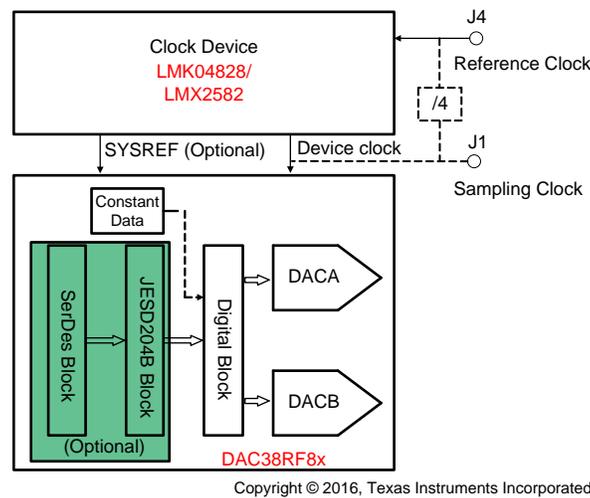
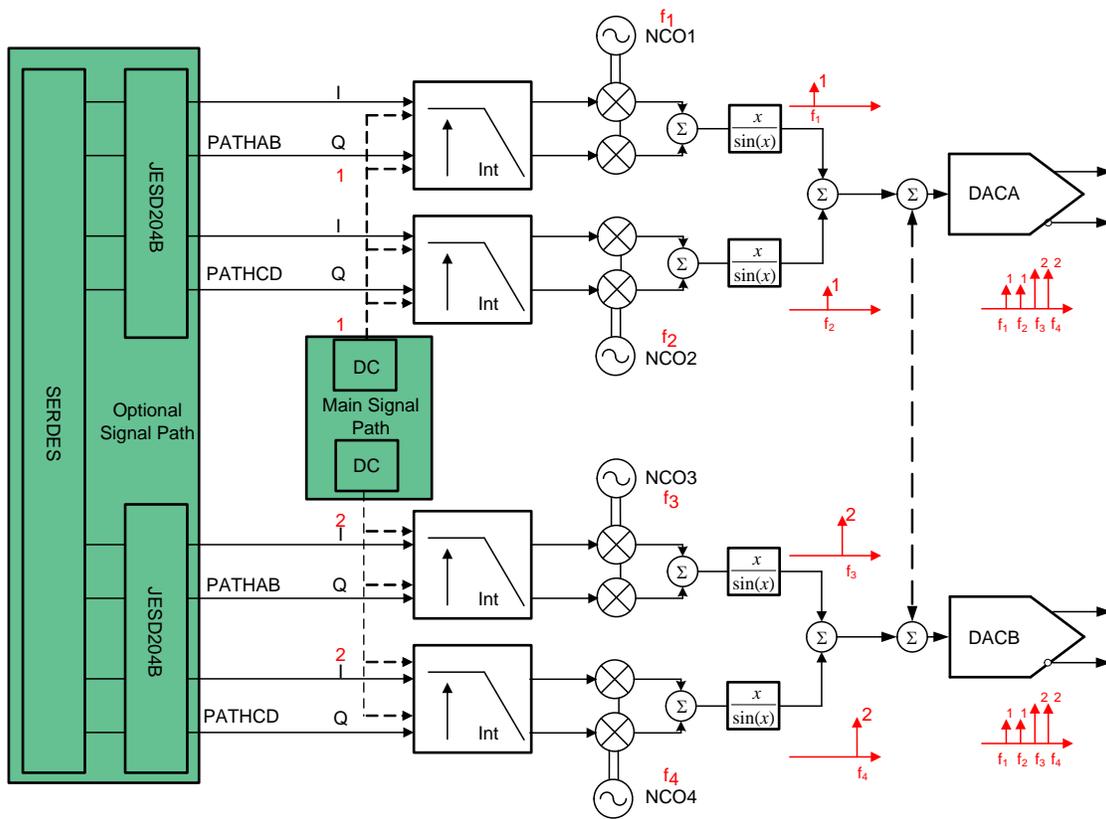


Figure 2. Block Diagram of Multitone Generator

Figure 3 shows the multitone generating logic in the following internal block diagram of the DAC38RF83.



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Figure 3. Internal Logic of DAC38RF83

Two DC blocks can be set with amplitudes of 1 and 2. NCO1 through NCO4 can be set with frequencies of f_1, f_2, f_3 and f_4 , respectively. Using different NCO frequencies, 4 tones can be placed at arbitrary frequency locations. The summation blocks can make summation up to 4 tones, then provide the data to the DAC output stage. Therefore, up to 4 tones can be generated at the output of the DAC channel A and channel B.

3 Highlighted Products

3.1 DAC38RF80 and DAC38RF83

For more information on these devices, view the respective datasheet at www.ti.com.

3.2 LMK04821, LMK04826, and LMK04828

For more information on these devices, view the respective datasheet at www.ti.com.

4 System Design Theory

4.1 Complex Mixer in the DAC38RF83

The DAC38RF83 family of RF sampling DACs has internal DUCs for baseband-to-RF upconversion. Up to 4 complex mixers are available for the DUC. Figure 4 shows the block diagram for each complex mixer.

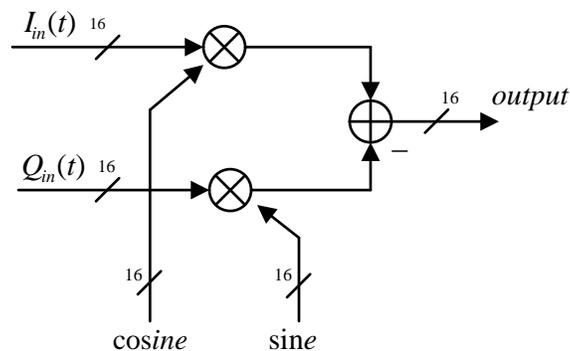


Figure 4. DUC Logic

Equation 2 describes the process of baseband-to-RF signal upconversion. The baseband signal BB comes in the form of complex quadrature data. If the data stream comes from the JESD204B link, the baseband data can either be quadrature or DC data (if needed). The quadrature data is generated through the Hilbert transform filter. Keep in mind, the complex number j is to simply account for the orthogonality of the relationship between I_{in} and Q_{in} .

$$BB = I_{in} + jQ_{in} \quad (2)$$

The block diagram of the DUC in Figure 4 is essential in performing a complex upconversion. The complex upconversion is mathematically represented as $e^{j2\pi f_{LO}t}$, and can also be represented as $\cos 2\pi f_{LO}t + j\sin 2\pi f_{LO}t$. Because the RF output signal at the DUC output is essentially a real analog signal, a real operator must be added at the final DUC output to complete the modeling of the RF upconversion. The real RF output signal can be expressed by Equation 3.

$$\begin{aligned} RF &= \text{real}\{BB(t)e^{j2\pi f_{LO}t}\} = \text{real}\{(I_{IN} + jQ_{IN})e^{j2\pi f_{LO}t}\} \\ &= \text{real}\{(I_{IN} + jQ_{IN})(\cos 2\pi f_{LO}t + j\sin 2\pi f_{LO}t)\} \\ &= \text{real}\{I_{IN} \cos 2\pi f_{LO}t - Q_{IN} \sin 2\pi f_{LO}t + j\sin 2\pi f_{LO}t + jQ_{IN} \cos 2\pi f_{LO}t\} \\ &= I_{IN} \cos 2\pi f_{LO}t - Q_{IN} \sin 2\pi f_{LO}t \end{aligned} \quad (3)$$

Because the BB signal is a complex, CW waveform (for example through the baseband JESD204B TX logic device and JESD204B data stream), the resulting RF signal is as follows in Equation 4.

$$\begin{aligned} BB &= A \cos 2\pi f_{IN} t + jA \sin 2\pi f_{IN} t \\ RF &= A \cos 2\pi f_{IN} t \cos 2\pi f_{LO}t - A \sin 2\pi f_{IN} t \sin 2\pi f_{LO}t \\ &= A \cos 2\pi(f_{IN} + f_{LO})t \end{aligned} \quad (4)$$

With a full-scale complex baseband signal of cosine and sine waves (for example, amplitude of unity for both waves), the resulting RF signal is also a full-scale cosine wave that has been upconverted by the digital local oscillator (LO) frequency. If the baseband signal is a DC signal (for example through the DAC38RF83 constant data path), the resulting RF signal is as follows in Equation 5.

$$RF = A\cos 2\pi f_{LO}t - A\sin 2\pi f_{LO}t = \sqrt{2}\sin(2\pi f_{LO}t - 45^\circ) \quad (5)$$

The combination of cosine and sine waves is a trigonometry identity, which results in a sine wave with an amplitude of $\sqrt{2}A$ and a phase shift of -45° . The amplitude exceeds unity, which may cause digital saturation and must be attenuated in the digital domain. Section 4.2 describes the amplitude adjustment needed for the constant data path.

4.2 Digital LO Generation

The DAC38RF83 has dual-channel outputs. In each channel, 2 DUCs are implemented. The output of the 2 DUCs are summed together to feed into the digital input of the DAC stage. The same implementation is used in the other DAC output channel. Moreover, the digital outputs of the 4 DUCs can be summed together to feed into any digital input of these 2 DAC channels. The summation function is explained in Section 4.5.

For each DUC, the DUC block handles 1 IQ pair of samples coming from the JESD block or internal DC data (constant data path). Each DUC has 1 NCO, 1 complex mixer, and 1 summation block. Due to the real nature of the DAC output signal, the design uses a summation block to convert the complex mixer result to a real signal.

Figure 5 shows the internal implementation of the DUC block digital LO. Each DUC of the DAC38RF83 has its own programmable digital LO.

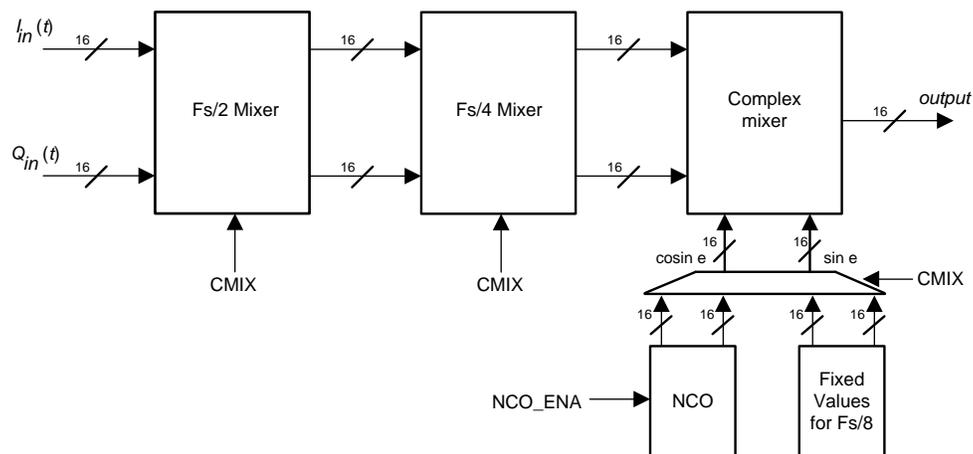


Figure 5. Digital Mixer Implementation

The digital LO has three modes:

- **Low-Power Fs/2 and Fs/4 Coarse Mixer Mode**

This mode aims to save power by not using the full-digital LO generation through the NCO. By using basic arithmetic to generate the $F_s/2$, $F_s/4$, and $-F_s/4$ mixing sequences, the coarse mixer can shift the input signal with the fixed mixing sequence $F_s/2$, $+F_s/4$, and $-F_s/4$. Treating the 2 complex channels as complex vectors of the form $I(t)+jQ(t)$, the real output of the $F_s/2$, $+F_s/4$, and $-F_s/4$ modes is as follows in Equation 6.

$$\text{Output} = I(t)\cos(2\pi f_{CMIX}t) - Q(t)\sin(2\pi f_{CMIX}t) \quad (6)$$

Where f_{CMIX} can be either $F_s/2$, $+F_s/4$, or $-F_s/4$. Because the sine and cosine terms are a function of $F_s/2$, $F_s/4$, or $-F_s/4$ mixing frequencies, the possible resulting value of the terms can only be 1, -1 , or 0. This simplified mixing sequence allows the bypassing of the full-complex signal multiplier and full NCO. The mixer gain is unavailable in this mode (detailed later). The $F_s/2$, $+F_s/4$, and $-F_s/4$ mixer blocks perform mixing through negating and swapping the I/Q channel on certain sequence of samples as provided in Table 1

Table 1. Fs/2, Fs/4, and -Fs/4 Mixing Sequence

MODE	MIXING SEQUENCE
Normal (coarse mixer bypassed)	Iout = {+I1, +I2, +I3, +I4...}
	Qout = {+Q1, +Q2, +Q3, +Q4...}
Fs/2	Iout = {+I1, -I2, +I3, -I4...}
	Qout = {+Q1, -Q2, +Q3, -Q4...}
Fs/4	Iout = {+I1, -Q2, -I3, +Q4...}
	Qout = {+Q1, +I2, -Q3, -I4...}
-Fs/4	Iout = {+I1, +Q2, -I3, -Q4}
	Qout = {+Q1, -I2, -Q3, +I4}

• **Medium-Power Fs/8 Mode**

The Fs/8 mode is a hybrid mix, which uses all the multipliers of the full NCO mixer; however, fixed Fs/8 values are presented at the input for sine and cosine. The fixed values allow the NCO part of the mixer to be turned off to reduce power consumption. The output of the Fs/8 coarse mixer is as follows in Equation 7

$$\text{Output} = (I(t)\cos(2\pi f_{\text{CMIX}}t) - Q(t)\sin(2\pi f_{\text{CMIX}}t))2^{(\text{mixer_gain}-1)} \tag{7}$$

f_{CMIX} is the frequency of Fs/8, mixer_gain is the gain control bit of the mixer, which allows the output signal of the multiplier to reduce by 6 dB. Because the multipliers of the full NCO mixer are used in Fs/8 mode case, the mixer_gain bit is applied. The DAC38RF83 can provide different Fs/8 coarse mixing options: Fs/8, 3Fs/8, 5Fs/8, and 7Fs/8.

• **Full NCO Mode**

In full NCO mode, both multipliers and full NCO are used. Figure 6 shows the NCO block.

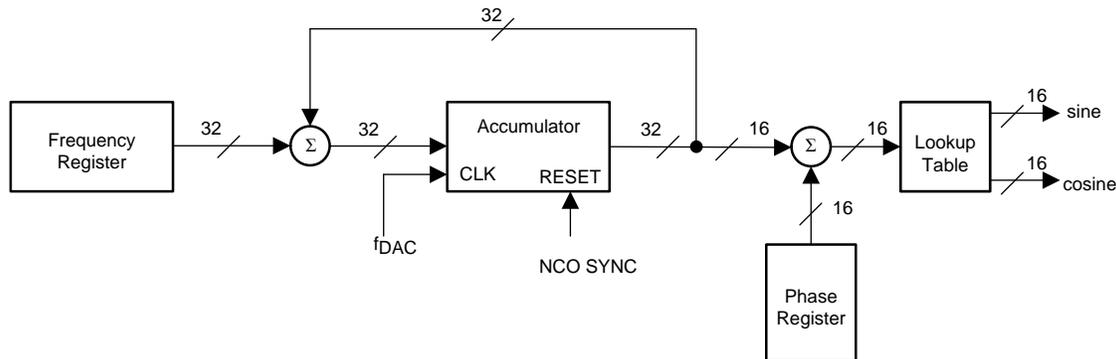


Figure 6. NCO Implementation

The frequency accumulator word is a 48-bit value, and it is offset with a 16-bit phase offset value that is added to the upper 16 bits, before being applied to the sine and cosine lookup tables. The real output of the complex mixer block is as follows in Equation 8.

$$\text{Output} = (I(t)\cos(2\pi f_{\text{NCO}}t + \delta) - Q(t)\sin(2\pi f_{\text{NCO}}t + \delta))2^{(\text{mixer_gain}-1)} \tag{8}$$

Similarly, the multipliers of the mixer are used, so the mixer_gain bit, which is used to control the gain of the mixer, is applied. δ is the initial phase offset of the NCO.

4.3 Mixer Gain Control

The maximum output amplitude out of the signal multiplier (in medium-power Fs/8 mode or full flexible NCO mode) occurs if input, I(t) and Q(t), are simultaneously full-scale amplitudes and the sine and cosine arguments are equal to $2\pi f_{\text{CMIX}}t + (2N - 1)\pi / 4$, where N = 1, 2, 3, and so on. Figure 7 shows the location of the maximum output amplitude when I(t) = Q(t).

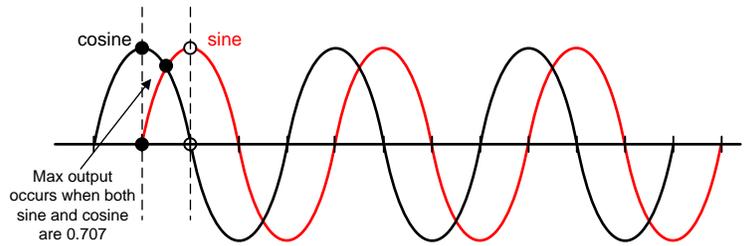


Figure 7. Location of Maximum Output Amplitude When I(t) = Q(t)

The mixer I/Q input can come from the JESD204B block or internal DC constant path. If the BB signal is a DC signal (for example through the DAC38RF83 constant data path or JESD block), the resulting RF signal is $\sqrt{2}A\sin M(2\pi f_{LO} t - 45^\circ)$ whose amplitude exceeds unity, which may cause digital saturation and must be attenuated in the digital domain.

The DAC38RF83 provides a mixer_gain option to control the gain of the mixer when the signal multiplier is used. Equation 8 shows the real output of the mixer is shown in . When mixer_gain = 1, and both I(t) and Q(t) are simultaneously full-scale amplitude, the maximum output out of the mixer is $0.707 + 0.707 = 1.414(3 \text{ dB})$, which can cause clipping of the signal, and should therefore be used with caution.

When mixer_gain = 0 (default setting), the gain through the mixer is $\sqrt{2}/2$ or -3 dB . In most cases, this loss in signal power is undesirable. TI recommends using the gain function to increase the signal by 3 dB to compensate the loss. Hence, the mixer_gain control bit provides the 6-dB gain boost option.

4.4 Amplitude Adjustment

4.4.1 Input Code Amplitude

The DAC38RF83 family has the capability to accept either offset binary or two's complement input code format. The DAC38RF83 works at 14-bit mode or 12-bit mode. The input code resolution is 16-bit based, and most significant bit (MSB) aligned, therefore either the last 4 bits or last 2 bits are dummy bits. The data format depends on user preference and system programming environment. For user input quadrature CW tones, as shown in Equation 2, the maximum input code can only range from positive full-scale code to negative full-scale code. For constant input code from the SPI register, as shown in Equation 5, the maximum input code can only range from $1 / \sqrt{2}$ of positive full-scale code to $1 / \sqrt{2}$ of negative full-scale code. Exceeding the maximum input code saturates the digital signal and degrades the analog output performance. Table 2 shows the example binary codes and decimal equivalent codes. To convert offset binary to two's complement code, simply invert the MSB.

Table 2. Binary and Decimal Equivalent Code of Offset Binary Format and Two's Complement Format

INPUT SCALE	OFFSET BINARY (16 BIT)	DECIMAL EQUIVALENT	TWO'S COMPLEMENT CODE	DECIMAL EQUIVALENT
+Full-scale	1111-1111-1111-1111	65535	0111-1111-1111-1111	32767
+0.75 Full-scale	1110-0000-0000-0000	57344	0110-0000-0000-0000	24576
+0.707 Full-scale	1101-1010-0111-1110	55934	0101-1010-0111-1110	23166
+0.5 Full-scale	1100-0000-0000-0000	49152	0100-0000-0000-0000	16384
+0.25 Full-scale	1010-0000-0000-0000	40960	0010-0000-0000-0000	8192
Zero	1000-0000-0000-0000	32768	0000-0000-0000-0000	0
-0.25 Full-scale	0110-0000-0000-0000	24576	1110-0000-0000-0000	-8192
-0.5 Full-scale	0100-0000-0000-0000	16384	1100-0000-0000-0000	-16384
-0.707 Full-scale	0010-0101-1000-0010	9602	1010-0101-1000-0010	-23166
-0.75 Full-scale	0010-0000-0000-0000	8192	1010-0000-0000-0000	-24576
-Full-scale	0000-0000-0000-0000	0	1000-0000-0000-0000	-32768

4.4.2 Output Current Adjustment

The DAC analog full-scale output current comes from 2 parts: I_{RBIAS} and $I_{coarseTrim}$, which can be expressed as Equation 9.

$$I_{OUT_{FS}} = I_{RBIAS} + I_{CoarseTrim} \tag{9}$$

I_{RBIAS} is the fixed current setting through the adjustment by the external RBIAS resistor. Normally, TI recommends setting RBIAS to 3.6 KΩ for a fixed current through RBIAS of 250 uA (on-chip bandgap reference voltage is 0.9 V). This 250 uA is scaled 128 times internally, then gives I_{RBIAS} . I_{RBIAS} can be calculated by Equation 10.

$$I_{RBIAS} = 128 \times (V_{BG} \div R_{BIAS}) = 128 \times (0.9 \text{ V} \div 3.6 \text{ K}\Omega) = 32 \text{ mA} \tag{10}$$

$I_{coarseTrim}$ is the current from course trim current sources, which can be configured by the user through a SPI register setting (register field DACFS[3:0]). The register setting can adjust $I_{coarseTrim}$, which provides a way to let the user program the output full scale current. Equation 11 shows the detailed setting of $I_{coarseTrim}$.

$$I_{coarseTrim} = 2 \times (\text{DACFS} - 11) \tag{11}$$

Register field DACFS[3:0] has a range from decimal value 0 to 15, which leads to $I_{OUT_{FS}}$ from 10 mA up to 40 mA.

4.5 Complex Mixer Output Summing

Followed by the complex mixer, an inverse sinc FIR filter compensates the droop because of sample and hold of the DAC. The output of inverse sinc FIR filter comes into a summation block, which can sum up to four paths from the output of the total four DUCs. Namely, the output summation block allows addition of samples from each DUC in the current channel. It is also possible to add the outputs from DUCs in adjacent channels. The function of the block can be represented by Equation 12.

$$\text{OUTSUM}_{\text{output}} = \text{SAME}_{AB} + \text{SAME}_{CD} + \text{ADJ}_{AB} + \text{ADJ}_{CD} \tag{12}$$

$\text{OUTSUM}_{\text{output}}$ is the output of the summation block. SAME_{AB} is the input data of the summation block from DUC path AB in the same DAC channel. SAME_{CD} is the input data from DUC path CD in the same DAC channel. ADJ_{AB} is the input data from DUC path AB in the adjacent DAC channel. ADJ_{CD} is the input data from DUC path CD in the adjacent DAC channel. Because DUC operates with 16-bit-width, the data coming from each DUC is also 16 bits. Due to the summation operation, we should perform a rounding operation to avoid data overflow 16 bits wide. After addition, rounding reduces the word size back to 16 bits. If two DCUs are added together, the least significant bit (LSB) bit [0] of the summation result is obsolete, and bit [16:1] is used as the final 16-bit summation result. Depending on how many outputs of DUCs are added, the exact number of rounding bits is decided. Table 3 shows the rounding scheme.

Table 3. Rounding Scheme of Summation Block

NUMBER OF CHANNELS ADDED	NUMBER OF BITS ROUNDED
0	0, Use bits [15:0] from the result
1	1, Use bits [16:1] from the result and bit [0] used for rounding
2	2, Use bits [17:2] from the result and bits [1:0] used for rounding
3	3, Use bits [18:3] from the result and bits [2:0] used for rounding
4	4, Use bits [19:4] from the result and bits [3:0] used for rounding

4.6 HD2 and IM2 Consideration

An ideal, linear, 2-port RF component transfers input signal to output signal without any distortion. However, in practice, the DAC is an active component in the RF system, which behaves with some kind of nonlinearity. By using the Taylor series expansion, the design approaches the nonlinearity behavior of the DAC mathematically. By applying 2-tone signal ω_1 and ω_2 as the input, the second-order item of nonlinearity generates distortion components HD2 (second-order harmonic distortion) and IM2 (second-order intermodulation distortion). IM2 has $\omega_1 - \omega_2$ and components. When ω_1 and ω_2 are very close, $\omega_1 - \omega_2$ locates around 0, and $\omega_1 + \omega_2$ locates around HD2. However, due to Nyquist folding back, second-order distortions can fall in-band. This concept is explained in Section 4.7.

4.7 HD3 and IM3 Consideration

Similar to the second-order distortion, caused by the second item of nonlinearity expansion, by applying 2-tone signal ω_1 and ω_2 as the input, the third-order item generates HD3 (third-order harmonic distortion) and IM3 (third-order harmonic distortion). IM3 distortion has components of $2\omega_1 - \omega_2$, $2\omega_2 - \omega_1$, $2\omega_1 + \omega_2$, and $2\omega_2 + \omega_1$. When ω_1 and ω_2 are very close to each other, IM3 has components $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ around ω_1 and ω_2 . $2\omega_1 + \omega_2$ and $2\omega_2 + \omega_1$ are located around HD3. Similar to the case of HD2, because of the Nyquist folding back, HD3 and IMD3 may also fall in-band. As Figure 8 shows, due to the nonlinearity caused by the DAC internal sampling holding process, harmonic distortion folds back to the first Nyquist zone. The fundamental is in the first Nyquist zone, so the folding back harmonic distortion may fall in-band, which degrades the in-band SFDR performance. By performing a good sampling frequency plan, users can avoid the folding back harmonic distortion falling in-band.

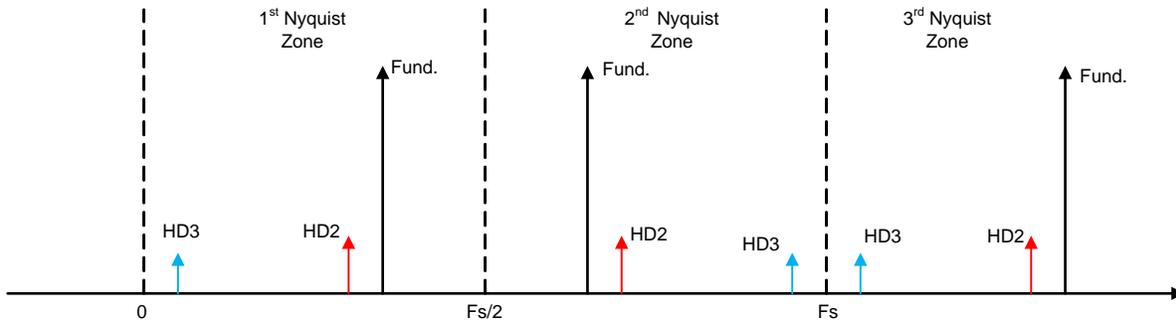


Figure 8. Harmonics Folding Back

NOTE: The amplitude variation followed by the $\sin(x) / x$ function, caused by the sampling and hold process, is ignored in this plot.

4.8 DAC Phase Noise Consideration

Let us consider the impact of phase noise due to a divider. If an ideal divider is used, the time jitter of a certain clock edge remains the same at the input and output of the clock divider. Figure 9 shows a divide-by-two case.

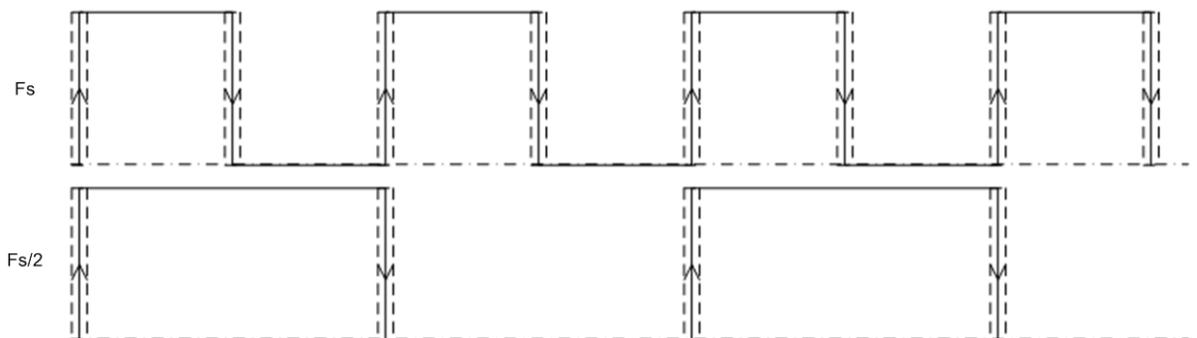


Figure 9. Time Jitter of Divided Down Clock

Jitter is a conversion of clock-phase noise power to the RMS movement of the clock sampling instant in seconds. When the clock is divided down by N, the phase noise at the divider output is improved by $20 \times \log_{10}(N)$, while the time domain jitter remains the same. Namely, there is lower-jitter energy for the divided clock in a certain clock period.

When it comes to the DAC output phase, users can see that the ideal DAC functions as a clock divider. For every divide-by-N output, the output phase noise improves by $20 \times \log_{10}(N)$ because the rising- and falling-edge jitter contents are cut back by N. For instance, if the DAC output is at $F_s/2$, the phase noise improves by 6 dB. Actual DAC output noise includes the DAC intrinsic noise, power supply noise from the DAC core, and clock phase noise.

If optimal phase noise is required, TI recommends the highest sample rate with the lowest output frequency. Also use the best performance clock and power supply rails.

4.9 Synchronize Mixers and NCOs

To achieve phase alignment among the four NCOs and four digital mixers, the DAC38RF83 offers several ways to synchronize digital mixers and NCOs. Figure 10 shows the synchronization scheme for each DUC path. The other three DUCs inside the DAC have the same synchronization design.

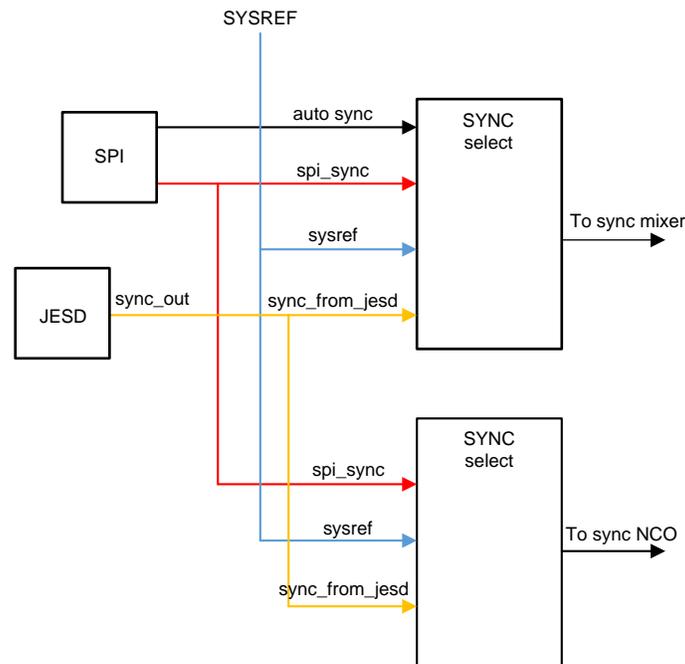


Figure 10. NCO and Mixer Synchronization

The mixer can be synchronized by the auto-sync signal from the SPI block. The auto-sync signal is a synchronization signal generated after a write operation to a particular SPI register is completed. The spi_sync signal is generated when the SPI bit SPI_SYNC is written high, which provides synchronization to the mixer or NCO. The SYSREF signal captured by the device clock can be also used for the synchronization purpose. The sync_from_jesd signal is generated from the JESD block. When the ILA sequence is complete, the JESD204B block issues one pulse on the sync_out signal, which can be used to synchronize the mixer and NCO.

5 Getting Started Hardware

5.1 Required Hardware

The required hardware for the TIDA-01084 reference design is as follows:

- DAC38RF83 EVM Rev D – 1x EVM. (Evaluation of the DAC38RF83 is accomplished by ordering the DAC38RF82EVM which also covers the DAC38RF83.)
- Signal generator – used to provide a reference clock to the DAC when the internal PLL of the DAC is used, or to provide a sampling clock to the DAC when an external sampling clock is used.

5.2 DAC38RF83 EVM Setup in On-Chip PLL Mode

The DAC38RF83 has an on-chip PLL, which can be used for generating the sampling clock from a relative low-frequency clock. The reference clock is provided at the J4 SMA input on the EVM board, and the recommended power is 8 dBm. Meanwhile jumper JP10 should be disconnected to power down the onboard clock divider.

5.3 DAC38RF83 EVM Setup in External Clock Mode

The DAC38RF83 can accept a sampling clock of up to 9 GSPS directly with bypassed on-chip PLL. The sampling clock is provided through the J1 SMA input on the EVM board, and the recommended power is 16 dBm. Meanwhile, the jumper JP10 should be connected, to power up the onboard clock divider, which is used to divide the external clock then fed into the LMK04828.

6 Getting Started Firmware

6.1 Required Software

The DAC38RF83 EVM GUI is used to control and program the onboard DAC38RF83 and onboard LMK04828.

7 Test Setup

This section details the test setup step-by-step to output four CW tones at the DAC channel A output.

7.1 Setup With Clocking From On-Chip PLL

1. Disconnect jumper JP10 of the DAC38RF83 EVM.
2. Apply 5-V power supply to J21 of the DAC38RF83 EVM. D11 turns green when power is provided.
3. Use the USB 2.0 type B cable to connect the PC with J16 of the DAC38RF83 EVM.
4. Connect the external 1105.92-MHz, 8-dBm clock from the signal generator to J4 SMA input of the DAC38RF83 EVM.
5. Launch the DAC38RF83 EVM GUI.
6. Click the Reconnect FTDI? button in the upper right corner to establish the link between the PC and DAC38RF83 EVM onboard FTDI chip.
7. Toggle the Not in RESET button twice to reset the DAC38RF83. Click the LOAD DEFAULT button to load the default register values of the DAC38RF83 and LMK04828.
8. Set the value as in [Figure 11](#), then click on the CONFIGURE DAC button to configure the DAC38RF83 according to the setting created.
9. Click on the PLL AUTO TUNE button to lock the DAC38RF83 on-chip PLL.
10. Click on the Reset DAC JESD Core & SYSREF TRIGGER button.

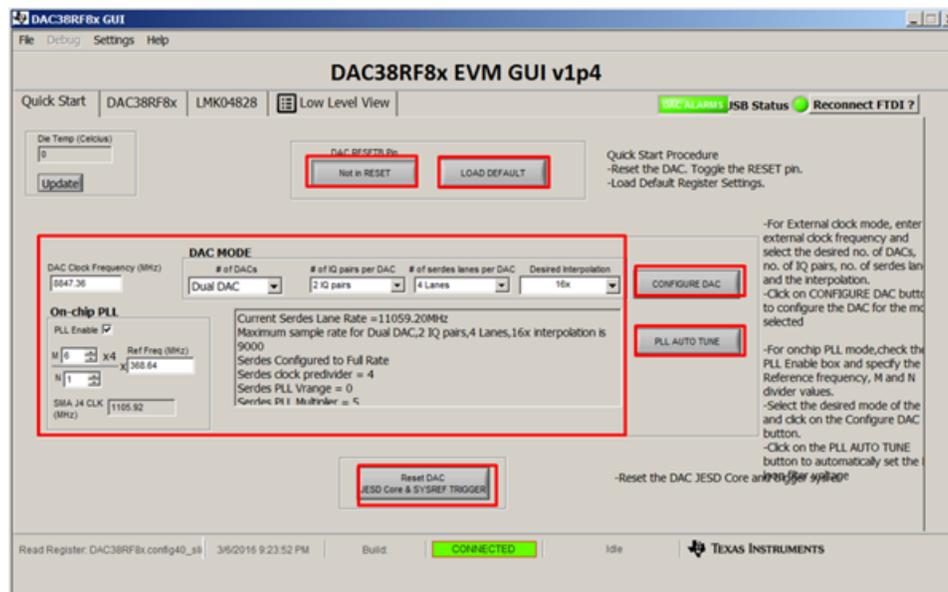


Figure 11. Quick Start Page of GUI

11. Set the Digital(DAC A) tab as shown in [Figure 12](#). Two NCOs are enabled with frequency settings of 2135 MHz and 2145 MHz. Enable the constant input data block, and then set the value to 0x5A73, which is -3 dB back off from the full scale, to avoid digital saturation. The summation block adds the DAC A and DAC B outputs of up to two DUCs outputs, which provide four tones output at DAC A. Click on the UPDATE NCO button to resync the NCO output.

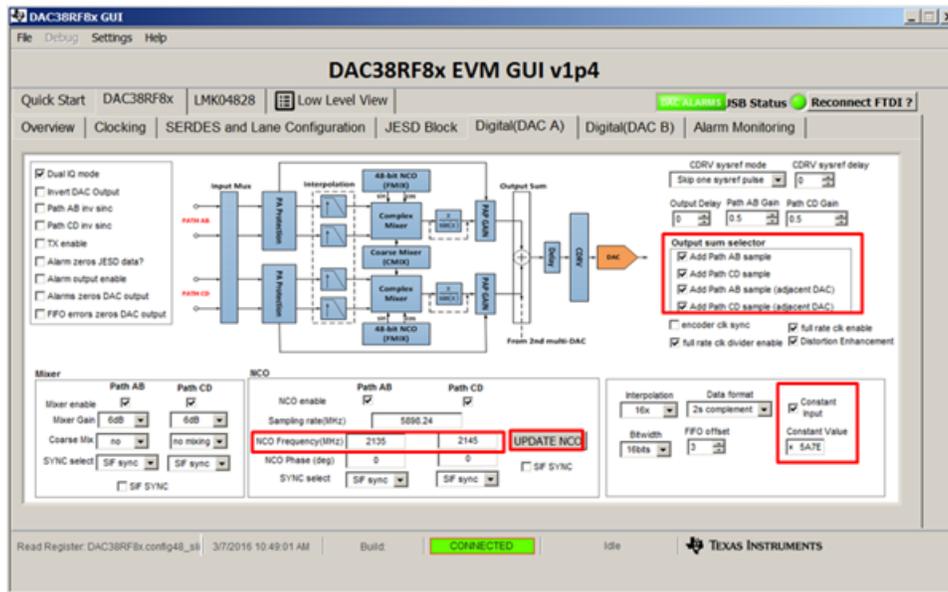


Figure 12. Digital Setting of DAC A

- Set the Digital(DAC B) tab as below. Two NCOs are enabled with frequency settings of 2125 MHz and 2155 MHz. Enable the constant input data block and set the value to 0x5A73, which is -3 dB back off from the full scale, to avoid digital saturate. Click on the UPDATE NCO button to resync the NCO output.

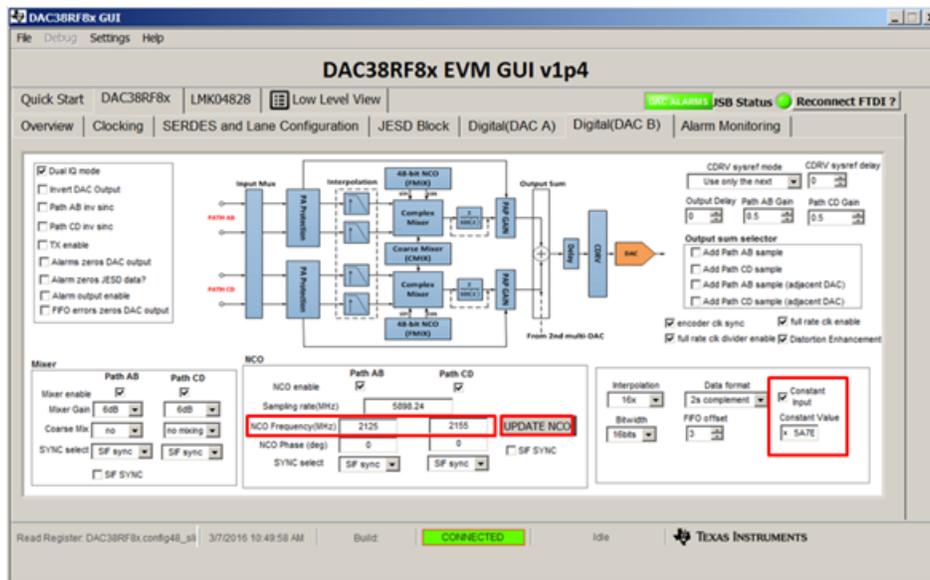


Figure 13. Digital Setting of DAC B

7.2 Setup With Clocking From External Sampling Clock

1. Connect jumper JP10 of the DAC38RF83 EVM.
2. Follow Steps 2 and 3 of [Section 7.1](#).
3. Connect the external 8847.36 MHz, 16-dBm clock from the signal generator to the J1 SMA input of the DAC38RF83 EVM.
4. Follow Steps 5 and 6 of [Section 7.1](#).
5. Set the value as shown in [Figure 14](#), then click on the CONFIGURE DAC button to configure the DAC38RF83 according to the setting created.

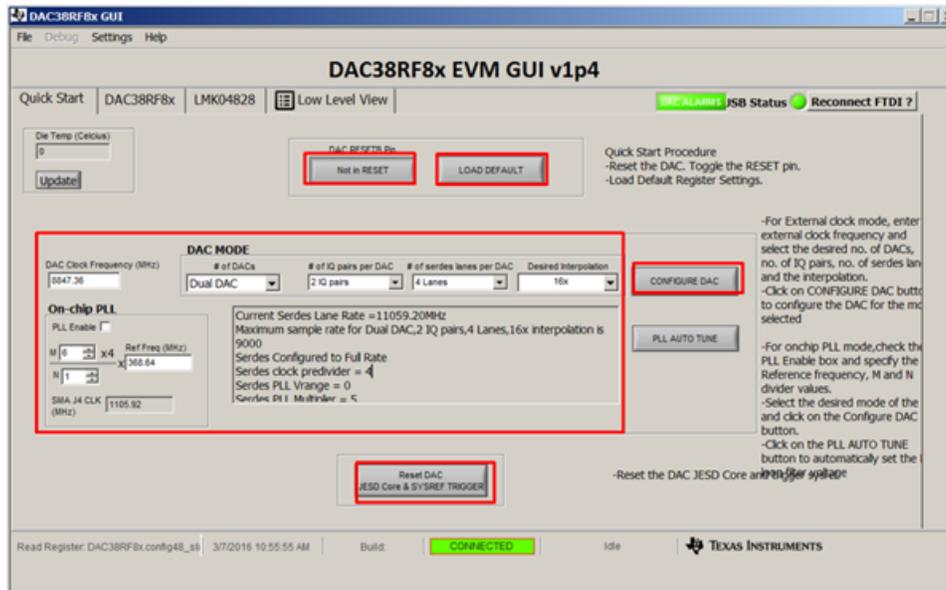


Figure 14. Quick Start Page of GUI

6. Click on the Reset DAC JESD Core & SYSREF TRIGGER button.
7. Follow Steps 10 and 11 of [Section 7.1](#).

8 Test Data

8.1 Output-Tone Phase Noise Performance

Set the DAC38RF83 EVM to external clock mode with of a sampling rate of 6000 MHz, which is provided by the SMA100A. Set the coarse gain setting to 10. Back off the digital constant data by 3 dB to avoid saturation. Use different coarse mixer settings to generate a single CW tone at different frequencies. Compare the phase noise of the output signal tone with respect to the phase noise of the sampling clock, as shown in Figure 15.

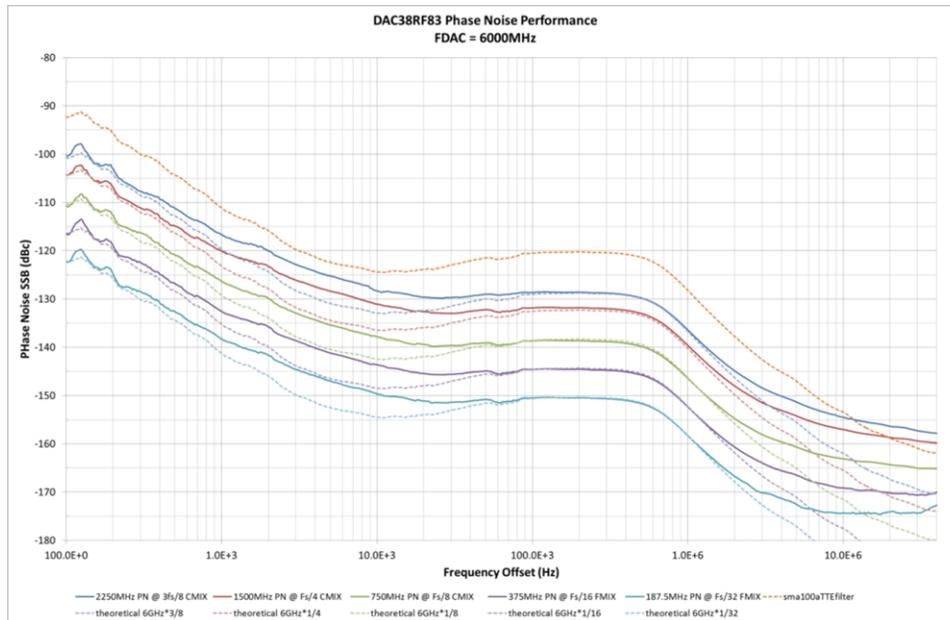


Figure 15. Measured Phase Noise and Theoretical Phase Noise of CMIX Output Tones

The phase noise of the DAC output tone may be contributed to power-supply phase noise, clock phase noise, and DAC-intrinsic phase noise. The DAC-intrinsic phase noise can be divided into clock-correlated phase noise and clock-uncorrelated phase noise. The clock-uncorrelated phase noise may come from 1/F noise and shot noise, which is determined by the semiconductor. The clock-correlated phase noise is a part of the DAC-intrinsic phase noise, which is correlated to the phase noise of the sampling clock.

To get the DAC-intrinsic phase noise, it is assumed that the clock-correlated phase noise is negligible. First, the phase noise of the DAC output tone can be measured by a phase noise analyzer in logarithm (dB). Second, convert the measured phase noise in logarithm (dB) to linear power. Third, measure the clock phase noise with the phase noise analyzer in logarithm (dB), and calculate the divided-down phase noise of the clock in logarithm (dB), which is the ideal phase noise of the DAC output, then convert it into linear power. Then, by subtracting the ideal output phase noise in linear power from the measured DAC output phase noise linear power, results in the DAC intrinsic phase noise in linear power. Lastly, by converting the linear power to logarithm (dB) gives the DAC intrinsic phase noise at different output frequencies, as shown in Figure 16.

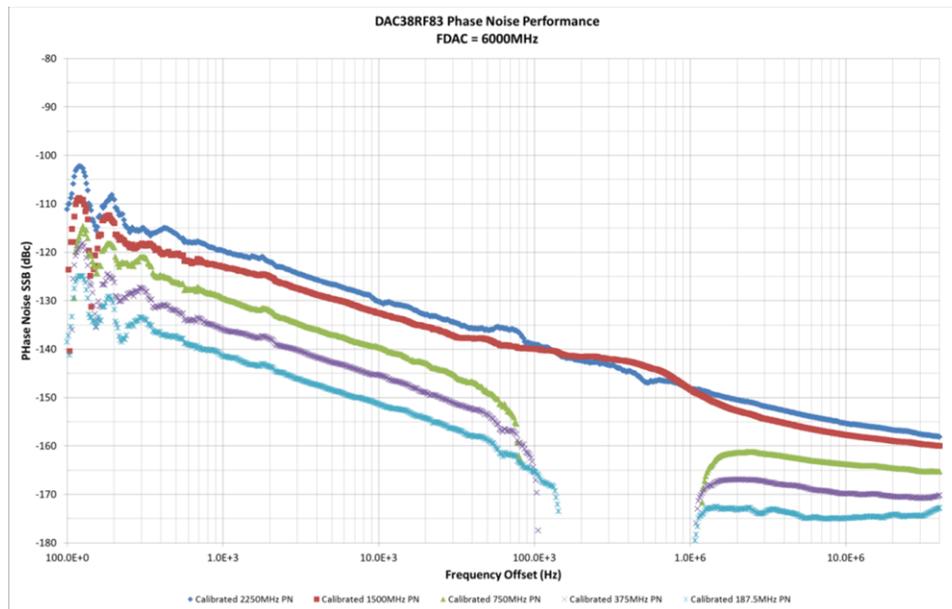


Figure 16. DAC Intrinsic Noise at Different Output Frequencies

8.2 Four-Tones Output of DACA

Figure 17 shows the spectrum of the DACA output with the implementation of a simple multitone generator. Four tones are centered at 2140 MHz with a separation of 10 MHz from each other.

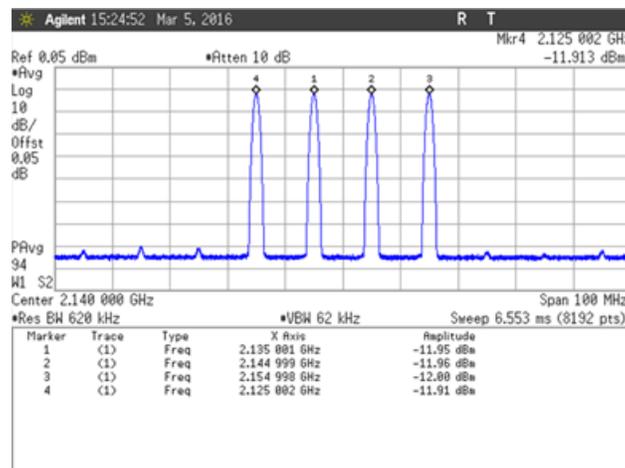


Figure 17. Output Four Tones Spectrum

8.3 HD2 and IMD2 Performance

Set the DAC38RF83 EVM to external clock mode with a sampling rate of 5898.24 MHz. Set the coarse gain setting to 10. Back off the digital constant data by 3 dB to avoid saturation. Use DAC channel A to output two tones at $F_1 = 2135$ MHz, and $F_2 = 2145$ MHz with a separation of 10 MHz. HD2 and IMD2 are caused by the second-order item of nonlinearity. Due to the Nyquist folding back, distortion like HD2, IMD2, and IMD4, which are greater than $F_s/2$, fold back to the first Nyquist zone. As seen in Figure 18, F_1 and F_2 are 10 MHz apart from each other, and HD2 of F_1 and HD2 of F_2 is 2×10 MHz apart from each other. The IMD2, IMD4, and HD2 artifacts are within the 1.6-GHz range, which designers need to plan ahead of time, to prevent the artifacts from falling into major communications bands.

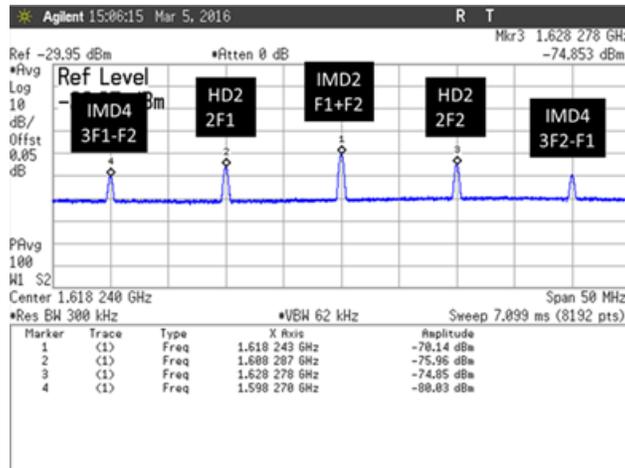


Figure 18. HD2 and IMD2

8.4 HD3 and IMD3 Performance

Set the DAC38RF83 EVM to external clock mode with a sampling rate of 5898.24 MHz. Set the coarse gain setting to 10. Back off the digital constant data by 3 dB to avoid saturation. Use DAC channel A to output two tones at $F_1 = 2135$ MHz, and $F_2 = 2145$ MHz with a separation of 10 MHz. HD3 and IMD3 are caused by the third-order item of nonlinearity. IMD3 components like $2F_1 - F_2$ and $2F_2 - F_1$ are close to F_1 and F_2 , respectively, if F_1 and F_2 are close to each other. Figure 19 shows the IMD3 performance.

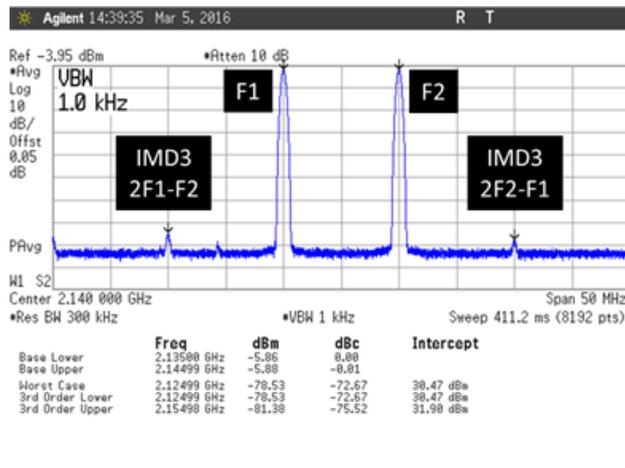


Figure 19. IMD3

By backing off the output tone power, we can get the IMD3 and IIP3 versus output power.

Table 4. IMD3 Versus Back Off Power

DIGITAL BACK OFF (dBFs)	OUTPUT POWER (dBm)	IMD3 (dBc)	IP3 (dBm)
0	-5.86	-72.67	30.47
-3	-8.87	-70.44	26.35
-6	-11.97	-68.12	22.09
-9	-14.97	-69.05	19.57
-12	-18.03	-68.55	16.32

Backing off the power of the digital input signal may result in less significant improvement when compared to traditional analog devices (see Table 4). This behavior is mainly due to the quantization noise and associated discrete levels in the RF DAC. IMD3 components $2F_1+F_2$, $2F_2+F_1$, and HD3 are close to each other if F_1 and F_2 are close to each other, at roughly three times the fundamental frequency. If these distortions are greater than $F_s/2$, aliasing occurs, and the distortion can be checked at the first Nyquist zone, as shown in Figure 20. Because F_1 and F_2 are 10 MHz apart from each other, HD3 are 3×10 MHz apart from each other. The IMD3 and HD3 artifacts are within the 500-MHz range, which designers need to plan ahead of time, to prevent the artifacts from falling into major communications bands.

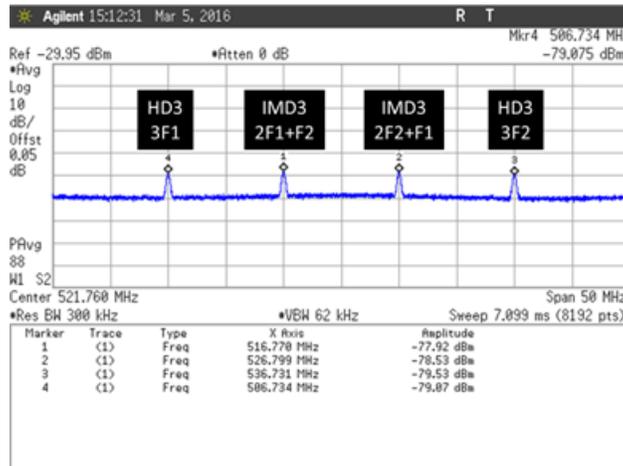


Figure 20. IMD3 and HD3

8.5 SYNC Output Tones

Use DAC channel A to output a single tone at 500 MHz, and DAC channel B to output a single tone at 500 MHz. Each DAC channel has the input digital data from its own DUC path AB. Using the spi_sync signal to achieve the phase alignment between DACA and DACB is not reliable, because the spi_sync signal is asynchronous to both DUC digital blocks. In this design, a global SYSREF pulse is the most reliable method for synchronizing the phase between DACA and DACB. Figure 21 shows the synchronization of the DACA and DACB output through a single SYSREF pulse.

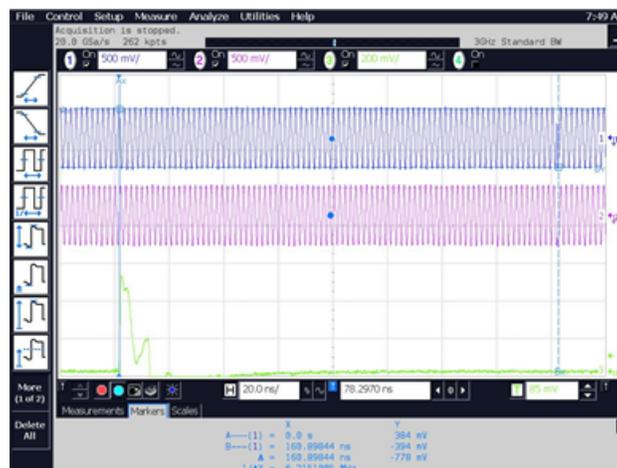


Figure 21. Synchronization of DACA and DACB Output

The green waveform shown in [Figure 21](#) is a single SYSREF pulse (input to the scope is AC coupled). The blue waveform is the DAC A output at 500 MHz. The red waveform is the DAC B output at 500 MHz. Initially, the two tones have the same frequency of 500 MHz, but different phases. After the SYSREF is captured, approximately 160.9 ns are required to align the phase. [Figure 22](#) shows a closer look at the transition from misaligned tones to aligned tones.

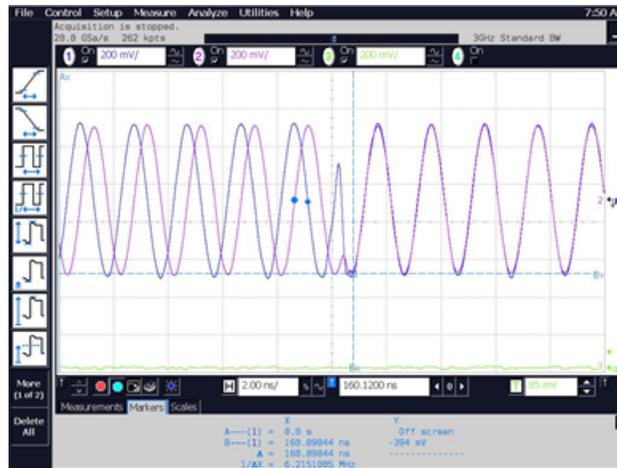


Figure 22. Transition From Misaligned Tones to Aligned Tones

It has been observed that it takes the same time to switch from one frequency to another frequency. In [Figure 23](#), the initial output frequency of DACB output is 500 MHz. By capturing the SYSREF signal, the DACB output frequency is changed to 800 MHz, while the DACA output stays at 500 MHz. Approximately 160.53 ns are required to complete the frequency switching.

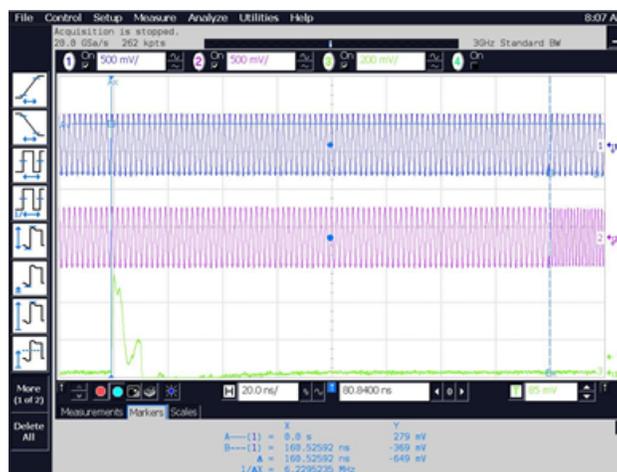


Figure 23. Transition From 500 MHz to 800 MHz

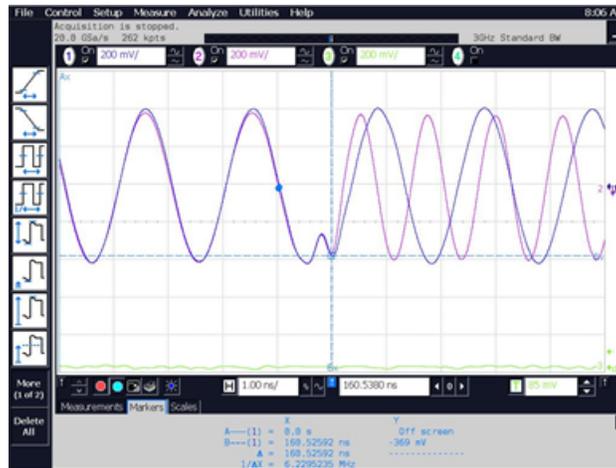


Figure 24. Closer Look at Transition From 500 MHz to 800 MHz

When changing from one frequency to another, the NCO frequency register (for example, `FREQ_NCOAB[47:0]`) should be set through SPI writing. If the NCO phase register (for example, `PHASE_NCOAB[15:0]`) must be updated at the same time, the NCO phase register writing should also be performed. The NCO phase setting is 16 bits wide, and the NCO frequency setting is 48 bits wide. The DAC38RF83 register is 16 bits wide. Therefore, the NCO frequency setting is completed by writing three registers. For a SPI register writing, 24 SPI clock cycles are needed, which includes an 8-bit instruction cycle, and a 16-bit data cycle.

The maximum SPI clock rate of the DAC38RF83 is 10 MHz. Therefore, the theoretical time needed for one NCO frequency update is 7.2 μ s, and the time needed for one NCO phase update is 2.4 μ s. Another factor to consider, when the user wants to update the NCO frequency or phase of the other channel, the SPI page should be reselected by writing the page set register `PAGE_SET[15:0]`. Hence, setting the page adds 2.4 μ s. In summary, the theoretical maximum time needed for one NCO frequency and phase update should be 12 μ s. If the `SYSREF` is used to synchronize the NCO and mixer output, the DAC outputs the synchronized waveform in approximately 160 ns after the `SYSREF` is issued.

9 Design Files

9.1 Schematics

To download the schematics, see the design files at [TIDA-01084](#).

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01084](#).

9.3 Layer Plots

To download the layer plots, see the design files at [TIDA-01084](#).

10 Software Files

To download the software files, see the design files at [TIDA-01084](#).

11 Terminology

- CW – Continuous wave
- DAC – Digital-to-analog converter
- SERDES – Serializers and deserializers for high-speed serial link
- JESD204B – JEDEC standardized data transfer format for high-speed data converters
- DDS – Direct digital synthesis
- DUC – Digital upconverter
- LO – Local oscillator

12 About the Author

YARN GUO is an analog field applications engineer at Texas Instruments, serving the Shenzhen, China area. After earning his MSEE from South China University of Technology in 2015, he went through TI's Analog Rotational Program under High-Speed Products and supported various high-speed ADCs and DACs. Yarn is an active member of the TI E2E™ Community and can be reached through [e2e.ti.com](#) for support.

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