User's Guide
SLAU711–March 2017

HSDC Pro With Xilinx® KCU105

This user's guide describes the functionality, hardware, operation, and software instructions to implement the High Speed Data Converter Pro Graphic User Interface (HSDC Pro GUI) with the KCU105, a Xilinx® Kintex® UltraScale™ field-programmable gate array (FPGA) evaluation kit.

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1 Introduction

The Kintex UltraScale FPGA KCU105 evaluation kit is a development board created by Xilinx. The KCU105 uses Ethernet and dual USB-to-UART capabilities to interface with a host computer and set up the FPGA. Texas Instruments has created a platform where the KCU105 can interface with TI's latest and most popular JESD204B-based high speed data converter evaluation modules (EVM) as if it were connected to a TI development board. The platform also allows users to operate the High Speed Data Converter Pro Graphic User Interface (HSDC Pro GUI) software to capture data from an Analog-to-Digital converter (ADC) as well as generate data for a Digital-to-Analog converter (DAC).

2 Functionality

The KCU105 has a standard FMC connector that proves an interface between FMC-based development boards and all TI JESD204B ADC and DAC EVMs. For communicating, the KCU105 uses Ethernet to acquire and receive data, and do register read and writes using a host PC across a Serial Peripheral Interface (SPI). The KCU105 has a dual USB-to-UART bridge interface for system control as well as reading necessary information such as the board IP address. The KCU105 also has an industry-standard JTAG connection for configuring the FPGA using the Vivado® Design Suite, a design tool by Xilinx.

The firmware designed for this integration is used to support HSDC Pro, communication through SPI, and any TI FMC-based JESD204B EVM at any line rate. This user's guide is a starting point, but the firmware is over complicated for designing a regular system. The firmware is located at the following Xilinx web site: https://www.xilinx.com/member/jesd204_eval/uhwd_2016_3_v1_0.zip. The zip file includes documentation of an example design that can be generated in Vivado 2016.3. In the Vivado project, the firmware can be stripped down and designed for a more practical system.

NOTE: Run the command **set TARGET "TI"** before creating the project to generate TI bitstreams.

3 Required Hardware

3.1 Xilinx® KCU105

The Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit is required to test the TI EVMs. For KCU105 configuration and descriptions, see the product page featuring the KCU105 Evaluation Kit: https://www.xilinx.com/products/boards-and-kits/kcu105.html.

3.2 TI ADC/DAC Evaluation Module

A TI JESD204B ADC or DAC EVM is required in the example test instructions in Section 7. For TI's EVM programmable configuration, see the product page featuring the EVM on www.ti.com.

3.3 Test Equipment

Depending on the device under test, the follow test equipment may be required:

- Low-noise RF signal generator. Recommendations:
  - HP 8644B, Rohde & Schwarz SMA100A, or equivalent
- Spectrum analyzer with RF frequency ranges. Recommendations:
  - Agilent E443A, Rohde & Schwarz FSP, or equivalent
- Bandpass filters for desired analog input. Recommendations:
  - Trilithic 5VH-series Tunable BPF, K&L BT-series Tunable BPF, TTE KC6 or KC7-series Fixed BPF
- Signal path cables, SMA or BNC with BNC-SMA adapters

4 Required Software

4.1 HSDC Pro GUI

Download the latest version of the HSDC Pro GUI (slwc107x.zip) to a local directory on a host PC. This can be found on the TI website by entering “HIGH SPEED DATA CONVERTER PRO GUI INSTALLER” in the search parameter window at www.ti.com.

Unzipping the software package generates a folder called *High Speed Data Converter Pro - Installer vx.xx.exe*, where x.xx is the version number. Run this program to start the installation.

Follow the on-screen instructions during installation.

NOTE: If an older version of the GUI has already been installed, make sure to uninstall it before loading a newer version.

Click on the **Install** button. A new window opens. Click the **Next** button.

Accept the License Agreement. Click on **Next** to start the installation. After the installer has finished, click on **Next** one last time.

The installation is now complete. The GUI executable and associated files will reside in the following directory.

```
C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro
```

When new TI high speed data converter EVMs or JESD204B interface modes become available that are not currently supported by the latest release of HSDC Pro GUI, the HSDCProv_xpxx_Patch_setup executable, available on the TI website under the High Speed Data Converter Pro Software product folder (http://www.ti.com/tool/dataconverterpro-sw), will allow the user to add these to the GUI device list. After the patch has been downloaded, follow the on-screen instructions to run the patch. The software displays the files that will be added. After running the patch, open HSDC Pro and the new parts and modes will appear in the ADC and DAC device drop-down selection box. The patch is always specific to a core GUI version and will not work for a GUI version for which the patch was not explicitly created.

4.1.1 Xilinx® Vivado® Design Suite

The Vivado Design Suite by Xilinx, is required in order to load firmware to the FPGA. See the Vivado Design Suite on Xilinx.com: https://www.xilinx.com/products/design-tools/vivado for more details. The latest build that supports this integration is Vivado 2016.3.

4.2 Serial Terminal Emulator

A serial terminal emulator is required to establish a serial port connection through the KCU105 dual UART interface. Any sort of serial terminal software, such as TeraTerm, PuTTY, or Hercules, can be used. For this user's guide, TeraTerm is used as the main terminal emulator. See the TeraTerm web page for more details.

5 DAC and ADC GUI Configuration File Changes When Using a Xilinx® Development Platform

The configuration files that come with the TI ADC and DAC EVM GUIs are set up to operate with the Altera® based, TI TSW14J56EVM. With the latest firmware, some GUIs can be configured as if they were connected to the TSW14J56EVM. If that is not the case, then the EVM may be configured with Xilinx-specified configuration files or a couple of changes to the settings of the LMK0482x registers. See Section 7 for details.

The firmware for the Xilinx Development Platforms use a separate clock input for REFCLK and core clock to give maximum flexibility and support all line rates and subclasses with a single programmable design. The Xilinx IP used in the firmware can be driven by a single clock in many circumstances (see the clocking section of the Xilinx IP product guide for more details). THE REFCLK and core clock are determined by the line rate conditions shown in Table 1.

Table 1. Multiplier Line Rate Ranges

	Max Lr (Gbps)	1.2	1.6	1.9	2	2.4	3.2	3.9	4	4.9	6.5	7.9	8.1	8.2	9.8	12.5
	Min Lr (Gbps)	1	1.20	1.60	1.90	2.00	3.20	3.01	3.90	4.00	4.90	6.50	7.90	8.10	8.20	9.80
Multiplier																
2			X	X												
10			X	X	X	X	X	X	X	X	X	X	X	X		
20					X	X	X	X	X	X	X	X	X	X	X	X
40									X	X	X	X	X	X	X	X

Line rate switching is supported across the entire speed range supported by transceivers. The ratio of REFCLK to line rate multipliers is also programmable. The multiplier is programmed by the *.ini* files located in HSDC Pro. Note: REFCLK = line rate / Multiplier

Example: A line rate of 5.0G is in the range between 4.90 Gbps and 6.5 Gbps and is supported by the multiplier values of 10, 20, and 40. Therefore, the possible values for REFCLK are:

5.0G / 10 = 500 MHz, 5.0G / 20 = 250 MHz, 5.0G / 40 = 125 MHz

6 KCU105 Quick Start-Up Instructions

The following instructions are steps to starting the Xilinx KCU105 board. These instructions are **required** to establish a connection for any EVM being used.

6.1 USB Interface and Drivers

1. Connect the EVM to FMC HPC connector J22 on the KCU105.
2. Connect the power cable to the KCU105 and turn the power switch to "ON".
3. Connect the two USB cables between the KCU105 and a host computer: one between the USB to JTAG interface J1, and the other between the dual USB-UART port J4. Ensure that Silicon Labs® drivers are installed. See the KCU105 user guide on Xilinx.com for details about the Silicon Labs CP2105GM dual USB-to-UART Bridge interface on the KCU105.
4. Connect a USB cable between the EVM and host computer.
5. Open a serial port connection with any serial terminal emulator.
6. Initialize a serial port communication to Silicon Labs Dual CP210x USB to UART Bridge: **Enhanced** COM Port. Set the baud rate of this serial connection to "115200", and leave all other defaults as set.
7. Open another serial port connection and connect to Silicon Labs Dual CP210x USB to UART Bridge: Standard COM Port. Ensure the baud rate of this serial connection is "9600", leaving all other defaults as set.
8. Connect an Ethernet cord from the KCU105 to a port such as an Ethernet switch or router that is in the same local network as the host computer. Other Ethernet interfaces are shown in the *UltraScale Hardware Demonstration* user guide on Xilinx.com.

Figure 1 shows a block diagram of the set up.

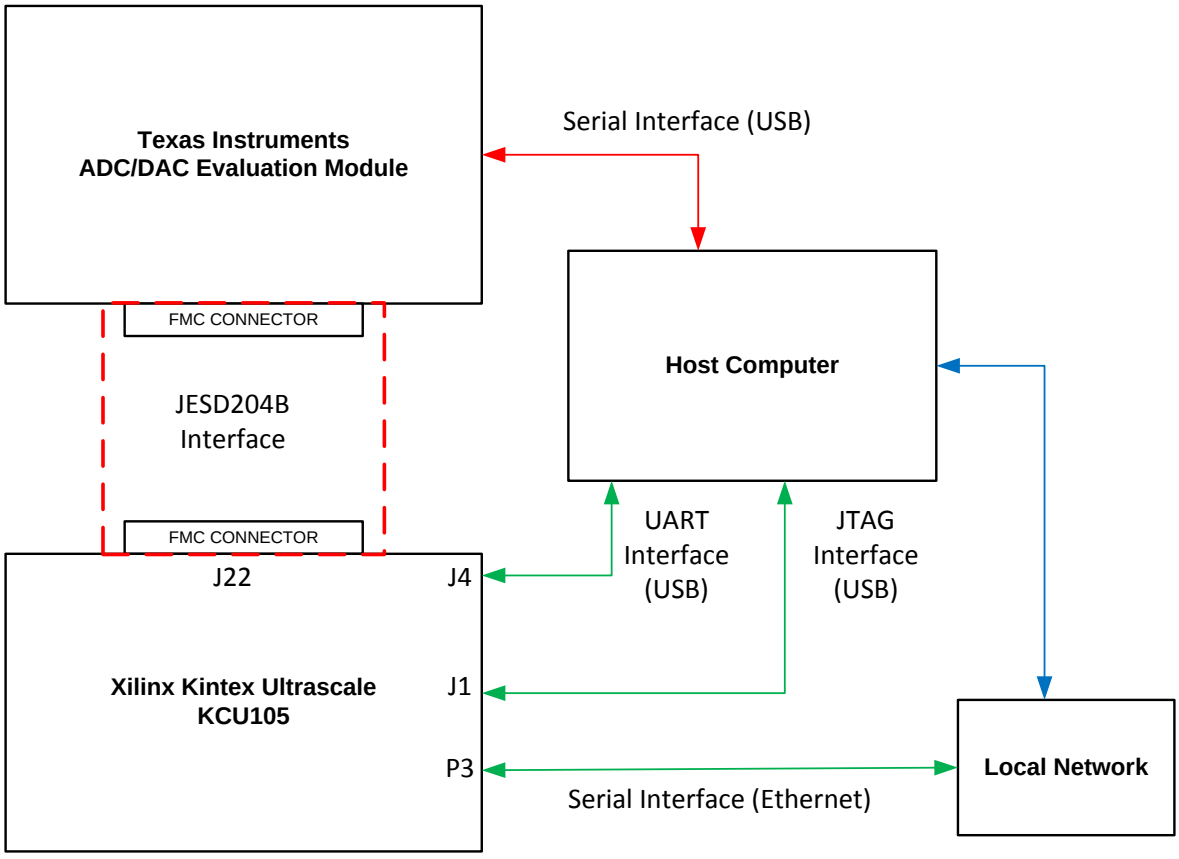

Figure 1. TI EVM With KCU105 Block Diagram

6.2 Programing the FPGA

Complete the following steps to program the FPGA:

1. Open the Xilinx Vivado 2016.3 design tool.
2. Double click on “Open Hardware Manager”.
3. Click on “Open Target” (located on the green bar), and select “Open New Target" (also at Tools → Open New Target).
4. Click on “Next” twice. Select the Hardware Target, and click “Next” again.
5. Click on “Finish”.
6. Click on “Program device” (located on the green bar). Select "xcku040_0" (also at Tools → Program device).
7. Select the proper bit stream file. The firmware is found in: **“C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\KCU105 Details\Firmware\KCU105_TI_DHCP.bit"**.

NOTE: If there is an error regarding ASCII characters, drag the bit file to the desktop and target the file there.

8. Click on “Program.”
9. A new window will open showing the status of the programming. Once this reaches 100%, the FPGA is programmed. Make sure the calibration passes and that there are no errors.

Vivado 2016.3 should look similar to Figure 2 after programming the KCU105 correctly.

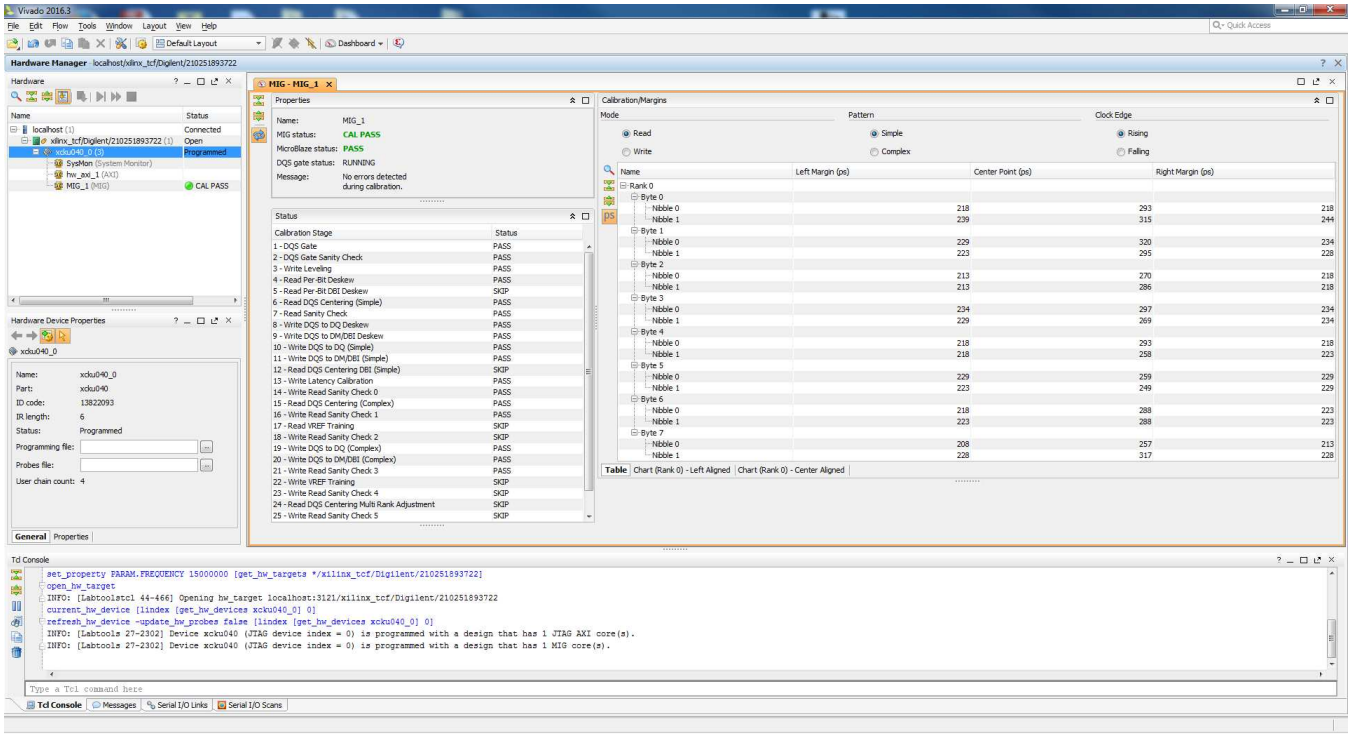

Figure 2. Passed Calibration in Vivado® 2016.3

6.3 Adjusting FPGA FMC Settings

The FMC VADJ voltage must be set to 1.8V in order for the platform to work. This is set in the Enhanced COM Port terminal.

1. Navigate to the Enhanced COM Port window. Return to the main menu by entering "0" in the terminal.
2. Enter **4** to "Adjust FPGA Mezzanine Card (FMC) settings".
3. Enter **4** again to "Set FMC VADJ to 1.8V".
4. Enter **0** to return to the main menu.
5. To check this voltage, enter **2** to "Get the Power Systems Voltages".
6. Enter **7** to "Get VADJ1D8 voltage". The voltage should appear above the menu.
7. Enter **0** to return to the main menu.

Figure 3 highlights setting the FMC VADJ to 1.8V in the Enhanced COM Port terminal.

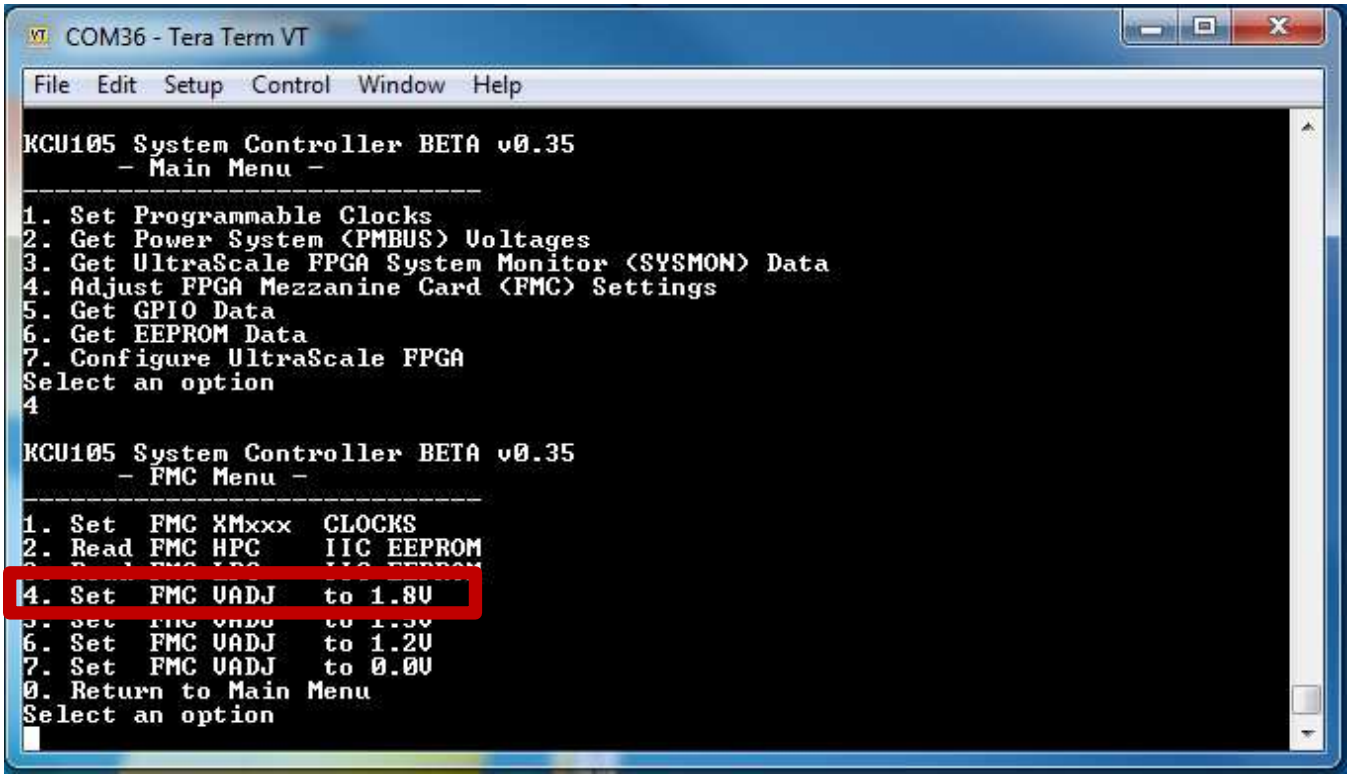

Figure 3. Setting FMC VADJ in Enhanced COM Port

6.4 IP Address and Connecting to HSDC Pro

Once the firmware has been loaded and the FPGA is programmed, the board IP address and port number will be available on the Standard COM port, shown in Figure 4.

This is required to establish a connection between the KCU105 and HSDC Pro. To connect to HSDC Pro, do the following steps:

1. Open the HSDC Pro GUI as administrator.
2. In the "Select Board" pop up, check "Connect to KCU105". Enter the IP address followed by a colon and port number. There is also an option to select from the drop-down menu. Both IP address and port number can be found in the Standard COM port terminal.
3. Press "OK" to connect to the KCU105.

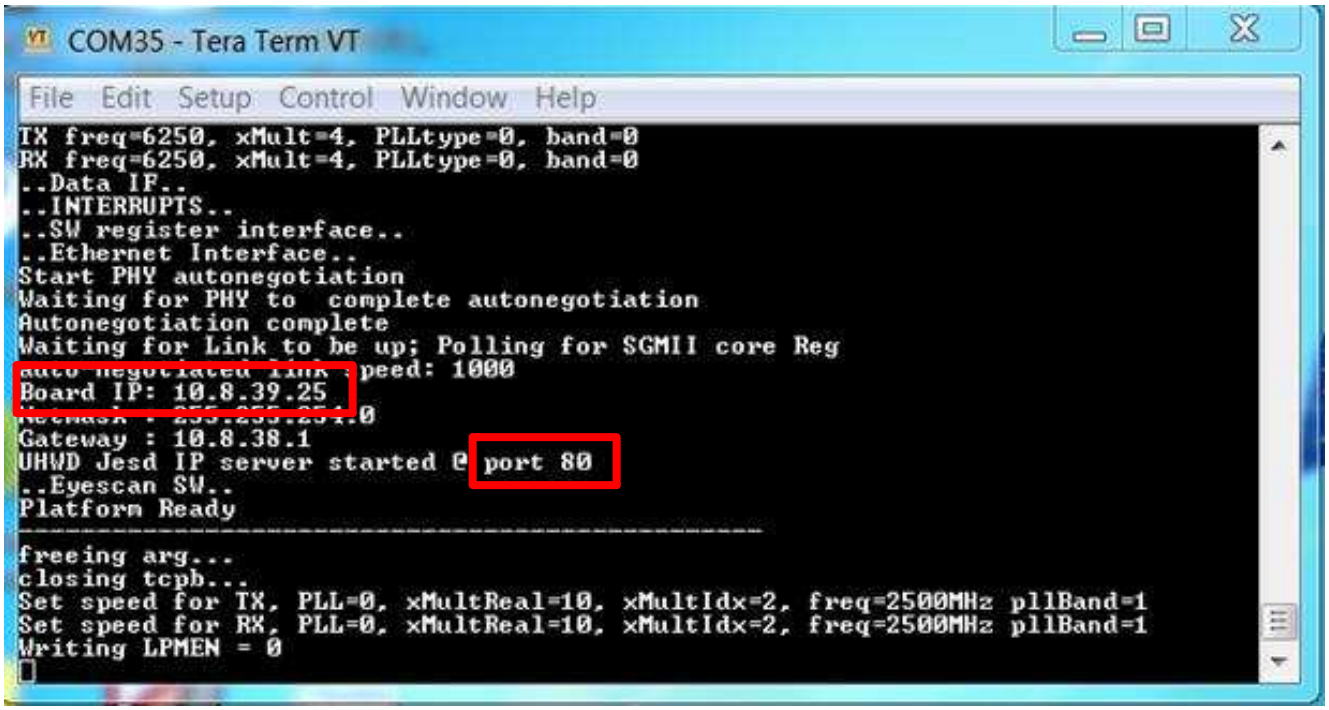

Figure 4. IP Address in Standard COM Port

Figure 5 is a screenshot of HSDC Pro connecting to the KCU105.

Figure 5. HSDC Pro Connecting to KCU105

7 Board Setup Examples

This section provides examples using the Xilinx KCU105 development platform with various JESD204B TI EVMs. Based on the EVM, the example will show what needs to be modified in order for the integration to work. The instructions in Section 6 **must be completed** before continuing with the following examples.

7.1 DAC38J84EVM with KCU105 Board Setup Example

The following section provides an example of testing the DAC38J84EVM using a KCU105 development platform. With the updated firmware, users can use the DAC38J84 GUI as if it was connected to TI's TSW14J56. Make sure the instructions in Section 6 are completed before testing the EVM. Figure 6 shows a setup between the DAC38J84EVM and KCU105.

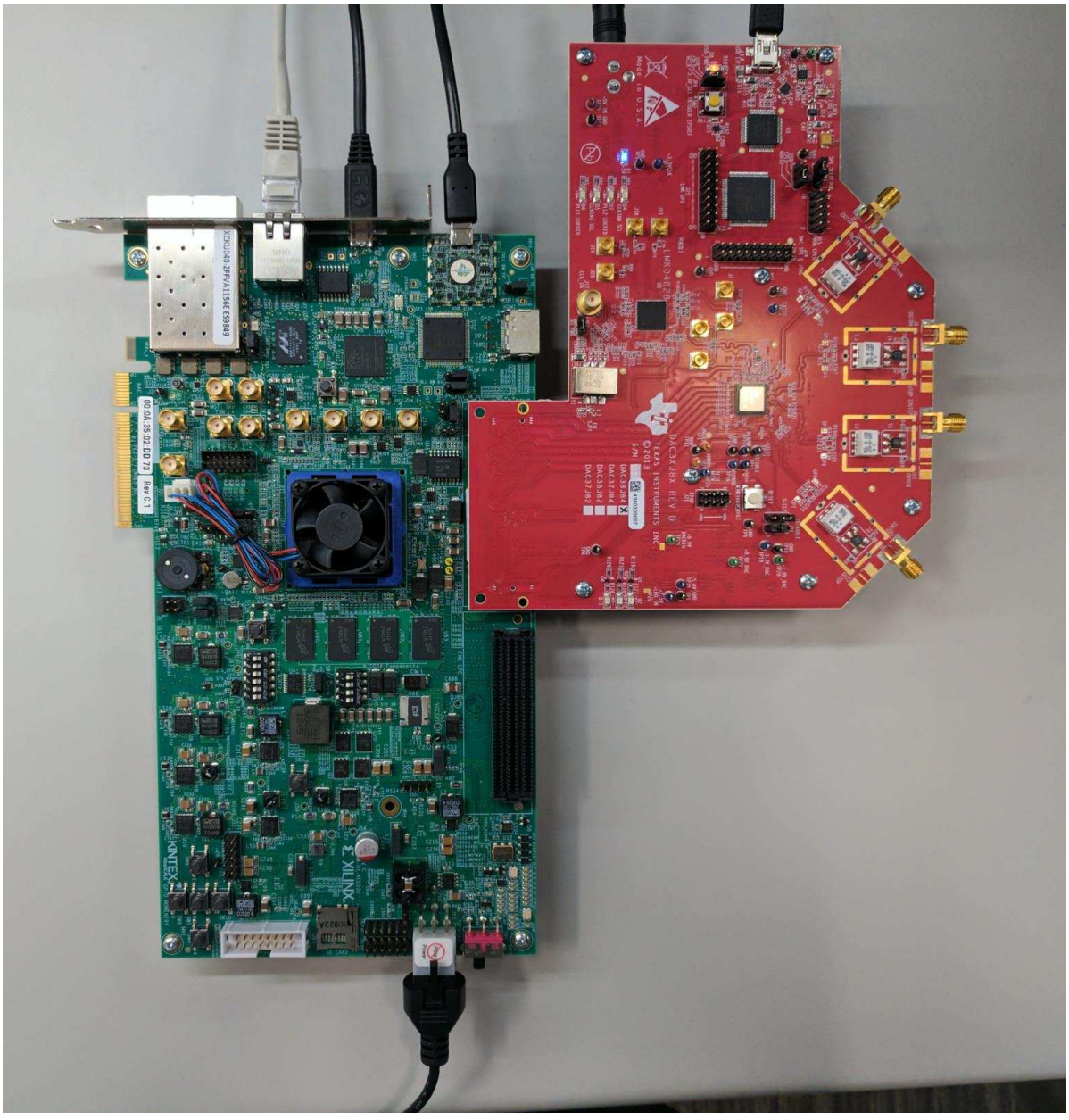

Figure 6. DAC38J84EVM Setup With KCU105

Set up the hardware as follows:

1. Connect the power cable to the DAC38J84EVM and open the DAC3XJ8X GUI. The GUI is found under "Software" on www.ti.com featuring the DAC38J84EVM.
2. Configure the GUI as done in the following:
   (a) *EVM Clocking Mode* – "Onboard"
   (b) *DAC Data Input Rate* – "1228.8" MSPS
   (c) *Number of SerDes Lanes* per DAC – "8"
   (d) *Interpolation* – "2"
   Figure 7 is a screenshot of a configured GUI for a DAC38J84EVM 8411 JESD204B mode.

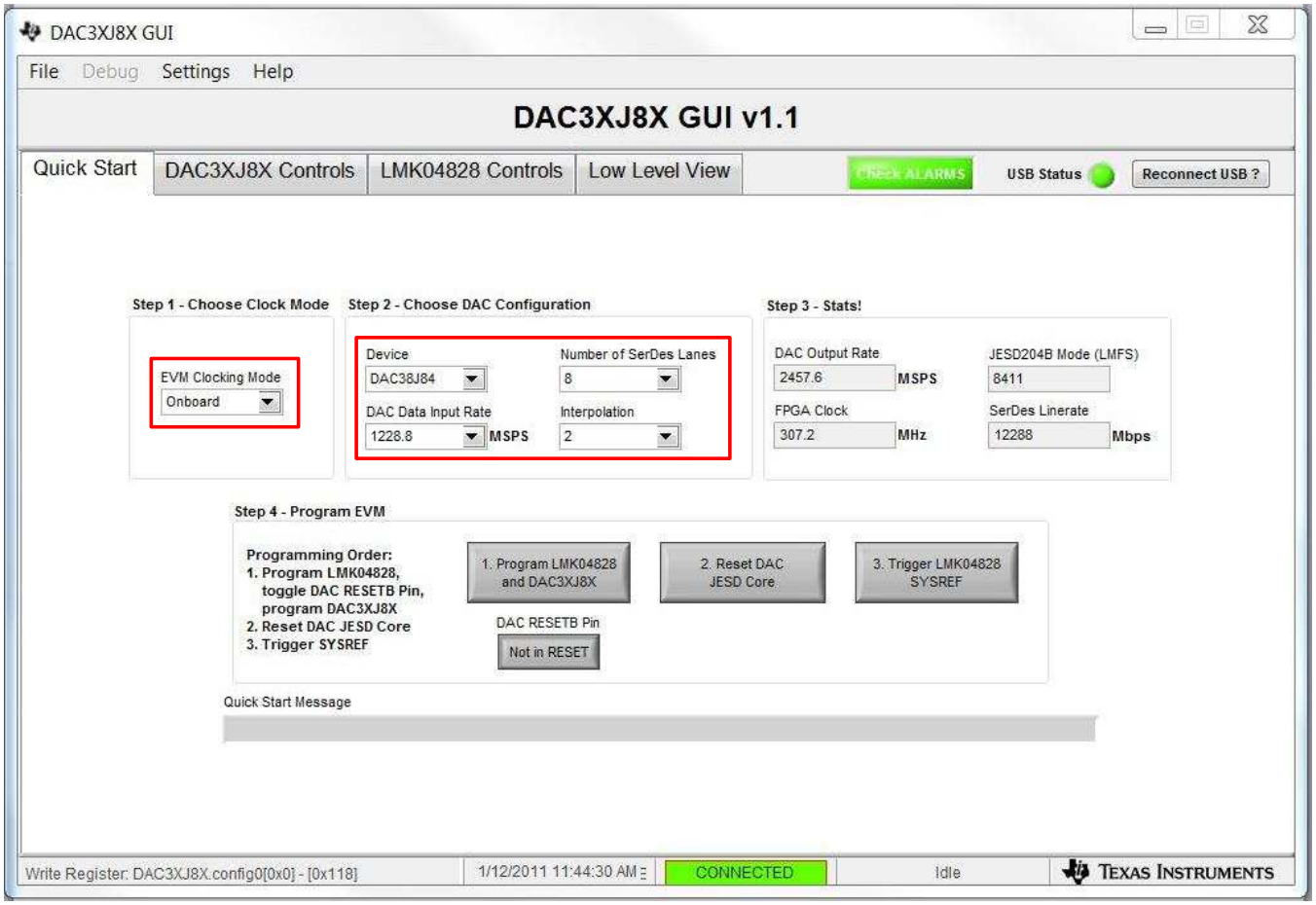

Figure 7. DAC38J84EVM GUI Configuration

3. Press the **1. Program LMK04828 and DAC3XJ8X** button.
4. Open HSDC Pro, press on the *DAC* tab, and select "DAX3XJ84_LMF_841" from the drop-down menu.
5. Add the *Data Rate (SPS)* and change the *DAC Option* to "2's Complement". Make sure the number of samples is set to at least 8192, but do not exceed 32,768. Figure 8 shows a configured GUI for a 169.35-MHz tone.

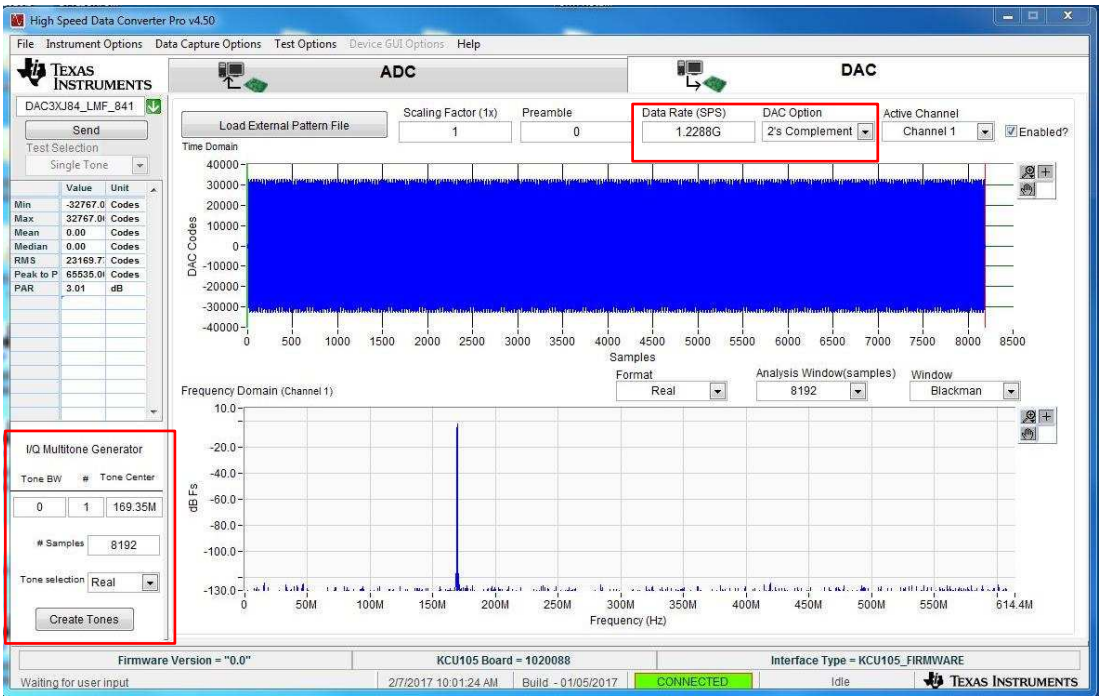

Figure 8. Generating a Tone With HSDC Pro GUI

6. Click the **Create Tones** button and press the **Send** button.
7. The new lane rate (12.288 GHz) and FPGA Clock (307.2 MHz) settings should be shown.
8. Go back to the DAC38J84 GUI and press **2. Reset DAC JESD Core** and **3. Trigger LMK04828 SYSREF**.
9. Connect channel one of the DAC38J84EVM to a spectrum analyzer and verify the signal. Figure 9 shows the analog output generated by the DAC38J84EVM.

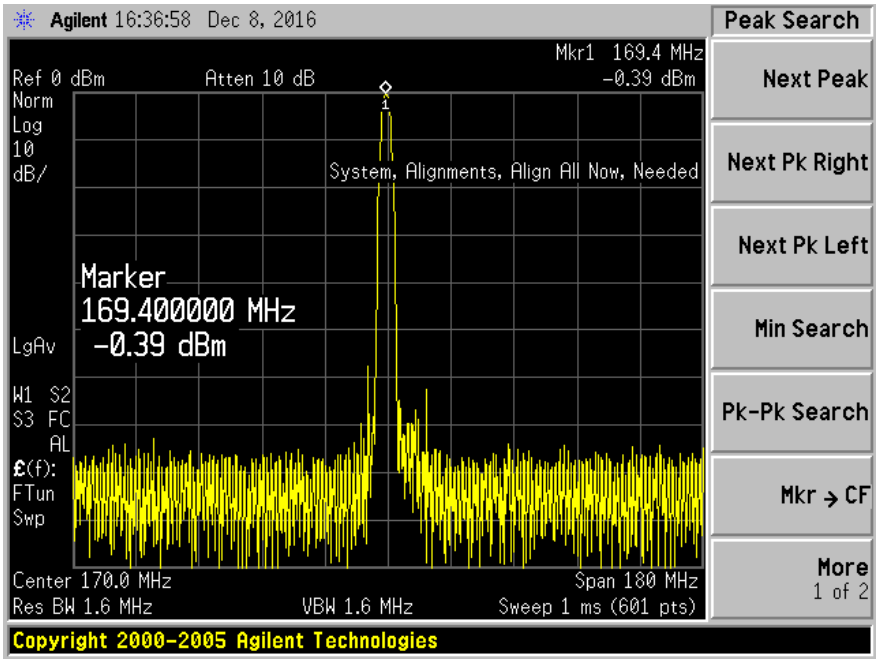

Figure 9. Analog Output by DAC38J84EVM

7.1.1 DAC38J84EVM Second Example

In this example, the same mode is used, but a different configuration that shows the limitations of the KCU105.

1. Configure the GUI as shown in Figure 10:
   (a) *EVM Clocking Mode* – "Onboard"
   (b) *DAC Data Input Rate* – "368.64" MSPS
   (c) *Number of SerDes Lanes* per DAC – "8"
   (d) *Interpolation* – "4"

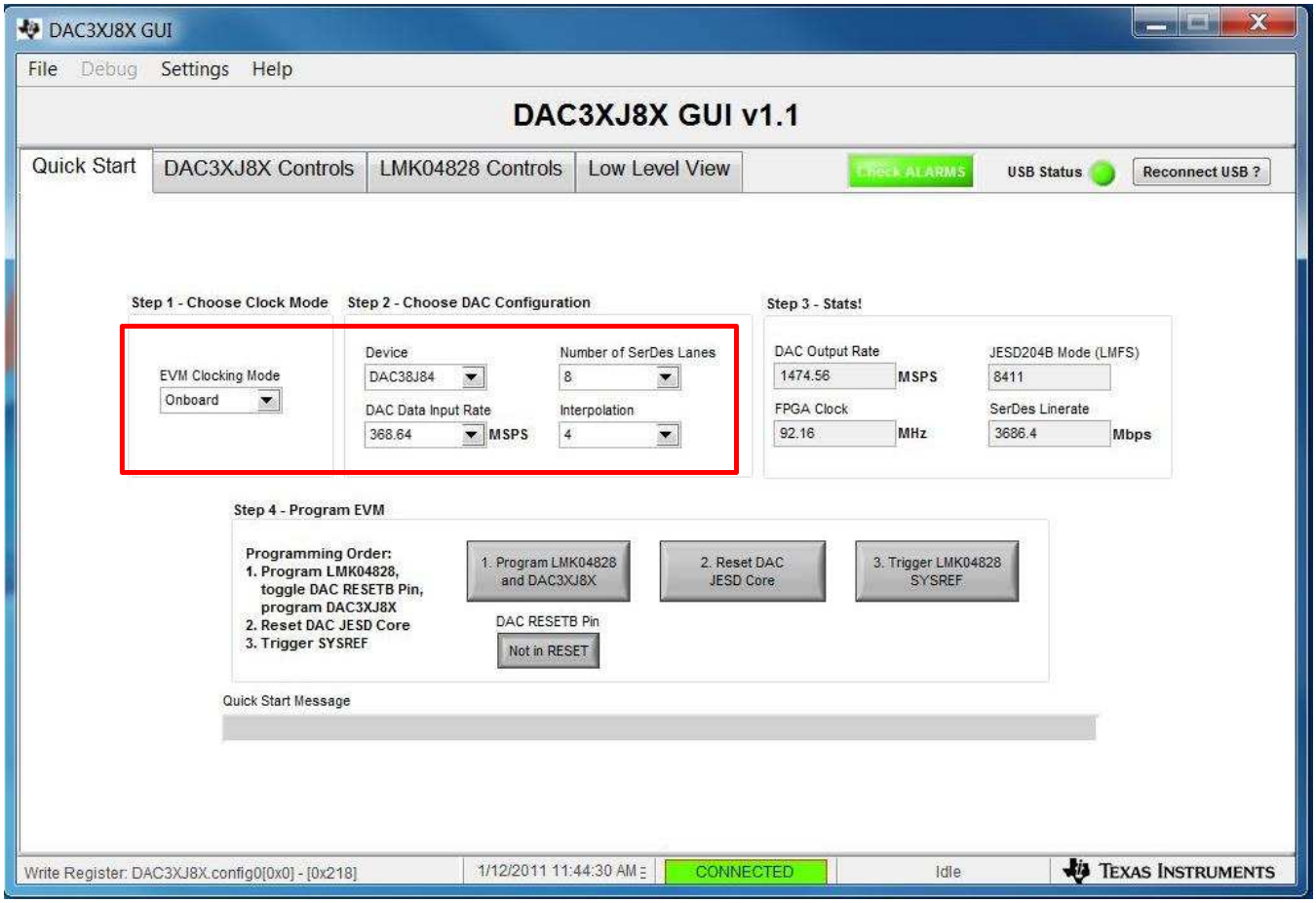

Figure 10. DAC38J84EVM GUI Configuration

By default, the DAC GUI is configured to generate an FPGA reference clock as line rate/40. Since the linerate is shown to be 3.6G the valid Multiplier line rate is only supported by x10 and x20 (refer to Table 1). In order to support this mode, the settings of the LMK04828 registers needs to be changed. From the GUI, navigate to the *LMK04828 Controls* tab. Under *Clock Outputs*, update the DCLK Divider to "16" in the DAC GUI as shown in Figure 11.

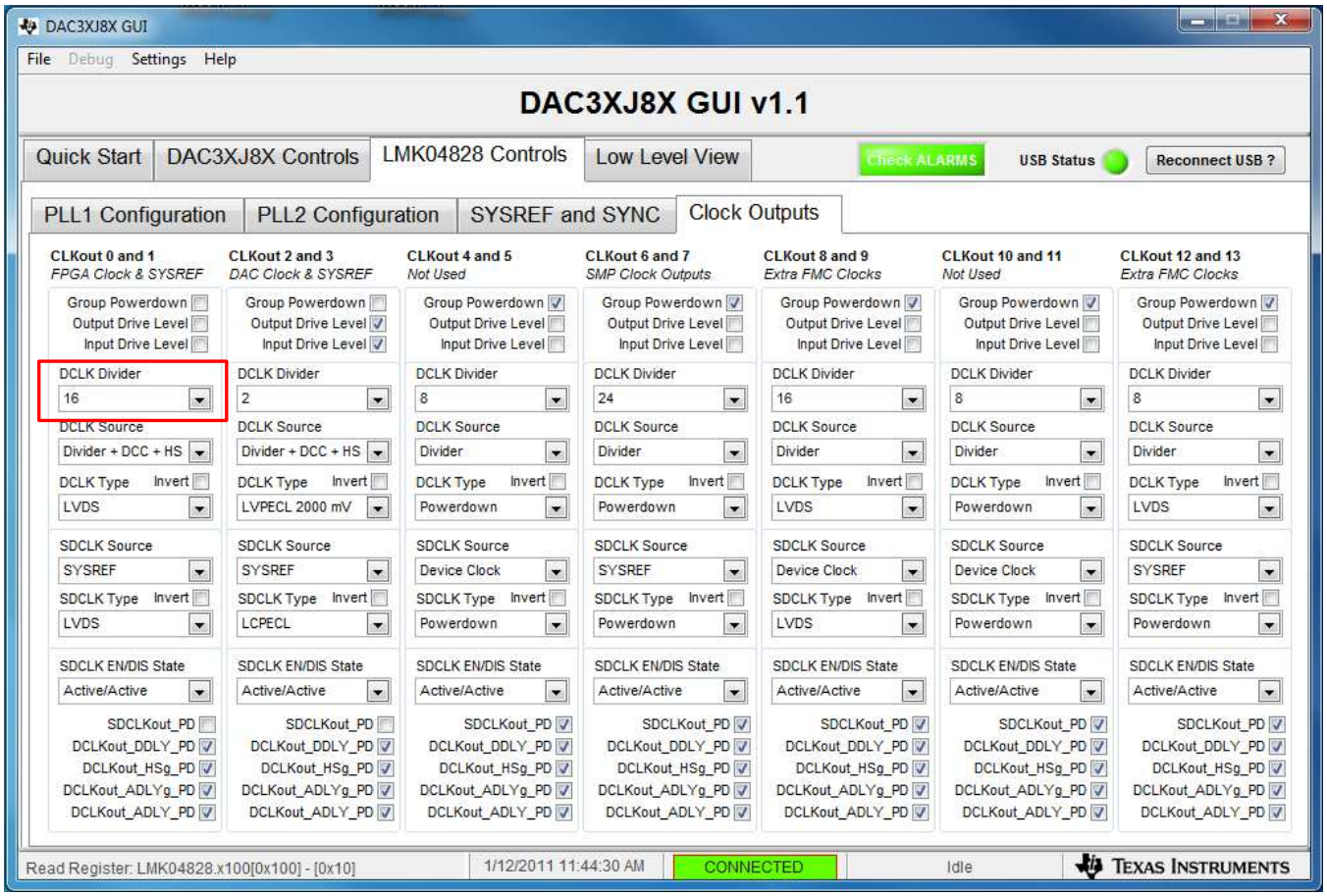

Figure 11. DAC38J84EVM GUI DCLK Divider

Follow the procedure in Section 7.1 beginning with step number 4 to configure HSDC Pro and produce a tone. Note that the data rate has changed to 1474.56 MSPS.

7.2 ADC12J4000EVM With KCU105 Board Setup Example

The following section provides an example testing the ADC12J4000EVM in bypass mode using a KCU105 development platform.

NOTE: There is a jumper "KC705 JTAG" on the ADC12J4000EVM that will prevent the firmware from downloading if it is not shunted. By default, the board will have this jumper OPEN. The jumper is **required** to be shunted in order for this integration to work. The jumper is located on the top of the board near the FMC connector.

Make sure the instructions in Section 6 are completed before testing the EVM. Figure 12 shows a setup between the ADC12J4000EVM and KCU105.

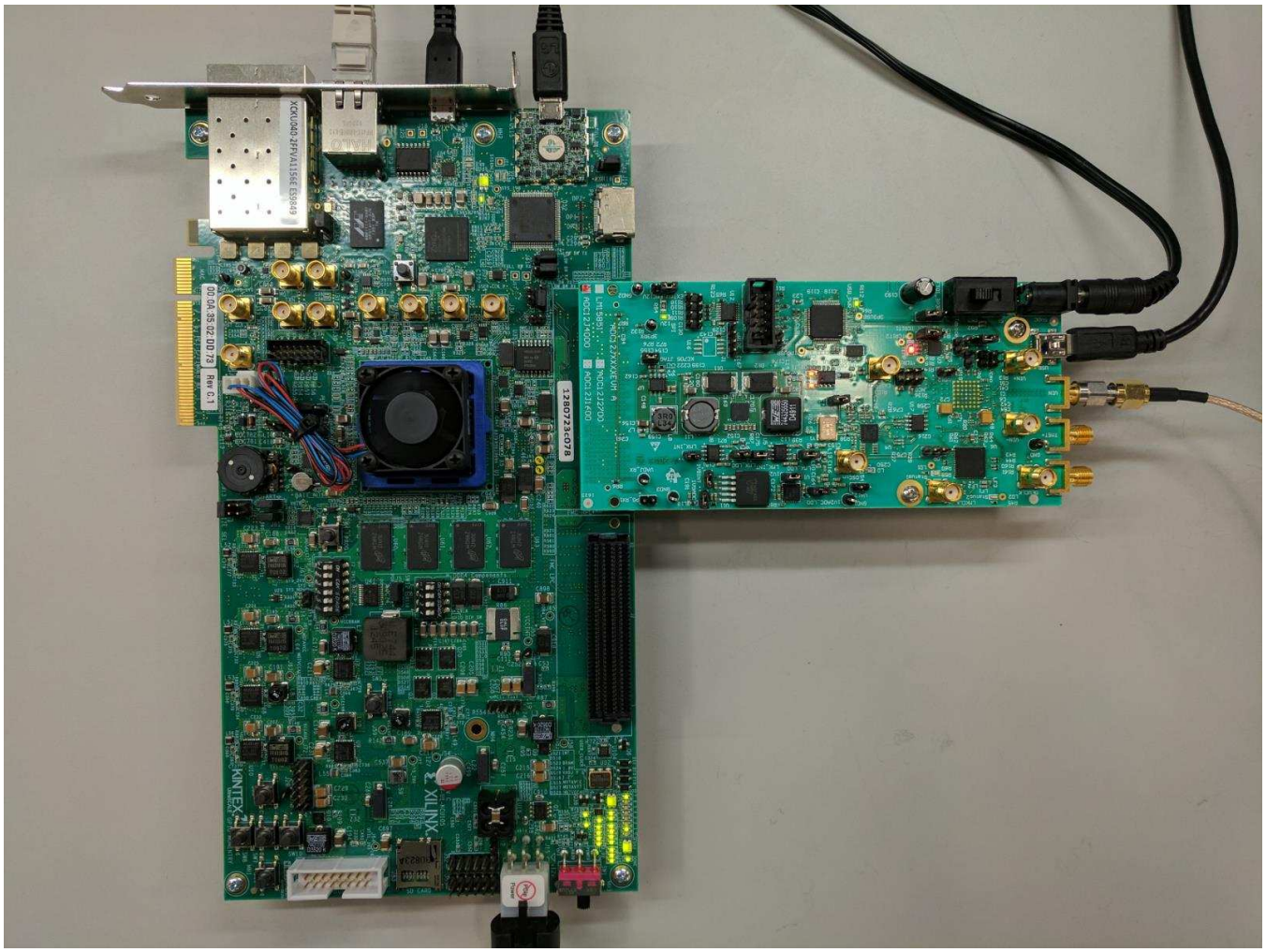

Figure 12. ADC12J4000EVM Setup With KCU105

Set up the hardware as follows:

1. Connect the power supply cables and power up the ADC12J400.
2. Open the ADC12J4000 GUI. The GUI is found under "Software" on www.ti.com featuring the ADC12J4000EVM.
3. Choose "On-board" as the *Clock Source*, set *On-board Fs Selection* to "Fs = 4000 Msps", and set *Decimation and Serial Data Mode* to "Bypass Mode; DDR".
4. Click **Program Clocks and ADC**. Figure 13 shows a screenshot of the configured GUI.

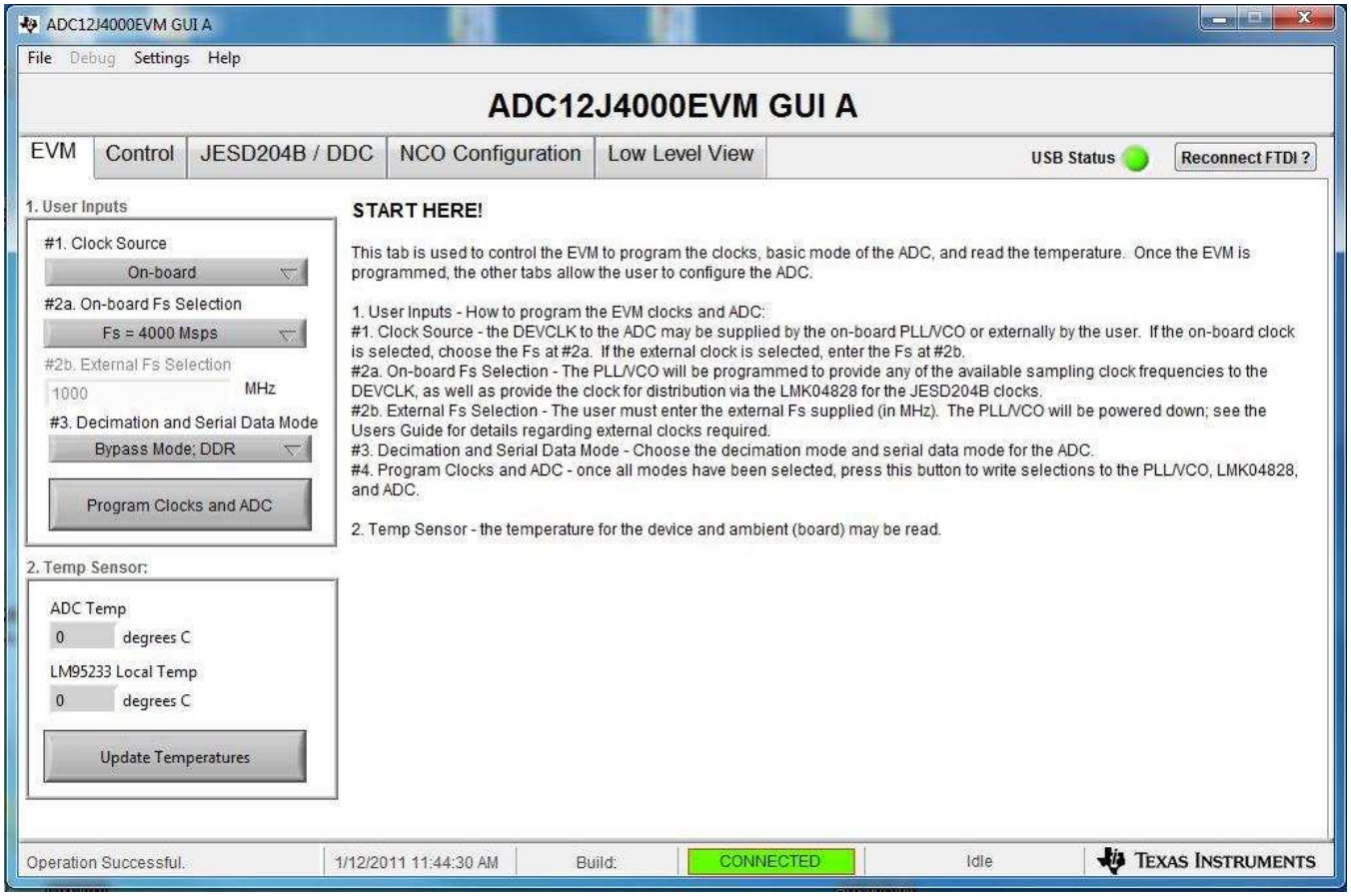

Figure 13. Configured ADC12J4000EVM GUI

5. Open HSDC Pro, select the *ADC* tab, and select "ADC12J4000_BYPASS" using the device drop-down menu.
6. Enter "4G" in the *ADC Output Data Rate* window. Verify the number of samples do not exceed 32,768.
7. Click the **Capture** button, and the new line rate (8G) and JESD reference clock (200M) should show.

Figure 14 shows a captured result sending a 170-MHz single tone through Vin at –1 dBFS.

Figure 14. HSDC Pro ADC12J4000EVM Captured Result

7.3 ADC32RF45EVM With KCU105 Board Setup Example

The following section provides an example testing the ADC32RF45EVM in 8224 mode using an external clock in Bypass mode. Make sure the instructions in Section 6 are completed before testing the EVM. Figure 15 shows a setup between the ADC32RF45EVM and KCU105.

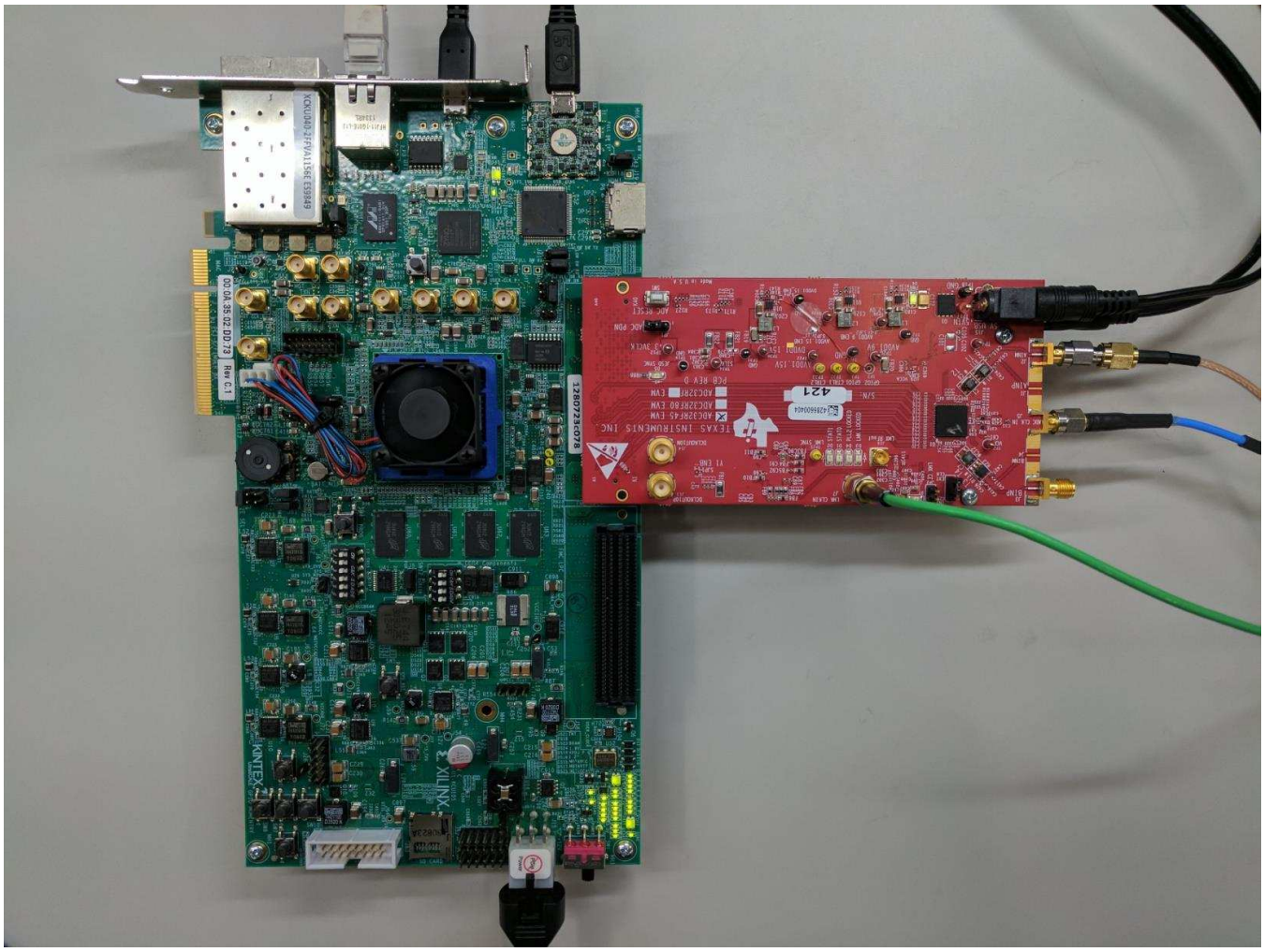

Figure 15. ADC32RF45EVM Setup With KCU105

Set up the hardware as follows:

1. Connect an external 2 GHz at 12-dBm source to ADC_CLK_IN (J5) of the ADC32RF45EVM.
2. Connect an external 2 GHz at 12-dBm source to LMK_CLKIN (J7) of the ADC32RF45EVM. This source must be synchronized with the ADC_CLK_IN source.
3. Connect the power supply cable to the EVM and open the ADC32RFxx EVM GUI. The GUI is found under "Software" on www.ti.com featuring the ADC32RF45EVM.
4. Go to the *Quick Setup* tab and configure the GUI as shown in Figure 16:
   (a) *Clock Source to ADC* – "External Clocking"
   (b) *ADC32RF45 Mode* – "Bypass"
   (c) *BYPASS* – "14 bit"

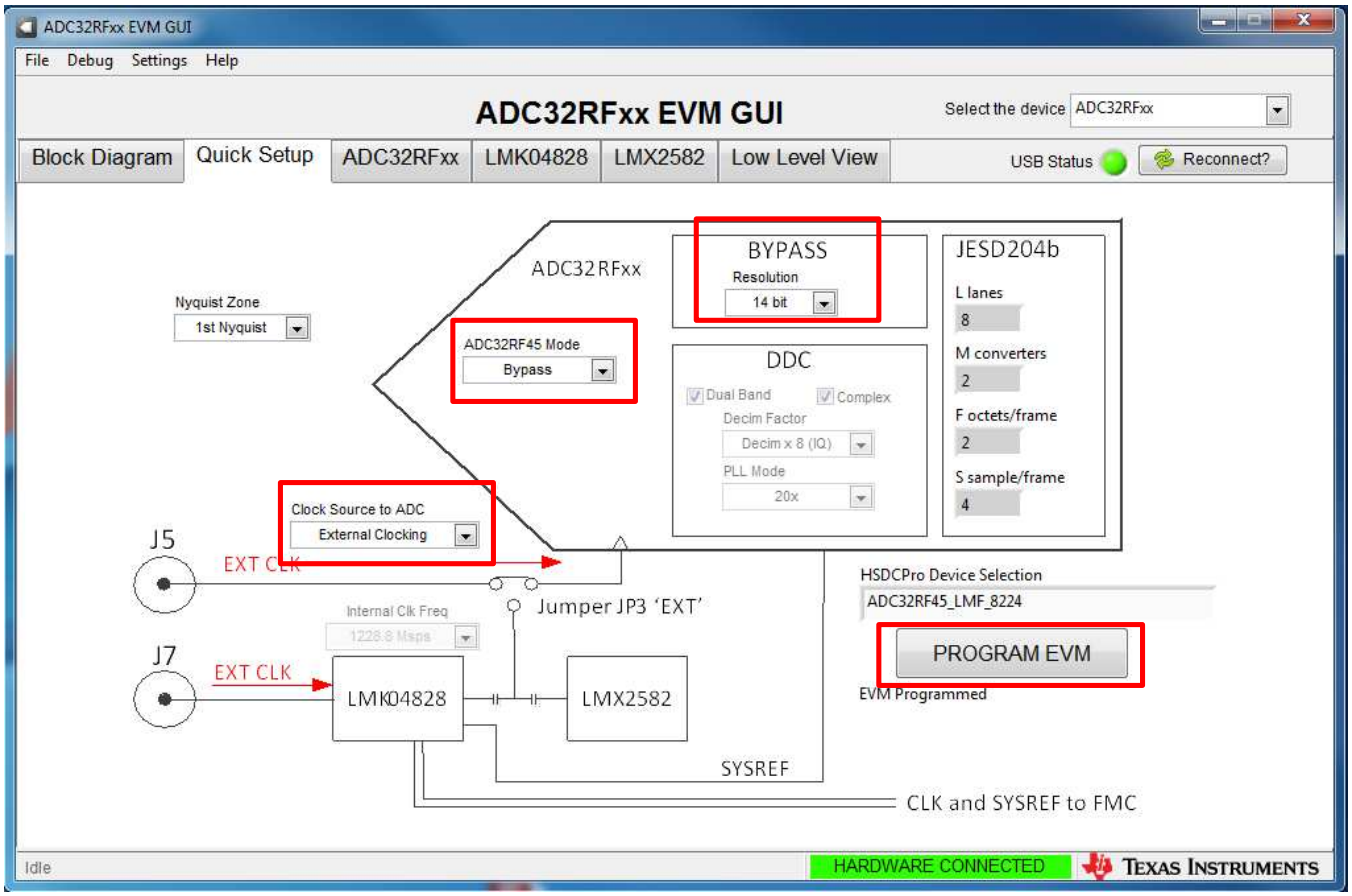

Figure 16. ADC32RF45EVM GUI Quick Setup

5. Click on **PROGRAM EVM**.
6. Go to the *Clock Outputs* tab under the *LMK04828* tab.
7. Verify *CLKout 0 and 1* divider is set to "8" as shown in Figure 17.

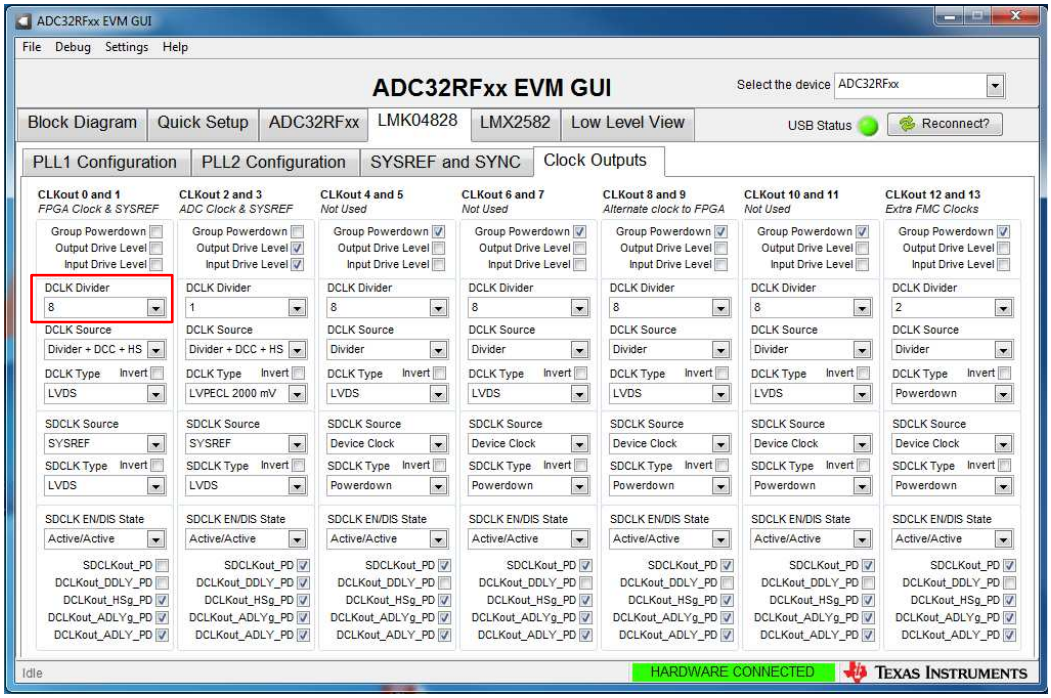

Figure 17. ADC32RFEVM GUI Clock Outputs

8. Click on the *SYSREF and SYNC* tab. Verify the *SYSREF Divider* is set to "1024".
9. In the *ADC Configuration* tab under *ADC32RFxx*, set the *JESD204b Lane De-emphasis* setting to "0" dB for all lanes, as shown in Figure 18.

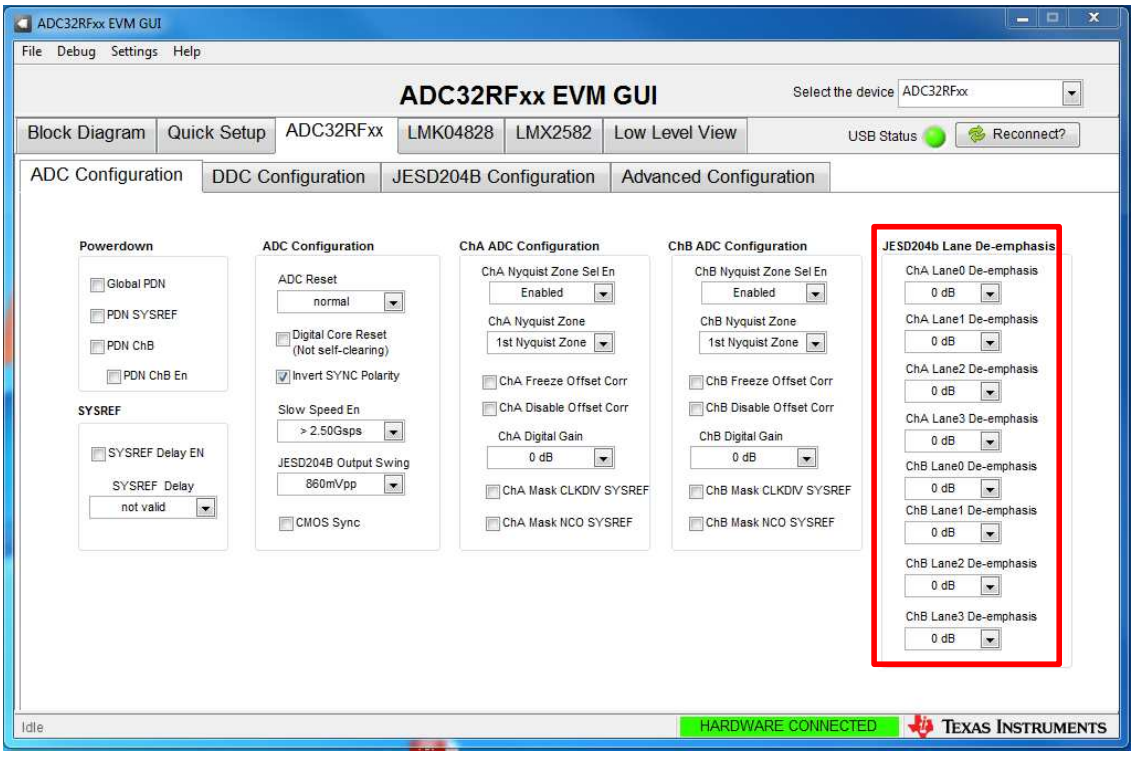

Figure 18. ADC32RF45 GUI Lane De-Emphasis

10. Open HSDC Pro, select the *ADC* tab, and select "ADC32RF34_8224" using the drop-down menu.
11. Enter "2G" for *ADC Output Data Rate*, the new lane rate (10G) and reference clock settings (200M) will be shown. Verify the number of samples do not exceed 32,768.
12. Click the **Capture** button. Figure 19 shows a captured result sending a 170-MHz single tone through Vin at –2 dBFS to AINP (J2).

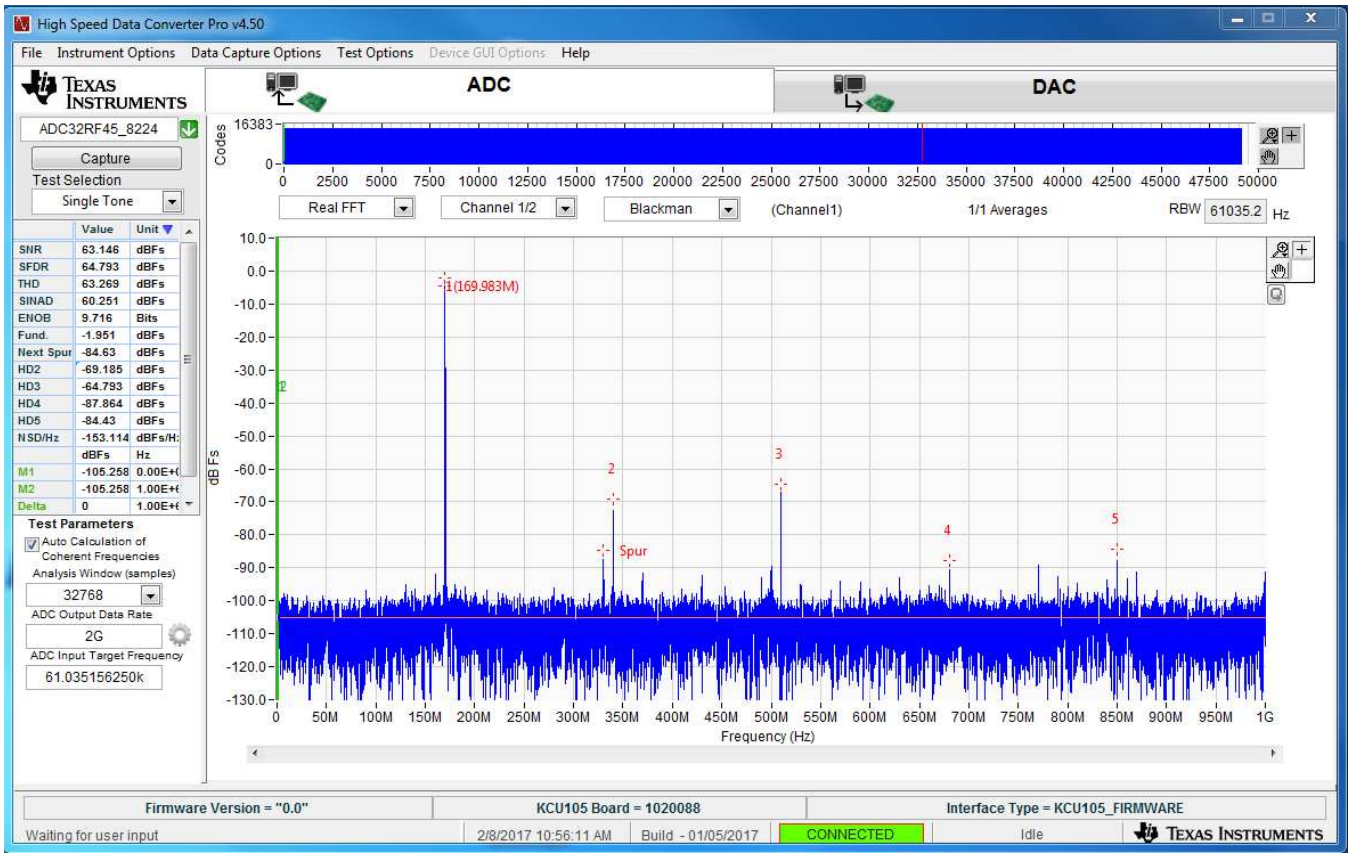

Figure 19. ADC32RF45EVM Capture on HSDC Pro

7.4 ADS54J20EVM With KCU105 Board Setup Example

The following section provides an example testing the ADS54J20EVM in 8224 mode with the KCU105 development platform. EVMs in the same family, such as the ADS54J40EVM and ADS54J60EVM, can be configured with the same instructions and proper configuration files. Make sure the instructions in Section 6 are completed before testing the EVM. Figure 20 shows a setup between the ADS54J20EVM and the KCU105.

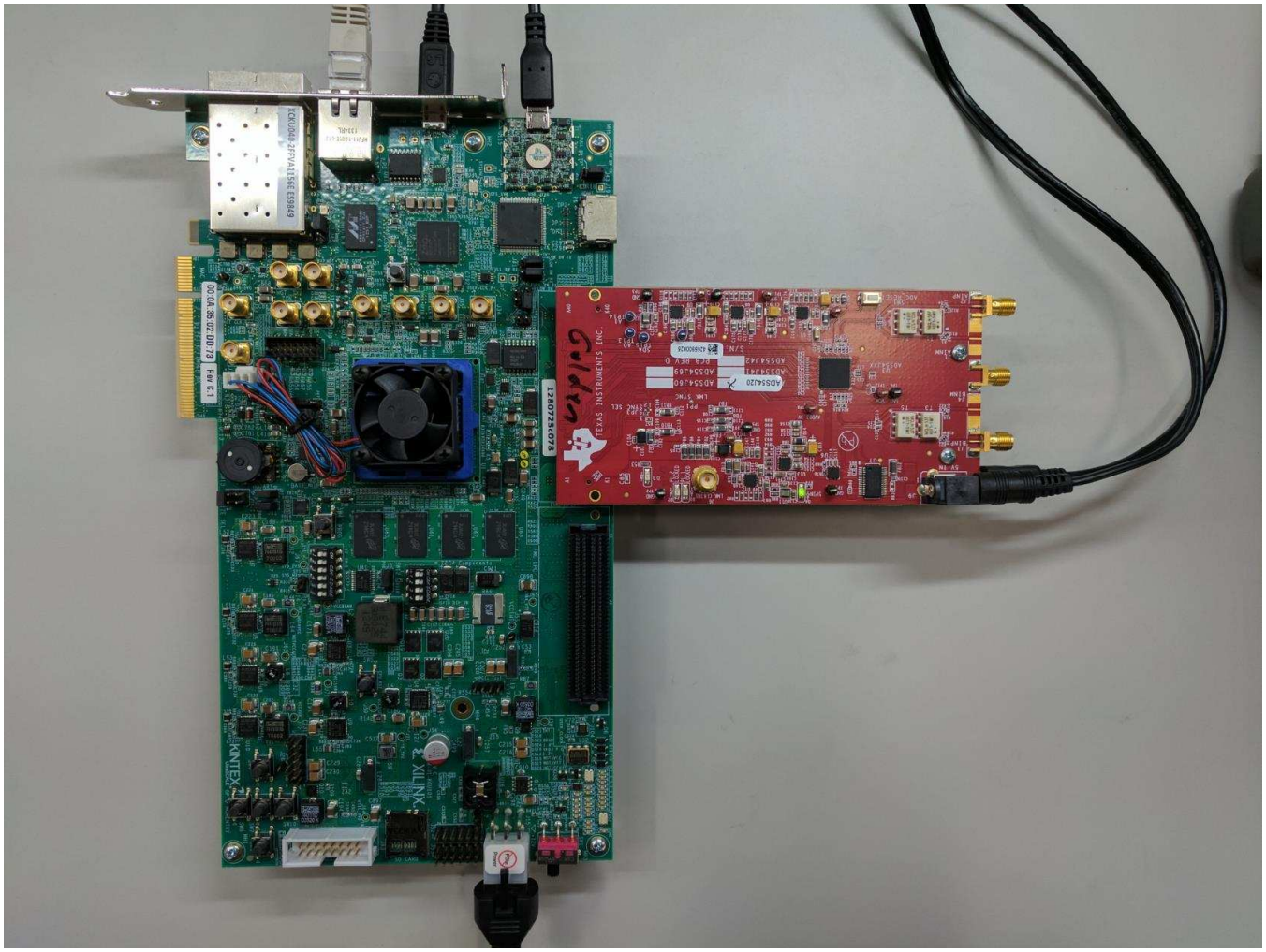

Figure 20. ADS54J20EVM Setup With KCU105

Set up the hardware as follows:

1. Power up the ADS54J40 and open the ADS54JxxEVM GUI. The GUI is found under "Software" on www.ti.com featuring the ADS54J20EVM.
2. Navigate to the *LMK04828* tab, and click the **RESET** button
3. On the *Low Level View* tab, load the following configuration files: "LMK_983p04_8224_VC707.cfg" as shown in Figure 21.

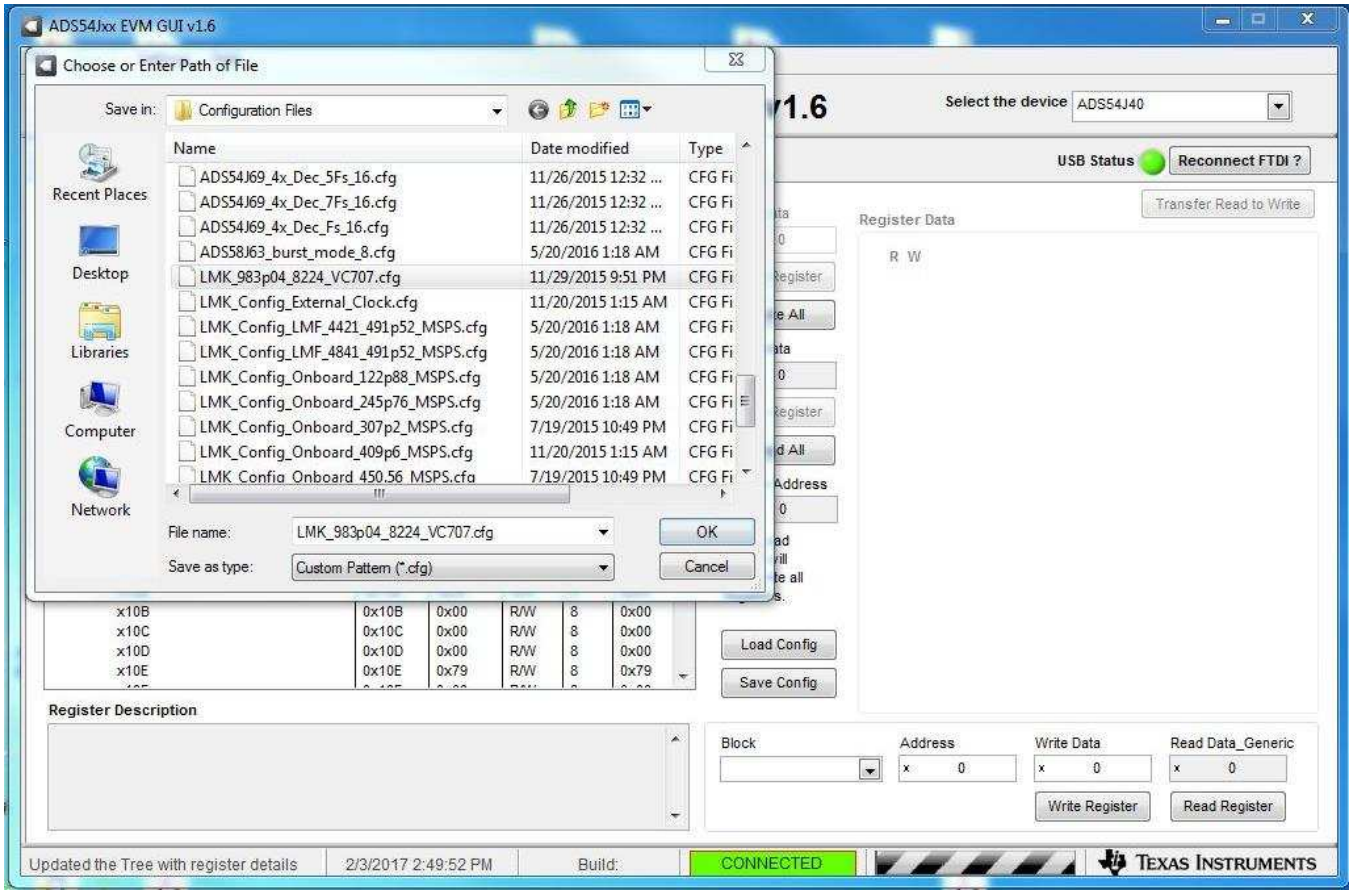

Figure 21. Configuration Files for ADS54J20EVM GUI

4. Press the **ADC RESET** button (SW1) on the EVM to provide a hardware reset to the ADC
5. On the L*ow Level View Tab*, load the ADC configuration file: "ADS54J20_LMF_8224.cfg".

6. Open HSDC Pro, select "ADS54J20_LMF_8224" in the drop-down arrow.
7. Verify the number of samples do not exceed 32,768. Enter "983.04M" in the *ADC Output Data Rate* window.
8. The GUI will display the new lane rate (4.9152G) and JESD reference clock required by the capture platform FPGA (245.76M).
9. Click on **OK**. Click the **Capture** button. Figure 22 shows a captured result sending a 170-MHz single tone through Vin at –1 dBFS.

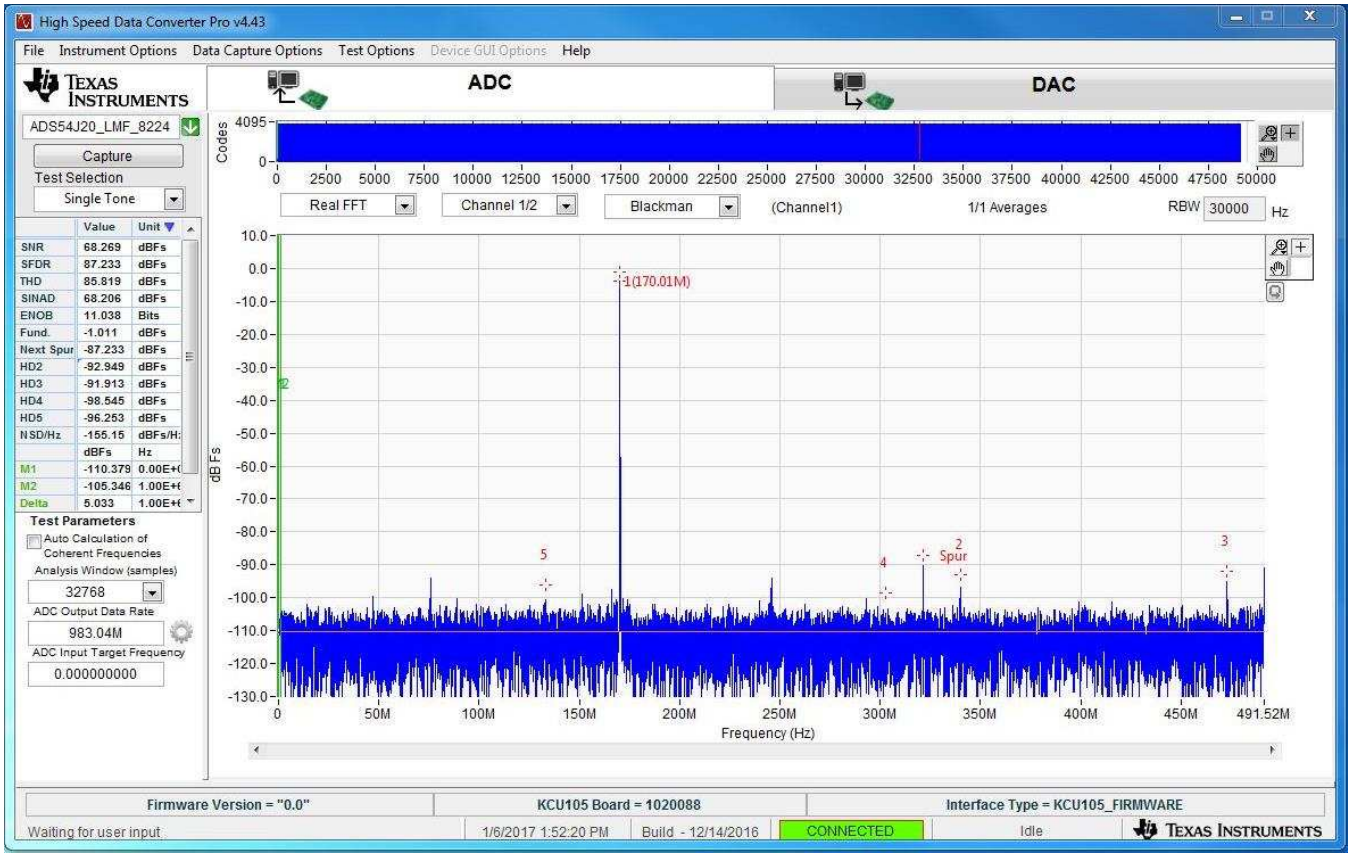

Figure 22. HSDC Pro ADS43J20EVM Captured Result

7.5 ADS42JB49EVM With KCU105 Board Setup Example

The following section provides an example testing the ADS42JB49EVM in 421 mode with the KCU105 development platform. EVMs in the same family, such as the ADS42JB69EVM, can be configured with the same instructions and proper configuration files. Make sure the instructions in Section 6 are completed before testing the EVM. Figure 23 shows a setup between the ADS42JB49EVM and the KCU105.

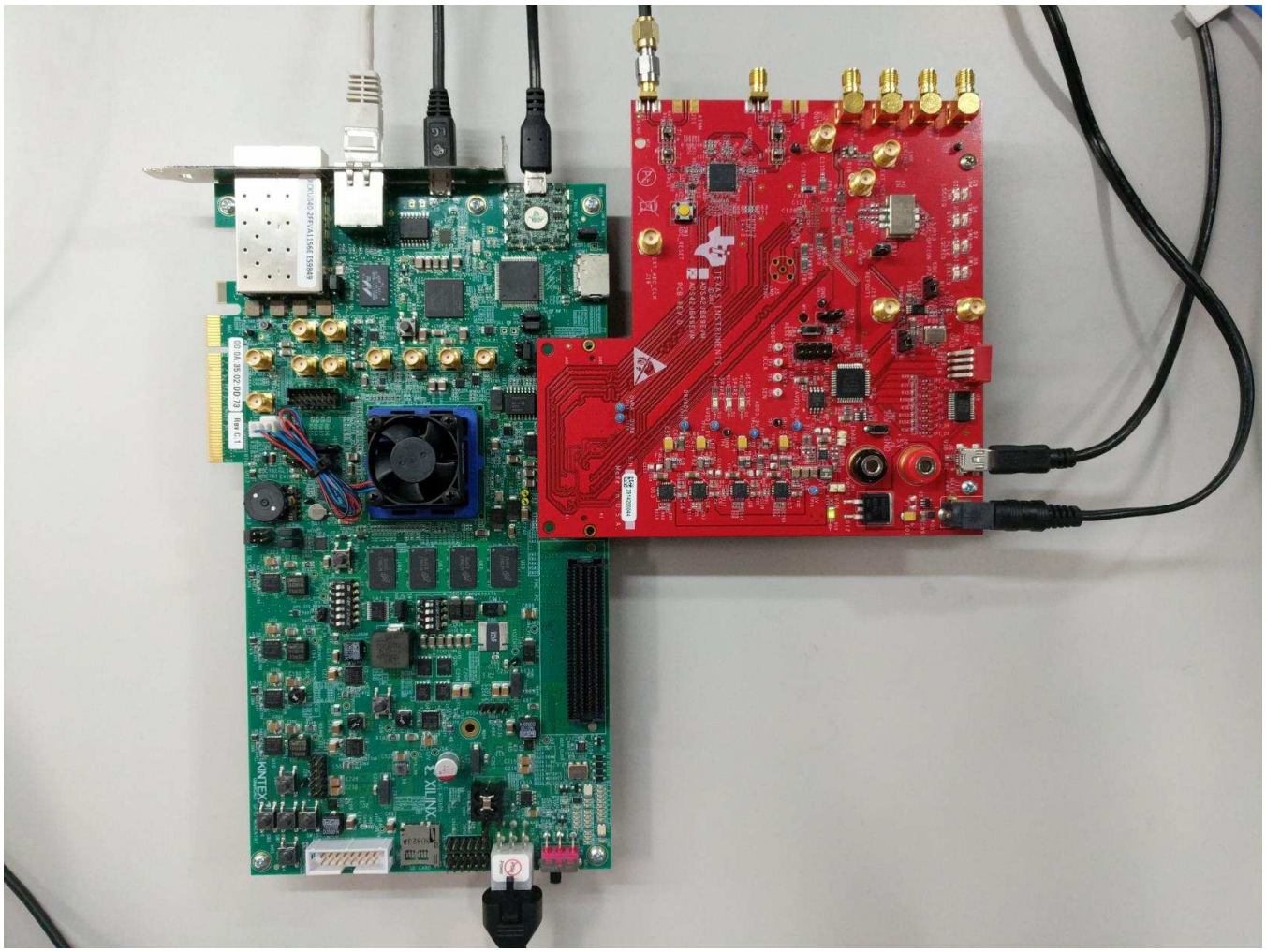

Figure 23. ADS42JB49EVM Setup With KCU105

Set up the hardware as follows:

1. Connect the power cable to the ADS42JB49EVM and open the ADS42JBXX GUI. The GUI is found under "Software" on www.ti.com featuring the ADS42JB69EVM.
2. Go to the *ADS42JBXX* tab and click on **Device Reset** in the top left corner.
3. Go to the *LMK0428* tab and click on **RESET** in the top left corner.
4. Go to the *Low Level View* tab and click on **Load Config**. Load the configuration file: "ADS42JB69_EVM_LMF421_250M.cfg".

5. Open HSDC Pro, select the *ADC* tab, and then select "ADS42JB49_LMF_421" using the device drop-down menu.
6. Verify the number of samples do not exceed 32,768.
7. Enter "250M" in the *ADC Output Data Rate* window. The GUI will display the new lane rate (2.5G) and JESD reference clock required by the capture platform FPGA (250M).
8. Click on **OK**. Connect an analog input signal to the SMA connect (J1)
9. Click the **Capture** button. Figure 24 shows a captured result sending a 80-MHz single tone through Vin at –1 dBFS.

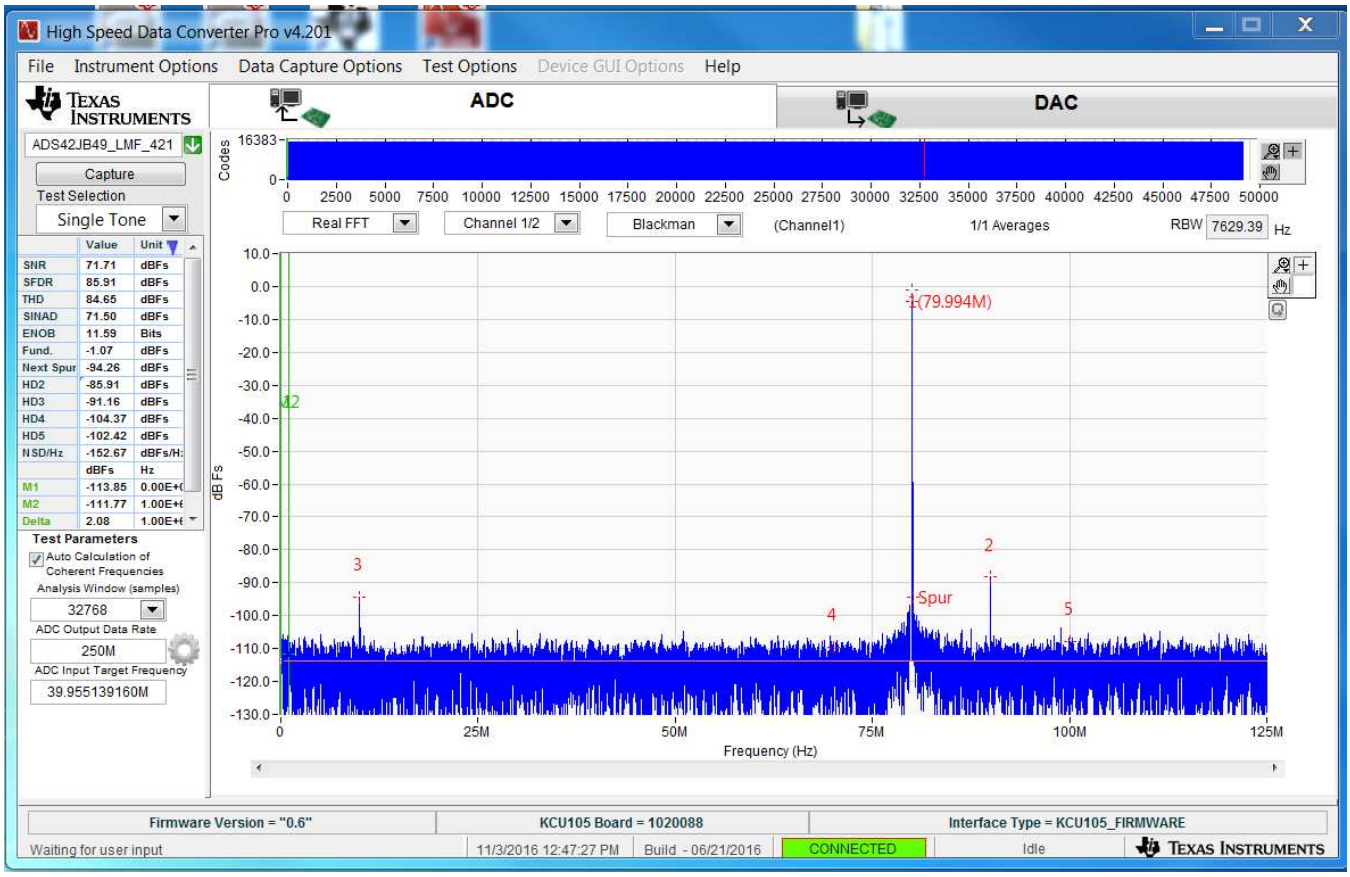

Figure 24. HSDC Pro ADS42JB49EVM Captured Result

7.6 DAC38RF82EVM With KCU105 Board Setup Example

The following section provides an example of testing the DAC38RF82EVM using a KCU105 development platform. With the updated firmware, users can use the DAC38RFXX GUI as if it was connected to a TI TSW14J56. Make sure the instructions in Section 6 are completed before testing the EVM. Figure 25 shows a setup between the DAC38J84EVM and KCU105.

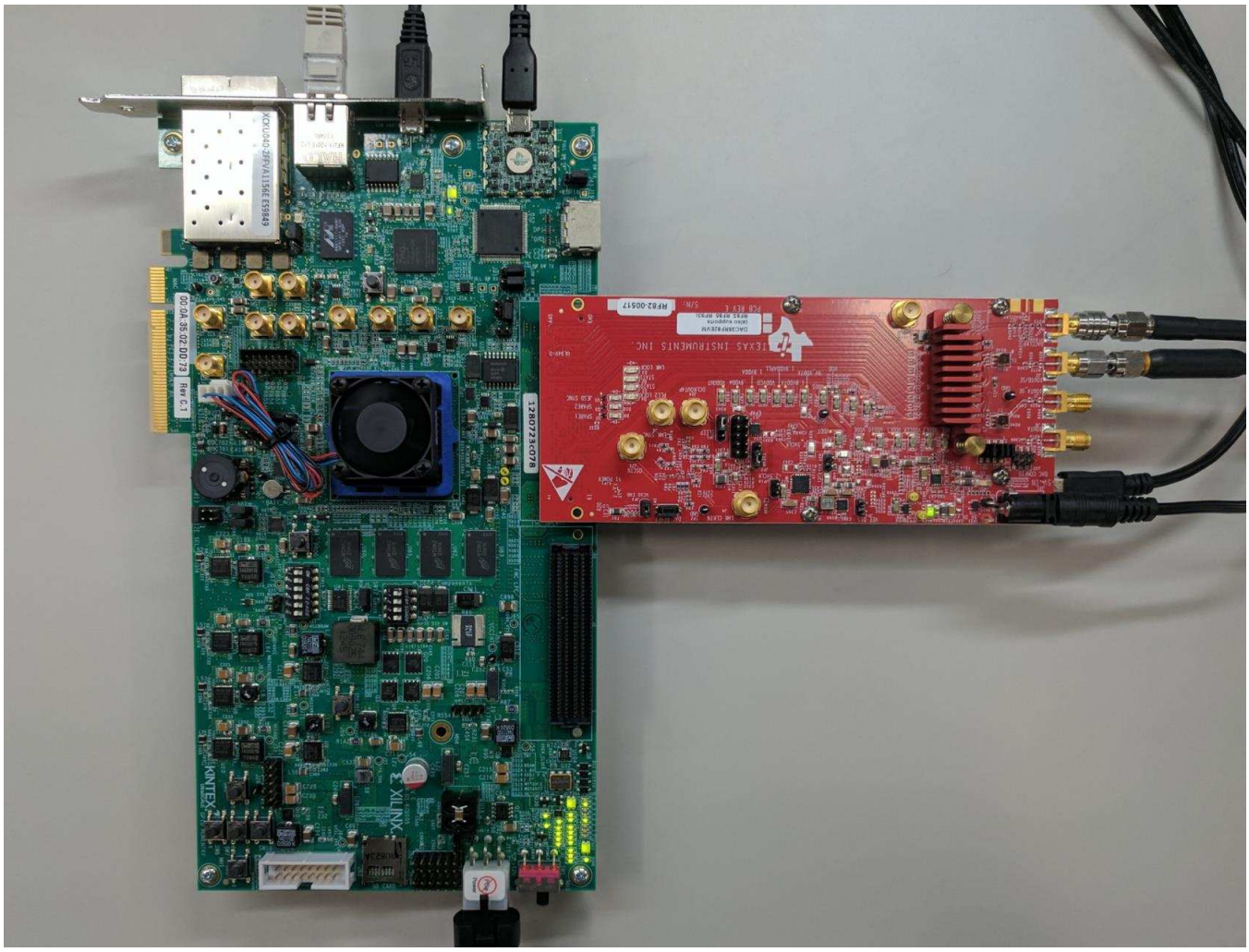

Figure 25. DAC38RF82EVM Setup With KCU105

7.6.1 External Clock Mode DAC38RF82EVM

This section shows how to set up an DAC38RF82EVM using an external clock. This example will configure the JESD204B DAC in an 841 mode.

Set up the hardware as follows:

1. Connect a 6 GHz, 14-dBm output from a signal generator to DACCLK (J1) of the DAC38RF82EVM.
2. Verify that jumper labeled JP10 is SHUNT 1-2 to enable external clock mode.
3. Connect a power cable to the DAC38RF82EVM and open the DAC38RFXX GUI. The GUI is found under "Software" on www.ti.com featuring the DAC38RF82EVM.
4. On the *Quick Start* tab, toggle *DAC RESETB Pin* and press the **Load Default** button.
5. Configure the GUI as shown in Figure 26:
   (a) *DAC Clock Frequency (MHz)* – "6000"
   (b) *# of DACs* – "Dual DAC"
   (c) *# of IQ pairs per DAC* – "1 IQ pair"
   (d) *# of serdes lanes per DAC* – "4 Lanes"
   (e) *Desired Interpolation* – "16x"

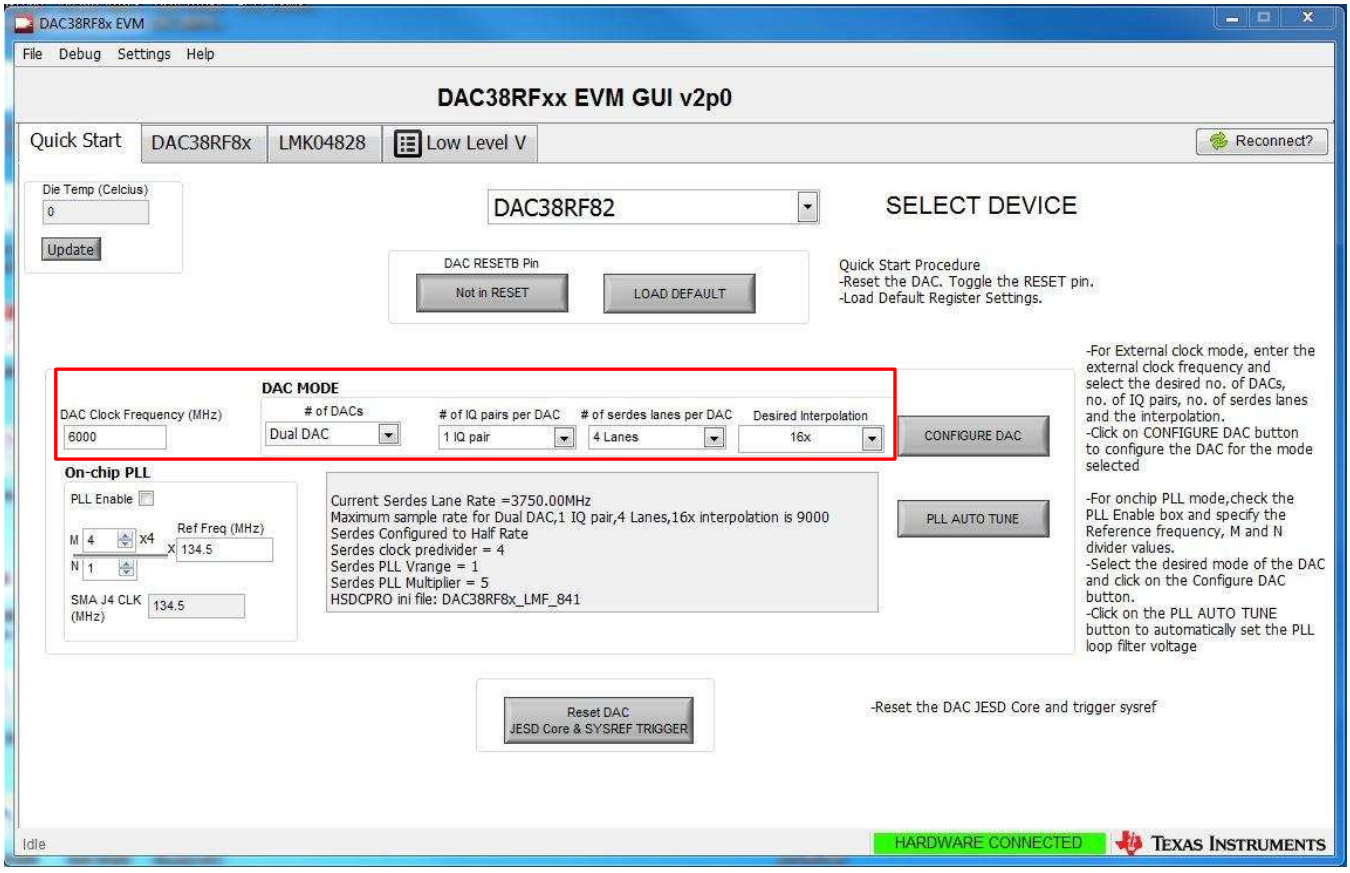

Figure 26. DAC38RFXX EVM GUI in External Clock Mode

6. Press the **CONFIGURE DAC** button, then the **PLL AUTO TUNE** button, then the **Reset DAC JESD Core & SYSREF TRIGGER** button.
7. Navigate to the *LMK04828* tab. Change the *DCLK Divider* on *CLKout 0 and 1* to "8" as shown in Figure 27. This will provide the right reference clock to send to the KCU105.

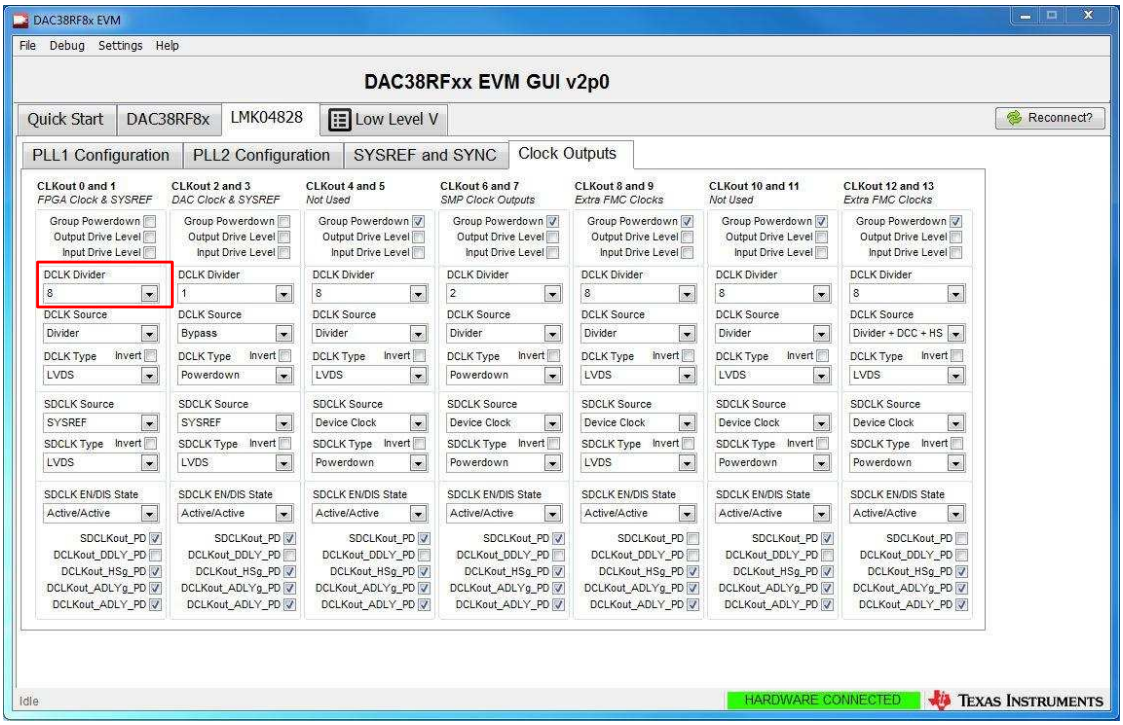

Figure 27. DAC38RF82EVM GUI DCLK Divider

8. Open HSDC Pro, press the *DAC* tab, and select "DAX38RF8X_LMF_841" from the drop-down menu.
9. Enter "375M" as the *Data Rate (SPS)*and change the *DAC Option* to "2's Complement". Make sure the number of samples is set to at least 8192, but do not exceed 32,768. Figure 28 shows a configured GUI for a 150-MHz tone.

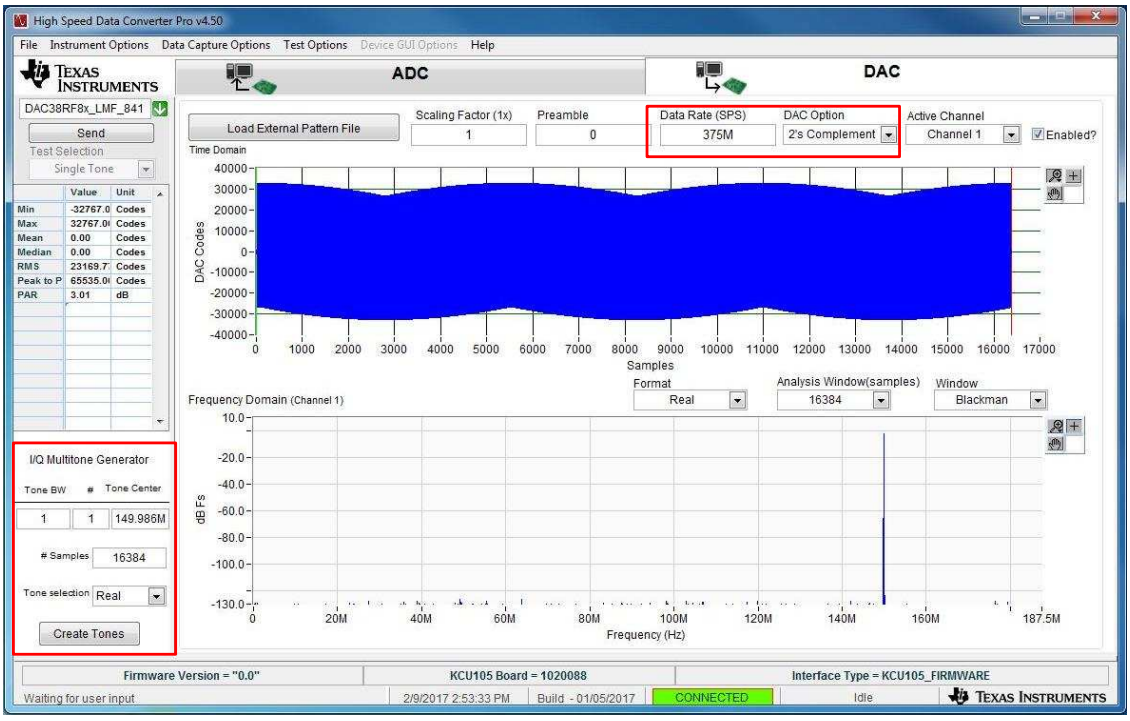

Figure 28. Generating a 150-MHz Tone on HSDC Pro

10. Click the **Create Tones** button and press the **Send** button.
11. The new lane rate (3.750 GHz) and FPGA Clock (375 MHz) settings should be shown.
12. Go back to the DAC38RFXX GUI and press the **Reset DAC JESD Core & SYSREF TRIGGER** button.
13. Connect channel one of the DAC38RF82EVM (J6) to a spectrum analyzer and verify the signal. Figure 29 shows the analog output generated by the DAC38RF82EVM

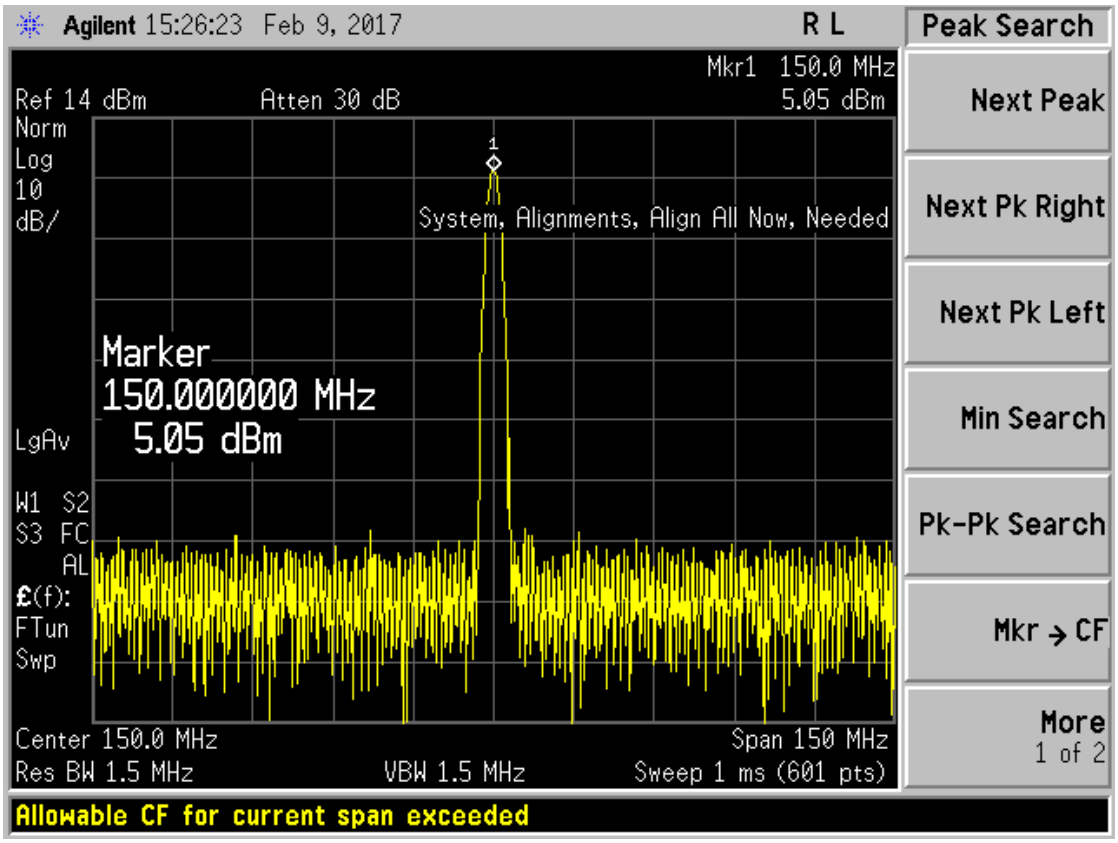

Figure 29. Analog Output From DAC38RF82EVM

7.6.2 Phased-Locked Loop (PLL) Mode DAC38RF82EVM

This section shows how to setup an DAC38RF82EVM using the internal PLL to generate the clocking. This example will configure the JESD204B DAC in an 841 mode.

Set up the hardware as follows:

1. Connect a 245.76 MHz, 12-dBm output from a signal generator to EVM LMK CLKIN (J4) of the DAC38RF82EVM.
2. Verify that the jumper labeled JP10 is OPEN.
3. Connect a power cable to the DAC38RF82EVM and open the DAC38RFXX GUI. The GUI is found under "Software" on www.ti.com featuring the DAC38RF82EVM.
4. On the *Quick Start* tab, toggle the *DAC RESETB Pin* and press the **Load Default** button
5. Configure the GUI as shown in Figure 30:
   (a) *PLL Enable* – "Check"
   (b) *M* – "9", *N* – "1"
   (c) *Ref Freq (MHz)* – "245.76"
   (d) *# of DACs* – "Dual DAC"
   (e) *# of IQ pairs per DAC* – "1 IQ pair"
   (f) *# of serdes lanes per DAC* – "4 Lanes"
   (g) *Desired Interpolation* – "18x"

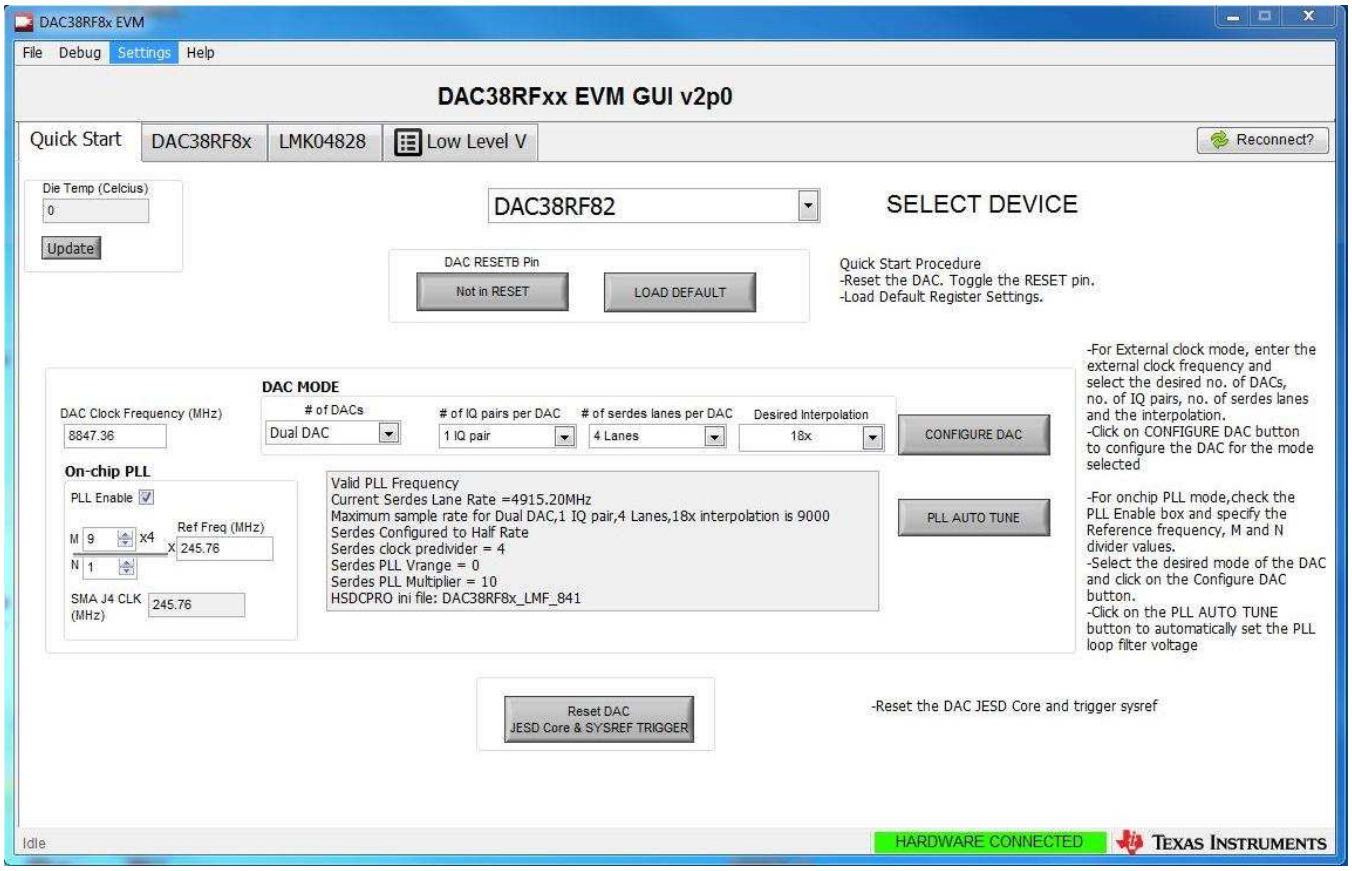

Figure 30. DAC38RFXX EVM GUI in PLL Mode

6. Press the **CONFIGURE DAC** button, followed by the **PLL AUTO TUNE** button, then the **Reset DAC JESD Core & SYSREF TRIGGER** button.

7. Navigate to the *DAC38RF8x* tab. Under *Digital(DAC A)*, enable the *Mixer* and *NCO* as shown in Figure 31. Set the *Mixer Gain* to "6dB", and the *NCO Frequency (MHz)* to "1960".
8. Click the **UPDATE NCO** button. Go back to the *Quick Start* tab and press **Reset DAC JESD Core & SYSREF TRIGGER** button. This can also be done on the *Digital(DAC B)* tab, which will provide an *NCO Frequency* on channel B.

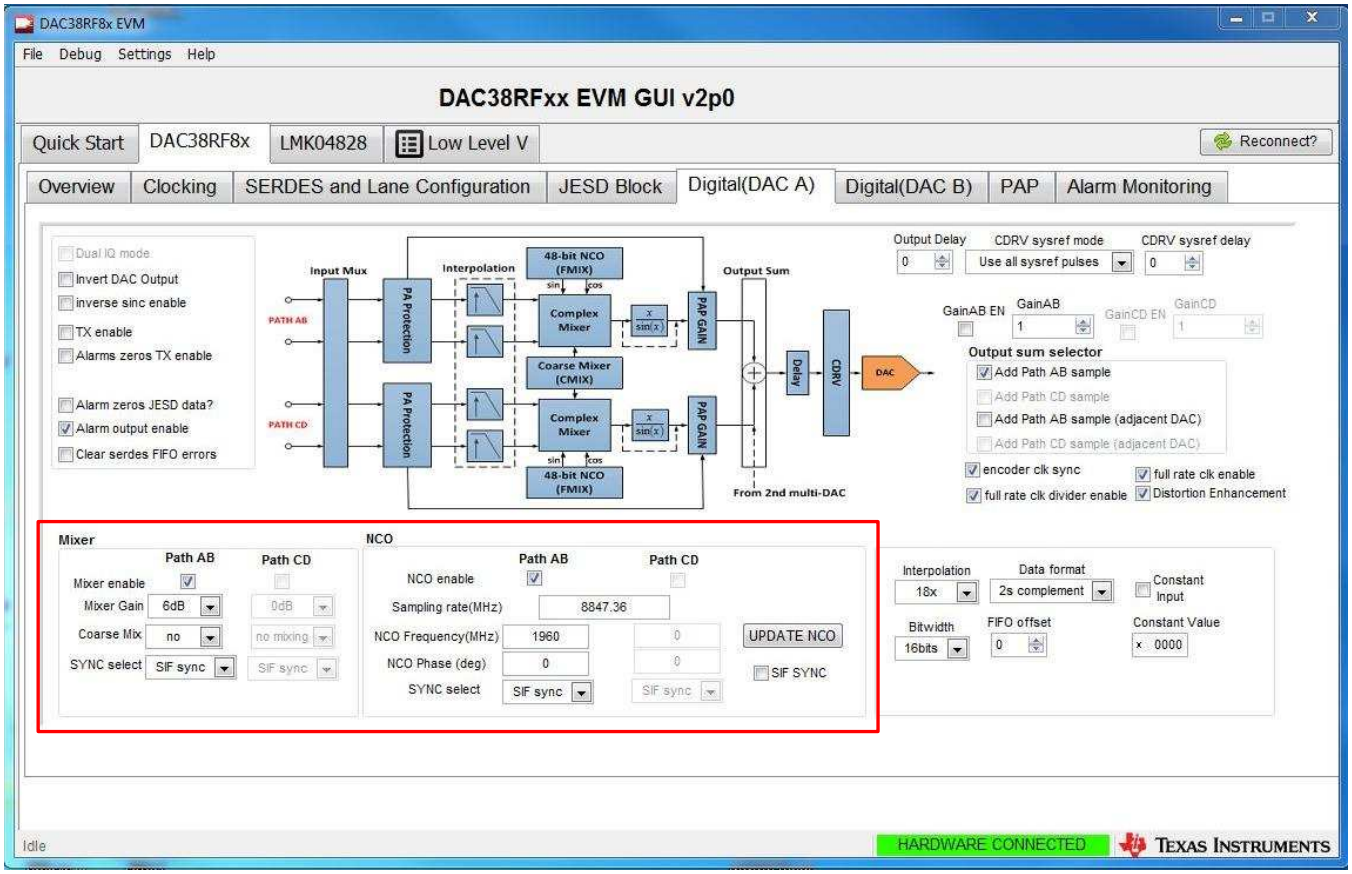

Figure 31. DAC38RF82EVM GUI NCO Frequency Settings

9. In HSDC Pro, press on the *DAC* tab, and select "DAX38RF8X_LMF_841" from the drop-down menu.
10. Enter "491.52" as the *Data Rate (SPS)* and change *DAC Option* to "2's Complement". Make sure the number of samples is set to at least 8192, but no more than 32,768.
11. Set the following in the *I/Q Multitone Generator*:
    (a) *Tone BW* – "1"
    (b) # of Tones – "1"
    (c) *Tone Center* – "0" (This will change to the closest value possible to DC.)
    (d) *Tone selection* – "Complex"
    Figure 32 is a screenshot of a proper configuration on HSDC Pro.

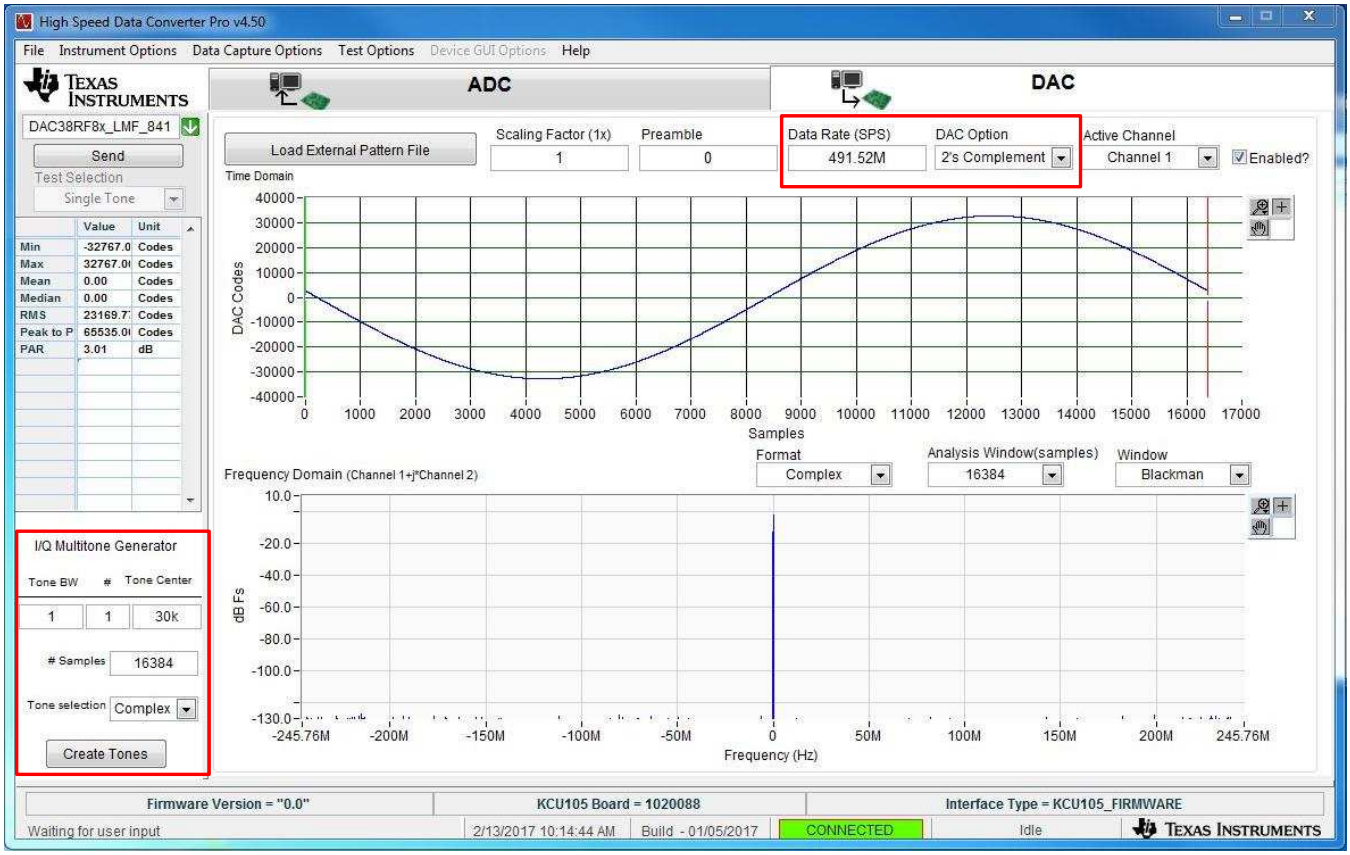

Figure 32. HSDC Pro Configuration for PLL Mode

12. Click the **Create Tones** button and press **Send**.
13. The new lane rate (4.915 GHz) and FPGA Clock (122.88 MHz) settings should be shown.

14. Go back to the DAC38RFXX GUI and press the **Reset DAC JESD Core & SYSREF TRIGGER** button.
15. Connect channel one of the DAC38RF82EVM (J6) to a spectrum analyzer and verify the signal. Figure 33 shows the analog output generated by the DAC38RF82EVM.

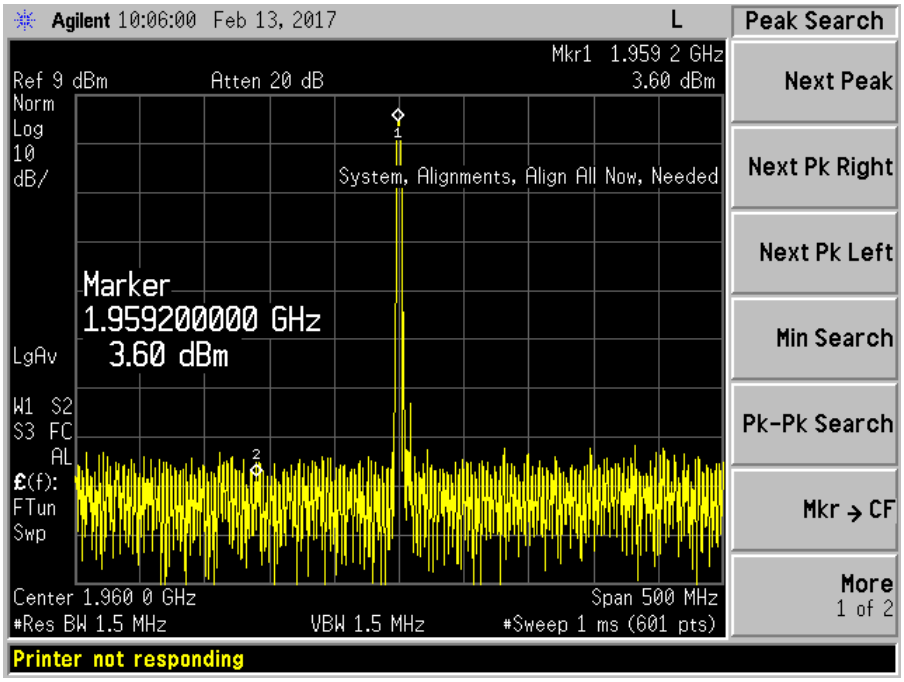

Figure 33. Analog Output From DAC38RF82EVM

8 Eyescan Analysis

One of the features of the KCU105 is the ability to receive data and measure the horizontal and vertical eye opening. This Eyescan feature is used as an diagnosis tool to debug the digital signals in each enabled lane. The latest version of HSDC Pro supports this feature and generates an eye diagram consisting of a bit error rate (BER) heat map.

The following section provides a quick start-up example that highlights the software features of the Eyescan analysis.

1. Verify that the ADC EVM provides a good FFT capture on HSDC Pro.
2. In HSDC Pro, under the *Instrument Options* tab, click on **SERDES Test Options**.
3. A new window should appear with the following features:
   (a) *Lane* - Selects one of the lanes to analyze (the lane number is respective to the KCU105)
   (b) *Horz Step* - Resolution of the horizontal scan (For optimal resolution, choose 4 or lower)
   (c) *Vert Step* - Resolution of the vertical scan (For optimal resolution, choose 4 or lower)
   (d) *Max Prescale* - The amount of time spent at each vertical and horizontal sample (A higher value will result in a finer BER)
   (e) *LPM*, *DFE* - Specifies whether the transceiver is in LPM or DFE mode
   (f) *Standard EyeQ* - Overlays one of the JESD204 receive eye-mask templates onto the Eye diagram
4. After configuring the parameters, click the **START** button. The scan may take a few seconds to a few minutes, depending on the parameters chosen.

Figure 34 shows an eye diagram of a 8224 mode ADC32RF45EVM sampling at 2 GHz with a lane rate of 10 GHz.

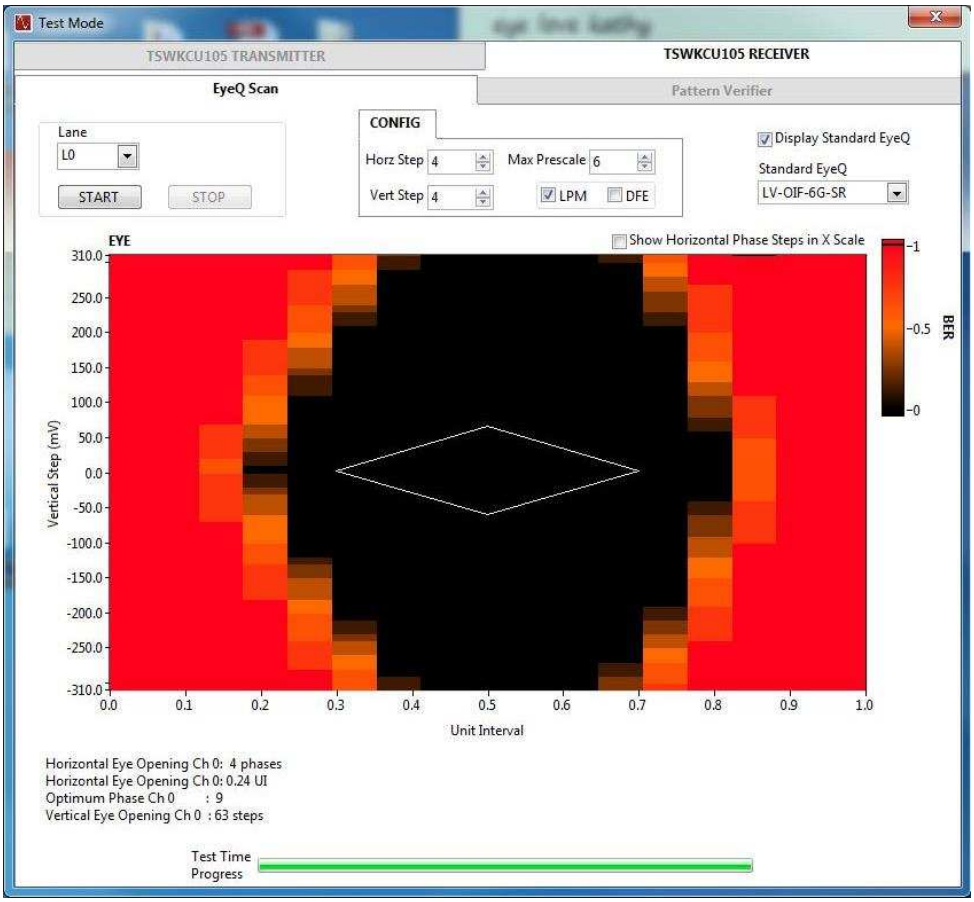

Figure 34. Eye Diagram Example Plot

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      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

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