7.3.1.2.5 JESD204B Pattern Test

The DAC3xJ8x family of devices supports the following test patterns for JESD204B:

• Link layer test pattern

– Verify repeating /D.21.5/ high frequency pattern for random jitter (RJ)

– Verify repeating /K.28.5/ mixed frequency pattern for deterministic jitter (DJ)

– Verify repeating initial lane alignment (ILA) sequence

– RPAT, JSPAT or JTSPAT pattern can be verified using errors counter of 8b/10b errors produced over an amount of time to get an estimate of BER.

The test procedures for link layer test pattern are as follow:

1. Enable the link layer test pattern through register jesd\_test\_seq in config74 register (0x4A). The respective setting for each test is as follow:
	1. 2b’00 : test sequence disabled
	2. 2b’01 : verify repeating D.21.5 high frequency pattern for random jitter
	3. 2b’10 : verify repeating K.28.5 mixed frequency pattern for deterministic jitter
	4. 2b’11 : verify repeating ILA sequence
2. Clear bits 8 to15 of the config4 register (address 0x04) to disable the “lane error” alarm mask. Clear the bits according to the respective active lanes (for example, bit 8 is for lane0, bit 15 is for lane 7). If any error occurs on the respective lanes, the error result will show up at bit 8 of the config100 to config107 register, and the CMOS ALARM pin will trigger to signal the error.
3. Set the JESD204B TX logic device to output the corresponding test pattern.
4. Once the associated pattern is transmitted from the JESD204B TX logic device for the link layer pattern test, the error will be reflected on bit 8 of config100 to config107 for the respective JESD204B RX lane and also the CMOS ALARM pin. The polarity of CMOS ALARM pin depends alarm\_out\_pol bit in bit 3 of config0 register.

• Transport layer test pattern: implements a short transport layer pattern check based on F = 1,2,4 or 8. The

short test pattern has a duration of one frame period and is repeated continuously for the duration of the test.

Refer to JESD204B standard section 5.1.6 for more details.

– F = 1 : Looks for a constant 0xF1.

– F = 2 : Each frame should consist of 0xF1, 0xE2

– F = 4 : Looks for a constant 0xF1, 0xE2, 0xD3, 0xC4

– F = 8 : Each frame should consist of 0xF1, 0xE2, 0xD3, 0xC4, 0xB5, 0xA6, 0x97, 0x81

The test procedures for transport layer test pattern are as follow:

1. Set shortest\_ena to 1b’1 in bit 12 of the config2 register (address 0x02). This enables short transport layer checker.
2. Clear bits 8 to15 of the config6 register (address 0x06) to disable the “Short Test Error” alarm mask. Clear the bits according to the respective active lanes (for example, bit 8 is for lane0, bit 15 is for lane 7). If any error occurs on the respective lanes, the error result will show up at bit 8 to 15 of the config109 register, and the CMOS ALARM pin will trigger to signal the error.
3. Set the JESD204B TX logic device to output the corresponding test pattern.
4. Check the result at bits 8 to 15 of the config109 register and also the CMOS ALARM pin. The polarity of CMOS ALARM pin depends alarm\_out\_pol bit in bit 3 of config0 register.