DAC38J84 Clock and SerDes Configuration

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Purpose

This application note is meant to take the reader through a step-by-step process for setting up the DAC38J84 clocking scheme. After reading this application note the reader should understand the external clocking requirements, how to set the DAC38J84 internal clock dividers, how to program the internal PLL, and how to setup the SerDes block.

External Clocks

DACCLK

The clock provided to the DACCLK pins can be used as the DAC output clock or as the reference to the internal PLL. Up to a 2.5 GHz clock can be provided at these pins. These pins have an internal 100-Ω termination resistor and a 0.5-V common-mode is required. Due to the low common-mode voltage, it is recommended to AC-couple to the DACCLK pins to let the pins self-bias. A clocking standard with a large voltage swing is recommended, such as LVPECL. The AC termination for LVPECL is given in figure 1 below.

**Figure 1: AC termination for LVPECL clock**

SYSREF

The clock supplied to the SYSREF pins should follow the standards for the SYSREF signal defined in the JESD204B specification. It must be synchronous with DACCLK and have sufficient setup and hold times with respect to DACCLK for proper alignment of the local multi-frame clock (LMFC) edge for deterministic latency. If a multiple pulse or continuous SYSREF signal is provided to the SYSREF pins, the frequency of the signal must be chosen such that the LMFC frequency is an integer multiple of the SYSREF frequency. This prevents the SYSREF signal from occurring in the middle of an LMFC cycle which will trigger a SYSREF alarm. The frequency of the LMFC is given by:

Where linerate is the throughput rate of a single lane given in bits/s and F and K are as defined in the JESD204B standard. The frequency of SYSREF can then be define as:

Where n is an integer, such that an integer number of LMFC cycles occur in a single SYSREF cycle. For ease, the SYSREF frequency can simply be set to the LMFC frequency.

In the case of a non-periodic SYSREF signal (gapped pulse, or multiple-pulse) the SYSREF signal should be DC-coupled to the DAC38J84 SYSREF input. The SYSREF input pins require a 0.5-V common-mode voltage, while most clocking standards have common-mode voltages above 1 V. If the LMK04828 is used as the clock source, then the LCPECL output format can be used. The LCPECL output format has a common-mode voltage of 1.1 V, which can be lowered through a resistive voltage divider to 0.55 V using the termination scheme shown in figure 2. The left side resistor network should be kept close to the clock chip to provided proper source termination to maintain good signal integrity at the DAC’s SYSREF pins.

**Figure 2: DC termination for LCPECL clock**

Internal PLL

The DAC38J84 has an internal PLL that can be used to generate the high-frequency DAC output clock from a lower frequency clock provided to the DACCLK pins. This can simplify board layout and relax the requirements for the external clock. The clock at the DACCLK pins first goes through the N divider, which divides the reference clock down for the phase-frequency detector (PFD). The frequency presented to the PFD must be less than 160 MHz, but should be as high as possible to maintain the best phase noise performance.

Next, the M divider should be chosen such that the PFD frequency times the M divider is equal the desired DAC output rate.

There are two VCOs in the DAC38J84 that must be chosen based on the desired DAC update rate and the prescalar. The prescalar and VCO should be chosen to meet the requirement below.

The VCO centered at 4 GHz has a tuning range of xxxx to xxxx. The VCO centered at 5 GHz has a turning range of xxxx to xxxx. The VCO center frequency can be tuned using the VCO\_Tune parameter. This parameter should be interatively changed until the PLL Out of Lock detector is disabled.

CP current, bias current….

SerDes Configuration

The SerDes reference clock is used as the reference for the PLL that generates the clock for the SerDes sampling circuit. The SerDes core can run at full rate, half rate, quarter rate, and eight rate. Based on which rate is used, the SerDes clock frequency must be:

Where *rate* is the SerDes core rate (full = 1, half = 0.5, quarter = 0.25, eighth = 0.125). The SerDes core rate is chosen such that the SerDes clock is between 1562.5 MHz to 3125 MHz. If the chosen SerDes rate results in a SERDES\_CLK outside of the required range, then the rate should be changed to the next higher or next lower rate to meet the requirement. The multiplier (MPY) and SerDes reference divider can then be chosen to achieve the calculated SerDes clock. If the frequency at the DACCLK pins is greater than or equal to the SerDes clock divided by 5, set MPY to 5 and calculate the SerDes reference divider using the equation below. REF\_CLOCK is the input to the SerDes ref divider and can be either the DACCLK or the output of the PLL by setting CONFIG59[15].

If DACCLK is less than the SerDes clock divided by 5, set the SerDes reference divider to 1 and calculate MPY using the equation below:

The field mem\_rw\_cfgpll\_VRANGE (CONFIG60[9]) should be set to 1 if SerDes\_CLK is less than 2170 MHz and 0 if greater than or equal to 2170 MHz.

The SerDes core has other parameters that should set based on the table below.

|  |  |  |  |
| --- | --- | --- | --- |
| **Field Name** | **Register** | **Bit(s)** | **Recommended Value (binary)** |
| mem\_rw\_cfgpll\_ENDIVCLK | CONFIG60 | 15 | 0 |
| mem\_rw\_cfgrx0\_ENOC | CONFIG61 | 7 | 1 |
| mem\_rw\_cfgrx0\_EQ | CONFIG61 | 4:3 | 01 |
| mem\_rw\_cfgrx0\_EQBOOST | CONFIG61 | 5 | 0 |
| mem\_rw\_cfgrx0\_EQHLD | CONFIG61 | 6 | 0 |
| mem\_rw\_cfgrx0\_CDR | CONFIG61 | 2:0 | 000 |
| mem\_rw\_cfgrx0\_ALIGN | CONFIG62 | 12:11 | 00 |
| mem\_rw\_cfgrx0\_TERM | CONFIG62 | 10:8 | 001 |
| mem\_rw\_cfgrx0\_BUSWIDTH | CONFIG62 | 4:2 | 010 |
| mem\_rw\_cfgrx0\_SLEEPRX | CONFIG62 | 1 | 0 |

JESDCLK

The JESDCLK is used to the clock the JESD204B core inside of the DAC38J84. The JESD clock divider (JESDCLK\_DIV) is a function of the DAC interpolation, the number of lanes (L) and the number of DACs (M). The JESDCLK divider can be calculated using the equation below:

Register CONFIG37 should be programmed for the calculated JESDCLK divider per the table below.

|  |  |
| --- | --- |
| **Calculated JESDCLK Divider (JESDCLK\_DIV)** | **CONFIG37[15:0]** |
| 1 | 0x0000 |
| 2 | 0x2000 |
| 4 | 0x4000 |
| 8 | 0x6000 |
| 16 | 0x8000 |
| 32 | 0xA000 |