Bandwidth of the differential input filter has to be at last 10x higher than the sample rate. Sample rate = 40SPS.

Fdiff = 450Hz

Common mode filter should be 20x the frequency of differential filter.

Fcomm = 9000Hz

Common mode filter cap will be 10x smaller than the differential caps

PT1000 RTD

Temperatures -20 to 60 Degrees C

921.6 to 1232 ohms

with 1mA = 0.9216 to 1.232V

Rref = 1430 ohms

Gain = 1

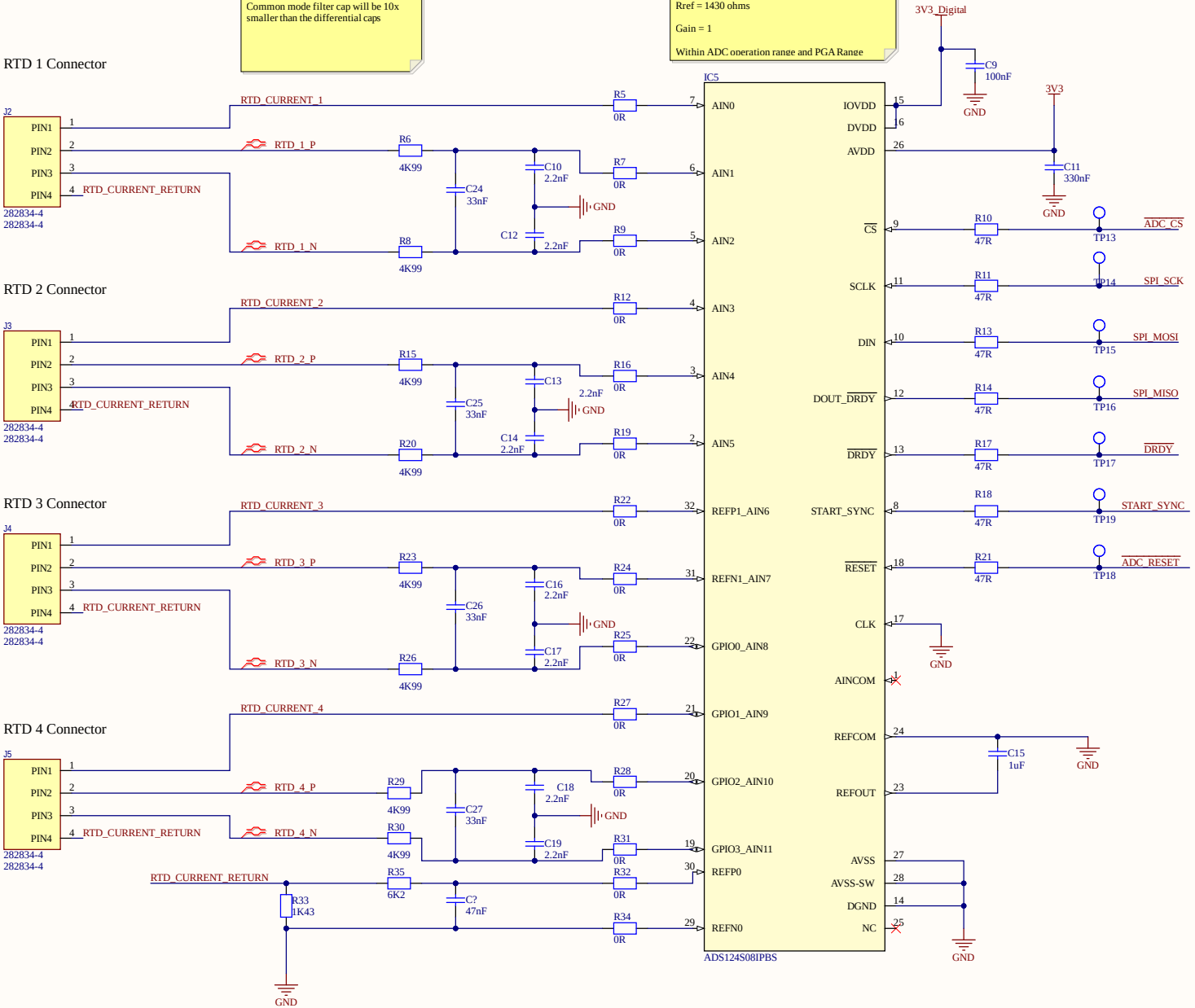
Within ADC operation range and PGA Range

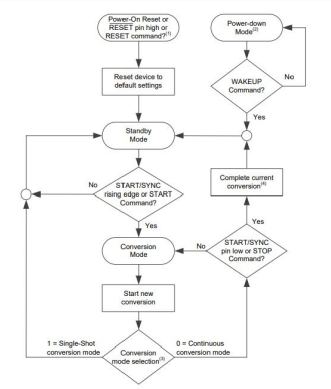
RTD 1 Connector

RTD 2 Connector

RTD 3 Connector

RTD 4 Connector





Sinc3 filter gives better noise performance than the low latency filter but has a 3 cycle latency at the data output.

ADC Can be started by pulling ADC_CS low, then starting conversion using either START_SYNC or by SPI Command

AINCOM used for single ended measurements. Unused analog pins to be left floating

Using internal oscillator so tieing CLK to gnd

Differential filter on the Reference resistor input is required.

Set the frequency to 400hz as it should match the frequency of the analog inputs.

Common mode filter not required as the reference is tied to gnd

Dout / D Ready is a dual pin used to signal when data is ready and also acts as SPI data input.

Or the DRDY pin can be used