Table 10. Internal Reference Settling Time

REFOUT CAPACITOR	SETTLING ERROR	SETTLING TIME (ms)
1 µF	0.01%	4.5
	0.001%	5.9
10 µF	0.01%	4.9
	0.001%	6.3
47 µF	0.01%	5.5
	0.001%	7.0

Title: ANALOG INPUT
VARIATION: MANCHESTER 2.0
Drawn By: V.VLACH
Approved By: *
Check By: *
Size: D | DWG # 11052351 | Revision: A
Date: 7/10/23 | Sheet 9 of 12
File: 08_analog input.SchDoc 7/10/2023

STERIS Corporation
5960 Heisley Road
Mentor, Ohio 44060

MULTI BOARD #
None

STERIS Corporation

3 WIRE RTD INPUTS

J8
RTD-0
RTD+1
REF_0+
RTD+0
REF_0+
RTD-1

J7
RTD-3
RTD+2
REF_0+
RTD+3
REF_1+
RTD-2

J5
RTD-4
RTD+5
REF_1+
RTD+4
REF_1+
RTD-5

GND_EARTH

D11 SD103AWS *RTD+0_EXC
C62 10nF
R56 4.7k 1% 0402 *RTD+0
C61 100nF C0G
R51 4.7k 1% 0402 *RTD-0
C60 10nF
D10 SD103AWS *RTD-0_EXC

D13 SD103AWS *RTD+1_EXC
C71 10nF
R61 4.7k 1% 0402 *RTD+1
C68 100nF C0G
R57 4.7k 1% 0402 *RTD-1
C67 10nF
D12 SD103AWS *RTD-1_EXC

D9 SD103AWS *RTD+2_EXC
C56 10nF
R48 4.7k 1% 0402 *RTD+2
C52 100nF C0G
R47 4.7k 1% 0402 *RTD-2
C50 10nF
D8 SD103AWS *RTD-2_EXC

D7 SD103AWS *RTD+3_EXC
C46 10nF
R44 4.7k 1% 0402 *RTD+3
C41 100nF C0G
R39 4.7k 1% 0402 *RTD-3
C36 10nF
D6 SD103AWS *RTD-3_EXC

D3 SD103AWS *RTD+4_EXC
C5 10nF
R36 4.7k 1% 0402 *RTD+4
C4 100nF C0G
R17 4.7k 1% 0402 *RTD-4
C3 10nF
D2 SD103AWS *RTD-4_EXC

D5 SD103AWS *RTD+5_EXC
C26 10nF
R38 4.7k 1% 0402 *RTD+5
C25 100nF C0G
R37 4.7k 1% 0402 *RTD-5
C23 10nF
D4 SD103AWS *RTD-5_EXC

2.5_VDCA 2.5_VDCA 2.5_VDCA 2.5_VDCA
R315 0.1% 0402 R324 0.1% 0402 R325 0.1% 0402 R326 0.1% 0402
D161 MMBD1503A *RTD+1
D162 MMBD1503A *RTD-1

RTD+1 D177 SP4024-01FTG-C
RTD-1 D178 SP4024-01FTG-C

2.5_VDCA -2.5_VDCA 2.5_VDCA -2.5_VDCA 2.5_VDCA -2.5_VDCA 2.5_VDCA -2.5_VDCA
R336 0.1% 0402 R337 0.1% 0402 R338 0.1% 0402 R339 0.1% 0402 R340 0.1% 0402 R426 0.1% 0402 R427 0.1% 0402 R428 0.1% 0402
D163 MMBD1503A *RTD+2
D164 MMBD1503A *RTD-2
D165 MMBD1503A *RTD+5
D166 MMBD1503A *RTD-5

2.5VDCA -2.5VDCA 2.5VDCA -2.5VDCA
R429 0.1% 0402 R430 0.1% 0402 R658 0.1% 0402 R659 0.1% 0402
D167 MMBD1503A *RTD+0
D168 MMBD1503A *RTD-0

RTD+2 D179 SP4024-01FTG-C
RTD-2 D180 SP4024-01FTG-C
RTD+5 D181 SP4024-01FTG-C
RTD-5 D182 SP4024-01FTG-C
RTD+0 D183 SP4024-01FTG-C
RTD-0 D184 SP4024-01FTG-C

2.5VDCA -2.5VDCA 2.5VDCA -2.5VDCA 2.5VDCA -2.5VDCA 2.5VDCA -2.5VDCA
R660 0.1% 0402 R661 0.1% 0402 R662 0.1% 0402 R663 0.1% 0402 R664 0.1% 0402 R665 0.1% 0402 R666 0.1% 0402 R667 0.1% 0402
D169 MMBD1503A *RTD+3
D170 MMBD1503A *RTD-3
D171 MMBD1503A *RTD+4
D172 MMBD1503A *RTD-4

RTD+3 D185 SP4024-01FTG-C
RTD-3 D186 SP4024-01FTG-C
RTD+4 D187 SP4024-01FTG-C
RTD-4 D188 SP4024-01FTG-C

U27 ADS114S08
C70 0.33uF 16V X7R 0603 2.5_VDCA
2.5_VDCA 3V3
C72 100nF 50V
AIN0 *RTD+1
AIN1 *RTD+1_EXC
AIN2 *RTD-1_EXC
AIN3 *RTD-1
AIN4 *RTD-5
AIN5 *RTD-5_EXC
REFP1_(AIN6 S08 ONLY) *RTD-5_EXC
REFN1_(AIN7 S08 ONLY) *RTD-5
GPIO2_(AIN8 S08 ONLY) *RTD+2
GPIO1_(AIN9 S08 ONLY) *RTD+2_EXC
GPIO2_(AIN10 S08 ONLY) *RTD-2_EXC
GPIO3_(AIN11 S08 ONLY) *RTD-2
AINCOM
REFP0 REF_0+
REFN0
AVDD DVDD 1V8OUT
REFOUT REFCOM
C66 1µF 50V X7R 0805 2.5_VDCA
SCLK DOUT_DRDY_N DIN DRDY_N
RESET_N START_SYNC
R45 10K 1% 0402 3V3
CLK
NC AVSS AVSS_SW PAD DGND
SCLK ADC_CS1 MOSI2 MISO2 DRDY#1
R175 33 1% 0402
C500 10nF
R633 4.7k 1% 0402
R65 1.87k 0.1% 0402 10ppm
R634 4.7k 1% 0402
C501 100nF C0G
C502 10nF
REF_0+ -2.5_VDCA
C73 100nF -2.5_VDCA 50V
-2.5_VDCA

If gain is needed to measure a single-ended signal, the PGA must be enabled. In this case, a bipolar supply is required for the ADS114S0x to meet the input voltage requirement of the PGA.

U33 LM27762
5VDCA
C88 1µF 10V X7R 0603
C89 4.7µF 25V X5R 0805
C91 10µF 10V X5R 0603 2.5VDCA
VIN CPOUT OUT+ C1- C1+ FB+ PGOOD FB- EN+ EN- OUT- GND PAD
R72 536k 1% 0402
R71 499K 1% 0402
R80 499K 1% 0402
R79 536k 1% 0402
C87 2.2µF 10V 0603
C92 2.2µF 10V 0603
-2.5VDCA

U21 ADS114S08
C54 0.33uF 16V X7R 0603 -2.5VDCA
2.5VDCA 3V3
C55 100nF 50V
AIN0 *RTD+3
AIN1 *RTD+3_EXC
AIN2 *RTD-3_EXC
AIN3 *RTD-3
AIN4 *RTD+0
AIN5 *RTD+0_EXC
REFP1_(AIN6 S08 ONLY) *RTD-0_EXC
REFN1_(AIN7 S08 ONLY) *RTD-0
GPIO2_(AIN8 S08 ONLY) *RTD+4
GPIO1_(AIN9 S08 ONLY) *RTD+4_EXC
GPIO2_(AIN10 S08 ONLY) *RTD-4_EXC
GPIO3_(AIN11 S08 ONLY) *RTD-4
AINCOM
REFP0
REFN0
AVDD DVDD 1V8OUT
REFOUT REFCOM
C47 1µF 50V X7R 0805 2.5VDCA
SCLK DOUT_DRDY_N DIN DRDY_N
RESET_N START_SYNC
R46 10K 1% 0402 3V3
CLK
NC AVSS AVSS_SW PAD DGND
SCLK ADC_CS2 MOSI2 MISO2 DRDY#2
R176 33 1% 0402
C503 10nF
REF_1+
R635 4.7k 1% 0402
R50 1.87k 0.1% 0402 10ppm
R636 4.7k 1% 0402
C504 100nF C0G
C505 10nF
-2.5VDCA
C57 100nF -2.5VDCA 50V
-2.5VDCA

If gain is needed to measure a single-ended signal, the PGA must be enabled. In this case, a bipolar supply is required for the ADS114S0x to meet the input voltage requirement of the PGA.

Title:	RTD INPUTS
VARIATION:	MANCHESTER 2.0
Drawn By:	V.VLACH
Approved By:	*
Check By:	*
Size:	D
DWG #	11052351
Revision:	A
Date:	7/10/23
Sheet	10 of 12
File:	10_RTD_INPUTS.SchDoc
	7/7/2023

STERIS Corporation
5960 Heisley Road
Mentor, Ohio 44060

MULTI BOARD #
None

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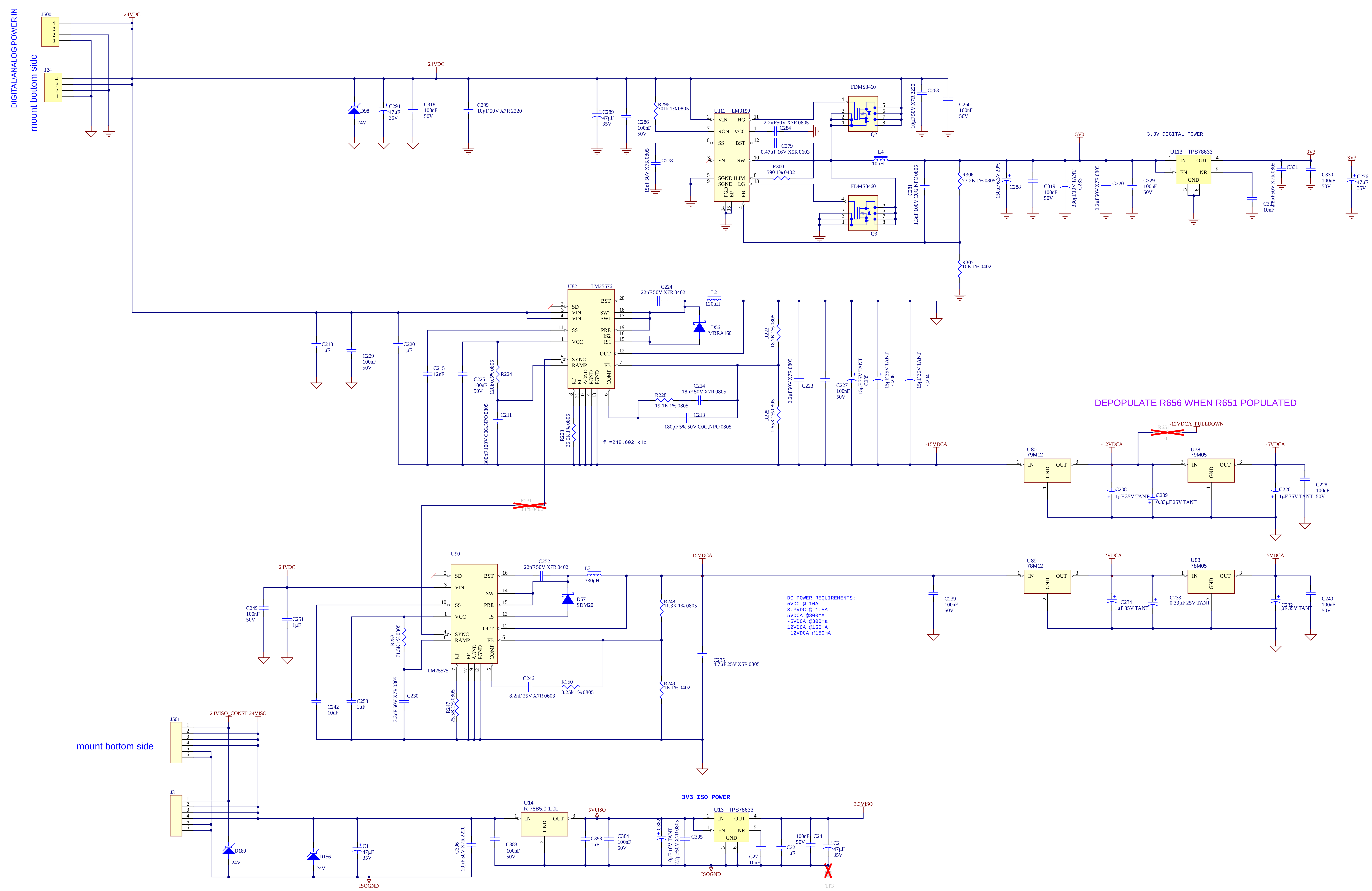

DIGITAL/ANALOG POWER IN
mount bottom side
J500
J24
24VDC
D98
24V
C294
47µF
35V
C318
100nF
50V
C299
10µF 50V X7R 2220
C289
47µF
35V
C286
100nF
50V
R296
301k 1% 0805
U111 LM3150
VIN
RON
SS
EN
SGND
HG
VCC
BST
SW
ILIM
LG
FB
C284
2.2µF 50V X7R 0805
C279
0.47µF 16V X5R 0603
R300
590 1% 0402
C278
15nF 50V X7R 0805
FDMS8460
Q2
Q3
C263
10µF 50V X7R 2220
C260
100nF
50V
L4
10µH
C281
1.3nF 100V C0G,NPO 0805
R306
73.2K 1% 0805
R305
10K 1% 0402
5V0
C288
150nF 6.3V 20%
C319
100nF
50V
C283
330µF 10V TANT
C320
2.2µF 50V X7R 0805
C329
100nF
50V
3.3V DIGITAL POWER
U113 TPS78633
IN
OUT
EN
NR
GND
C331
2.2µF 50V X7R 0805
C332
10nF
3V3
C330
100nF
50V
C276
47µF
35V
U82 LM25576
SD
VIN
SS
VCC
SYNC
RAMP
RT
EP
AGND
PGND
COMP
BST
SW2
SW1
PRE
IS2
IS1
OUT
FB
C224
22nF 50V X7R 0402
L2
120µH
D56
MBRA160
C218
1µF
C229
100nF
50V
C220
1µF
C215
12nF
C225
100nF
50V
R224
120k 0.5% 0805
C211
390pF 100V C0G,NPO 0805
R223
25.5K 1% 0805
f =248.602 kHz
R228
19.1K 1% 0805
C214
18nF 50V X7R 0805
C213
180pF 5% 50V C0G,NPO 0805
R222
18.7K 1% 0805
R225
1.65K 1% 0805
C223
2.2µF 50V X7R 0805
C227
100nF
50V
C205
15µF 35V TANT
C206
15µF 35V TANT
C204
15µF 35V TANT
DEPOPULATE R656 WHEN R651 POPULATED
-15VDCA
-12VDCA
-12VDCA_PULLDOWN
-5VDCA
U80
79M12
U78
79M05
C208
1µF 35V TANT
C209
0.33µF 25V TANT
C226
1µF 35V TANT
C228
100nF
50V
U90
LM25575
C252
22nF 50V X7R 0402
L3
330µH
D57
SDM20
15VDCA
R248
11.3K 1% 0805
R249
1K 1% 0402
C235
4.7µF 25V X5R 0805
C249
100nF
50V
C251
1µF
R253
71.5K 1% 0805
C242
10nF
C253
1µF
C230
3.3nF 50V X7R 0805
R247
25.5K 1% 0805
C246
8.2nF 25V X7R 0603
R250
8.25k 1% 0805
DC POWER REQUIREMENTS:
5VDC @ 10A
3.3VDC @ 1.5A
5VDCA @300mA
-5VDCA @300ma
12VDCA @150mA
-12VDCA @150mA
C239
100nF
50V
U89
78M12
12VDCA
U88
78M05
5VDCA
C234
1µF 35V TANT
C233
0.33µF 25V TANT
C232
1µF 35V TANT
C240
100nF
50V
mount bottom side
J501
J1
24VISO_CONST
24VISO
D189
24V
D156
24V
C1
47µF
35V
ISOGND
C386
10µF 50V X7R 2220
U14
R-78B5.0-1.0L
C383
100nF
50V
5V0ISO
C393
1µF
C384
100nF
50V
3V3 ISO POWER
U13 TPS78633
C382
10µF 10V TANT
C385
2.2µF 50V X7R 0805
C395
C27
10nF
C22
1µF
C24
100nF
50V
C2
47µF
35V
3.3VISO
TP1

Title: Power SECTION VARIATION: MANCHESTER 2.0			STERIS Corporation 5960 Heisley Road Mentor, Ohio 44060
Drawn By: V.VLACH Approved By: Check By:			
Size: D	DWG # 11052351	Revision: A	MULTI BOARD # None
Date: 7/10/23		Sheet 11 of 12	
File: 11_POWER.SchDoc		6/30/2023	

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