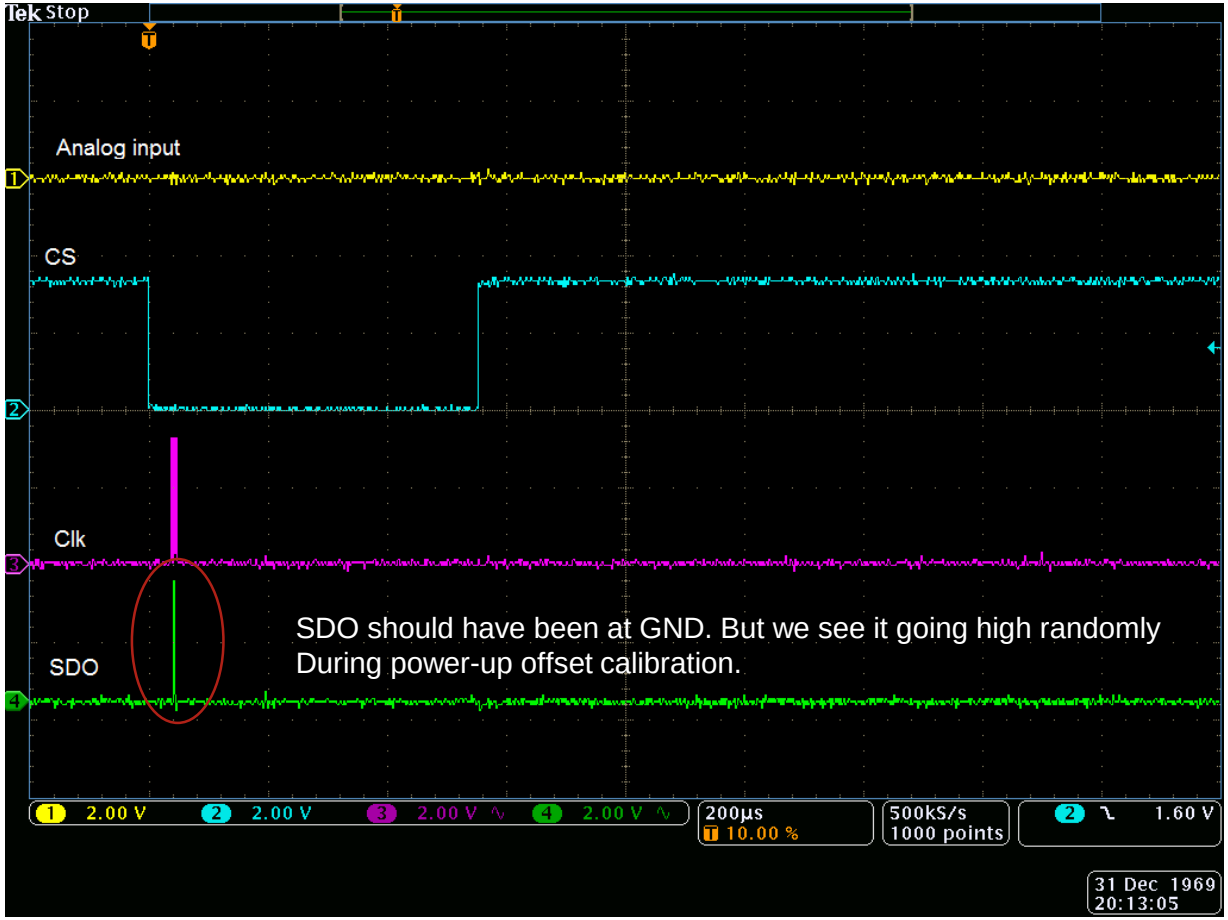
Initial conditions

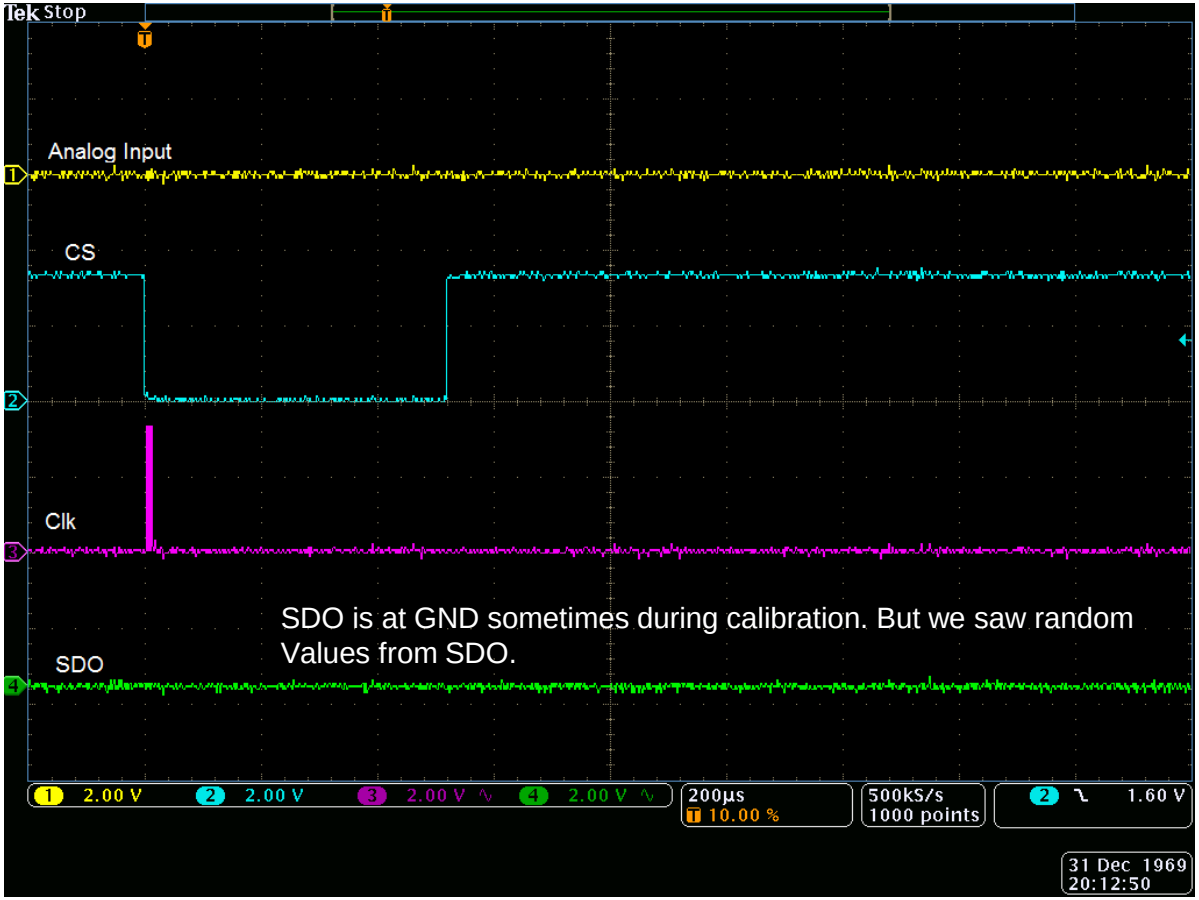
- Analog input is zero (Verified)
- AVDD AND DVDD = 3.3V (Verified)
- Offset calibration timing (followed as per datasheet)- waveform attached
- SPI timing (followed as per datasheet) – waveform attached

Power on offset calibration – case1 SDO is not low (happens randomly).



NOTE: Supply to the chip is 3.3V and stable before calibration is started

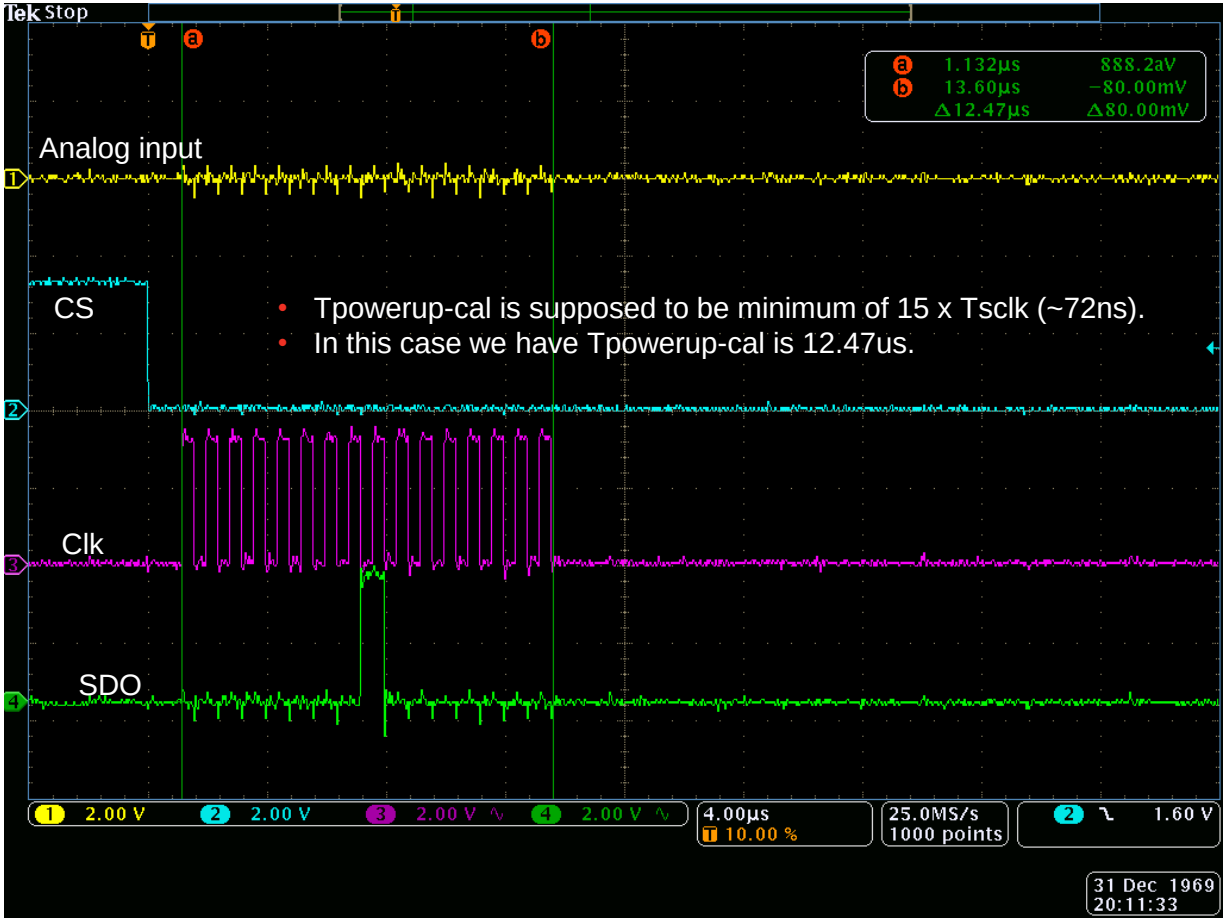
Power on off set calibration – case2, SDO is low (happens randomly)



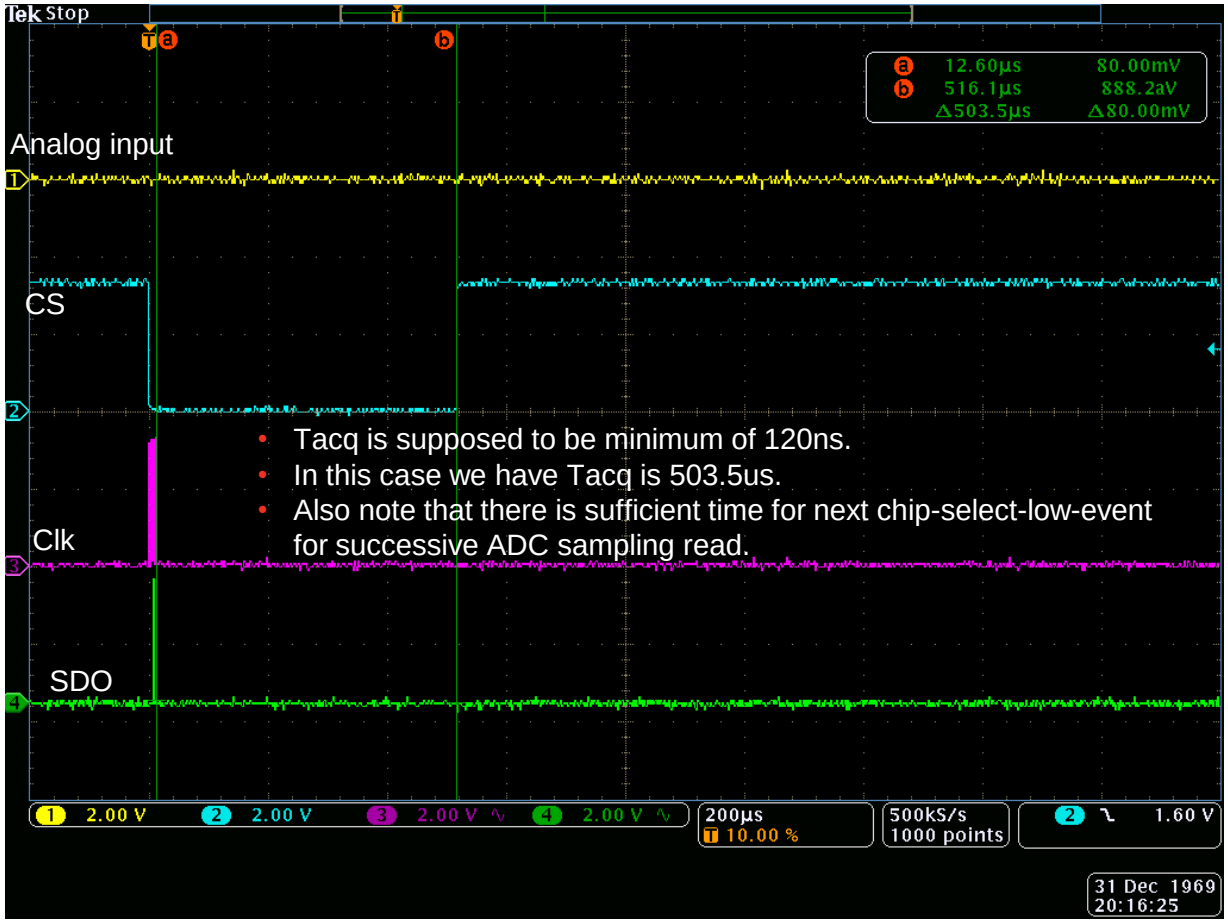
NOTE: Supply to the chip is 3.3V and stable before calibration is started

Power on offset calibration timing -1

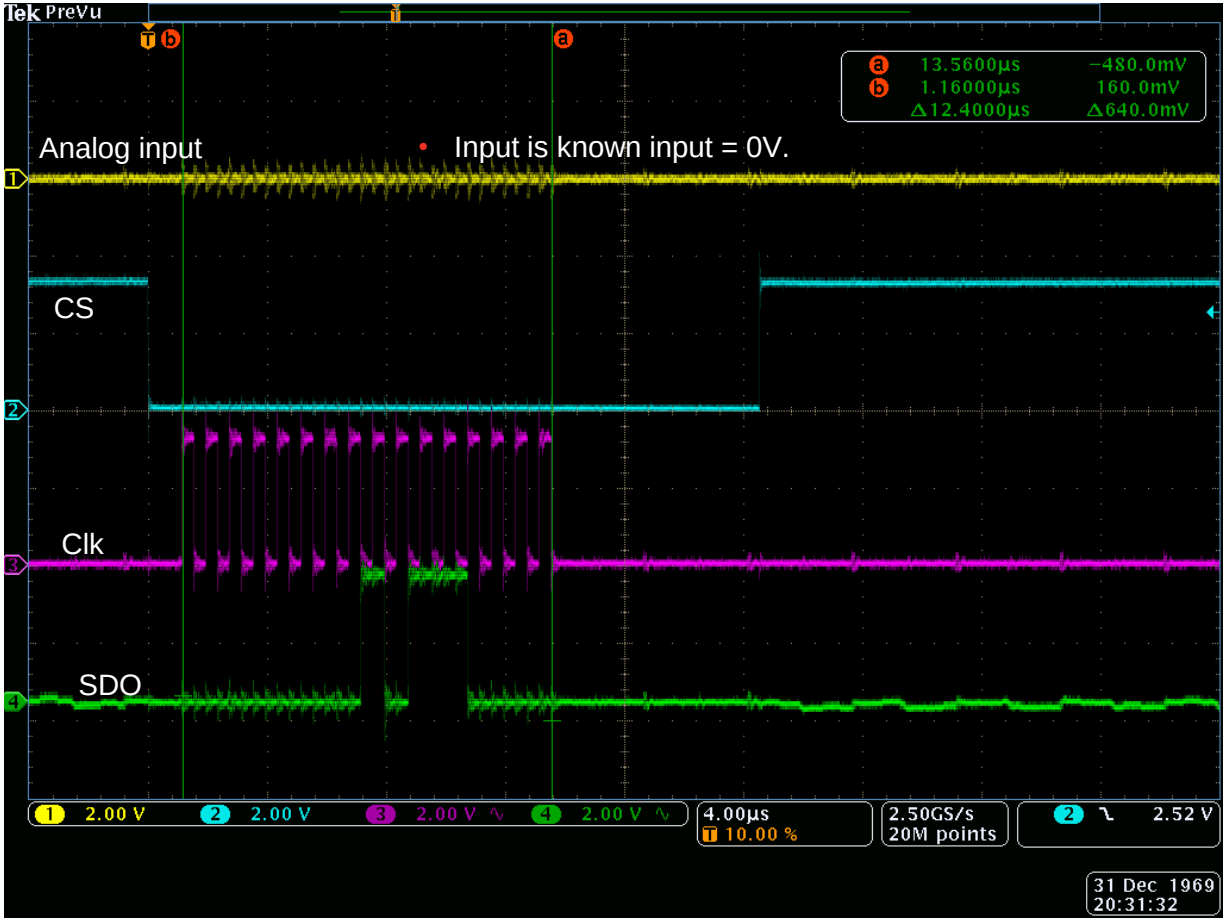
Power on offset calibration timing -2



Power on offset calibration timing -3



SPI read timing when Analog input=0V



SPI read timing when Analog input=3.3V