Texas Instruments Incorporated
Military Products Department
Military High Reliability Integrated Circuits
Processing Conformance Report

Device Type: **ADC12D1600CCMLS**
SMD: **N/A**
Processing Type: **CLASS V**

PCR Lot Number: **STM294480**
Device Description:

Assembly Location: **GDA**
Wafer Lot #: **VM02B5HK**
Wafer #: **2**

Assembly Date Code Year: **2012** Week: **06** Lot Window:
Wafer Lot Date Code Year: **2011** Qtr: **4Q** Die Rev: **A** W/F Code: **GH**

Integrated Circuits referenced above have received the following processing per recorded lot history.

	SCREEN	METHOD	(MIL-STD-883)
☑	INTERNAL VISUAL PRECAP	2010	CONDITION A (100X)
☑	INTERNAL VISUAL PRECAP	2010	CONDITION A (40X)
☐	INTERNAL VISUAL PRECAP	2010	CONDITION A (L/A)
	Wafer Number(s) used in Production:	**2**	
☑	TEMPERATURE CYCLING	1010	CONDITION C
☑	CENTRIFUGE	2001	CONDITION E,Y1 PLANE
☑	PIND TEST	2020	CONDITION A
☐	RADIOGRAPHY	2012	☐ MONITOR OR ☐ 100%
☒	INTERIM ELECTRICAL TEST		25c DC / FUNCTIONAL
☑	BURN IN	1015	TEMP (°C) **150** TIME (Hrs) **240**
	FINAL ELECTRICAL TEST TEMP	☒ 25c ☒ 125c ☒ -55c ☐	☐
	TEST PROGRAM #(s)	**ADC12D16QMLLFRB1**	**ADC12D16QML FHB1** **ADC12D16QML FCB1**
☒	HERMETICITY	1014	
	FINE LEAK		CONDITION A OR B
	GROSS LEAK		CONDITION C
☑	EXTERNAL VISUAL	2009	(100%)
☒	EXTERNAL VISUAL	2009	(L/A)

QUALITY CONFORMANCE ATTRIBUTE DATA GROUP "A " SUMMARY

	SUBGROUP	TEST & TEMP	SAMPLE SIZE
☑	A-1/4/7	DC ELECTRICAL - AMBIENT	116 OR 100%
☑	A-2/5/8	DC ELECTRICAL - MAXIMUM	116 OR 100%
☒	A-3/6/8	DC ELECTRICAL - MINIMUM	116 OR 100%
☑	A-9	AC ELECTRICAL - AMBIENT	116 OR 100%
☒	A-10	AC ELECTRICAL - MAXIMUM	116 OR 100%
☑	A-11	AC ELECTRICAL - MINIMUM	116 OR 100%

Device Lead-Finish complies with MIL-PRF-38535 A.3.5.6.3 Microcircuit finishes: "Finishes of all external leads or terminals and all external package elements shall conform to either A.3.5.6.3.2 or A.3.5.6.3.3 as applicable. The use of pure tin, as an underplate or final finish, is prohibited both internally and externally. The tin content of solder shall not exceed 97 percent. Tin shall be alloyed with a minimum of 3 percent lead by weight.

SOLDER PROCESSING DATE (IF APPLICABLE):
NOTE: The following documents MUST be pulled and sent with each lot.
(A copy to be placed in each box)
1) PROCESS CONFORMANCE REPORT
2) GENERIC GROUP B QCI SUMMARY REPORT
3) GENERIC GROUP D QCI SUMMARY REPORT
4) WAFER LOT ACCEPTANCE REPORT FOR THE WAFER LOT USED IN THIS ASSEMBLY LOT.

Prepared By: **Eulalia Alvarez** Date: **12/10/2013**

QCI Group B - Lot #: **STM294480** Date Code: **1206** Pkg Type: **376CGA** Lead Finish: **A**
QCI Group C - Lot #: **STM294480** Date Code: **1206** MCG: **81** Wafer Lot Date Code: **1D**
QCI Group D - Lot #: **STM294480** Date Code: **1206** Pkg Type: **376CGA** Lead Finish: **A**
QCI Group E - Lot #: Wafer Lot #:
Wafer Lot Accept - Lot #: **VM02B5HK** Wafer Lot #: **VM02B5HK**

Group B Summary Report

Lot Number: STM294480
Date Code: 2012-06
Test Start: 12/09/2012
Pin: 376

Device Name: ADC12D1600CCMLS
Assembly Site: GDA
Test Complete: 12/14/2012
Package: CGA

Lead Finish: A
Package Family: GROUP 21

66666 Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
B2	RESISTANCE TO SOLVENTS	TM2015	3	0	1
B3	SOLDERABILITY	TM2003	3	0	1
B5	BOND STRENGTH	2011	4	0	1
B5	DIE ATTACH STRENGTH	2019 OR 2027	4	0	

Notes: 1.Resistance to solvents testing required only on devices using inks or paints as a marking medium.
1. 22 leads / 3 packages minimum. Not required for solder columns
1. 15 wires / 4 units mimimum

Comments:
B5 tested with no columns. B2 and B3 tested with columns

Prepared By: Eulalia Alvarez
Prepared By Email: Eulalia.Alvarez@ti.com
Prepare Date: 12/10/2013

Group C Summary Report

Lot Number:	STM294480	Device Name:	ADC12D1600CCMLS	Assembly Site:	GDA
Lot Date Code:	2012-06	Wafer Lot Date Code:	2011-4Q-A-GH	Wafer Lot Number:	VM02B5HK
Parent Die:	ADC12D500	Die Attach:	QMI	Window:	4Q 2006 to 3Q 2007
Pin:	376	Package:	CGA	MCG:	81
Test Start:	10/16/2012	Test Complete:	11/28/2012		

Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
C1	Steady-state life test	1005		0	1
C1	Endpoint Electrical Test		45	0	2

Notes: 1. 1,000 hours/125C or equivalent. (If greater than 1,000 hours/125C enter actual conditions into comments below)
2. Endpoint electrical testing in accordance with device test specification.

Comments:

Prepared By: Eulalia Alvarez Prepared By Email: Eulalia.Alvarez@ti.com Prepare Date: 10/09/2015

Group D Summary Report

Lot Number: STM294480
Date Code: 2012-06
Test Start: 12/03/2012
Pin: 376
Window: 06 2012 to 42 2012

Device Name: ADC12D1600CCMLS
Assembly Site: GDA
Test Complete: 12/16/2012
Package: CGA

Lead Finish: A
Package Family: GROUP 21

66666 Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
D1	Physical Dimensions	2016	15	0	
D2	Lead Integrity	2004 and 2028	45	0	1
D2	Seal (Fine and Gross)	1014		0	
D3	Thermal Shock	1011	15	0	2
D3	Temperature Cycle	1010		0	3
D3	Moisture Resistance	1004		0	
D3	Visual Examination	1004 and 1010		0	
D3	Seal (Fine and Gross)	1014		0	
D3	End-point electrical test			0	4
D4	Mechanical Shock	2002	15	0	5
D4	Vibration, Variable Freq	2007		0	6
D4	Constant acceleration	2001		0	7
D4	Seal (Fine and Gross)	1014		0	
D4	Visual Examination	1010 and 1011		0	
D4	End-point electrical test			0	4
D5	Salt Atmosphere	1009	15	0	10
D5	Visual Inspection	1009		0	
D5	Seal (Fine and Gross)	1014		0	
D6	Internal water vapor	1018	3 (5)	0 (1)	8
D7	Adhesion of lead finish	2025	15	0	9
D8	Lid Torque	2024	5	0	11

Notes: 1. Condition B2, 3 devices, 45 leads total. For PGA and rigid leads use Condition B1 or Method 2028. For LCCC packages only, use condition D and SS of 15 based on the number of pads tested from 3 devices minimum.
2. Condition B, 15 cycles.
3. Condition C, 100 cycles.
4. Endpoint electrical testing in accordance with device test specification.
5. Condition B.
6. Condition A.
7. Condition E (20KG) Y1 axis only.
4. Endpoint electrical testing in accordance with device test specification.
10. Condition A.
8. 5000 PPM and 100C. Sample size is 3/0 or 5/1.
9. 15 leads, not performed for LCCC. Any deviations to test methods or conditions, such as centrifuge, will be specificed in the device travler.
11. Glass Frit Seal Only - N/A for MMT Assembly.

Comments:
D6 tested with no columns D1, D3, D4, D5 tested with columns on. D7 and D8 not applicable

Prepared By: Eulalia Alvarez
Prepared By Email: Eulalia.Alvarez@ti.com
Prepare Date: 12/10/2013

WLA Summary Report

Lot Number: VM02B5HK
Wafer Lot Date Code: 2006-4Q-A-GH
Parent Die: ADC12D500A
Test Start: 12/03/2012

Device Name: ADC12D1600CCMLS
Wafer Lot Number: VM02B5HK
Lead Finish: A
Test Complete: 12/10/2012

MCG: 81

Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
WLA-1	Wafer Thickness	5007	2 wafers/lot	0	1
WLA-2	Metallization Thickness	5007	1 wafer/lot	0	2
WLA-3	Thermal Stablility	5007	1 wafer/lot	0	2,3
WLA-4	SEM Inspection Lot Acceptance	2018	2 wafers/lot	0	2
WLA-4	Lab Performing Analysis:			SVA	
WLA-5	Glassivation Thickness	1005	1 wafer/lot	0	2
WLA-6	Gold Backing Thickness	1005	1 wafer/lot	0	2,4
WLA-7	Steady-state life test	1005		0	5
WLA-7	Endpoint Electrical Test	2003	45	0	6

Notes: 1. This test is not required when the finished wafer design thickness is greater than 10 mils before backgrind.
2. In-line monitor data for this wafer lot may be used.
3. Applicable to all linear, all MOS, all bipolar digital operating at 10V or more. (VFB/VT/C-V)
4. Gold backed wafers only.
5. 1,000 hours/125C or equivalent
6. Endpoint electrical testing in accordance with device test specification

Comments:

Prepared By: a0411966
Prepared By Email:
Prepare Date: 12/18/2012